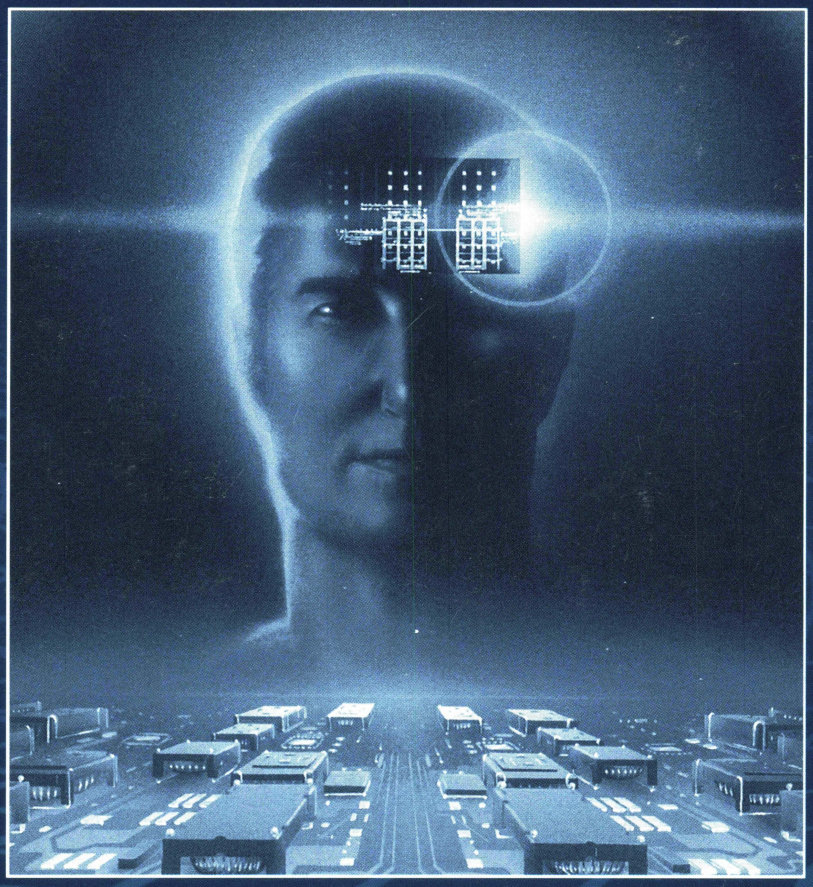
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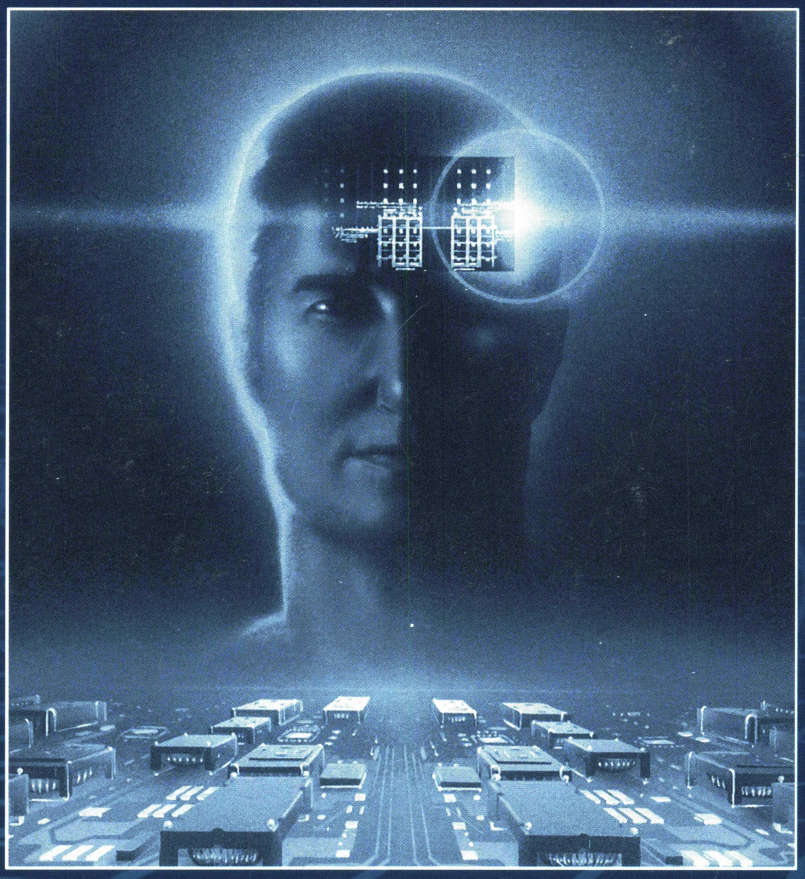


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FOR COMMERCIAL, INDUSTRIAL AND AUTOMOTIVE APPLICATIONS

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This Intelligent Power ICs Databook represents the full line of Harris Semiconductor Intelligent Power products for commercial, industrial and automotive applications and supersedes previously published Intelligent Power product databooks under the Harris, GE, RCA or Intersil names. For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG-201.21; ordering information below).

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HARRIS SEMICONDUCTOR

INTELLIGENT POWER

INTEGRATED CIRCUITS

FOR COMMERCIAL, INDUSTRIAL & AUTOMOTIVE APPLICATIONS

General Information 1

Low Side Switches 2

High Side Switches 3

Half Bridges 4

AC to DC Converters 5

Full Bridges 6

Regulators/Power Supplies 7

Protection Circuits 8

Multiplex Communication Circuits 9

Special Functions 10

Application Notes 11

Harris Quality and Reliability 12

Packaging Information 13

How To Use Harris AnswerFAX 14

Sales Offices 15

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DATA SHEET IDENTIFICATION	PRODUCT STATUS	DEFINITION
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Preliminary	Pre Production Samples Available	This datasheet contains preliminary data, and supplementary data will be published at a later date. Harris Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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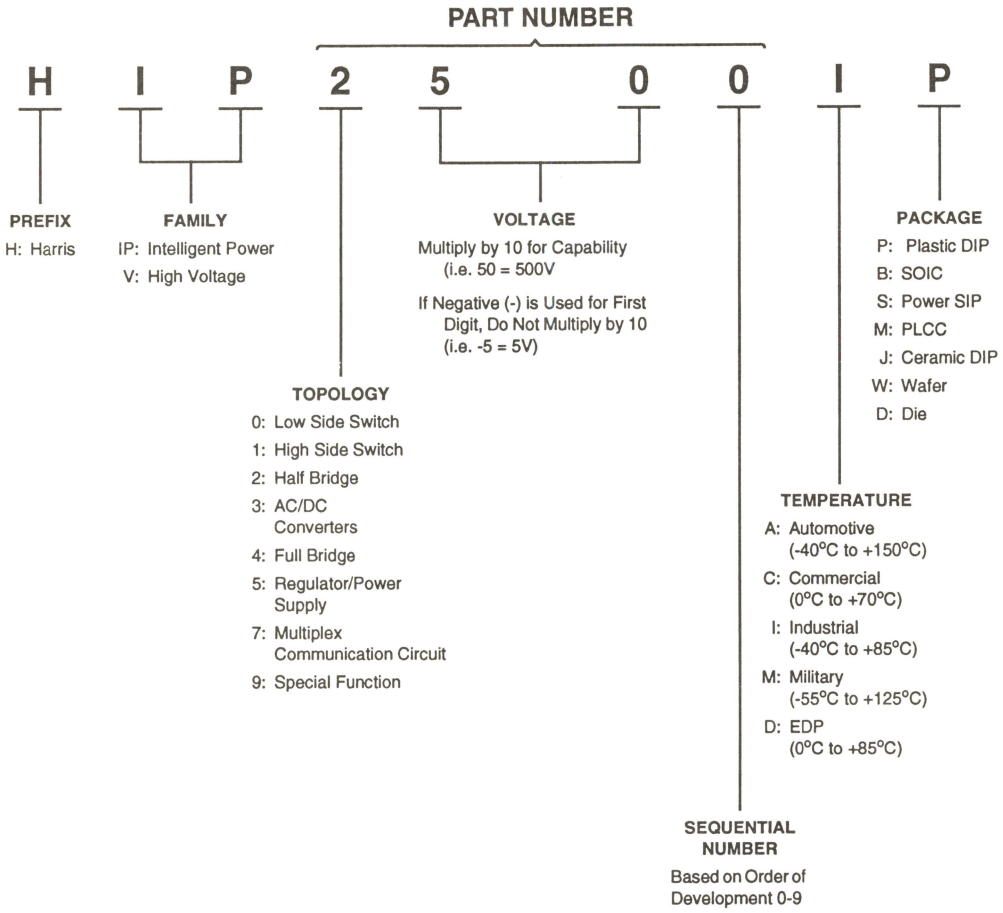
INTELLIGENT POWER ICs 1

GENERAL INFORMATION

	PAGE
GENERAL ORDERING INFORMATION	1-3
ALPHA NUMERIC PRODUCT INDEX	1-4
PRODUCT INDEX BY FAMILY	1-6
APPLICATION INDEX	1-9
INTELLIGENT POWER PRODUCTS CROSS REFERENCE LIST	1-12

General Ordering Information

PRODUCT CODE EXAMPLE



Alpha Numeric Product Index

		PAGE
CA723	Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors	7-3
CA723C	Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors	7-3
CA1523	Voltage Regulator Control Circuit for Variable Switching Regulator	7-11
CA1524	Regulating Pulse Width Modulator	7-16
CA2524	Regulating Pulse Width Modulator	7-16
CA3020	Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz	10-3
CA3059	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
CA3079	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
CA3085	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3085A	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3085B	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3094	Programmable Power Switch/Amplifier for Control and General Purpose Applications	10-11
CA3165	Electronic Switching Circuit	10-25
CA3228	Speed Control System with Memory	10-31
CA3242	Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load	2-3
CA3262	Quad-Gated Inverting Power Drivers	2-7
CA3262A	Quad-Gated Inverting Power Drivers	2-7
CA3272	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
CA3272A	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
CA3273	High-Side Driver	3-3
CA3274	Current Limiting Power Switch With Current Limiter Sense Flag	10-40
CA3275	Dual Full Bridge Driver	6-3
CA3277	Dual 5V Regulator with Serial Data Buffer Interface for Microcontroller Applications	7-39
CA3282	CMOS Octal Serial Solenoid Driver	2-20
CA3292A	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
CA3524	Regulating Pulse Width Modulator	7-16
CDP68HC68S1	Serial Bus Interface	9-3
HIP0080	Quad Inverting Power Drivers with Serial Diagnostic Interface	2-28
HIP0081	Quad Inverting Power Drivers with Serial Diagnostic Interface	2-28
HIP0082	Quad Power Driver with Serial Diagnostic Interface	2-36
HIP1030	1A High Side Driver with Overload Protection	3-6
HIP1031	Half Amp High Side Driver with Overload Protection	3-10
HIP1090	Protected High Side Power Switch with Transient Suppression	3-13
HIP2030	30V MCT/IGBT Gate Driver	4-3
HIP2500	Half Bridge 500V_{DC} Driver	4-10

		PAGE
HIP4010	Power Full Bridge Driver for Low Voltage Motor Drive with Direction and Brake Control	6-7
HIP4011	Three Phase Brushless DC Motor Controller	6-11
HIP4080	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-14
HIP4080A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-28
HIP4081	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-41
HIP4081A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-54
HIP4082	80V/1.25A Peak Current Full Bridge FET Driver	6-67
HIP5060	Power Control IC Single Chip Power Supply	7-47
HIP5061	7A, High Efficiency Current Mode Controlled PWM Regulator	7-53
HIP5062	Power Control IC Single Chip Dual Switching Power Supply	7-73
HIP5063	Power Control IC Single Chip Power Supply	7-80
HIP5500	High Voltage IC Half Bridge Gate Driver	7-84
HIP5600	Thermally Protected High Voltage Linear Regulator	7-94
HIP7010	J1850 Byte Level Interface Circuit	9-17
HIP7020	J1850 Bus Transceiver I/O for Multiplex Wiring	9-33
HIP7030A0	J1850 8-Bit 68HC05 Microcontroller Emulator Version	9-40
HIP7030A2	J1850 8-Bit 68HC05 Microcontroller	9-50
HIP7038A8	J1850 8-Bit 68HC05 Microcontroller 8K EEPROM Version	9-99
HIP9010	Engine Knock Signal Processor	10-44
HIP9020	Programmable Quad Buffer with Pre and Post Scaler Dividers	10-54
HV400	High Current MOSFET Driver	3-18
HV400MJ/883	High Current MOSFET Driver	3-28
HV-2405E	World-Wide Single Chip Power Supply	5-15
ICL7660	CMOS Voltage Converter	7-109
ICL7660S	Super Voltage Converter	7-118
ICL7662	CMOS Voltage Converter	7-128
ICL7663S	CMOS Programmable Micropower Positive Voltage Regulator	7-138
ICL7665S	CMOS Micropower Over/Under Voltage Detector	7-145
ICL7667	Dual Power MOSFET Driver	3-38
ICL7673	Automatic Battery Back-Up Switch	7-155
ICL8211	Programmable Voltage Detectors	7-161
ICL8212	Programmable Voltage Detectors	7-161
SP600	Half Bridge 500V_{DC} Driver	4-16
SP601	Half Bridge 500V_{DC} Driver	4-23
SP710	Protected Power Switch with Transient Suppression	8-3
SP720	Electronic Protection Array for ESD and Overvoltage Protection	8-5
SP720MD	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP720MD-8	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP720MM	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP720MM-8	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP721	Electronic Protection Array for ESD and Overvoltage Protection	8-14

Product Index by Family

		PAGE
AC TO DC CONVERTERS		
CA3059, CA3079	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
HV-2405E	World-Wide Single Chip Power Supply	5-15
FULL BRIDGES		
CA3275	Dual Full Bridge Driver	6-3
HIP4010	Power Full Bridge Driver for Low Voltage Motor Drive with Direction and Brake Control	6-7
HIP4011	Three Phase Brushless DC Motor Controller	6-11
HIP4080	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-14
HIP4080A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-28
HIP4081	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-41
HIP4081A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-54
HIP4082	80V/1.25A Peak Current Full Bridge FET Driver	6-67
HALF BRIDGES		
HIP2030	30V MCT/IGBT Gate Driver	4-3
HIP2500	Half Bridge 500V_{DC} Driver	4-10
SP600	Half Bridge 500V_{DC} Driver	4-16
SP601	Half Bridge 500V_{DC} Driver	4-23
HIGH SIDE SWITCHES		
CA3273	High-Side Driver	3-3
HIP1030	1A High Side Driver with Overload Protection	3-6
HIP1031	Half Amp High Side Driver with Overload Protection	3-10
HIP1090	Protected High Side Power Switch with Transient Suppression	3-13
HV400	High Current MOSFET Driver	3-18
HV400MJ/883	High Current MOSFET Driver	3-28
ICL7667	Dual Power MOSFET Driver	3-38
LOW SIDE SWITCHES		
CA3242	Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load	2-3
CA3262A, CA3262	Quad-Gated Inverting Power Drivers	2-7
CA3272, CA3272A, CA3292A	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
CA3282	CMOS Octal Serial Solenoid Driver	2-20
HIP0080, HIP0081	Quad Inverting Power Drivers with Serial Diagnostic Interface	2-28
HIP0082	Quad Power Driver with Serial Diagnostic Interface	2-36

		PAGE
MULTIPLEX COMMUNICATION CIRCUITS		
CDP68HC68S1	Serial Bus Interface	9-3
HIP7010	J1850 Byte Level Interface Circuit	9-17
HIP7020	J1850 Bus Transceiver I/O for Multiplex Wiring	9-33
HIP7030A0	J1850 8-Bit 68HC05 Microcontroller Emulator Version	9-40
HIP7030A2	J1850 8-Bit 68HC05 Microcontroller	9-50
HIP7038A8	J1850 8-Bit 68HC05 Microcontroller 8K EEPROM Version	9-99
PROTECTION CIRCUITS		
SP710	Protected Power Switch with Transient Suppression	8-3
SP720	Electronic Protection Array for ESD and Overvoltage Protection	8-5
SP720MD-8, SP720MD, SP720MM-8, SP720MM	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP721	Electronic Protection Array for ESD and Overvoltage Protection	8-14
REGULATORS/POWER SUPPLIES		
CA723, CA723C	Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors	7-3
CA1523	Voltage Regulator Control Circuit for Variable Switching Regulator	7-11
CA1524, CA2524, CA3524	Regulating Pulse Width Modulator	7-16
CA3085, CA3085A, CA3085B	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3277	Dual 5V Regulator with Serial Data Buffer Interface for Microcontroller Applications	7-39
HIP5060	Power Control IC Single Chip Power Supply	7-47
HIP5061	7A, High Efficiency Current Mode Controlled PWM Regulator	7-53
HIP5062	Power Control IC Single Chip Dual Switching Power Supply	7-73
HIP5063	Power Control IC Single Chip Power Supply	7-80
HIP5500	High Voltage IC Half Bridge Gate Driver	7-84
HIP5600	Thermally Protected High Voltage Linear Regulator	7-94
ICL7660	CMOS Voltage Converter	7-109
ICL7660S	Super Voltage Converter	7-118
ICL7662	CMOS Voltage Converter	7-128
ICL7663S	CMOS Programmable Micropower Positive Voltage Regulator	7-138
ICL7665S	CMOS Micropower Over/Under Voltage Detector	7-145
ICL7673	Automatic Battery Back-Up Switch	7-155
ICL8211, ICL8212	Programmable Voltage Detectors	7-161

SPECIAL FUNCTIONS

		PAGE
CA3020	Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz	10-3
CA3094	Programmable Power Switch/Amplifier for Control and General Purpose Applications	10-11
CA3165	Electronic Switching Circuit	10-25
CA3228	Speed Control System with Memory	10-31
CA3274	Current Limiting Power Switch with Current Limiter Sense Flag	10-40
HIP9010	Engine Knock Signal Processor	10-44
HIP9020	Programmable Quad Buffer with Pre and Post Scaler Dividers	10-54

Application Index

		PAGE
POWER SUPPLY APPLICATIONS		
CA723	Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors	7-3
CA723C	Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors	7-3
CA1523	Voltage Regulator Control Circuit for Variable Switching Regulator	7-11
CA1524	Regulating Pulse Width Modulator	7-16
CA2524	Regulating Pulse Width Modulator	7-16
CA3020	Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz	10-3
CA3085	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3085A	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3085B	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3094	Programmable Power Switch/Amplifier for Control and General Purpose Applications	10-11
CA3277	Dual 5V Regulator with Serial Data Buffer Interface for Microcontroller Applications	7-39
CA3524	Regulating Pulse Width Modulator	7-16
HIP2030	30V MCT/IGBT Gate Driver	4-3
HIP2500	Half Bridge 500V_{DC} Driver	4-10
HIP4080, A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-14
HIP4081, A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-41
HIP4082	80V/1.25A Peak Current Full Bridge FET Driver	6-67
HIP5060	Power Control IC Single Chip Power Supply	7-47
HIP5061	7A, High Efficiency Current Mode Controlled PWM Regulator	7-53
HIP5062	Power Control IC Single Chip Dual Switching Power Supply	7-73
HIP5063	Power Control IC Single Chip Power Supply	7-80
HIP5500	High Voltage IC Half Bridge Gate Driver	7-84
HIP5600	Thermally Protected High Voltage Linear Regulator	7-94
HV400	High Current MOSFET Driver	3-18
HV-2405E	World-Wide Single Chip Power Supply	5-15
ICL7660	CMOS Voltage Converter	7-109
ICL7660S	Super Voltage Converter	7-118
ICL7662	CMOS Voltage Converter	7-128
ICL7663S	CMOS Programmable Micropower Positive Voltage Regulator	7-138
ICL7665S	CMOS Micropower Over/Under Voltage Detector	7-145
ICL7667	Dual Power MOSFET Driver	3-38
ICL7673	Automatic Battery Back-Up Switch	7-155
ICL8211	Programmable Voltage Detectors	7-161
ICL8212	Programmable Voltage Detectors	7-161

PAGE

MOTOR CONTROL APPLICATIONS

CA3059	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
CA3079	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
CA3273	High-Side Driver	3-3
CA3275	Dual Full Bridge Driver	6-3
HIP2030	30V MCT/IGBT Gate Driver	4-3
HIP2500	Half Bridge 500V_{DC} Driver	4-10
HIP4010	Power Full Bridge Driver for Low Voltage Motor Drive with Direction and Brake Control	6-7
HIP4011	Three Phase Brushless DC Motor Controller	6-11
HIP4080, A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-14
HIP4081, A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-41
HIP4082	80V/1.25A Peak Current Full Bridge FET Driver	6-67
SP600	Half Bridge 500V_{DC} Driver	4-16
SP601	Half Bridge 500V_{DC} Driver	4-23

POWER INTERFACE AND AUTOMOTIVE APPLICATIONS

CA3059	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
CA3079	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
CA3242	Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load	2-3
CA3262	Quad-Gated Inverting Power Drivers	2-7
CA3262A	Quad-Gated Inverting Power Drivers	2-7
CA3272	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
CA3272A	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
CA3273	High-Side Driver	3-3
CA3274	Current Limiting Power Switch with Current Limiter Sense Flag	10-40
CA3282	CMOS Octal Serial Solenoid Driver	2-20
CA3292A	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
HIP0080, A	Quad Inverting Power Drivers with Serial Diagnostic Interface	2-28
HIP0081, A	Quad Inverting Power Drivers with Serial Diagnostic Interface	2-28
HIP0082	Quad Power Driver with Serial Diagnostic Interface	2-36
HIP1030	1A High Side Driver with Overload Protection	3-6
HIP1031	Half Amp High Side Driver with Overload Protection	3-10
HIP1090	Protected High Side Power Switch with Transient Suppression	3-13
HIP2500	Half Bridge 500V_{DC} Driver	4-10
HIP4011	Three Phase Brushless DC Motor Controller	6-11
HIP4080	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-14
HIP4081	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-41
HIP5500	High Voltage IC Half Bridge Gate Driver	7-84

PAGE

POWER INTERFACE AND AUTOMOTIVE APPLICATIONS (Continued)

HIP7010	J1850 Byte Level Interface Circuit	9-17
HIP7020	J1850 Bus Transceiver I/O for Multiplex Wiring	9-33
HIP7030A0	J1850 8-Bit 68HC05 Microcontroller Emulator Version	9-40
HIP7030A2	J1850 8-Bit 68HC05 Microcontroller	9-50
HIP7038A8	J1850 8-Bit 68HC05 Microcontroller 8K EEPROM Version	9-99
HIP9010	Engine Knock Signal Processor	10-44
HIP9020	Programmable Quad Buffer with Pre and Post Scaler Dividers	10-54
ICL7667	Dual Power MOSFET Driver	3-38
SP600	Half Bridge 500V_{DC} Driver	4-16
SP601	Half Bridge 500V_{DC} Driver	4-23

PROTECTION APPLICATIONS

SP710	Protected Power Switch with Transient Suppression	8-3
SP720	Electronic Protection Array for ESD and Overvoltage Protection	8-5
SP720MD	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP720MD-8	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP720MM	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP720MM-8	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP721	Electronic Protection Array for ESD and Overvoltage Protection	8-14

Intelligent Power Products Cross Reference List

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
AM723HC	CA0723CT	Pin	AMD
AM723HC	LM723CH	Pin	AMD
AM723HM	CA0723T	Pin	AMD
AM723HM	LM723H	Pin	AMD
AN377	CA3089E	Function	Panasonic
ATT2405	HV3-2405E-5	Pin	AT&T
ATT2405	HV3-2405E-9	Upgrade/Pin	AT&T
CA3089	CA3089E	Pin	Philips
CA3089N	CA3089E	Pin	Signetics
CA3189N	CA3189E	Pin	Signetics
CC192	HIP9010AB	Function	Bosch
D469ADJ	HIP0080AM	Function	Siliconix
D469ADJ	HIP0081AS1	Function	Siliconix
D469ADJ	HIP0081AS2	Function	Siliconix
DS3658N	CA3262AE	Upgrade/Pin	National Semi
DS3658N	CA3262E	Pin	National Semi
DS3668N	CA3242E	Pin	National Semi
HA12411	CA3189E	Upgrade	Hitachi
HA12418	CA3189E	Upgrade	Hitachi
ICL7660AMTV	ICL7660MTV	Pin	Maxim
ICL7660AMTV	ICL7660SMTV	Upgrade/Pin	Maxim
ICL7660CPA-2	ICL7660CPA	Pin	Maxim
ICL7660CPA-2	ICL7660SCPA	Upgrade/Pin	Maxim
ICL7660CSA	ICL7660CBA	Pin	Maxim
ICL7660CSA	ICL7660SCBA	Upgrade/Pin	Maxim
ICL7660CTV	ICL7660CTV	Pin	Maxim
ICL7660CTV	ICL7660SCTV	Upgrade/Pin	Maxim
ICL7660EPA	ICL7660IPA	Pin	Maxim
ICL7660EPA	ICL7660SIPA	Upgrade/Pin	Maxim
ICL7660ESA	ICL7660IBA	Pin	Maxim
ICL7660ESA	ICL7660SIBA	Upgrade/Pin	Maxim
ICL7660IJA	ICL7660IBA	Pin	Maxim

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
ICL7660IJA	ICL7660SIBA	Upgrade/Pin	Maxim
ICL7660ITV	ICL7660ITV	Pin	Maxim
ICL7660ITV	ICL7660SITV	Upgrade/Pin	Maxim
ICL7662CBA	ICL7662MTV	Pin	Maxim
ICL7662CBD	ICL7662CBD	Pin	Maxim
ICL7662CPA-2	ICL7662CPA	Pin	Maxim
ICL7662CTV	ICL7662CTV	Pin	Maxim
ICL7662MTV	ICL7662MTV	Pin	Maxim
ICL7663ACPA	ICL7663SACPA	Pin	Maxim
ICL7663ACSA	ICL7663SACBA	Pin	Maxim
ICL7663AIJA	ICL7663SAIJA	Pin	Maxim
ICL7663AITV	ICL7663SAITV	Pin	Maxim
ICL7663BCPA	ICL7663SACPA	Pin	Maxim
ICL7663BIJA	ICL7663SAIJA	Pin	Maxim
ICL7663BITV	ICL7663SAITV	Pin	Maxim
ICL7663CPA	ICL7663SCPA	Pin	Maxim
ICL7663CSA	ICL7663SCBA	Pin	Maxim
ICL7663CTV	ICL7663SCTV	Pin	Maxim
ICL7663IJA	ICL7663SIJA	Pin	Maxim
ICL7663ITV	ICL7663SAITV	Pin	Maxim
ICL7665ACJA	ICL7665SACJA	Pin	Maxim
ICL7665ACPA	ICL7665SACPA	Pin	Maxim
ICL7665ACSA	ICL7665SACBA	Pin	Maxim
ICL7665AEPA	ICL7665SAIPA	Pin	Maxim
ICL7665AIPA	ICL7665SAIPA	Pin	Maxim
ICL7665AISA	ICL7665SACBA	Pin	Maxim
ICL7665BCJA	ICL7665SACJA	Pin	Maxim
ICL7665BCPA	ICL7665SACPA	Pin	Maxim
ICL7665BCSA	ICL7665SACBA	Pin	Maxim
ICL7665CJA	ICL7665SCJA	Pin	Maxim
ICL7665CPA	ICL7665SCPA	Pin	Maxim

NOTE: 1. * Indicates Specifications May Vary

Intelligent Power Products Cross Reference List (Continued)

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
ICL7665CSA	ICL7665SCBA	Pin	Maxim
ICL7665EPA	ICL7665SIPA	Pin	Maxim
ICL7665ESA	ICL7665SIBA	Pin	Maxim
ICL7665IJA	ICL7665SIJA	Pin	Maxim
ICL7665IPA	ICL7665SIPA	Pin	Maxim
ICL7667CBA	ICL7667CBA	Pin	Maxim
ICL7667CJA	ICL7667CJA	Pin	Maxim
ICL7667CPA	ICL7667CPA	Pin	Maxim
ICL7667CPA-2	ICL7667CPA	Pin	Maxim
ICL7667CTV	ICL7667CTV	Pin	Maxim
ICL7667EPA	ICL7667CTV	Pin	Maxim
ICL7667MJA	ICL7667MJA	Pin	Maxim
ICL7667MTV	ICL7667MTV	Pin	Maxim
ICL8211CPA	ICL8211CPA	Pin	Maxim
ICL8211CSA	ICL8211CBA	Pin	Maxim
ICL8211CTY	ICL8211CTY	Pin	Maxim
ICL8211MTY	ICL8211MTY	Pin	Maxim
ICL8211MTY/ 883	ICL8211MTY/ 883B	Pin	Maxim
ICL8212CPA	ICL8212CPA	Pin	Maxim
ICL8212CSA	ICL8212CBA	Pin	Maxim
ICL8212CTY	ICL8212CTY	Pin	Maxim
ICL8212MTV	ICL8212MTY	Pin	Maxim
ICL8212MTV/ 883	ICL8212MTY/ 883B	Pin	Maxim
IR2110	HIP2500IP	Pin*	I.R.
IR2110-2	HIP2500IP1	Pin*	I.R.
IR2110S	HIP2500IB	Pin*	I.R.
IR2155	HIP5500IB	Upgrade	I.R.
IR2155	HIP5500IP	Upgrade	I.R.
IXCP10M25	HIP5600IS	Upgrade	IXYS
L4939	CA3277E	Function	SGS Thompson

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
L6221A	CA3262AE	Upgrade	SGS Thompson
L6222	CA3262AE	Upgrade	SGS Thompson
LM100	CA3085	Pin	National Semi
LM100	CA3085AE	Function	National Semi
LM100	CA3085E	Function	National Semi
LM1391N	CA1391E	Pin	National Semi
LM1394N	CA1394E	Pin	National Semi
LM1921T	HIP1030AS	Pin	National Semi
LM2111N	CA2111AE	Pin	National Semi
LM3011H	CA3011	Pin	National Semi
LM3089N	CA3089E	Pin	National Semi
LM3126N	CA3126E	Pin	National Semi
LM3189N	CA3189E	Pin	National Semi
LM3524	CA3524E	Pin	National Semi
LM723CN	CA0723CE	Pin	National Semi
LM723CN	LM723CN	Pin	National Semi
LM723H	LM723H	Pin	National Semi
LM723N	CA0723E	Pin	National Semi
LM723N	LM723N	Pin	National Semi
LMC7660IN	ICL7660IPA	Pin	National Semi
LMC7660IN	ICL7660SIPA	Upgrade/Pin	National Semi
LT1158	HIP4080IP	Upgrade	Linear Tech
LT1158	HIP4081IP	Upgrade	Linear Tech
LT1170CT	HIP5061DS	Function	Linear Tech
LT3524J	CA3524F	Pin	Linear Tech
LT3524N	CA3524E	Pin	Linear Tech
LTC1044CD	ICL7660IBA	Pin	Linear Tech
LTC1044CD	ICL7660SIBA	Upgrade/Pin	Linear Tech
LTC1044CH	ICL7660ITV	Pin	Linear Tech
LTC1044CH	ICL7660SITV	Upgrade/Pin	Linear Tech
LTC1044CLP-1	ICL7660IPA	Pin	Linear Tech

NOTE: 1. * Indicates Specifications May Vary

Intelligent Power Products Cross Reference List (Continued)

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
LTC1044CLP-1	ICL7660SIPA	Upgrade/Pin	Linear Tech
LTC1044CLP-2	ICL7660IPA	Pin	Linear Tech
LTC1044CLP-2	ICL7660SIPA	Upgrade/Pin	Linear Tech
LTC1044CN8	ICL7660IPA	Pin	Linear Tech
LTC1044CN8	ICL7660SIPA	Upgrade/Pin	Linear Tech
LTC1044CP	ICL7660IPA	Pin	Linear Tech
LTC1044CP	ICL7660SIPA	Upgrade/Pin	Linear Tech
LTC1044CS8	ICL7660IBA	Pin	Linear Tech
LTC1044CS8	ICL7660SIBA	Upgrade/Pin	Linear Tech
LTC1044MH	ICL7660MTV	Pin	Linear Tech
LTC1044MH	ICL7660SMTV	Upgrade/Pin	Linear Tech
LTC1044MLB	ICL7660MTV	Pin	Linear Tech
LTC1044MLB	ICL7660SMTV	Upgrade/Pin	Linear Tech
MAX1044CPA	ICL7660CPA	Pin	Maxim
MAX1044CPA	ICL7660SCPA	Upgrade/Pin	Maxim
MAX1044CSA	ICL7660CBA	Pin	Maxim
MAX1044CSA	ICL7660SCBA	Upgrade/Pin	Maxim
MAX1044EPA	ICL7660IPA	Pin	Maxim
MAX1044EPA	ICL7660SIPA	Upgrade/Pin	Maxim
MAX1044ESA	ICL7660IBA	Pin	Maxim
MAX1044ESA	ICL7660SIBA	Upgrade/Pin	Maxim
MAX660CPA	ICL7660CPA	Pin	Maxim
MAX660CPA	ICL7660SCPA	Upgrade/Pin	Maxim
MAX660CSA	ICL7660CBA	Pin	Maxim
MAX660CSA	ICL7660SCBA	Upgrade/Pin	Maxim
MAX660CTV	ICL7660CTV	Pin	Maxim
MAX660CTV	ICL7660SCTV	Upgrade/Pin	Maxim
MAX660EPA	ICL7660IPA	Pin	Maxim
MAX660EPA	ICL7660SIPA	Upgrade/Pin	Maxim
MAX660ESA	ICL7660IBA	Pin	Maxim
MAX660ESA	ICL7660SIBA	Upgrade/Pin	Maxim
MAX663CPA	ICL7663SCPA	Pin	Maxim

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
MAX663CPA-2	ICL7663SCPA	Pin	Maxim
MAX663CSA	ICL7663SCBA	Pin	Maxim
MAX663EJA	ICL7663SAIJA	Pin	Maxim
MAX663EJA	ICL7663SIJA	Pin	Maxim
MAX663EPA	ICL7663SIPA	Pin	Maxim
MAX663ESA	ICL7663SAIBA	Pin	Maxim
MAX663ESA	ICL7663SIBA	Pin	Maxim
MAX663IJA	ICL7663SCJA	Pin	Maxim
MAX663MJA	ICL7663SIJA	Pin	Maxim
MC1357P	CA2111AE	Pin	Motorola
MC1391P	CA1391E	Pin	Motorola
MC1394P	CA1394E	Pin	Motorola
MC1590	CA3012	Function	Motorola
MC1723CP	CA0723CE	Pin	Motorola
MC33033P	HIP4011IS	Function	Motorola
MC3399T	HIP1030AS	Function	Motorola
MC3399T	HIP1031AS	Function	Motorola
MC3399T	HIP1090AS	Function	Motorola
MC34152P	ICL7667CPA	Pin	Motorola
MC34160P	CA3277E	Function	Motorola
NTE1682	CA3237E	Function	NTE Electronics
SG2524BJ	CA2524F	Pin	Silicon General
SG2524BN	CA2524E	Pin	Silicon General
SG2524CF	CA2524F	Pin	Philips
SG2524CF	CA2524F	Pin	Signetics
SG2524CF	CA2524F	Pin	Silicon General
SG2524CN	CA2524E	Pin	Philips
SG2524CN	CA2524E	Pin	Signetics
SG2524J	CA2524F	Pin	Silicon General
SG2524N	CA2524E	Pin	SGS Thompson
SG2524N	CA2524E	Pin	Silicon General

NOTE: 1. * Indicates Specifications May Vary

Intelligent Power Products Cross Reference List (Continued)

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
SG2524N	CA2524E	Pin	Texas Instr.
SG3058J	CA3058	Pin	Silicon General
SG3059J	CA3059	Pin	Silicon General
SG3059N	CA3059EX	Pin	Silicon General
SG3079J	CA3079	Pin	Silicon General
SG3079N	CA3079EX	Pin	Silicon General
SG3524J	CA3524F	Pin	Silicon General
SG3524N	CA3524E	Pin	Silicon General
SG723CN	CA0723CE	Pin	Silicon General
SG723CN	CA0723CE	Pin	Silicon General
SG723CN	LM723CN	Pin	Silicon General
SG723CT	CA0723CT	Pin	Silicon General
SG723CT	LM723CH	Pin	Silicon General
SG723T	CA0723T	Pin	Silicon General
SG723T	LM723H	Pin	Silicon General
Si7660AA	ICL7660MTV	Pin	Siliconix
Si7660AA	ICL7660SMTV	Upgrade/Pin	Siliconix
Si7660AA/883	ICL7660MTV/ 883B	Pin	Siliconix
Si7660AA/883	ICL7660SMTV/ 883B	Upgrade/Pin	Siliconix
Si7660BA	ICL7660ITV	Pin	Siliconix
Si7660BA	ICL7660SITV	Upgrade/Pin	Siliconix
Si7660CA	ICL7660CTV	Pin	Siliconix
Si7660CA	ICL7660SCTV	Upgrade/Pin	Siliconix
Si7660CJ	ICL7660CPA	Pin	Siliconix
Si7660CJ	ICL7660SCPA	Upgrade/Pin	Siliconix
Si7660DJ	ICL7660IPA	Pin	Siliconix
Si7660DJ	ICL7660SIPA	Upgrade/Pin	Siliconix
Si7660DY	ICL7660CBA	Pin	Siliconix
Si7660DY	ICL7660IBA	Pin	Siliconix
Si7660DY	ICL7660SCBA	Upgrade/Pin	Siliconix
Si7660DY	ICL7660SIBA	Upgrade/Pin	Siliconix

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
Si7661AA	ICL7662MTV	Pin	Siliconix
Si7661AA/ 883B	ICL7662MTV/ 883B	Pin	Siliconix
Si7661BA	ICL7662ITV	Pin	Siliconix
Si7661CA	ICL7662CTV	Pin	Siliconix
Si7661CJ	ICL7662CPA	Pin	Siliconix
Si7661CY	ICL7662CBD	Pin	Siliconix
Si9910DJ	CA3262AE	Function	Siliconix
Si9910DJ	HIP1090AS	Function	Siliconix
SI9976CJ	HIP4080IP	Upgrade	Siliconix
SI9976CJ	HIP4081IP	Upgrade	Siliconix
SI9976DY	HIP4080IB	Upgrade	Siliconix
SI9976DY	HIP4081IB	Upgrade	Siliconix
SN75437ANE	CA3262AE	Pin	Texas Instr.
SN75437NE	CA3262E	Pin	Texas Instr.
SN75440NE	CA3242E	Function	Texas Instr.
SN76242N	CA3070	Function	Texas Instr.
SN76689N	CA3089E	Function	Texas Instr.
TBD0723	CA0723CT	Pin	SGS Thompson
TC4405CPA	HIP4080IP	Upgrade	Teledyne
TC4423CPA	ICL7667CPA	Pin	Teledyne
TC4423MJA	ICL7667MJA	Pin	Teledyne
TC4423MJA/ 883	ICL7667MJA/ 883B	Pin	Teledyne
TC4432COA	HIP4080IP	Upgrade	Teledyne
TCA3089	CA3089E	Pin	SGS Thompson
TCA3089	CA3089E	Pin	Sprague
TCA3189	CA3189E	Upgrade	SGS Thompson
TDA3189	CA3189E	Upgrade	Sprague
TDB0723	LM723CH	Pin	SGS Thompson
TDB0723A	CA0723CE	Pin	SGS Thompson

NOTE: 1. * Indicates Specifications May Vary

Intelligent Power Products Cross Reference List (Continued)

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
TDB0723A	LM723CN	Pin	SGS Thompson
TDC0723	CA0723T	Pin	TRW
TDC0723	LM723H	Pin	TRW
TPIC2801KV	CA3282AS1	Pin	Texas Instr.
TPIC2801KV	CA3282AS2	Pin	Texas Instr.
TPIC2802KV	CA3282AS2	Function	Texas Instr.
TSC4423CPA	ICL7667CPA	Pin	Teledyne
TSC4423MJA	ICL7667MJA	Pin	Teledyne
TSC7660COA	ICL7660CBA	Pin	Teledyne
TSC7660COA	ICL7660SCBA	Upgrade/Pin	Teledyne
TSC7660CPA	ICL7660CPA	Pin	Teledyne
TSC7660CPA	ICL7660SCPA	Upgrade/Pin	Teledyne
TSC7660CTV	ICL7660CTV	Pin	Teledyne
TSC7660CTV	ICL7660SCTV	Upgrade/Pin	Teledyne
TSC7662ACPA	ICL7662CPA	Pin	Teledyne
U5R7723312	CA0723T	Pin	Fairchild
U5R7723312	LM723H	Pin	Fairchild
U5R7723393	CA0723CT	Pin	Fairchild
U6A7723393	CA0723CE	Pin	Fairchild
U6A7723393	LM723CN	Pin	Fairchild
µA1391T	CA1391E	Pin	Fairchild
µA1394T	CA1394E	Pin	Fairchild
µA1394TC	CA1394E	Pin	Fairchild
µA3089E	CA3089E	Pin	Fairchild
µA723CA	CA0723CE	Pin	Signetics
µA723CA	LM723CN	Pin	Signetics
µA723CL	CA0723CT	Pin	Texas Instr.
µA723CL	LM723CH	Pin	Texas Instr.
µA723CN	CA0723CE	Pin	Philips
µA723CN	CA0723CE	Pin	Signetics

COMPETITOR PART NUMBERS	HARRIS PART NUMBERS	PIN/ FUNCTION UPGRADE	COMPETITOR
µA723CN	CA0723CE	Pin	Texas Instr.
µA723CN	LM723CN	Pin	Philips
µA723CN	LM723CN	Pin	Signetics
µA723CN	LM723CN	Pin	Texas Instr.
µA723HC	CA0723CT	Pin	AMD
µA723HC	LM723CH	Pin	Motorola
µA723HM	CA0723T	Pin	Fairchild
µA723HM	LM723H	Pin	Fairchild
µA723ML	CA0723T	Pin	Fairchild
µA723ML	LM723H	Pin	Texas Instr.
µA723MN	CA0723E	Pin	Texas Instr.
µA723PC	CA0723CE	Pin	Motorola
µA723PC	LM723CN	Pin	Motorola
µA780PC	CA3070	Upgrade	Fairchild
µA787PC	CA3126E	Upgrade	Fairchild
UC1524AJ	CA1524F	Pin	Unitrode
UC1524N	CA1524E	Pin	Unitrode
UC3524N	CA3524E	Pin	Unitrode
UDN2541B	CA3262AE	Pin	Sprague
UDN2547EB	CA3272Q	Pin	Sprague
ULN-2111A	CA2111AE	Pin	Sprague
ULN-2124A	CA3070	Pin	Sprague
ULN-2287A	CA3088E	Pin	Sprague
ULN-2289A	CA3089E	Function	Sprague
ULN-2289A	CA3089E	Function	Sprague
ULN-2291M	CA1391E	Pin	Sprague
ULN2111N	CA2111AQ	Pin	Sprague
ULN2212	CA3012	Function	Sprague
ULN3889A	CA3189E	Upgrade	Sprague
VI-7660-2	ICL7660CTV	Pin	Datel
VI-7660-2	ICL7660SCTV	Upgrade/Pin	Datel

NOTE: 1. * Indicates Specifications May Vary

INTELLIGENT POWER ICs 2

LOW SIDE SWITCHES

		PAGE
LOW SIDE SWITCHES SELECTION GUIDE		2-2
LOW SIDE SWITCHES DATA SHEETS		
CA3242	Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load	2-3
CA3262A, CA3262	Quad-Gated Inverting Power Drivers	2-7
CA3272, CA3272A, CA3292A	Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output	2-13
CA3282	CMOS Octal Serial Solenoid Driver	2-20
HIP0080, HIP0081	Quad Inverting Power Drivers with Serial Diagnostic Interface	2-28
HIP0082	Quad Power Driver with Serial Diagnostic Interface	2-36

Low Side Switches Selection Guide

BIPOLAR TYPES	TYPE NUMBERS				
	CA3242 QUAD	CA3262 QUAD	CA3262A QUAD	CA3272 CA3272A QUAD	CA3292A QUAD
Max. Output Voltage, No Load	50V	60V	60V	60V	32V Typ (Clamp)
Max. Rated DC Load Current	0.6A	0.7A	0.7A	0.6A	0.6A
Max. V_{SAT} Output Voltage	0.8V at 0.6A	0.6V at 0.6A	0.5V at 0.6A	0.4V at 0.5A	0.4V at 0.5A
Max. Load Switching Voltage, V_{CESUS} or V_{CLAMP} Limited	35V	40V	40V	40V	28V
Output Current Limiting and/or Shutdown Protection	1.4A (Latches-Off)	1.6A	1.3A	1.2A	1.2A
Output Thermal Limiting and/or Shutdown Protection (Temperature T_J)	No	+155°C	+155°C	+165°C	+165°C
Thermal Shutdown, Hysteresis	No	No	No	15°C	15°C
Fault Indicator Flag	No	No	No	Yes	Yes
Diagnostic Feedback	No	No	No	No	No
Temperature Range -40°C to +(Max) °C	105	85	125	125	125
Package	16 DIP	16 DIP	16 DIP and 28 PLCC	28 PLCC	28 PLCC

MOSFET TYPES	TYPE NUMBERS			
	HIP0080 QUAD	HIP0081 QUAD	HIP0082 QUAD	CA3282 OCTAL
Max. Output Voltage, No Load	36V Typ (Clamp)	80V Typ (Clamp)	80V Typ (Clamp)	32V Typ (Clamp)
Max. Rated DC Load Current	1A	2A	2A and 5A	1A
Max. R_{ON} Output Resistance	1.0Ω at 0.5A	0.5Ω at 1A	0.57Ω at 2A	1.0Ω at 0.5A
Max. Load Switching Voltage (V_{CESUS} or V_{CLAMP} Limited)	27V	73V	72V	30V
Output Current Limiting and/or Shutdown Protection	1.8A (Latches-Off)	3.5A (Latches-Off)	2.7A and 5.7A (Latches-Off)	1.5A (Latches-Off)
Output Thermal Limiting and/or Shutdown Protection, T_J	+150°C	+150°C	+165°C (Flag)	No
Thermal Shutdown, Hysteresis	15°C	15°C	15°C	No
Fault Indicator Flag	Yes	Yes	Yes	Yes
Diagnostic Feedback	Yes	Yes	Yes	Yes
Temperature Range -40°C to +(Max) °C	125	125	125	125
Package	28 PLCC	15 SIP	15 SIP	15 SIP

HARRIS SEMICONDUCTOR

CA3242

Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load

April 1994

Features

- Driven Outputs Capable of Switching 600mA Load Currents Without Spurious Changes in Output State
- Inputs Compatible with TTL or 5V CMOS Logic
- Suitable for Resistive or Inductive Loads
- Output Overload Protection
- Power-Frame Construction for Good Heat Dissipation

Applications

- Relays
- Solenoids
- AC and DC Motors
- Heaters
- Incandescent Displays
- Vacuum Fluorescent Displays

Description

The CA3242 quad-gated inverting power driver contains four gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

Output overload protection is provided when the load current (approximately 1.2A) causes the output V_{CE}(sat) to rise above 1.3V. A built-in time delay, nominally 25µs, is provided during output turn-on as output drops from V_{DD} to V_{SAT}. That output will be shut down by its protection network without affecting the other outputs. The corresponding Input or Enable must be toggled to reset the output protection circuit.

Steering diodes in the outputs in conjunction with external zener diodes protect the IC against voltage transients due to switching inductive loads.

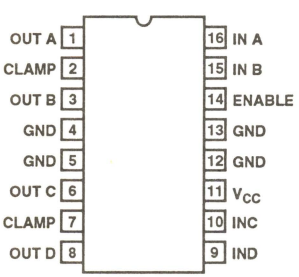
To allow for maximum heat transfer from the chip, the four center leads are directly connected to the die mounting pad. In free air, junction-to-air thermal resistance ($R_{\theta JA}$) is 60°C/W (typical). This coefficient can be lowered by suitable design of the PC board to which the CA3242 is soldered.

Ordering Information

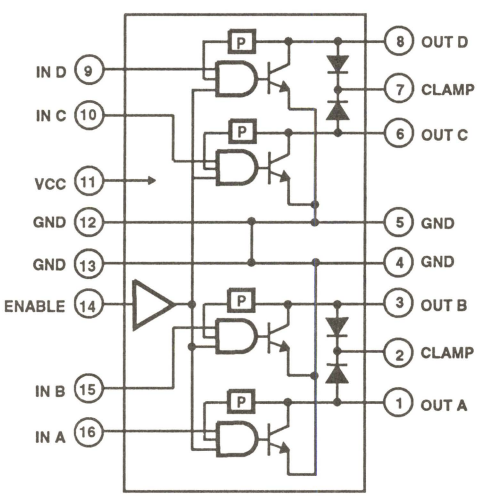
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3242E	-40°C to +105°C	16 Lead Plastic DIP

Pinout

CA3242 (PDIP)
TOP VIEW



Block Diagram



TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 1561.2

Absolute Maximum Ratings (Note 1)

Logic Supply Voltage, V_{CC} 7V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} ..... $50V_{DC}$
Output Sustaining Voltage, V_{CESUS} ..... $35V_{DC}$
Output Current, I_O ..... $1A_{DC}$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JL}
Plastic DIP	60°C/W	-
Plastic DIP (to Pins 4, 5, 12, 13)	-	12°C/W

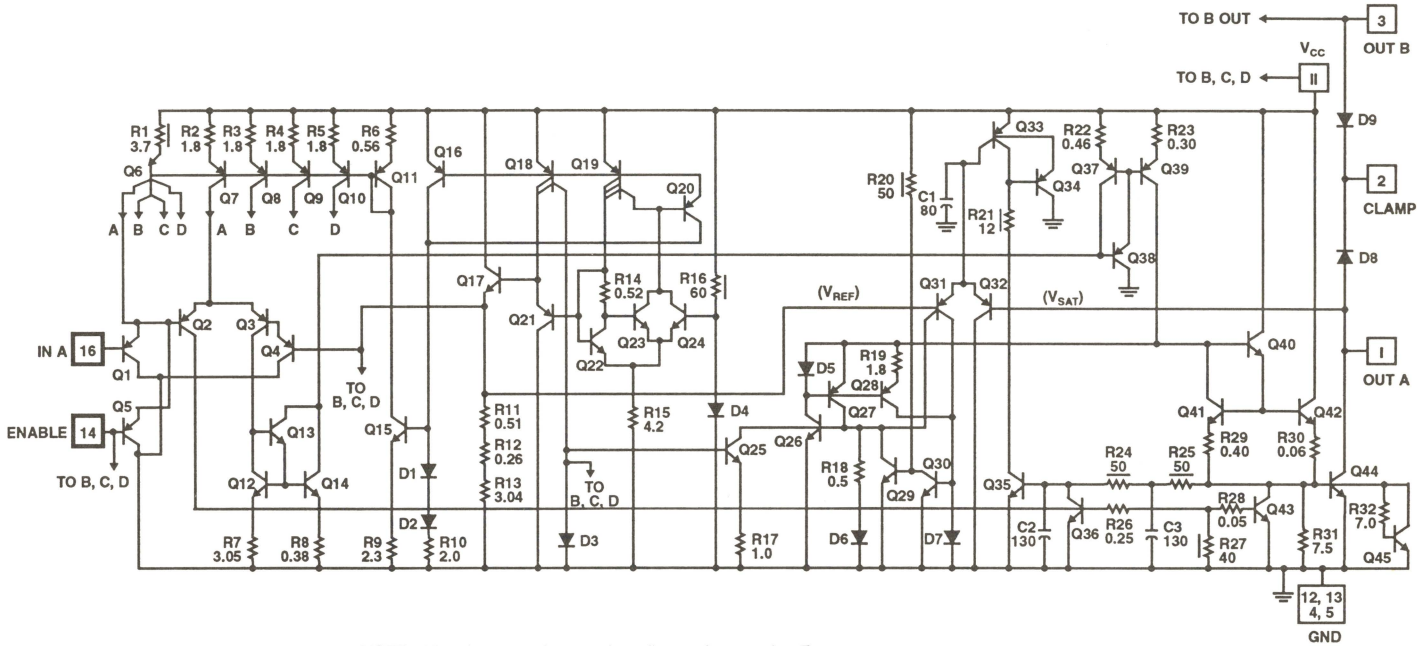
Power Dissipation, P_D
Up to 60°C 1.5W
Above 60°C ..... Derate Linearly at 16.6mW/°C
Up to 90°C w/Heat Sink (PC Board) 1.5W
Above 90°C w/Heat Sink (PC Board).. Derate Linearly at 25mW/°C
Ambient Temperature Range
Operating ..... -40°C to +105°C
Storage ..... -55°C to +150°C
Maximum Junction Temperature, T_J ..... +150°C
Lead Temperature (During Soldering)
At distance 1/16 inch ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = -40°C to +105°C, V_{CC} = 5V Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Output Leakage Current	I_{CEX}	V_{CE} = 50V, V_{IN} = 0.8V	-	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 100mA, V_{IN} = 0.8V	30	-	V
Collector Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100mA, V_{IN} = 2.4V	-	0.35	V
		I_C = 400mA, V_{IN} = 2.4V	-	0.6	V
		I_C = 600mA, V_{IN} = 2.4V	-	0.8	V
Input Low Voltage	V_{IL}		-	0.8	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	±10	µA
Input High Voltage	V_{IH}	I_C = 600mA	2	-	V
Input High Current	I_{IH}	I_C = 700mA, V_{IN} = 4.5V	-	10	µA
Supply Current ON	$I_{CC(ON)}$	I_C = 700mA, V_{CC} = V_{IH} = 5.5V	-	80	mA
Supply Current OFF	$I_{CC(OFF)}$		-	5	mA
Clamp Diode Leakage Current	I_R	V_R = 50V	-	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 1A	-	1.8	V
		I_F = 1.5A	-	2.5	V
Turn-On Delay	t_{PHL}		-	20	µs
Turn-Off Delay	t_{PLH}		-	30	µs

NOTE:
1. T_A = +25°C, Unless Otherwise Specified



NOTE: All resistance values are kΩ, all capacitors are in pF.

FIGURE 1. SCHEMATIC DIAGRAM OF THE CA3242 (SWITCH SECTION A)

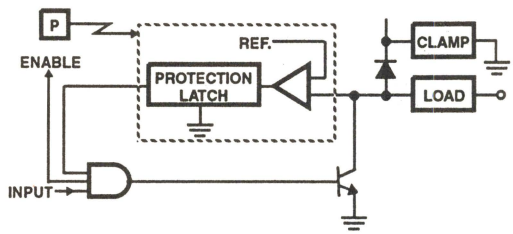


FIGURE 2. LOGIC DIAGRAM FOR EACH OUTPUT

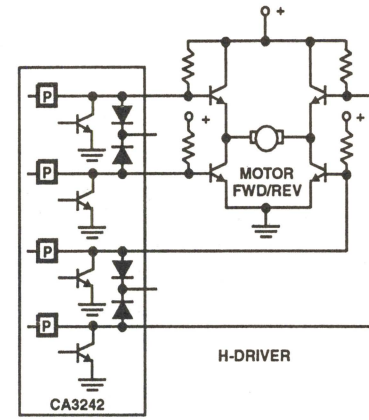


FIGURE 3. TYPICAL APPLICATIONS FOR THE CA3242 QUAD

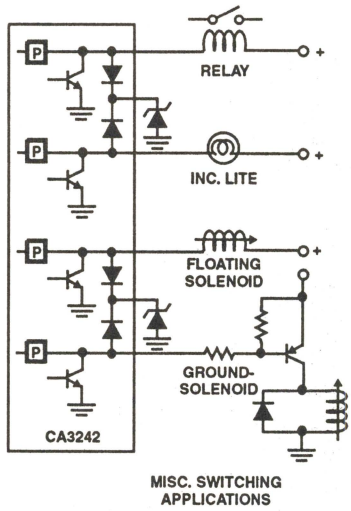


FIGURE 4. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER

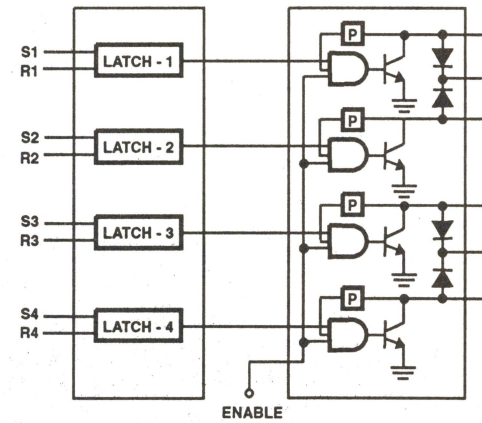


FIGURE 5. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER

CA3262A, CA3262

April 1994

Quad-Gated Inverting Power Drivers

Features

- Independent Over-Current Limiting on Each Output
- Independent Over-Temperature Limiting On Each Output
- Output Drivers Capable of Switching 700mA Load
- Inputs Compatible With TTL or 5V CMOS Logic
- Suitable For Resistive, Lamp or Inductive Loads
- Power-Frame Construction for Good Heat Dissipation
- Operational Temperature Ranges
  - CA3262A ..... -40°C to +125°C
  - CA3262 ..... -40°C to +85°C

Applications

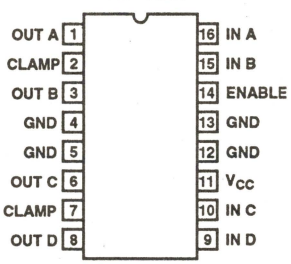
- Solenoid
- Relay
- Light
- Steppers
- Motors
- Displays

System Applications

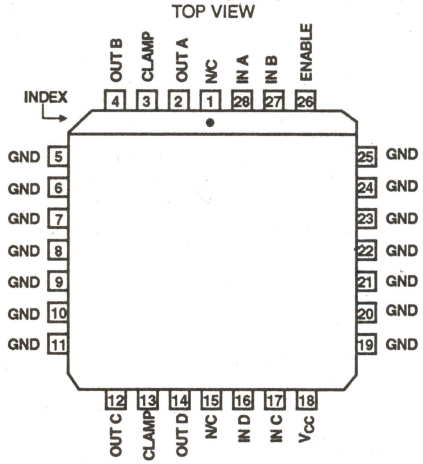
- Automotive
- Appliance
- Industrial Control
- Robotics

Pinouts

CA3262, CA3262A (PDIP)
TOP VIEW



CA3262A (PLCC)
TOP VIEW



Description

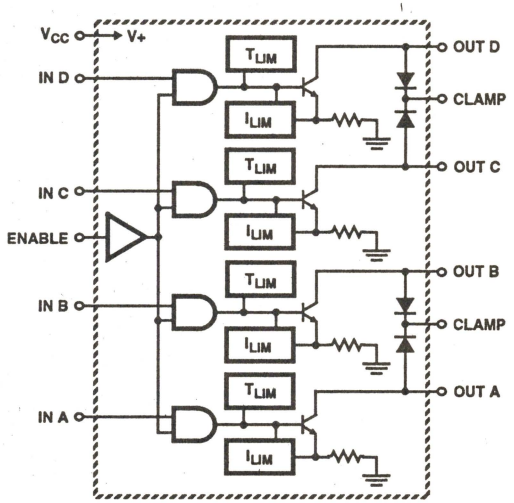
The CA3262 and CA3262A are used to interface low-level logic to high current loads. Each Power Driver has four inverting switches consisting of a non-inverting logic input stage and an inverting low-side driver output stage. All input stages have a common enable input. Each output device has independent current limiting (I_{LIM}) and thermal limiting (T_{LIM}) for protection from overload conditions. Steering diodes connected from each output (in pairs) to the Clamp pins may be used in conjunction with external zener diodes to protect the IC against overvoltage transients that result from inductive load switching. To allow for maximum heat transfer from the chip, all ground pins on the DIP and PLCC package are directly connected to the mounting pad of the chip. An integral heat spreading lead frame directly connects the bond pad and ground leads for good heat dissipation.

The CA3262 and CA3262A can drive four incandescent lamp loads without modulating their brilliance when the "cold" lamps are energized. Outputs may be parallel connected to drive high current loads. The maximum output current of each output is determined by the over-current limiting threshold which is typically 1.2A but may be as low as 0.7A.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CA3262E	-40°C to +85°C	16 Lead Plastic DIP
CA3262AE	-40°C to +125°C	16 Lead Plastic DIP
CA3262AQ	-40°C to +125°C	28 Lead PLCC

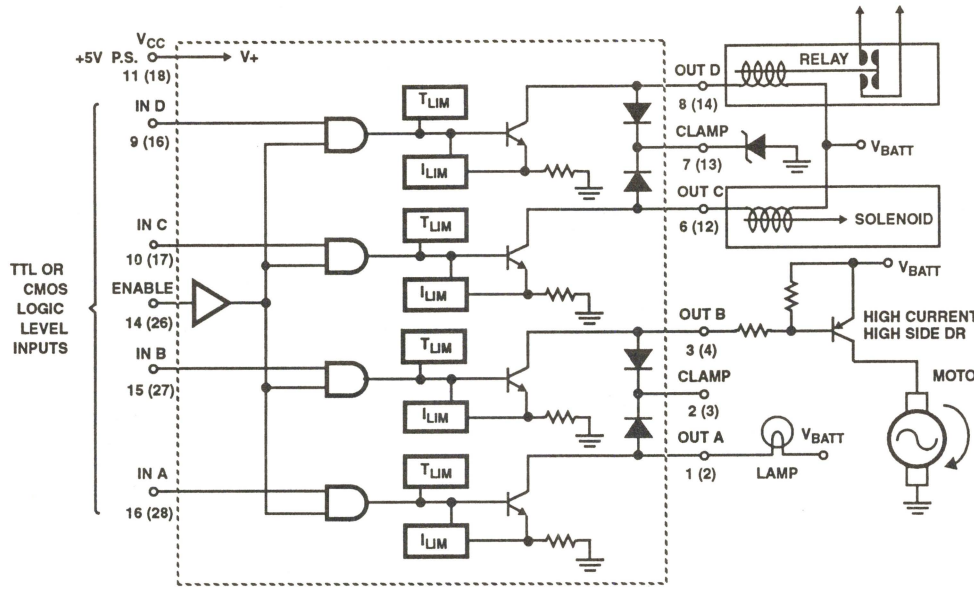
Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **1836.4**



TRUTH TABLE (Each Output)

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

PINS 4, 5, 12 & 13 GROUND (PACKAGE E)
PINS 5-11 & 19-25 GROUND (PACKAGE Q)
PIN #'S IN PARENTHESIS APPLY TO PACKAGE Q

FIGURE 1. QUAD INVERTING POWER DRIVER (QDR) SHOWN WITH TYPICAL APPLICATION LOADS

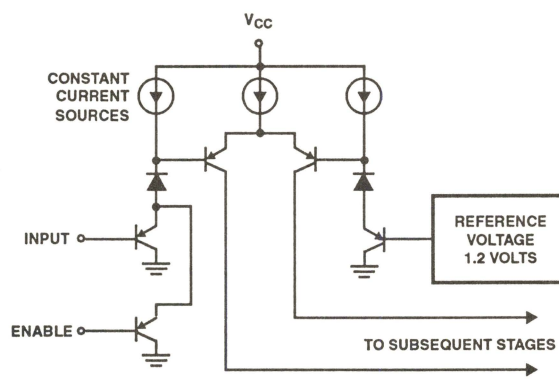


FIGURE 2. CA3262A EQUIVALENT SCHEMATIC OF ONE INPUT STAGE

Absolute Maximum Ratings

Logic Supply Voltage, V_{CC} 7.0V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} 60V
Output Sustaining Voltage, $V_{CE(SUS)}$ 40V
Output Transient Current ..... (Note 1)
Output Load Current ..... (Note 2)
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
CA3262AE, CA3262AQ ..... -40°C to +125°C
CA3262E ..... -40°C to +85°C

Thermal Information

Thermal Resistance (Note 3)	θ_{JA}
CA3262AQ	45°C/W
CA3262E, CA3262AE	60°C/W

Power Dissipation, P_D
CA3262E, CA3262AE
Up to +60°C (Free Air) 1.5W
Above +60°C ..... Derate Linearly at 16.6mW/°C
Up to +90°C With Heat Sink (PC Board) 1.5W
Above +90°C;
With Heat Sink (PC Board) ..... Derate Linearly at 25mW/°C
CA3262AQ
Up to +85°C (Free Air) 1.5W
Above +85°C ..... Derate Linearly at 23mW/°C
Up to +105°C with Heat Sink (PC Board) 1.5W
Above +105°C;
With Heat Sink (PC Board) ..... Derate Linearly at 33mW/°C
Maximum Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = 5.5V, T_A = -40°C to +125°C for CA3262A and V_{CC} = 5.5V, T_A = -40°C to +85°C for CA3262 Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Leakage Current	I_{CEX}	V_{CE} = 60V, V_{ENABLE} = 0.8V	-	-	100	-	0.6	50	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	Note 4	40	-	-	40	-	-	V
Collector Emitter Saturation Voltage (See Figures 4B & 5B)	$V_{CE(SAT)}$	V_{IN} = 2V, V_{CC} = 4.75V, I_C = 100mA	-	-	0.25	-	0.05	0.15	V
		I_C = 200mA	-	-	-	-	-	0.2	V
		I_C = 300mA	-	-	-	-	-	0.25	V
		I_C = 400mA	-	-	0.4	-	0.2	0.3	V
		I_C = 500mA	-	-	-	-	-	0.4	V
		I_C = 600mA	-	-	0.6	-	-	0.5	V
		I_C = 700mA, T_A = -40°C	-	-	0.6	-	-	0.5	V
Input Low Voltage	V_{IL}		-	-	0.8	-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	2	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	-	10	-	0.75	10	µA
Input High Current	I_{IH}	V_{IN} = V_{ENABLE} = 5.5V, I_C = 600mA	-	-	10	-	-	10	µA
Supply Current, All Outputs ON, (See Figures 4A and 5A)	$I_{CC(ON)}$	V_{IN} = 2V, V_{ENABLE} = 5.5V, I_{OUTA} = 250mA, I_{OUTB} = 250mA, I_{OUTC} = 250mA, I_{OUTD} = 250mA	-	-	70	-	(Note 4)	55	mA
Supply Current, All Outputs OFF, (See Figures 4A and 5A)	$I_{CC(OFF)}$	V_{IN} = 0V	-	-	5	-	(Note 4)	5	mA
Clamp Diode Leakage Current	I_R	V_R = 60V	-	-	100	-	-	50	µA
Clamp Diode Forward Voltage, (See Figures 4D and 5D)	V_F	I_F =1A, V_{IN} = 0V	-	-	1.7	-	-	1.7	V
		I_F =1.5A, V_{IN} = 0V	-	-	2.1	-	-	2.1	V
Turn-On Delay, (See Figures 4C and 5C)	t_{PHL}, t_{PLH}	I_{OUT} = 500mA	-	-	8	-	-	8	µs
Over Current Limiting	I_{LIM}	V_{OUT} = 2V, V_{IN} = 5.5V, V_{ENABLE} = 5.5V	0.7	-	(Note 1)	0.7	-	(Note 1)	A

Electrical Specifications V_{CC} = 5.5V, T_A = -40°C to +125°C for CA3262A and V_{CC} = 5.5V, T_A = -40°C to +85°C for CA3262 Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DESIGN PARAMETERS									
Over Temperature Limiting (Junction Temperature)	T_{LIM}		-	155	-	-	155	-	°C
Input Capacitance, Input	C_{IN}		-	-	-	-	3	-	pF
Enable Capacitance	C_{EN}		-	-	-	-	4.4	-	pF

NOTES:

1. The CA3262 and CA3262A have on-chip limiting for transient peak currents. Under short-circuit conditions with voltage applied to the collector of the output transistor and with the output transistor turned ON, the current will increase to 1.2A, typical. Over-Current Limiting protects a short circuit condition for a normal operating range of output supply voltage. During a short circuit condition, the output driver will shortly thereafter (approx. 5ms) go into Over-Temperature Limiting. While Over-Current Limiting may range to peak currents greater than 2A, each output will typically withstand a direct short circuit up to supply voltage levels of 16V. Excessive dissipation before thermal limiting occurs may cause damage to the chip for supply voltages greater than 18V. The CA3262 and CA3262A are rated to withstand peak current, cold turn-on conditions of #168 or #194 lamp loads.
2. The total DC current for the CA3262 and CA3262A with all 4 outputs ON should not exceed the total of (4 X 0.7A + Max. I_{CC}) ~ 2.85A. This level of current will significantly increase the chip temperature due to increased dissipation and may cause thermal shutdown in high ambient temperature conditions (See Absolute Maximum Ratings for Dissipation). Any one output may be allowed to exceed 0.7A but may be subject to Over-Current Limiting above the I_{LIM} min. limit of 0.7A. As a practical limit, no single output should be loaded to more than 1A max.
3. Normal applications require a surface mount of the 28 lead PLCC package on a PC Board. The package has a power lead frame construction where ground pins 5 - 11 and 19 - 25 conduct heat from the frame to the PC Board. With approximately a 2 square inch copper area adjacent to the ground pins, the thermal resistance on the mounted package may be as low as 30°C/W.
4. I_{CC} varies with temperature. Typically, $I_{CC(ON)}$ is 18mA at +125°C and 41mA at -40°C. Typically, $I_{CC(OFF)}$ is 2.2mA at +125°C and 1.2mA at -40°C.
5. Tested with a switched-off 500mA Load (24Ω series resistance), V_{BATT} = 12V and the outputs (V_{CE}) clamped to +40V maximum with an external zener diode.

Applications

Typical circuit configurations for applying the CA3262 and CA3262A are shown in the application circuit of Figure 1. To their rated capabilities, both circuits can be used to drive inductive, resistive and lamp loads. The CA3262A has a lower V_{SAT} than the CA3262 and is rated for +125°C ambient temperature applications. The CA3262 data sheet rating is +85°C. Otherwise, the protection features described apply to both the CA3262 and CA3262A.

The maximum voltage for full load current switching is the output sustaining voltage, $V_{CE(SUS)}$ which should not exceed 40 Volts. To provide a means of over-voltage protection, on-chip steering diodes are connected from each output to one of two CLAMP pins. Over-voltage pulses may be generated from inductive load switching and must be clamped or limited to a peak voltage less than $V_{CE(SUS)}$. To limit an inductive voltage pulse, a zener diode should be connected to the appropriate CLAMP pin. When the voltage pulse exceeds the zener threshold, the excess energy is dumped to ground via the on-chip steering diode and the external zener diode.

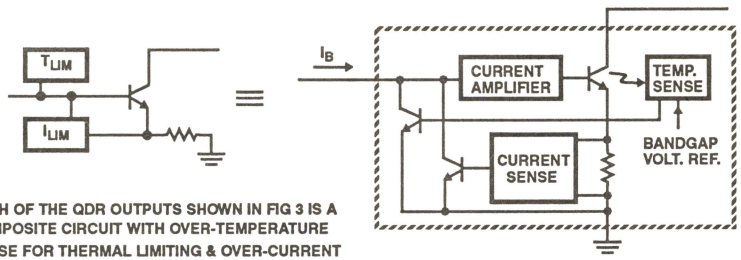
The on-chip diodes may be used in a free-wheeling mode by connecting the CLAMP pins to an external clamp supply voltage. Zener diode clamp protection is preferred over the power supply clamp option, primarily because the power supplies may be subject to large transient changes; including turn-ON and turn-OFF conditions where non-tracking conditions between supplies could allow forward conduction through the steering diodes. For all transient conditions of either method, the clamp voltage should greater than the maximum supply voltage of the switching outputs and less than $V_{CE(SUS)}$.

Note that the rate of change of the output current during load switching is fast. Therefore, even small values of inductance, including the inductance of a few meters of hook-up wire to the load circuit, can generate voltage spikes of considerable amplitude at the output terminals and may require clamping to protect the device ratings.

Current-limiting is provided as protection for shorted or overloaded output conditions. Voltage is sampled across a small metal resistor in the emitter of each output stage. When the voltage exceeds a preset comparator level, drive is reduced to the output. Current limiting is sustained unless thermal conditions exceed the preset thermal shutdown temperature of +155°C.

If an output is shorted, the remaining three outputs will continue to function normally unless the continued heat spreading is sufficient to raise the junction temperature at any other output to a level greater than +155°C. High ambient temperature conditions may allow this to happen. The degree of interaction is minimized at chip layout design by separating the output devices, each to a separate corner of the chip.

As noted, the thermal resistance values of both the DIP and PLCC packages are improved by direct connection of the leads to the chip mounting pad. In free air, the junction-to-air thermal resistance, θ_{JA} is +60°C/W (typical) for the DIP package and +42°C/W (typical) for the PLCC package. This coefficient can be lowered to +40°C/W and +30°C/W respectively by increasing ground copper area on the PC board next to the ground pins of the IC.



EACH OF THE QDR OUTPUTS SHOWN IN FIG 3 IS A COMPOSITE CIRCUIT WITH OVER-TEMPERATURE SENSE FOR THERMAL LIMITING & OVER-CURRENT SENSE TO PROVIDE CURRENT LIMITING

FIGURE 3. QUAD INVERTING POWER DRIVER (QDR) OUTPUT EQUIVALENT CIRCUIT

Typical Performance Curves

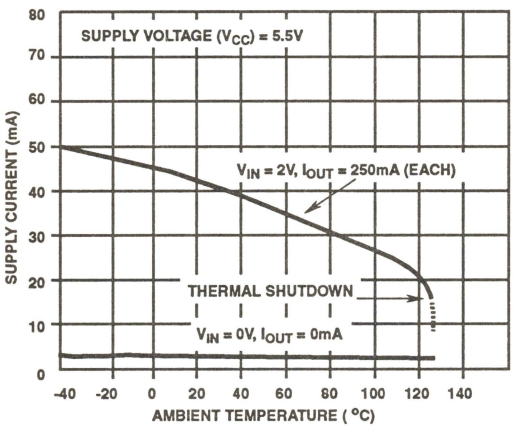


FIGURE 4A. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

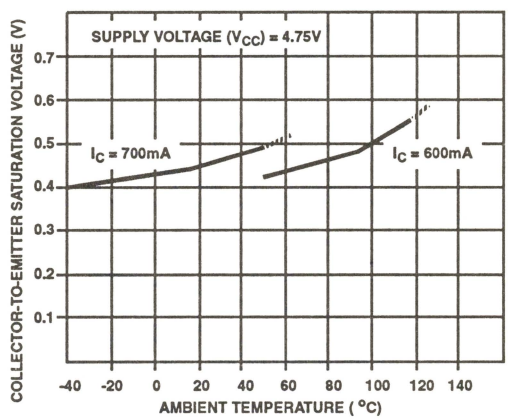


FIGURE 4B. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING POWER DRIVER OUTPUT

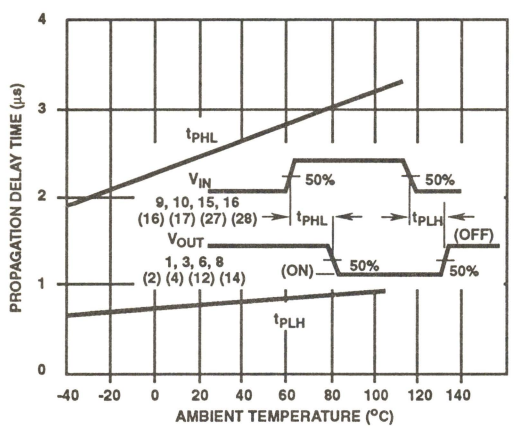


FIGURE 4C. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

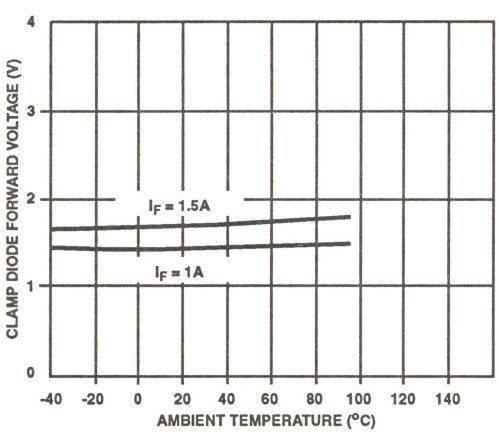


FIGURE 4D. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

FIGURE 4. TYPICAL CHARACTERISTICS OF THE CA3262E

Typical Performance Curves (Continued)

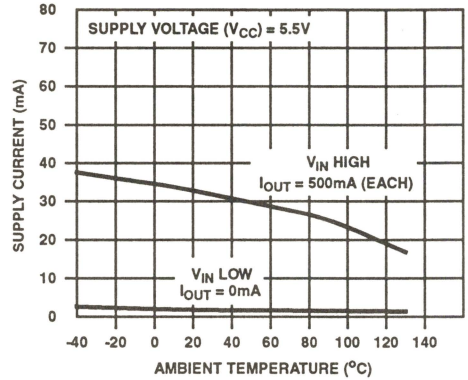


FIGURE 5A. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

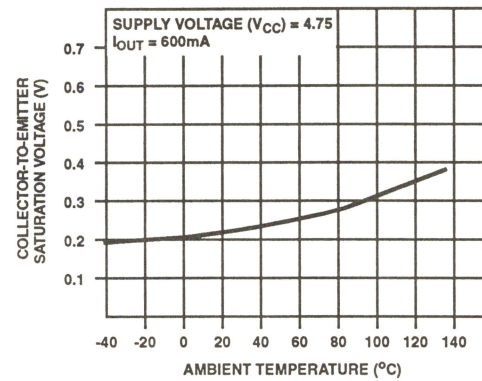


FIGURE 5B. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING-POWER DRIVER OUTPUTS

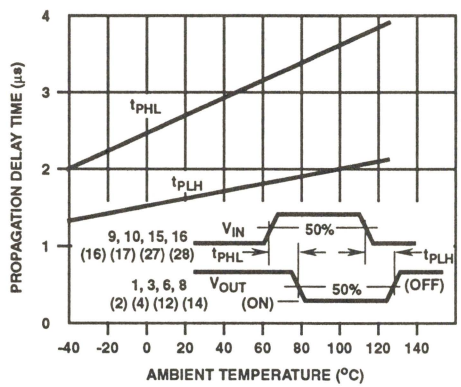


FIGURE 5C. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

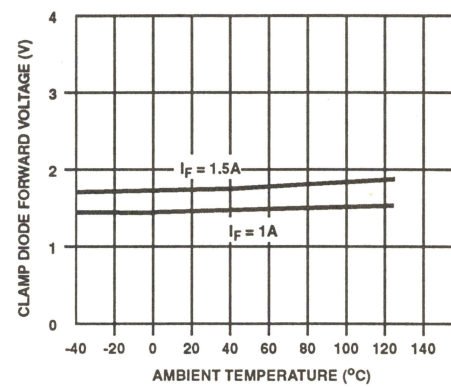


FIGURE 5D. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

FIGURE 5. TYPICAL CHARACTERISTICS OF THE CA3262AE & CA3262AQ

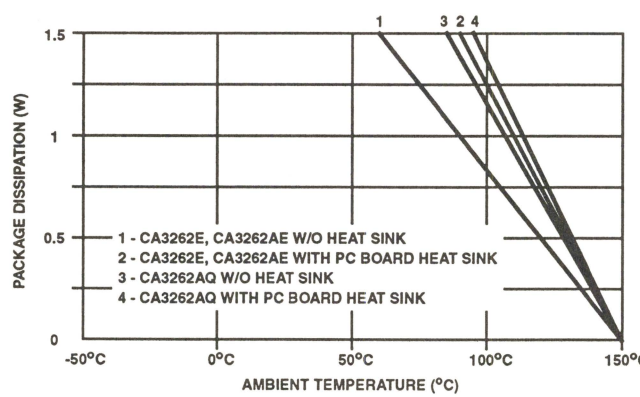


FIGURE 6. PACKAGE DISSIPATION RATING CHART

HARRIS SEMICONDUCTOR

CA3272
CA3272A, CA3292A

Quad-Gated Inverting Power Drivers with Fault Mode Diagnostic Flag Output

PRELIMINARY*

April 1994

Features

- Load Current Switching 600mA
- Suitable for Resistive or Inductive Loads
- Fault Mode Diagnostic Flag Output
- CA3292A Over-Voltage Zener Clamp
- Independent Over-Current Limiting
- Independent Over-Temperature Shutdown
- Temperature Shutdown Hysteresis
- 5V CMOS or TTL Input Logic
- High Dissipation Power-Frame Package
- Operating Temperature Range -40°C to +125°C

Applications

- Solenoids
- Relays
- Lamps
- Steppers
- Injectors
- Motors

System Applications

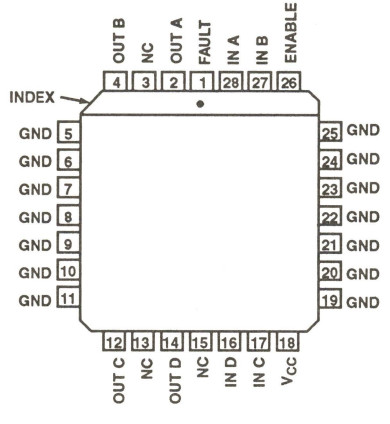
- Automotive
- Appliance
- Industrial Control
- Robotics

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3272Q	-40°C to +125°C	28 Lead PLCC
CA3272AQ	-40°C to +125°C	28 Lead PLCC
CA3292AQ	-40°C to +125°C	28 Lead PLCC

Pinout

CA3272, CA3272A, CA3292A (PLCC)
TOP VIEW



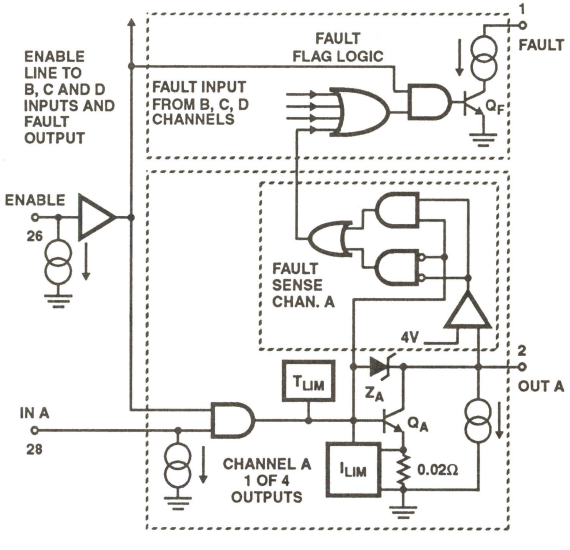
Description

The CA3272, CA3272A* and CA3292A* are Quad-Gated Inverting Power Drivers for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors and resistive loads such as incandescent lamps and other power drivers. Each output is an open collector protected power transistor driver. The CA3292A is similar to the CA3272 and CA3272A, except for an added collector-to-base zener diode that provides over-voltage clamping protection on each power switching output. The CA3292A block diagram is shown for one switching channel with fault detection logic plus the output fault driver circuit for all four switching channels. The CA3272A and CA3292A have increased pull-down current drive from the FAULT output pin. The FAULT output pin provides a flag output when a fault condition occurs. The complete Functional Block Diagram with all four Output Power Driver stages is shown on page 2.

The ENABLE input is common to each of the four power switches and when low, disables the FAULT output. From the Input to Output, each switch is inverting. When IN is high, OUT is low and the transistor switch is "ON" (conducting). The block diagram shows the functional logic associated with fault detection. The Fault Sense circuit detects the IN and OUT states and switches Q_F "ON" if a fault is detected. When a fault is detected, transistor Q_F activates a current sink pull-down at the FAULT pin. A resistive load from the FAULT pin to the power supply is used to detect a fault as a low state. Both shorted and open load conditions are detected.

Block Diagram of the CA3292A

(1 of 4 Outputs and Fault Logic)

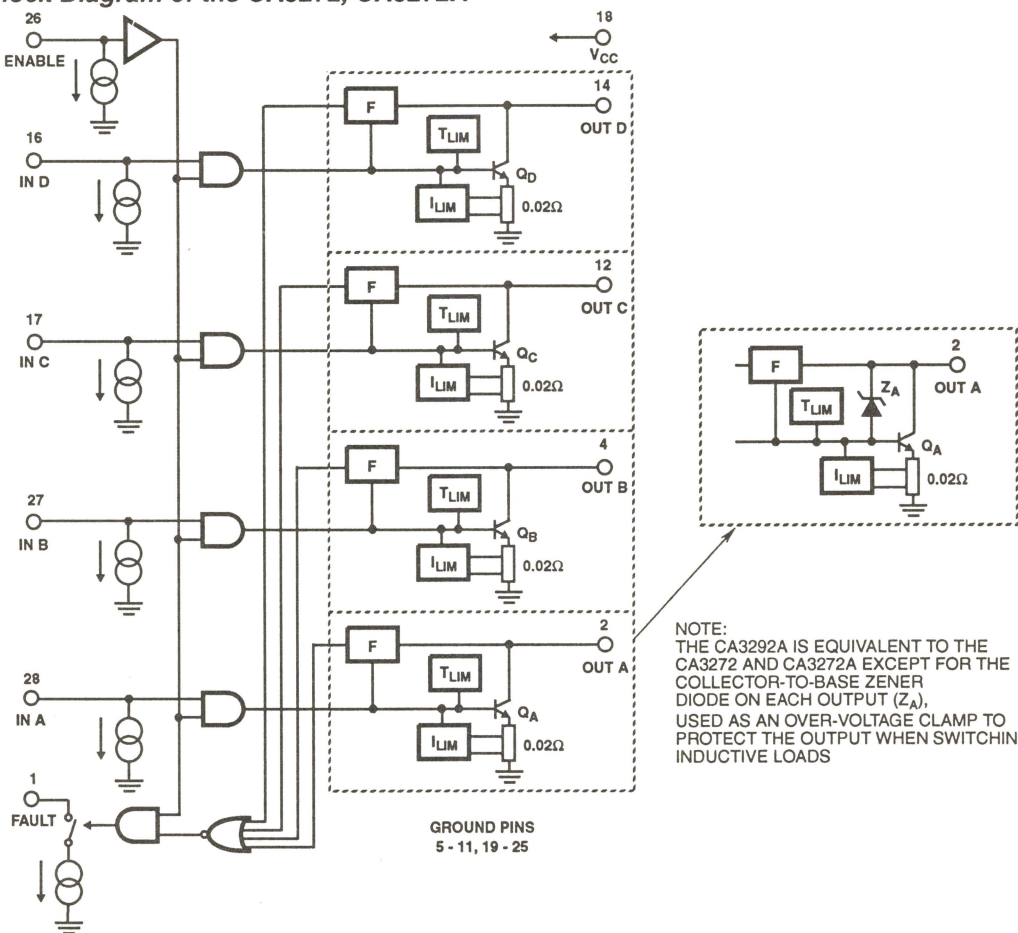


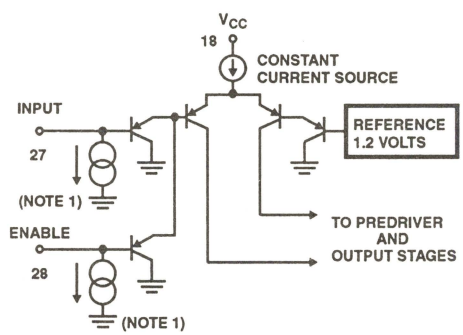
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2223.4**

Block Diagram of the CA3272, CA3272A





NOTE:
1. INPUT AND ENABLE PULLDOWN SOURCES FORCE OUTPUT TURN-OFF FOR UNTERMINATED INPUTS

FIGURE 1. SCHEMATIC OF ONE INPUT STAGE

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

FAULT LOGIC TABLE

IN	OUT	FAULT	MODE
H	L	H	Normal
H	H	L	Over Current, Over Temperature Open Load or Short to Power Supply
L	L	L	
L	H	H	Normal

Absolute Maximum Ratings

Output Voltage, V_O (CA3272, CA3272A) ..... +60V
Output Sustaining Voltage, $V_{CE(SUS)}$ (CA3272, CA3272A)..... 40V
Output Voltage, V_O (CA3292A)..... V_{CLAMP}
Output Clamp Energy, E_{OK} (CA3292A) ..... TBDmJ
Output Transient Current, (Note 1)..... 1.6A Max.
Output Load Current, (Note 2) 0.7A
Supply Voltage, V_{CC} ..... +7V
Logic Input Voltage, V_{IN} 15V
FAULT Output Voltage, V_F 16V
Operating Temperature Range.....-40°C to +125°C
Junction Temperature..... +150°C

Thermal Information

Thermal Resistance..... θ_{JA}
PLCC..... 45°C/W
PLCC (With PC Board Heat Sink)..... 30°C/W
Power Dissipation (No Heat Sink)
Up to +85°C 1.5W
Above +85°C .....Derate Linearly at 23mW/°C
Power Dissipation: (With PC Board Heat Sink, Note 3)
Up to +85°C 2.2W
Above +85°C .....Derate Linearly at 33mW/°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (Soldering 10s) .....+265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +125°C, V_{CC} = 5.5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3272			CA3272A, CA3292A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT PARAMETERS									
Output (OFF) Current	I_{CEX}	V_{IN} = 0.8V; V_{EN} = 5.5V; (Note 4) V_{CE} = 60V for CA3272, CA3272A; V_{CE} = 24V for CA3292A	-	30	100	-	30	100	µA
Output Sustaining Voltage: CA3272, CA3272A	$V_{CE(SUS)}$	Note 7	40	-	-	40	-	-	V
Output Clamp Voltage: CA3292A	V_{CLAMP}	I_C = 300µA; V_{EN} = 0.8V	-	-	-	28	32	36	V
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = 2V, V_{CC} = 4.75V, I_C = 400mA, T_A = +125°C	-	-	0.4	-	-	0.3	V
		I_C = 500mA, T_A = +25°C	-	-	0.5	-	-	0.4	V
		I_C = 600mA, T_A = -40°C	-	-	-	-	-	0.5	V
		I_C = 500mA, T_A = -40°C	-	-	0.6	-	-	-	V
LOGIC INPUT THRESHOLDS									
Input Low Voltage	V_{IL}	V_{CC} = 3.5V	-	-	0.8	-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	2	-	-	V
Input Low Current	I_{IL}	V_{IN} = V_{EN} = 0.8V; V_{CC} = 4.75V	10	45	70	10	45	70	µA
Input High Current	I_{IH}	V_{IN} = V_{EN} = 5.5V	10	45	70	10	45	70	µA
SUPPLY CURRENT									
All Outputs ON	$I_{CC(ON)}$	V_{IN} = V_{EN} = 5.5V; I_{OUTA} = I_{OUTB} = I_{OUTC} = I_{OUTD} = 400mA	-	-	65	-	-	65	mA
All Outputs OFF	$I_{CC(OFF)}$	V_{IN} = 0V	-	-	10	-	-	10	mA
PROPAGATION DELAY									
Turn-ON Delay	t_{PHL}	I_{LOAD} = 500mA	-	3	10	-	3	10	µs
Turn-OFF Delay	t_{PLH}	I_{LOAD} = 500mA	-	3	10	-	3	10	µs
FAULT PARAMETERS									
Output Low Current, $I_{F(SINK)}$ (with Fault)	I_{OL}	V_{IN} = 0.8V; V_{EN} = 2.0V; V_F = 4V V_{OUT} = Low = 1V; (Note 5)	0.04	0.09	0.12	1	2	4	mA
Output High Current, $I_{F(LK)}$	I_{OH}	No Fault (Note 5)	-	-	2	-	-	20	µA

Electrical Specifications T_A = -40°C to +125°C, V_{CC} = 5.5V, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3272			CA3272A, CA3292A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Low Voltage	V_{OL}	External Load Equal Min. I_{OL}	-	0.2	0.4	-	0.2	0.4	V
Output Driver Fault Sense, High Threshold (Open)	V_{HTHD}	V_{IN} = 0.8V; V_{EN} = 2V (Note 6)	3	4	5.5	3	4	5.5	V
Output Driver Fault Sense, Low Threshold (Short)	V_{LTHD}	V_{IN} = V_{EN} = 2V (Note 6)	3	4	5.5	3	4	5.5	V
PROTECTION PARAMETERS									
Over-Current Limiting	I_{LIM}	V_{IN} = V_{EN} = 2V, V_{OUT} = 4Ω to 16V	0.6	-	Note 1	0.6	-	Note 1	A
Over-Temperature Limiting (Junction Temperature)	T_{LIM}		-	165	-	-	165	-	°C
Over-Temperature Limiting, Hysteresis	T_{HYS}		-	15	-	-	15	-	Δ°C
DESIGN PARAMETERS									
Input Capacitance	C_{IN}		-	3	-	-	3	-	pF
Enable Capacitance	C_{EN}		-	4.6	-	-	4.6	-	pF

NOTES:

1. Output Transient Currents are controlled by on-chip limiting for each output. Under short-circuit conditions with voltage applied to the collector of the output transistor and with the output transistor turned ON, the current will increase to 1.2A, typical. Over-Current Limiting protects a short circuit condition for a normal operating range of output supply voltage. During a short circuit condition, the output driver will shortly thereafter (approx. 5ms) go into Over-Temperature Shutdown. While Over-Current Limiting may range to peak currents as high as 1.6A, each output will typically withstand a direct short circuit at normal single battery supply levels. Excessive dissipation before thermal shutdown occurs may cause damage to the chip for supply voltages greater than 16V. When sequentially switched, the outputs are rated to withstand peak current, cold turn-on conditions of lamp loads such as #168 or #194 lamps.
2. The total DC current with all 4 outputs ON should not exceed the total of (4 X 0.7A + Max. I_{CC}) ~ 2.85A. This level of current will significantly increase the chip temperature due to increased dissipation and may cause thermal shutdown in high ambient temperature conditions (See Absolute Maximum Ratings for Dissipation). Any one output may be allowed to exceed 0.7A but may be subject to Over-Current Limiting above the I_{LIM} minimum limit of 0.7A. No single output should be loaded to more than Over-Current Limiting above the I_{LIM} minimum limit of 0.7A. As a practical limit, no single output should be loaded to more than 1A maximum.
3. Normal applications require a surface mount of the 28 lead PLCC package on a PC Board. The package has a power lead frame construction where ground pins 5 - 11 and 19 - 25 conduct heat from the frame to the PC Board. With approximately a 2 square inch copper area adjacent to the ground pins, the thermal resistance on the mounted package may be as low as 30°C/W.
4. I_{CEX} is the static leakage current at each output when that output is OFF (ENABLE Low). Refer to the Figure 3 illustration of an output stage. The value of I_{CEX} is both the leakage into the output driver and a pull-down current sink, $I_{O(SINK)}$. The purpose of the current sink is to detect open load conditions.
5. The I_{OL} value of "Output Low Current, $I_{F(SINK)}$" at the FAULT pin is both the static leakage of the output driver Q_F and the current sink, $I_{F(SINK)}$. The current sink is active only when a fault exists. When no fault exists, the I_{OH} current at the FAULT pin is the maximum leakage current, $I_{F(LK)}$. Refer to Figure 2 for an illustration of the FAULT output and associated external components. Refer to FAULT LOGIC TABLE for Fault Modes.
6. The Voltages, V_{HTHD}, V_{LTHD} are the comparator threshold reference values (Min. & Max. Range) sensed as a high and low state transitions for voltage forced at the outputs. V_{HTHD} indicates an open load fault when the output is decreased to less than the threshold. V_{LTHD} indicates a shorted load when the output is increased greater than the threshold. The output voltage is changed until the FAULT pin indicates a Low (Fault). Refer to Figure 2 for test value of external resistor. Refer to I_{OL} and I_{OH} FAULT PARAMETERS Test Limits to determine V_{OL} and V_{OH} at the FAULT pin.
7. Tested with 120mA switched off in a Load of 70mH and 32Ω series resistance;
   CA3272, CA3272A: Outputs clamped with an external zener diode, limiting V_{OUT} to the $V_{CE(SUS)}$ maximum rating of +40V.
   CA3292A: Outputs limited to the V_{CLAMP} voltage by the internal collector-to-base zener diode and output transistor clamp.

Applications

The CA3272, CA3272A and CA3292A are quad-gated inverting low-side power drivers with a fault diagnostic flag output. Both circuits are rated for +125°C ambient temperature applications and have current limiting and thermal shutdown. While functionally similar to the CA3262AQ, they differ in the mode of over-voltage protection and have the added feature of a FAULT flag output. Also, inputs to channels A, B, C, D and ENABLE have internal pulldowns to turn "OFF" the outputs when the inputs are floating.

As noted in the Block Diagrams, the CA3292A is equivalent to the CA3272 and CA3272A except that it has internal clamp diodes on the outputs to handle inductive switching pulses from the output load. The structure of each CA3292A output includes a zener diode from collector-to-base of the output transistor. This is a different form of protection from other quad drivers with current steering clamp diodes on each output, paired to one of two "CLAMP" output pins. The CA3292A output transistor will turn-on at the zener diode clamp voltage threshold which is typically 32V and the output transistor will dump the pulse energy through the output driver to ground.

Each output driver is capable of switching 600mA load currents and operate at +125°C ambient temperature without interaction between the outputs. The CA3272, CA3272A and CA3292A can drive four incandescent lamp loads without modulating their brilliance when the "cold" lamps are energized. The outputs can be connected in parallel to drive larger loads. Overcurrent or short circuit output load conditions are fault protected by current limiting with a typical limit value of 1.2A. The current limiting range is set for 0.6A to 1.6A. The output stage does not change state (oscillate) when in the current limit mode. Any one output that faults (see Fault Logic Table) will switch the FAULT output at pin 1 to a constant current pull-down.

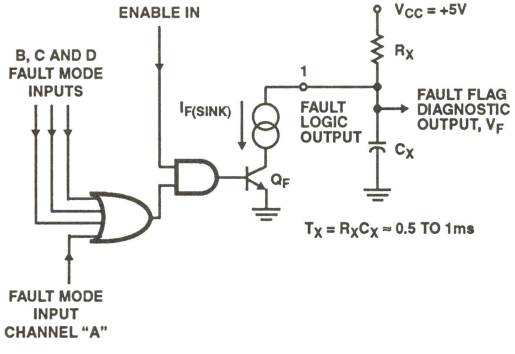


FIGURE 2. EXTERNAL FAULT OUTPUT CIRCUIT AND $I_{F(SINK)}$ AS FAULT SINK PULLDOWN CURRENT, WHICH IS ACTIVATED BY TRANSISTOR, Q_F, WHEN A FAULT EXISTS

The Fault Logic circuit, as shown in the Block Diagram for the CA3292A, applies to both the CA3272, CA3272A and CA3292A. The Fault Sense circuits do not override or control the power switching circuits of the IC. Their primary function is to provide an external diagnostic fault flag output. Each Power Switching Channel has diagnostic fault sensing input to the Fault Logic. The Fault Logic block of the functional Block Diagram illustrates the logic functions associated with Fault detection. The diagnostic output for each of the four channels of switching is processed through the fault logic circuit associated with each channel. It is then passed to an OR gate which controls the FAULT flag output transistor, Q_F thru a 2 input AND gate.

The ENABLE input is common to each of the 4 power switches and also disables the FAULT flag output at the 2 input AND gate when it is low. The Fault Logic circuit senses the IN and OUT states and switches Q_F "ON" if a fault is detected. Transistor Q_F activates a sink current source to pull-down the FAULT pin to a 0 (low) state when the fault is detected. Both shorted and open load conditions are detected.

It is normal for thermal shutdown and current limiting to occur sequentially during a short circuit fault condition. A precaution applies for potential damage from high transient dissipation during thermal shutdown. (See Note 1 following the Electrical Characteristics Table).

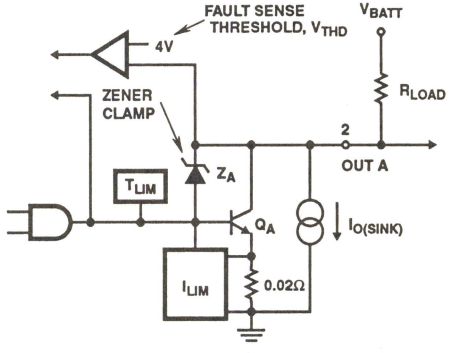


FIGURE 3. OUTPUT OPEN LOAD DETECTION WHERE $I_{O(SINK)}$ IS AN ACTIVE CURRENT SINK PULLDOWN FOR OPEN-LOAD FAULT DETECTION. THE CURRENT I_{CEX} IS $I_{O(SINK)}$ PLUS LEAKAGE CURRENTS OF THE OUTPUT DRIVER

Each of the outputs are independently protected with overcurrent limiting and over-temperature shutdown with thermal hysteresis. If an output is shorted, the remaining outputs function normally unless the temperature rise of the other output devices can be made to exceed their shutdown temperature of +165°C typical. When the junction temperature of a driver exceeds the +165°C thermal shutdown value, that output is turned off. When an output is shutdown, the resulting decrease in power dissipation allows the junction temperature to decrease. When the junction temperature decreases by approximately 15°C, the output is turned on. The output will continue to turn on and off for as long as the shorted condition exists or until shutdown by the input logic. The resulting frequency and duty cycle of the output current flow is determined by the ambient temperature, the thermal resistance of the package in the application and the total power dissipation in the package. Since each output is independently protected, the frequency and duty cycle of the current flow into multiple shorted outputs will not be related in time. Long lead lengths in the load circuit may lead to oscillatory behavior if more than two output loads are shorted.

Since a diagnostic flag indicates when an output is shorted, this information can be used as input to a microprocessor or dedicated logic circuit to provide a fast switch-off when a short occurs and, by sequence action, can be used to determine which output is shorted. A fault condition in any output load will cause the FAULT output to switch to a logic "low". Since a fault condition may be detected during switching, use of an appropriate size capacitor to filter the FAULT output is recommended. The recommended FAULT output circuit is shown in Figure 2. This will prevent the FAULT output voltage from reaching a logic level "0" within the maximum switching time.

The FAULT detection circuitry compares the state of the input and the state of the output for each A, B, C and D channel. The output is considered to be in a high state if the voltage exceeds the typical FAULT threshold reference voltage, V_{THD} of 4V. If the output voltage is less than V_{THD}, the output is considered to be in a low state. For example, if the input is high and the output is less than V_{THD}, a normal "ON" condition exists and the FAULT output is high. If the input is high and the output is greater than V_{THD}, a shorted load condition is indicated and the FAULT output is low. When the input is low and the output is greater than V_{THD}, a normal "OFF" condition is indicated and the FAULT output is high. If the input is low and the output is less than V_{THD}, an open load condition exists and the FAULT output is low. The Output Driver Fault Sense state is determined by high and low comparator threshold limits which are defined in the Fault Parameters section of the Electrical Specifications.

The FAULT output diagram of Figure 2 shows the circuit component interface for sensing a diagnostic fault condition. As noted, the time constant of $T_X = R_X C_X$ should be greater than the ON-OFF output switching times to avoid false fault readings during switching. For applications requiring fast period repetition rates, the maximum time constant should be significantly less than the period of switching. The shortest practical time constant is preferred to limit the duration of a fault condition.

To match a standard CMOS or TTL interface, the switched current at the FAULT pin must be converted to V_{IH} and V_{IL} voltage levels using the R_X external pullup resistor. The minimum specified I_{OL} limit at the FAULT output defines the Low (Fault) state which is used to test for a V_{OL} maximum limit of 0.4V. This makes the calculation for the V_{IL} input level relatively simple. Where V_F is the FAULT output voltage, V_{CC} is the power supply voltage, R_X is the pullup resistor to V_{CC} from the FAULT pin and I_{OL} is the fault condition sink current, $I_{O(SINK)}$, the low state equation is:

$$V_F = V_{CC} - RXIOL \leq V_{IL} \quad \text{(EQ. 1)}$$

As an example: Since TTL is the worst case for a low state, V_{IL} = 0.8V. Using V_{CC} = 5V, maximum $V_F = V_{OL}$ = 0.4V and minimum I_{OL} = 1mA for the CA3272A and CA3292A. At the worst case limit, the minimum value of R_X is:

$$R_X = (V_{CC} - V_{IL})/I_{OL} = (5 - 0.4)V/0.001mA = 4.6k\Omega$$

Where the minimum I_{OL} = 0.04mA for the CA3272 is much less, the same equation yields R_X = 115kΩ. In either case the preferred value for R_X would be greater than the values calculated.

For the logic V_{IH} High (normal state),

$$V_F = V_{CC} - R_X I_{OH} \geq V_{IH} \quad \text{(EQ. 2)}$$

Where the I_{OH} current is the specified leakage current, $I_{F(LK)}$ at the FAULT pin, it remains to check the calculated value for R_X as a leakage current times the chosen pullup resistance. To determine that the minimum V_{OH} from the FAULT pin is greater than V_{IH} to an external logic match, V_F is calculated using EQ(2). For example, using the R_X resistor value calculated for the CA3272,

$$V_F = [5 - (115k\Omega \times 2\mu A)] = 4.77V$$

which is more than suitable for CMOS or TTL Input switching levels; suggesting that a larger value of R_X could be used for a better noise margin in the Low fault state.

To detect an open load, each output has an internal low-level current sink, shown in Figure 3, which acts as a pull-down under open load fault conditions and is always active. The magnitude of this current plus any leakage associated with the output transistor will always be less than 100μA. (The data sheet specification for I_{CEX} includes this internal low-level sink current). The output load resistance must be chosen such that the voltage at the output will not be less than V_{THD} when the I_{CEX} sink current flows through it under worse case conditions with minimum supply voltage. For example, assume a 6.5V minimum driver output supply voltage, a FAULT threshold reference voltage of V_{THD} = 5.5V and an output current sink of I_{CEX} = 100μA. Calculate the maximum load resistance that will not result in a FAULT output low state when the output is OFF.

$$R_{LOAD}(max) = [V_{SUPPLY}(min) - V_{THD}(max)] / I_{CEX}(max) \quad \text{(EQ. 3)}$$

$$R_{LOAD}(max) = (6.5V - 5.5V) / 100\mu A = 10k\Omega \quad \text{(EQ. 4)}$$

Since the CA3272 and CA3272A do not have on-chip diodes to clamp voltage spikes which may be generated during inductive switching of the load circuit, an external zener diode (30V or less is recommended) should be connected between the output terminal and ground. Only those outputs used to switch inductive loads require this protection. Note that since the rate of change of output current is very high, even small values of inductance can generate voltage spikes of considerable amplitude on the output terminals which may require clamping. External free-wheeling diodes returned to the supply voltage are generally not acceptable as inductive clamps if the supply voltage exceeds 30V during transients. Typical loads for either the CA3272Q, CA3272AQ or CA3292AQ are shown in the application circuit of Figure 4A. Where inductive loads are driven from outputs A and B, no external zener diode clamp is needed for the CA3292AQ but is required for the CA3272Q or CA3272AQ as shown in Figure 4B.

The CA3272Q, CA3272AQ and CA3292AQ are supplied in the 28 lead Plastic Leaded Chip Carrier (PLCC) package with a specially configured lead frame to conduct heat from the package. To provide maximum heat transfer from the chip to PC Board or mounting surface, all ground leads are directly connected to the mounting pad of the chip. In free air the maximum junction-to-air thermal resistance, θ_{JA}, is maximum 43°C/W. This thermal resistance can be lowered to 30°C/W (typical) by suitable layout design of the PC board to which the package is soldered.

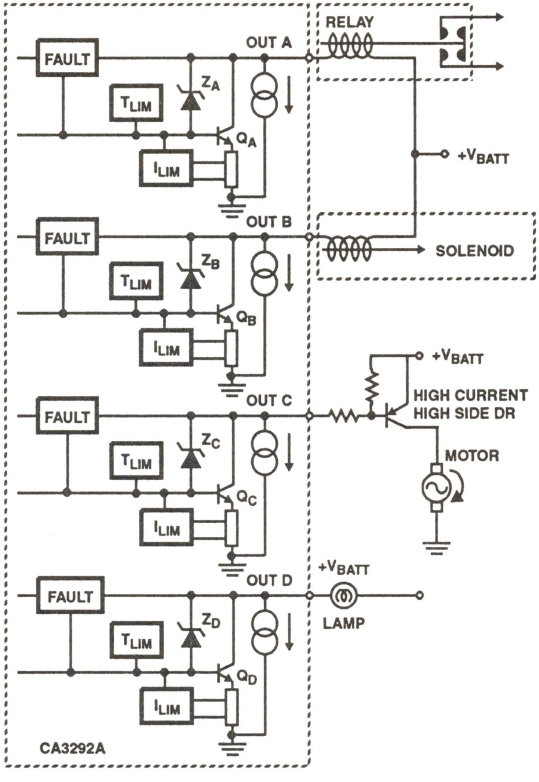


FIGURE 4A. TYPICAL APPLICATION CIRCUIT SHOWING OUTPUT LOAD CONTROL CAPABILITY OF THE CA3272Q, CA3272AQ OR CA3292AQ. THE INTERNAL DRIVE CIRCUIT WITH SELF PROTECTION AND FAULT OUTPUT IS THE CA3292AQ WITH THE OVER-VOLTAGE ZENER DIODE CLAMP

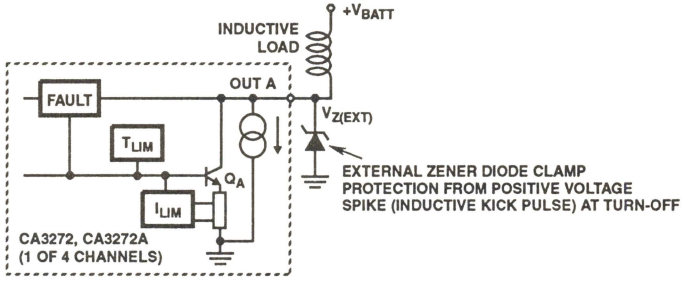


FIGURE 4B. CA3272 AND CA3272A OVER-VOLTAGE PROTECTION IS AN EXTERNAL ZENER DIODE CLAMP WHERE $V_{Z(EXT)} \leq V_{CE(SUS)}$. THE $V_{CE(SUS)}$ VOLTAGE RATING IS THE MAXIMUM VOLTAGE FOR FULL LOAD SWITCHING.

FIGURE 4.

HARRIS SEMICONDUCTOR

CA3282

CMOS Octal Serial Solenoid Driver

April 1994

Features

- Output Current Drive Capability
  - All Outputs ON, Equal . . . . . 0.625A Each
  - Per Output Individually . . . . . 1A Each
  - Maximum Total of Outputs ON 5A
- High Voltage Power BiMOS Outputs
  - 8 Open Drain NDMOS Drivers
  - Individual Output Latch
  - Over-Current Limit Protection 1.05A
  - Over-Voltage Clamp Protection. 30V
- High Speed CMOS Logic Control
  - Low Quiescent I_{DD} Current 5mA
  - SPI Bus Controlled Interface
  - Individual Fault Unlatch and Feedback
  - Common Reset Line
- Operating Temperature Range . . . . . -40°C to +125°C

Applications

- Automotive and Industrial Systems
- Solenoids, Relays and Lamp Drivers
- Logic and µP Controlled Drivers
- Robotic Controls

Description

The CA3282 is a logic controlled, eight channel octal serial solenoid driver. The serial peripheral interface (SPI) utilized by the CA3282 is a serial synchronous bus compatible with Harris CDP68HC05, or equivalent, microcomputers. As shown in the Block Diagram for the CA3282 each of the open drain NDMOS output drivers has individual protection for over-voltage and over-current. Each output channel has separate output latch control with fault unlatch and diagnostic feedback. Under normal ON conditions, each output driver is in a low, saturation state. Comparators in the diagnostic circuitry monitor the output drivers to determine if an out of saturation condition exists. If a comparator senses a fault, the respective output driver is unlatched. In addition, over current protection is provided with current limiting in each output, independent of the diagnostic feedback loop.

The CA3282 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, relays, and solenoids in applications where low operating power, high breakdown voltage, and high output current at high temperatures is required.

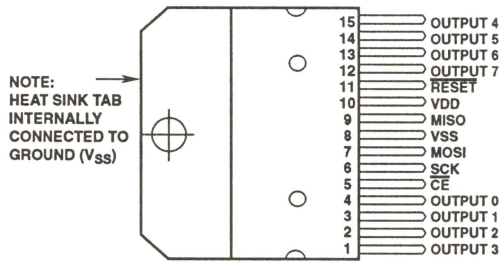
The CA3282 is supplied in 15 lead plastic SIP package with lead forms for either vertical or surface mount.

Ordering Information

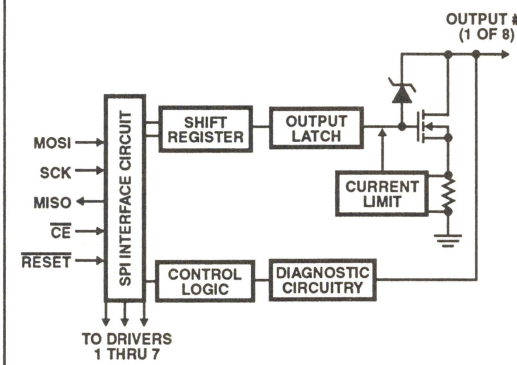
PART NUMBER	TEMP. RANGE	PACKAGE AND LEAD FORM
CA3282AS1	-40°C to +125°C	15 Lead Plastic SIP Staggered Vertical
CA3282AS2	-40°C to +125°C	15 Lead Plastic SIP Surface Mount

Pinout

CA3282 (SIP)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 2767.4

Absolute Maximum Ratings

Output Voltage, V_O (Note 1) ..... V_{OC} (Clamp)
Output Load Current, I_{LOAD} (Per Output, Individual) 1A
Output Load Current, I_{LOAD} (All 8 Outputs ON, Equal I_{OUT}) 0.625A
Output Load Current, I_{LOAD} (Max. Total of Outputs ON) 5.0A
DC Logic Supply, V_{DD} 7V
Input Voltage, V_{IN} ..... -0.7 to +7V
Operating Ambient Temperature Range ..... -40°C to +125°C
Operating Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range, TSTG ..... -55°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
15 Lead Plastic SIP	45°C/W (No Heat Sink)	3°C/W (Infinite Heat Sink)

Power Dissipation
Up to +125°C w/o Heat Sink 0.56W
Above +125°C w/o Heat Sink .....Derate Linearly at 22mW/°C
Up to +125°C w/Infinite Heat Sink 8.33W
Above +125°C w/Infinite Heat Sink: .. Derate Linearly at 333mW/°C
Lead Temperature (During Soldering)
At a distance 1/16 inch ± 1/32 inch (1.59 ± 0.79mm)
from case for 10s max ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5V, T_A = -40°C to +125°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Supply Current	I_{DD}	All Outputs ON, 0.5A Load Per Output	-	5	10	mA
Output Clamping Voltage	V_{OC}	I_{LOAD} = 0.5A, Output Programmed OFF	27	32	40	V
Output Clamping Energy	E_{OC}	I_{LOAD} = 0.5A, Output ON	20	-	-	mJ
Output Leakage Current	$I_{O\ LEAK}$	Output Programmed OFF				
		V_O = 24V	-	150	1000	µA
		V_O = 14V	-	150	500	µA
		V_O = 5V	-	150	200	µA
Output Saturation Voltage	V_{SAT}	I_{LOAD} = 0.5A	-	0.3	0.5	V
		I_{LOAD} = 0.75A	-	0.4	1.25	V
		I_{LOAD} = 1.0A	-	0.6	2.0	V
$R_{DS(ON)}$		I_{LOAD} = 0.5A	-	-	1	Ω
Output Current Limit	$I_{O\ LIMIT}$	Output Programmed ON, V_{OUT} > 3V	1.05	1.5	-	A
Turn-On Delay	t_{PHL}	I_O = 500mA, No Reactive Load	-	1	10	µs
Turn-Off Delay	t_{PLH}	I_O = 500mA, No Reactive Load	-	2	10	µs
Fault Reference Voltage	V_{OREF}	Output Programmed ON, Fault Detected If $V_O > V_{OREF}$	1.6	1.8	2.0	V
Fault Reset Delay (After $\overline{CE}$ Low to High Transition)	t_{UD}	See Figure 1	50	80	250	µs
Output OFF Voltage	V_{OFF}	Output Programmed OFF, Output Pin Floating	-	0	1	V
LOGIC INPUTS (MOSI, $\overline{CE}$, SCK and $\overline{RESET}$)						
Threshold Voltage at Falling Edge	V_{T-}	V_{DD} = 5V ± 10%	$0.2V_{DD}$	$0.3V_{DD}$	-	V
Threshold Voltage at Rising Edge	V_{T+}	V_{DD} = 5V ± 10%	-	$0.6V_{DD}$	$0.7V_{DD}$	V
Hysteresis Voltage	V_H	$V_{T+} - V_{T-}$	0.85	1.4	2.25	V
Input Current	I_I	V_{DD} = 5.5V, 0 < V_I < V_{DD}	-10	-	+10	µA
Input Capacitance	C_I	0 < V_I < V_{DD}	-	-	20	pF

Electrical Specifications V_{DD} = 5V, T_A = -40°C to +125°C, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUT (MISO)						
Output LOW Voltage	V_{OL}	I_{OL} = 1.6mA	-	0.2	0.4	V
Output HIGH Voltage	V_{OH}	I_{OL} = 0.8mA	V_{DD} - 1.3V	V_{DD} - 0.2V	-	V
Output Three State Leakage Current	I_{OL}	V_{DD} = 5.25V, 0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High	-10	-	+10	µA
Output Capacitance	C_{OUT}	0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High	-	-	20	pF

Serial Peripheral Interface Timing (See Figure 1)

PARAMETERS	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Operating Frequency	f_{OPER}		D.C.	Note 2	3.0	MHz
Cycle Time	(1) t_{CYC}		1.0	0.1	-	µs
Enable Lead Time	(2) t_{LEAD}		-	<100	1000	ns
Enable Lag Time	(3) t_{LAG}		-	<100	1000	ns
Minimum Clock HIGH Time	(4) t_{WSCKH}		-	50	410	ns
Minimum Clock LOW Time	(5) t_{WSCKL}		-	50	410	ns
Minimum Data Setup Time	(6) t_{SU}		-	20	150	ns
Minimum Data Hold Time	(7) t_H		-	20	150	ns
Enable Time	(8) t_{EN}		-	50	1000	ns
Disable Time	(9) t_{DIS}		-	150	1000	ns
Data Valid Time	(10) t_V		-	75	360	ns
Output Data Hold Time	(11) t_{HO}		0	50	-	ns
Rise Time (MISO Output)	(12) t_{rSO}	V_{DD} = 20% to 70%, C_L = 200pF	-	35	150	ns
Rise Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(12) t_{rSI}	V_{DD} = 20% to 70%, C_L = 200pF	-	-	90	ns
Fall Time (MISO Output)	(13) t_{fSO}	V_{DD} = 20% to 70%, C_L = 200pF	-	45	150	ns
Fall Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(13) t_{fSI}	V_{DD} = 20% to 70%, C_L = 200pF	-	-	90	ns

NOTES:

1. The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns-on the MOSFET; holding the Drain at the Output Clamp Voltage, V_{OC}.
2. Operating Frequency is typically greater than 10MHz but it is application limited primarily by external SPI input rise/fall times and MISO output loading.

Timing Diagrams

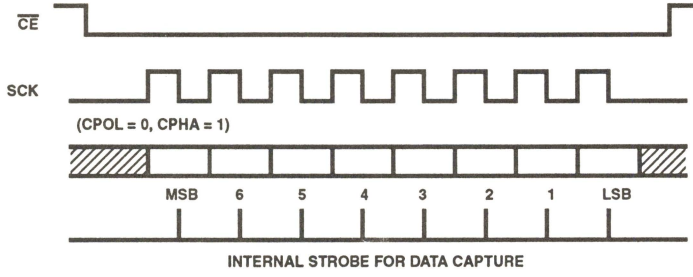


FIGURE 1A. DATA AND CLOCK TIMING DIAGRAM

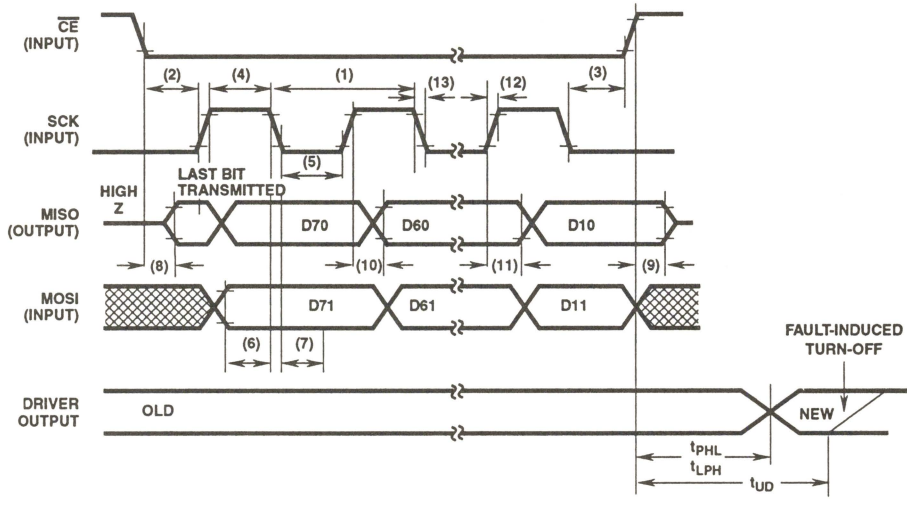


FIGURE 1B. SPI TIMING DIAGRAM

FIGURE 1.

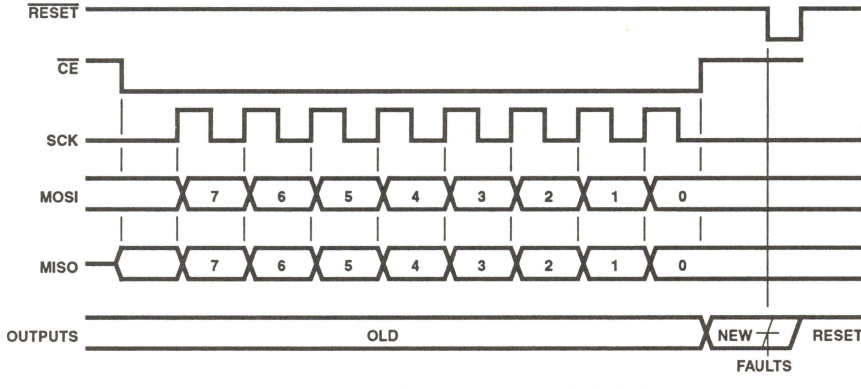


FIGURE 2. BYTE TIMING DIAGRAM WITH ASYNCHRONOUS RESET

Signal Descriptions

Power Output Drivers, Output 0 - Output 7- The input and output bits corresponding to Output 0 thru Output 7 are transmitted and received most significant bit (MSB) first via the SPI bus. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, with current limiting set to a minimum of 1.05A. An on-chip clamp circuit capable of handling 500mA is provided at each output for clamping inductive loads.

$\overline{\text{RESET}}$ - Active low reset input. When this input line is low, the shift register and output latches are configured to turn off all output drivers. A power on clear function may be implemented by connecting this pin to V_{DD} with an external resistor, and to V_{SS} with an external capacitor. In any case, this pin must not be left floating.

$\overline{\text{CE}}$ - Active low chip enable. Data is transferred from the shift register to the outputs on the rising edge of this signal. The falling edge of $\overline{\text{CE}}$ loads the shift register with the output voltage sense bits coming from the output stages. The output driver for the MISO pin is enabled when this pin is low. $\overline{\text{CE}}$ must be a logic low prior to the first serial clock (SCK) and must remain low until after the last (eighth) serial clock cycle. A low level on $\overline{\text{CE}}$ also activates an internal disable circuit used for unlatching output states that are in a fault mode as sensed by an out of saturation condition. A high on $\overline{\text{CE}}$ forces MISO to a high impedance state. Also, when $\overline{\text{CE}}$ is high, the octal driver ignores the SCK and MOSI signals.

SCK, MISO, MOSI - See Serial Peripheral Interface (SPI) section in this data sheet.

V_{DD} and V_{SS} (GND) - Positive and negative power supply lines.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) utilized by the CA3282 is a serial synchronous bus for control and data transfers. The Clock (SCK), which is generated by the microcomputer, is active only during data transfers. In systems using CDP68HC05 family microcomputers, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. The CPOL bit is used in conjunction with the clock phase bit, CPHA to produce the desired clock data relationship between the microcomputer and octal driver. The CPHA bit in general selects the clock edge which captures data and allows it to change states. For the CA3282, the CPOL bit must be set to a logic zero and the CPHA bit to a logic one. Configured in this manner, MISO (output) data will appear with every rising edge SCK, and MOSI (input) data will be latched into the shift register with every falling edge of SCK. Also, the steady state value of the inactive serial clock, SCK, will be at a low level. Timing diagrams for the serial peripheral interface are shown in Figure 1.

SPI Signal Descriptions

MOSI (Master Out/Slave In) - Serial data input. Data bytes are shifted in at this pin, most significant bit (MSB) first. The data is passed directly to the shift register which in turn controls the latches and output drivers. A logic "0" on this pin will program the corresponding output to be ON, and a logic "1" will turn it OFF.

MISO (Master In/Slave Out) - Serial data output. Data bytes are shifted out at this pin, most significant bit (MSB) first. This pin is the serial output from the shift register and is three stated when $\overline{\text{CE}}$ is high. A high for a data bit on this pin indicates that the corresponding output is high. A low on this pin for a data bit indicates that the output is low. Comparing the serial output bits with the previous input bits, the microcomputer implements the diagnostic data supplied by the CA3282.

SCK - Serial clock input. This signal clocks the shift register SCK and new MOSI (input) data will be latched into the shift register on every falling edge of SCK. The SCK phase bit, CPHA, and polarity bit, CPOL, must be set to 1 and 0, respectively in the microcomputer's control register.

Functional Descriptions

The CA3282 is a low operating power, high voltage, high current, octal, serial solenoid driver featuring eight channels of open drain NDMOS output drivers. The drivers have low saturation voltage and output short circuit protection, suited for driving resistive or inductive loads such as lamps, relays and solenoids. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. Each channel is independently controlled by an output latch and a common $\overline{\text{RESET}}$ line that disables all eight outputs. Byte timing with asynchronous reset is shown in Figure 2. The circuit receives 8 bit serial data by means of the serial input (MOSI), and stores this data in an internal register to control the output drivers. The serial output (MISO) provides 8 bit diagnostic data representing the voltage level at the driver output. This allows the microcomputer to diagnose the condition at the output drivers. The device is selected when the chip enable ($\overline{\text{CE}}$) line is low. When ($\overline{\text{CE}}$) is high, the device is deselected and the serial output (MISO) is placed in a tri-state mode. The device shifts serial data on the rising edge of the serial clock (SCK), and latches data on the falling edge. On the rising edge of chip enable ($\overline{\text{CE}}$), new input data from the shift register is latched in the output drivers. The falling edge of chip enable ($\overline{\text{CE}}$) transfers the output drivers fault information back to the shift register. The output drivers have low ON voltage at rated current, and are monitored by a comparator for an out of saturation condition, in which case the output driver with the fault becomes unlatched and diagnostic data is sent to the microcomputer via the MISO line. A typical microcomputer interface circuit is shown in Figure 3. Also, the CA3282 may be cascaded with another CA3282 octal driver.

Shift Register

The shift register has both serial and parallel inputs and outputs. Serial output and input data are simultaneously transferred to and from the SPI bus. The parallel outputs are latched into the output latch in the CA3282 at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

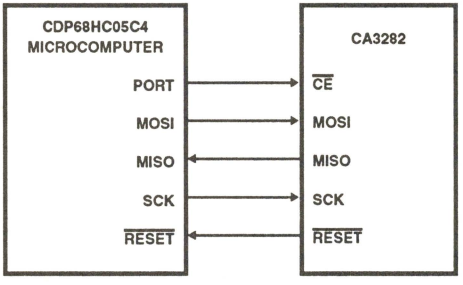


FIGURE 3. TYPICAL MICROCOMPUTER INTERFACE WITH THE CA3282

Output Latch

The output latch holds input data from the shift register which is used to activate the outputs. The latch circuit may be cleared by a fault condition (to protect the overloaded outputs), or by the $\overline{\text{RESET}}$ signal.

Output Drivers

The output drivers provide and active low output of 500mA nominal with current limiting set to 1.05A to allow for high inrush currents. In addition, each output is provided with a voltage clamp circuit to limit inductive transients. Each output driver is also monitored by a comparator for an out of saturation condition. If the output voltage of an ON output pin exceeds the saturation voltage limit, a fault condition is assumed and the latch driving this output is reset, turning the output off. The output comparators, which also provide diagnostic feedback data to the shift register, contain an internal pull-down current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

$\overline{\text{CE}}$ High to Low Transition

When $\overline{\text{CE}}$ is low the three state MISO pin is enabled. On the falling edge of $\overline{\text{CE}}$, diagnostic data from the output voltage comparators will be latched into the shift register. If an output is high, a logic one will be loaded into that bit in the shift register. If the output is low, a logic zero will be loaded. During the time that $\overline{\text{CE}}$ is low, data bytes controlling the output drivers are shifted in at the MOSI pin most significant bit (MSB) first. A logic zero on this pin will program the corresponding output to be ON, and a logic one will turn it OFF.

$\overline{\text{CE}}$ Low to High Transition

When the last data bit has been shifted into the CA3282, the $\overline{\text{CE}}$ pin should be pulled high. At the rising edge of $\overline{\text{CE}}$, shift register data is latched into the output latch and the outputs are activated with the new data. An internal 150ms delay timer will start at this rising edge to compensate for high inrush currents in lamps and inductive loads. During this period, the outputs will be protected only by the analog current limiting circuits since resetting of the output latches by fault conditions will be inhibited during this time. This allows the device to handle inrush currents immediately after turn on. When the 150ms delay has elapsed, the output voltages are sensed by the comparators and any out of saturation outputs are latched off. The serial clock input pin (SCK) should be low during $\overline{\text{CE}}$ transitions to avoid false clocking of the shift register. The SCK input is gated by $\overline{\text{CE}}$ so that the SCK input is ignored when $\overline{\text{CE}}$ is high.

Detecting Fault Conditions

Fault conditions may be checked as follows. Clock in a new control byte and wait approximately 150ms to allow the outputs to settle. Clock in the same control byte and note the diagnostic data output at the MISO pin. The diagnostic bits should be identical to the data clocked in. Any differences will indicate a fault in the corresponding outputs. For example, if an output was programmed ON by clocking in a zero, and the corresponding diagnostic bit for that output is a one, indicating the driver output is still high, then a short circuit or overload condition may have caused the output to unlatch. Alternatively, if the output was programmed OFF by clocking in one, and the diagnostic bit for that output shows a zero, then the probable cause is an open circuit resulting in a floating output.

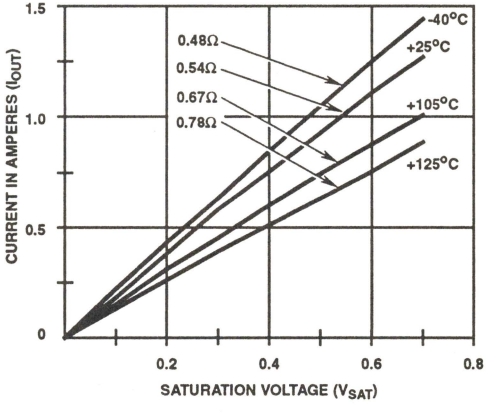


FIGURE 4A. CA3282 TYPICAL OUTPUT DRIVER $R_{DS(ON)}$ CHARACTERISTICS OF CURRENT OUT vs SATURATION VOLTAGE, V_{SAT} FOR A -40°C TO +125°C JUNCTION TEMPERATURE

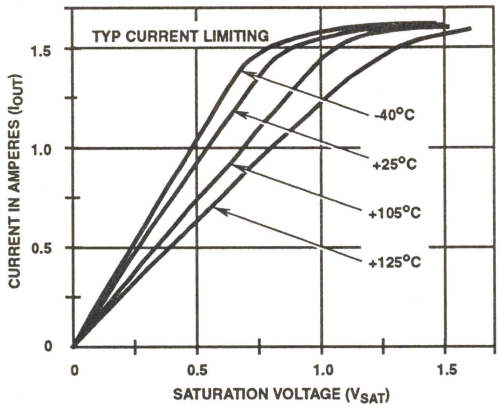


FIGURE 4B. CA3282 TYPICAL OUTPUT DRIVER $R_{DS(ON)}$ CHARACTERISTICS OF CURRENT OUT vs SATURATION VOLTAGE, V_{SAT} FOR A -40°C TO +125°C JUNCTION TEMPERATURE

Dissipation In Multiple Outputs

The CA3282 Octal Serial Solenoid Driver has multiple MOS Output Drivers and requires special consideration with regard to maximum current and dissipation ratings. While each output has a maximum current specification consistent with the device structure, all such devices on the chip can not be simultaneously rated to the same high level of peak current. The total combined current and the dissipation on the chip must be adjusted for maximum allowable ratings, given simultaneous multiple output conditions.

For the CA3282, the maximum positive output current rating is 1A when one output is ON. When ALL outputs are ON, the rating is reduced to 0.625A because the total maximum current is limited to 5A. For any given application, all output drivers on a chip may or may not have a different level of loading. The discussion here is intended to provide relatively simple methods to determine the maximum dissipation and current ratings as a general solution and, as a special solution, when all switched ON outputs have the same current loading.

General Solution

A general equation for dissipation should specify that the total power dissipation in a package is the sum of all significant elements of dissipation on the chip. However, in Power BiMOS Circuits very little dissipation is needed to control the logic and predriver circuits on the chip. The over-all chip dissipation is primarily the sum of the I^2R dissipation losses in each channel where the current, I is the output current and the resistance, R is the NMOS channel resistance, $R_{DS(ON)}$ of each output driver. As such, the total dissipation, P_D for n output drivers is:

$$P_D = \sum_{k=1}^{n} P_k \qquad \text{(EQ. 1)}$$

This expression sums the dissipation, P_K of each output driver without regard to uniformity of dissipation in each MOS channel. The dissipation loss in an NMOS channel is:

$$P_k = I^2 \times R_{DS(ON)} \qquad \text{(EQ. 2)}$$

where the current, I is the determined by the output load when the channel is turned ON. The channel resistance, $R_{DS(ON)}$ is a function of the circuit design, level of gate voltage and the chip temperature. Refer to the Electrical Specifications values for worse case channel resistance.

The temperature rise in the package due to the dissipation is the product of the on-chip dissipation, P_D and the package Junction-to-Case thermal resistance, θ_{JC}. To determine the junction temperature, T_J, given the case (heat sink tab) temperature, T_C, the linear heat flow solution is:

$$T_J = T_C + P_D \times \theta_{JC} \text{ or } T_C = T_J - P_D \times \theta_{JC} \qquad \text{(EQ. 3, 3A)}$$

Since this solution relates only to the package, further consideration must be given to a practical heat sink. The equation of linear heat flow assumes that the Junction-to-Ambient thermal resistance, θ_{JA}, is the sum of the thermal resistance from Junction-to-Case and the thermal resistance from Case (heat sink)-to-Ambient, θ_{CA}. The Junction-to-Ambient thermal resistance, θ_{JA} is the sum of all thermal paths from the chip junction to the ambient temperature (T_A) environment and can be expressed as,

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad \text{(EQ. 4)}$$

Equation 3 and Equation 3A may be expressed as,

$$T_J = T_A + P_D \times \theta_{JA} \text{ or } T_A = T_J - P_D \times \theta_{JA} \qquad \text{(EQ. 5, 5A)}$$

Not all Integrated Circuit packages have a directly definable case temperature because the heat is spread thru the lead frame to a PC Board which is the effective heat sink.

Calculation Example 1

For the CA3282, θ_{JC} = 3°C/W and the worst case junction temperature, as an application design solution, should not exceed 150°C. For any given application, Equation 1 determines the dissipation, P_D.

Assume the package is mounted to a heat sink having a thermal resistance of 6°C/W and, for a given application, the dissipation, P_D = 3 Watts. Assume the operating ambient temperature, T_A = 100°C. The calculated Junction-to-Ambient thermal resistance is:

$\theta_{JA} = \theta_{JC} + \theta_{CA}$ = 9°C/W

The solution for junction temperature by Equation 5 is:

T_J = 100°C + 3W x 9°C/W = 127°C

Calculation Example 2

Using the CA3282 maximum Junction-to-Ambient Thermal Resistance, θ_{JA} value of 45°C/W (no external heat sink) and the worst case Junction Temperature, T_C of 150°C we have an application design solution for the maximum ambient temperature or dissipation. For example; Using Equation 1and assuming a device dissipation, P_D of 1W, the maximum allowable Ambient Temperature, T_A from Equation 5A is calculated as follows:

T_A = +150°C - 1.0W x 45°C/W = 105°C

Equal Current Loading Solution

Where a given application has equal current loading in the output drivers, equal $R_{DS(ON)}$ and temperature conditions may be assumed. As such, a convenient method to show rating boundaries is to substitute the dissipation Equation 2 into the junction temperature Equation 3. For m outputs that are ON with equal currents, where $I = I_1 = I_2 ..... = I_m$, we have the following solution for dissipation:

$$P_D = m \times P_k = m \times I^2 \times R_{DS(ON)} \qquad \text{EQ (6)}$$

$$I = \sqrt{\frac{T_J - T_C}{m \times \theta_{JC} \times R_{DS(ON)}}} \qquad \text{EQ (7)}$$

The number of output drivers ON and conducting (m) may be from 1 to n. (i.e., For all 8 output drivers conducting, m = n = 8.) Maximum temperature, dissipation and current ratings must be observed. The drain current vs case temperature may be plotted for any value of m from 1 to 8, provided drain currents remain equal.

The curve of Figure 5 illustrates the boundary limits for temperature and dissipation. Figure 6 shows the maximum current for all 8 outputs ON with equal current plotted versus Case Temperature, T_C. Boundary conditions relate to the Absolute Maximum Ratings as defined in the Data Sheet.

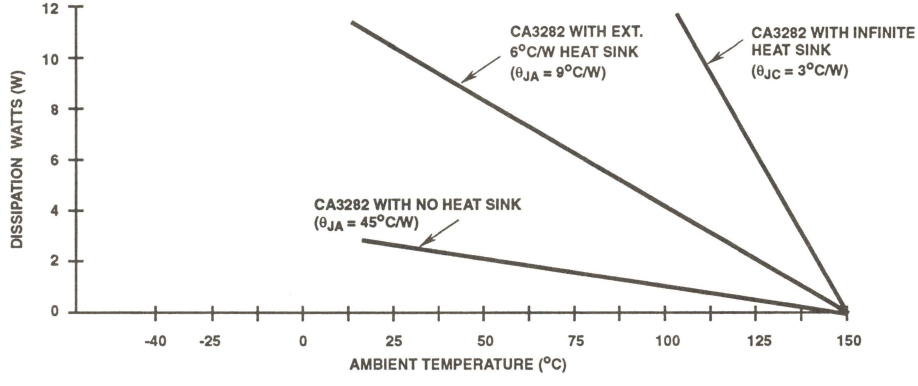


FIGURE 5. DISSIPATION DERATING CURVE

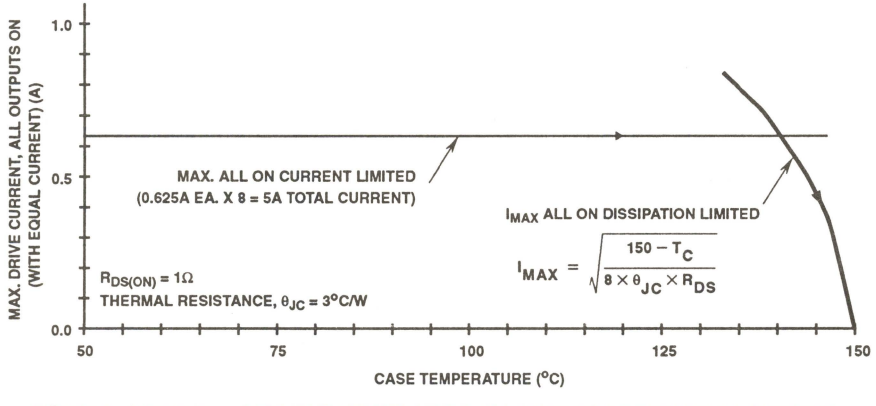


FIGURE 6. CURRENT vs CASE (TAB) TEMPERATURE, ALL OUTPUTS ON WITH EQUAL CURRENT

HARRIS SEMICONDUCTOR

HIP0080, HIP0081

PRELIMINARY

April 1994

Quad Inverting Power Drivers with Serial Diagnostic Interface

Features

- Low Side Power MOSFET Output Drivers
- Output Driver Protection
  - Over-Current Shutdown
  - Over-Temperature Shutdown with Hysteresis
  - Over-Voltage Internal Clamp
- Load Current Switching Capability
  - HIP0081 . . . 3A Pk, 2A DC - Each; 5A Total All ON
  - HIP0080 . . 1.5A Pk, 1A DC - Each; 3A Total All ON
- HIP0080 - Low Idle Current Shutdown Mode
- Regulated 5V Logic Interface
- 5V CMOS Logics Inputs
- Fault Mode Output for Shorts, Opens and Over-Temperature
- 16 Bit Serial Diagnostic Register
- SPI Bus Compatible Data Readout
- HIP0081 - Low θ_{JC} Power Package . . . . . 3°C/W
- -40°C to +125°C Operating Temperature

Applications

- Drivers For
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use
  - Automotive
  - Appliances
  - Industrial
  - Robotics

Description

The HIP0080/HIP0081 Quad Power Drivers contain four individually protected NDMOS power output transistor switches to drive inductive and resistive loads such as: relays, solenoids, injectors, AC and DC motors, heaters and incandescent lamp displays. The 4 Power Drivers are low-side switches driven by CMOS logic input control stages. Each Output Power Driver is protected against over-current, over-temperature and over-voltage. An internal drain-to-gate zener diode provides the clamping protection for over-voltage. Diagnostic circuits provide ground short, supply short, open load and thermal overload detection for each of the 4 output stages. Each of the 4 input drivers and their respective diagnostic filters are controlled by one ENABLE input.

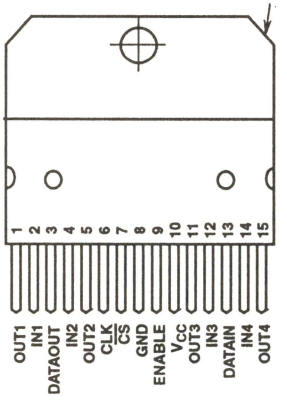
The inputs are CMOS logic compatible and individually control the output drivers with an active high state for turn-on. All other control inputs are active high with the exception of the Chip Select ($\overline{CS}$) which is active low. The DATAIN (DI) and DATAOUT (DO) are positive logic and the Clock (CLK) input for the Serial Interface is active on the rising edge of the CLK pulse. All inputs, except the HIP0080 ENABLE, include a nominal level of hysteresis. IN1, IN2, IN3, IN4 and ENABLE have pull-down resistors of approximately 100kΩ. This switches off any channel that has an unterminated input.

Filters are used on the outputs of the fault sensing comparators to avoid the detection of short duration transient spikes. The on-chip oscillator is used to clock an internal shift register in each filter. If the fault condition is longer than a preset number of clock cycles, the fault condition is recognized and the respective bit is set in the diagnostic register. No filter is used in the thermal-overload feedback circuit and the bit is set when thermal shutdown occurs.

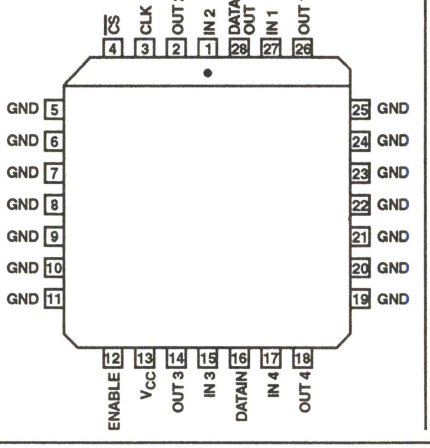
For normal operating conditions, a Reset turns off all outputs when the V_{CC} level drops below 3.5V. The internal bandgap and bias supply function includes a 5V regulated supply for the low voltage signal and logic circuits.

Pinouts

HIP0081 (SIP)
TOP VIEW



HIP0080 (PLCC)
TOP VIEW



Ordering Information

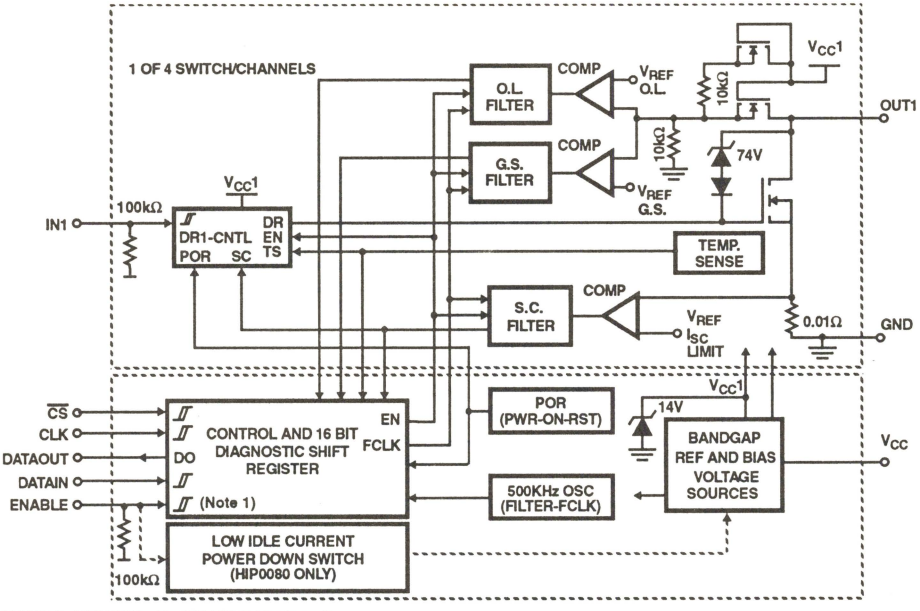
PART NUMBER	TEMP. RANGE	PACKAGE & LEAD FORM
HIP0081AS1	-40°C to +125°C	15 Lead Plastic SIP Staggered Vertical Mount
HIP0081AS2	-40°C to +125°C	15 Lead Plastic SIP Surface Mount
HIP0080AM	-40°C to +125°C	28 Lead PLCC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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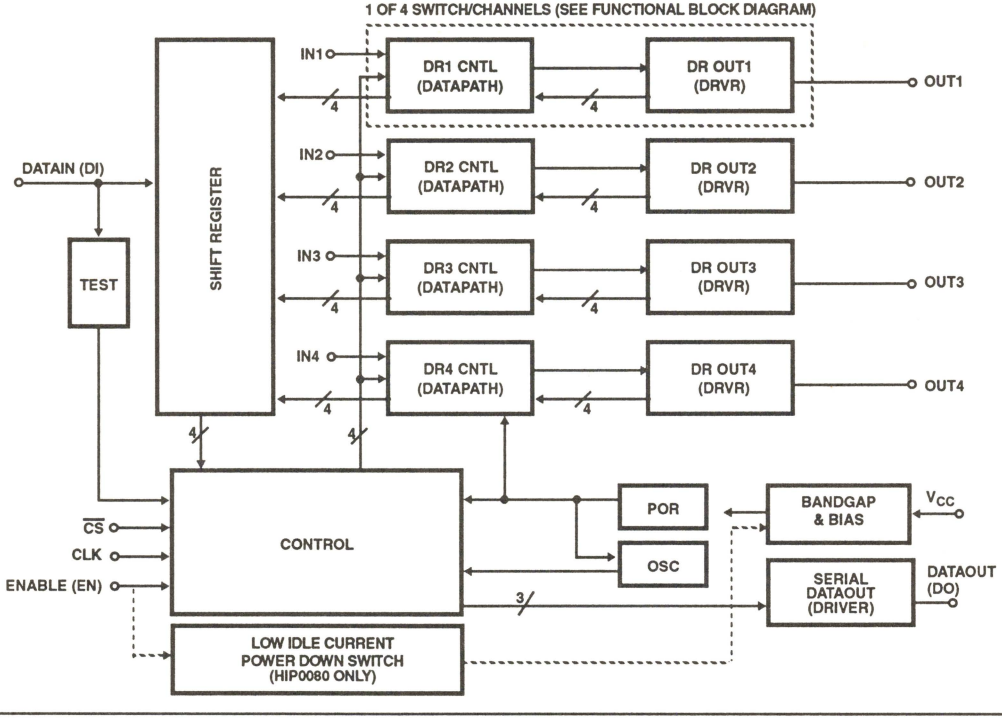
File Number **3018.2**

Functional Block Diagram



NOTE 1. HIP0080 - No ENABLE Hysteresis

Functional Signal Flow Diagram



Absolute Maximum Ratings

Supply Voltage (Logic & Control), V_{CC} ..... -16 to 45V
Power MOSFET Drain Voltage, V_O (Note 1) ..... -0.5 to V_{CLAMP}
Output Clamp Energy, E_{OK} (HIP0080) ..... TBDmJ
Output Clamp Energy, E_{OK} (HIP0081) ..... TBDmJ
Input Voltage (Logic and Driver Inputs), V_{IN} ..... -0.5V to 7V
Output Voltage, DATAOUT ..... 0.7V to 7V
Output Current
  HIP0080
    Each Output, $I_{OUT(PEAK)}$, (Note 2) ..... -0.5A to +1.5A
    Each Output, $I_{OUT(DC)}$ ..... 0A to +1A
    All 4 Outputs ON, Equal I_{OUT} ..... +0.75A each
    Total of 4 Outputs, Unequal I_{OUT} ..... +3A (to GND)
  HIP0081
    Each Output, $I_{OUT(PEAK)}$, (Note 2) ..... -2A to +3A
    Each Output, $I_{OUT(DC)}$ ..... 0A to +2A
    All 4 Output, ON, Equal I_{OUT} ..... +1.25A each
    Total of 4 Outputs, Unequal I_{OUT} ..... +5A (to GND)
Operating Ambient Temperature Range ..... -40°C to +125°C
Operating Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range, T_{STG} ..... -55°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HIP0080 (28 Lead PLCC Power Pkg) ...	45°C/W	-
HIP0081 (15 Lead SIP Power Pkg)	45°C/W	3°C/W

HIP0080 Power Dissipation: (with PC Board as Heat Sink, Note 3)
  Up to +85°C 2.2W
  Above +85°C ..... Derate Linearly at 33mW/°C
HIP0081 Power Dissipation
  Up to +125°C w/o Heat Sink 0.56W
  Above +125°C w/o Heat Sink ..... Derate Linearly at 22mW/°C
  Up to +125°C w/Infinite Heat Sink 8.33w
  Above +125°C
  w/Infinite Heat Sink ..... Derate Linearly at 333mW/°C
Lead Temperature (During Soldering)
  At a distance 1/16 inch ± 1/32 inch (1.59mm ± 0.79mm)
  From Case for 10s Max ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{CC} = 5.5V to 25V ± 5%, T_A = -40°C to +125°C; Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HIP0080			HIP0081			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER OUTPUTS									
Output ON Resistance (HIP0081)	R_{ON}	V_{CC} = 10 to 25V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 1A	-	-	-	-	-	0.5	Ω
		V_{CC} = 5.5 to 10V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 0.7A	-	-	-	-	-	1.0	Ω
Output ON Resistance (HIP0080)	R_{ON}	V_{CC} = 10 to 25V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 0.5A	-	-	1.0	-	-	-	Ω
		V_{CC} = 5.5 to 10V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 0.4A	-	-	2.0	-	-	-	Ω
HIP0081 Output Off Current	I_{OFF}	Inputs, IN_ Low, $V_{OUT_}$ = 60V	-	-	-	-	0.75	1.0	mA
HIP0081 Output Leakage Current	I_{OFFLK}	Inputs, IN_ Low, $V_{OUT_}$ = 60V V_{CC} = 0V	-	-	-	-	1.0	10	µA
HIP0080 Output Off Current	I_{OFF}	Inputs, IN_ Low, $V_{OUT_}$ = 25V Enable High	-	0.75	1	-	-	-	mA
HIP0080 Output Leakage Current	I_{OFFLK}	Inputs, IN_ Low, $V_{OUT_}$ = 25V Enable Low	-	1.0	10	-	-	-	µA
Over-Voltage Clamp Range	V_{CLAMP}	Output Programmed OFF, Input Low	27	-	43	73	-	89	V
Current Short Circuit Prot.	$I_{OUT(SC)}$	(Note 2)	1.3	-	2.5	2.2	-	4.8	A
Short Circuit Det. Delay	t_{SCDLY}		-	6	-	-	6	-	µs
Output ON-OFF Voltage Ramp Rate		(Resistive load)	-	10	-	-	10	-	V/µs
Turn-On Delay	t_{PHL}	V_{CC} = 14V, R_{LOAD} = 14Ω	-	-	8	-	-	8	µs
Turn-Off Delay	t_{PLH}	V_{CC} = 14V, R_{LOAD} = 14Ω	-	-	8	-	-	8	µs
SUPPLY									
Power Supply Current	I_{CC}		-	20	25	-	20	25	mA
Power Supply Reset Active	V_{CC_RST}		3	-	4	3	-	4	V

Electrical Specifications V_{CC} = 5.5V to 25V ± 5%, T_A = -40°C to +125°C; Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HIP0080			HIP0081			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Shut-Down Current Mode	I_{SHTDN}	Enable LOW	-	130	200	-	-	-	µA
INPUTS									
Low-Level Input Voltage	V_{IL}		-	-	1	-	-	1	V
High-Level Input Voltage	V_{IH}		3.5	-	-	3.5	-	-	V
Input Hysteresis Threshold	V_{IN_HYS}	(N.A. to HIP0080 ENABLE	0.85	-	2.25	0.85	-	2.25	V
Input Pull-Down Resistance	R_{PD}	IN1, IN2, IN3, IN4, ENABLE	50	100	200	50	100	200	KΩ
DATAOUT (Open Drain)									
Leakage Current	I_{DO_LEAK}	V_{DO} = 7V, DO OFF (High)	-	-	10	-	-	10	µA
Logic Low Output Voltage	V_{OL}	I_{OH} = 1.6mA, DO ON (Low)	-	-	0.4	-	-	0.4	V
Max. Logic Low Current	I_{OH}	V_{DO} = 4.5V, DO ON	1.6	-	-	1.6	-	-	mA
Oscillator Frequency	f_{OSC}		-	500	-	-	500	-	kHz
Serial Interface Clock Freq.	f_{CLK}	(Note 4)	-	-	2	-	-	2	MHz
DIAGNOSTIC AND PROTECTION									
Over-Temperature Shutdown Threshold			150	-	-	150	-	-	°C
Shutdown Temp. Hysteresis			-	15	-	-	15	-	°C
Output Short-to-GND Threshold		$V_{OUT_}$ = 5.5V to 16V	-	0.24 x V_{CC}	-	-	0.24 x V_{CC}	-	V
Short-to-GND Hysteresis		$V_{OUT_}$ = 5.5V to 16V	-	0.02 x V_{CC}	-	-	0.02 x V_{CC}	-	V
Open-Load Resistance for No-Load Warning		$V_{OUT_}$ = 5.5V to 16V	5	-	25	5	-	25	kΩ
Filter Delay Time for O.L. or Short-to-GND			-	12	-	-	12	-	µs

NOTES:

1. The MOSFET Output Drain is internally Clamped with a Drain-to-Gate zener diode that turns-on the MOSFET to hold the Drain at the V_{CLAMP} voltage. Refer to the Electrical Specifications Table for the V_{CLAMP} voltage limits.
2. Each Output has Over-Current Shutdown protection in the positive current direction. The maximum peak current rating is determined by the minimum Over-Current Shutdown as detailed in the Electrical Specification Table. In the event of an Over-Current Shutdown the input drive is latched OFF. The output short must be removed and the input toggled OFF and ON to restore the output drive.
3. Effective Heat Sinking for the HIP0080 PLCC package requires a PC Board solder mount. For a PC Board layout having a ground plane of copper extending away from the package, the junction-to-air thermal resistance may be as low as 30°C/W.
4. The maximum serial Clock Frequency may be limited by the time constant of the external load network at the DATAOUT pin.

Diagnostic Interface Overview

Each Quad Inverting Power Driver IC may be used as a single power switching driver, with or without the diagnostic interface. Where more than 4 Power Driver Switches are required, the HIP0080 or HIP0081 may be used in a multiple IC cascade connection. In cascade operation, the diagnostic data from all chips is read as a single serial sequence of fault bits. As shown in the Functional Block Diagram each output stage has voltage and temperature sensors to detect fault conditions while comparators and delay filters process the data. Four bits of diagnostic information is provided as fault feedback from each of the four output stages. When detected, the diagnostic data is put in a parallel diagnostic data register. Using the diagnostic control interface to address the system (one or more ICs in cascade), the fault data is transferred from the parallel diagnostic data register to a serial diagnostic data register as a sequence of 16 bits for each IC.

All diagnostic data bits may be read using the Chip Select ($\overline{CS}$) and the Clock (CLK) inputs. The CLK input must be low, when $\overline{CS}$ goes active low. After reading the first bit at DO to determine if there is an error flag, the following 16 bits of serial diagnostic data may be clocked out of DO. Clocking the CLK input synchronously shifts the serial register data out of DO while cascaded data (from other devices or sources) is shifted into the DI input. As data is shifted out of DO, the parallel diagnostic data register is cleared on the first rising edge of the CLK input, following the $\overline{CS}$ low. After each16 clocks, cascaded diagnostic data from the next IC in sequence is then shifted out of the DO output. Shifting the serial diagnostic data out of DO is done as a continuous sequence, reading the data from all ICs in cascade while $\overline{CS}$ remains low. New diagnostic data can be stored in the parallel diagnostic data registers on each IC while the existing serial diagnostic data is read.

Referring to Figure 1 and Figure 2, there are two sources that generate an OR'd Fault Flag at DO when $\overline{CS}$ goes low. The two fault data sources are (1) the on-chip fault detection and (2) the off-chip DI input from front end ICs in the cascade. The fault data bit, labeled DF (Data Fault) in Figure 2, contains the OR'd inputs from both sources. The DF bit is not part of the 16 bit serial diagnostic data sequence. In cascaded operation, the DI input for the first of the selected chips should be tied low. And, in single IC operation (no cascade), the DI input should also be tied low. In cascaded operation, the Error Flags are cascaded via the DI inputs.

The on-chip fault Error Flag goes high if any one of the 16 diagnostic data fault bits have been set HIGH. This fault Error Flag bit precedes the 16 diagnostic data fault bits and is OR'd with all diagnostic data fault bits. The DF bit flags the presence of an Error Flag fault on the IC and in any part of the cascaded string, including DI data input. As shown in figure 3 each IC in the cascade provides an output which is passed to the DI input of the following IC and is passed on as an OR'd bit to the DO output of the last IC in the cascade. A fault condition is immediately evident without reading all diagnostic data bits. However, all bits must be read to determine which chip and which diagnostic bit has been set. The Fault Flag is reset by the CLK input when the bits are read. When no fault condition is detected, it is not necessary to toggle the CLK input. When a fault is detected, at least one toggle of the clock is needed to reset the parallel diagnostic register which clears the register of all detected fault states.

The last IC in the string ORs its own 16 fault bits in the parallel diagnostic register data and sends this data bit to an Error Flag register. The Error Flag register outputs the presence of a fault in one or more bits of the parallel diagnostic data register. As shown in Figure 2, the Error Flag is the first bit in front of the serial register and is input to OR Gate, U7 with the DI input. The DI input passes thru AND Gate, U6 when the GATE signal is high and output via the amplifier U8 to DO. The output amplifier U8 is active only while $\overline{CS}$ is low. When $\overline{CS}$ is low, the RS Flip-Flop drives the GATE output high. When the GATE is high, the cascaded DF bits are jammed from DI to DO. All Error Flags in the cascade are cleared (by the CLK input) when the serial diagnostic data is clocked out of DO.

The GATE is an internal control signal that is forced high when the CLK input is low and $\overline{CS}$ goes low. The GATE will remain high, even when $\overline{CS}$ is returned to a high state, provided the CLK input has not changed from a low state. This condition still applies when fault data is detected. The DO output is not latched; however, the Error Flag is latched when $\overline{CS}$ goes low and will not be updated until the next time $\overline{CS}$ goes low. The fault data is preserved as long as the CLK input does not go high. If the CLK is high when $\overline{CS}$ goes low, the GATE will be disabled and no cascade data will be shifted from DI to DO. Under normal conditions, the CLK signal goes high to switch the GATE low and simultaneously shifts the first of 16 diagnostic data bits out of the serial diagnostic data register to DO. The $\overline{CS}$ low input is not latched and must be held low while all data is shift of out DO.

The diagnostic interfaces to the HIP0080 and HIP0081 are SPI compatible. The microcontroller is programmed to control the read and respond action based on the diagnostic readout. Normally the $\overline{CS}$ input is addressed and DO is read. If a fault is indicated by the Error Flag, all data is shifted out of DO and processed to determine the diagnostic fault condition. The Error Flag bit does require a separate input back to the microcontroller to initiate the serial data shift. When the CLK signal starts, the serial sequence starting with the first of the 16 serial diagnostic bits is input to the microcontroller.

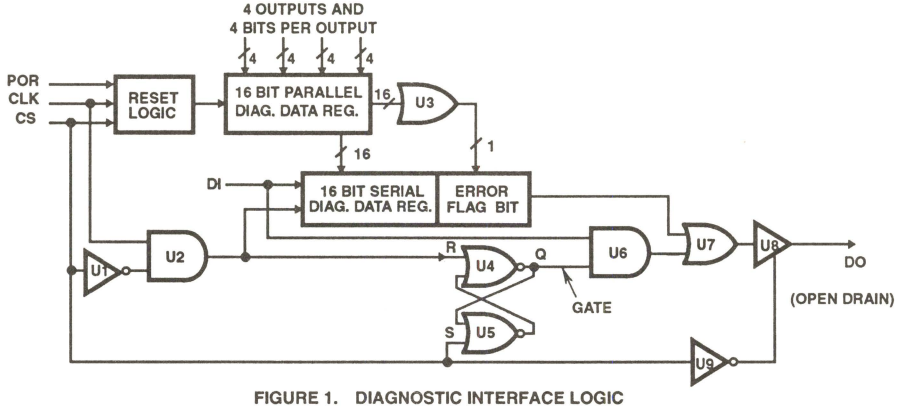


FIGURE 1. DIAGNOSTIC INTERFACE LOGIC

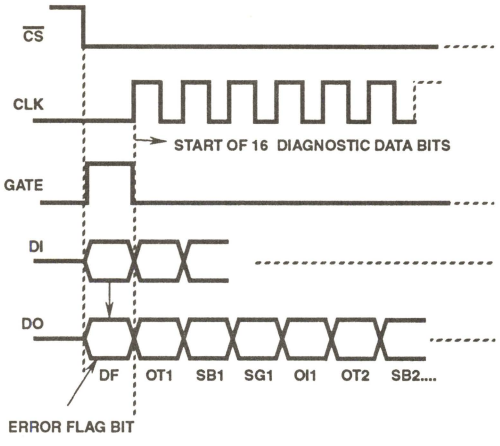


FIGURE 2. DATA AND CLOCK TIMING

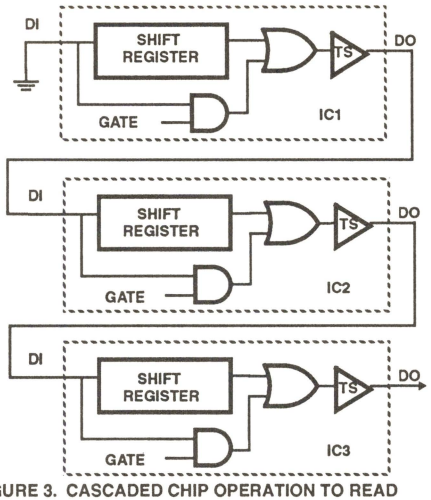


FIGURE 3. CASCADED CHIP OPERATION TO READ DIAGNOSTIC DATA

Serial Register Data Sequence

The fault data follows the Serial Register Data Sequence of Table 1 in bit sequence and, in cascade, by IC sequence. In each of the 4 power switching output channels, the diagnostic sense circuits set 1 bit in the parallel diagnostic register for each of 4 diagnostics fault conditions. A total of 16 diagnostics data bits are shifted to the serial register when $\overline{CS}$ goes low. Table 1 shows the order and sequence of the serial bits as they are shifted out of DO. The fault action that sets each of the diagnostics bits for each of the 4 switches is described below:

Bit 1 - Indicates a thermal overload when the sensed junction temperature of the output is greater than 150°C. When over-temperature is sensed, the sensor output directly gates-off the drive to the power output and the respective fault bit is set in the diagnostic register. When the chip is sufficiently cooled, the output is gated-on if the input remains ON.

Bit 2 - Indicates the fault condition for an output-to-supply short (shorted load). A small value of resistance (~0.01Ω) in the source-to-ground line of the output stage is used to sense the output short. A comparator senses the voltage level and filters the output to provide an input to the control stage and to the diagnostic register. The control state directly shuts down the output when an over-current condition is sensed. Under this condition of fault, the input driver is latched off. To restore the output drive, the short must be removed and the input toggled OFF and then ON. A short to the supply is the only error condition that requires an input toggle reset.

Bit 3 - Indicates the condition of an output to ground short. As shown in the Functional Block Diagram, each output stage has drain-to-supply ($V_{CC}1$) and drain-to-ground pull-up and pull-down resistors of approximately 10kΩ to sense this condition. When the output is off and the sense level is low, an output-to-ground short is detected by the comparator. This condition is sensed when the output is pulled lower than 0.24 x V_{CC} (typical).

Bit 4 - Indicates the condition of an open load on the output. The same divider noted for Bit 3 is used to set the output level. If the sense level is at or near the mid-range of the voltage supply, $V_{CC}1$ when the output is in the off condition, a no-load condition is detected.

TABLE 1. SERIAL REGISTER DATA SEQUENCE

CHANNEL NO.	BIT NO.	FAULT FUNCTION	FAULT SYMBOL
Switch Channel 1	1	Over-temperature	OT1
	2	Short to Supply	SB1
	3	Short to Ground	SG1
	4	Open Load	OI1
Switch Channel 2	5	Over-temperature	OT2
	6	Short to Supply	SB2
	7	Short to Ground	SG2
	8	Open Load	OI2
Switch Channel 3	9	Over-temperature	OT3
	10	Short to Supply	SB3
	11	Short to Ground	SG3
	12	Open Load	OI3
Switch Channel 4	13	Over-temperature	OT4
	14	Short to Supply	SB4
	15	Short to Ground	SG4
	16	Open Load	OI4

Dissipation In Multiple Outputs

The HIP0080 and HIP0081 Power Drivers have multiple MOS Output Drivers and require special consideration with regard to maximum current and dissipation ratings. While each output has a maximum current specification consistent with the device structure, all such devices on the chip can not be simultaneously rated to the same high level of peak current. The total combined current and the dissipation on the chip must be adjusted for maximum allowable ratings, given simultaneous multiple output conditions.

For the HIP0081, the maximum positive output current rating is 3A when one output is ON. When ALL outputs are ON, the rating is reduced to 1.2A because the total maximum current is limited to 5A. For any given application, all output drivers on a chip may or may not have a different level of loading. The discussion here is intended to provide relatively simple methods to determine the maximum dissipation and current ratings as a general solution and, as a special solution, when all switched ON outputs have the same current loading.

General Solution

A general equation for dissipation should specify that the total power dissipation in a package is the sum of all significant elements of dissipation on the chip. However, in Power BiMOS Circuits very little dissipation is needed to control the logic and predriver circuits on the chip. The overall chip dissipation is primarily the sum of the I^2R dissipation losses in each channel where the current, I is the output current and the resistance, R is the NMOS channel resistance, $R_{DS(ON)}$ of each output driver. As such, the total dissipation, P_D for n output drivers is

$$P_D = \sum_{K=1}^{n} P_K \qquad \text{(EQ. 1)}$$

This expression sums the dissipation, P_K of each output driver without regard to uniformity of dissipation in each MOS channel. The dissipation loss in an NMOS channel is

$$P_K = I^2 \times R_{DS(ON)} \qquad \text{(EQ. 2)}$$

where the current, I is the determined by the output load when the channel is turned ON. The channel resistance, $R_{DS(ON)}$ is a function of the circuit design, level of gate voltage and the chip temperature. Other switching losses may include I^2R lost in the interconnecting metal on the chip and bond wires of the package.

The temperature rise in the package due to the dissipation is the product of the dissipation, P_D and the thermal resistance, θ_{JC} of the package (Junction-to-Case). To determine the chip junction temperature, T_J, given the case (heat sink tab) temperature, T_C, the linear heat flow solution is

$$T_J = T_C + P_D \times \theta_{JC} \text{ or } T_C = T_J - P_D \times \theta_{JC} \qquad \text{(EQ. 3)}$$

Since this solution relates only to the package, further consideration must be given to a practical heat sink. The equation of linear heat flow assumes that the thermal resistance from Junction-to-Ambient (θ_{JA}) is the sum of the thermal resistance from Junction-to-Case and the thermal resistance from Case (heat sink)-to-Ambient. The Junction-to-Ambient thermal resistance, θ_{JA} is the sum of all thermal paths from the chip junction to the ambient temperature (T_A) environment and can be expressed as

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad \text{(EQ. 4)}$$

The Junction-to-Ambient equivalent to Equation 3, 3A is

$$T_J = T_A + P_D \times \theta_{JA} \text{ or } T_A = T_J - P_D \times \theta_{JA}. \qquad \text{(EQ. 5, 5A)}$$

Not all Integrated Circuit packages have a directly defineable case temperature because the heat is spread thru the lead frame to a PC Board which is the effective heat sink.

Calculation Example 1

For the HIP0081, θ_{JC} = 3°C/W and the worst case junction temperature, as an application design solution, should not exceed 150°C. For a given application, Equation 1 determines the dissipation, P_D.

Assume the package is mounted to a heat sink having a thermal resistance of 6°C/W and, for a given application, assume the dissipation is 3W and the ambient temperature (T_A) is 100° C From Equation 4, θ_{JA} is 9°C/W. The solution for junction temperature (T_C) by Equation 3 is

$$T_J = +100°C + 3W \times 9°C/W = +127°C$$

Calculation Example 2

Assume for the HIP0080, θ_{JA} = 30°C/W mounted on a PC Board with good heat sinking characteristics. Again, the worst case junction temperature, as an application design solution, should not exceed +150°C. Assume from the application, based on Equation 1, the dissipation, P_D = 1.5W. The maximum junction temperature is known and can be used to determine the maximum allowable ambient temperature from Equation 5A as follows:

$$T_A = +150°C - 1.5W \times 30°C/W = 105°C$$

Equal Current Loading Solution

Many applications may have equal current loading in the output drivers with equal saturated turn ON and temperature conditions. As such, a convenient method to show rating boundaries is to substitute the dissipation Equation 2 into the junction temperature Equation 3. For m outputs that are ON and conducting with equal currents, where $I=I_1=I_2.....=I_m$, we have the following solution for dissipation:

$$P_D = m \times P_K = m \times I^2 \times R_{DS(ON)} \qquad \text{(EQ. 6)}$$

$$I = \sqrt{\frac{T_J - T_C}{m \times \theta_{JC} \times R_{DS(ON)}}} \qquad \text{(EQ. 7)}$$

The number of output drivers ON and conducting (m) may be from 1 to n. (i.e., For all four output drivers of the HIP0081 ON, m=4.) Maximum temperature, dissipation and current ratings must be observed. For a defined number of conducting Power MOS Output Drivers, we can plot the results for m devices showing I vs T_C.

Given the HIP0081 as an example, Figure 4 and Figure 5 illustrate the boundaries for temperature and current. Figure 4 shows the maximum current for a single output ON while Figure 5 shows the maximum current for all four outputs ON with equal current plotted versus Case Temperature, T_C. Boundary conditions relate to the Absolute Maximum Ratings as defined in the Data Sheet.

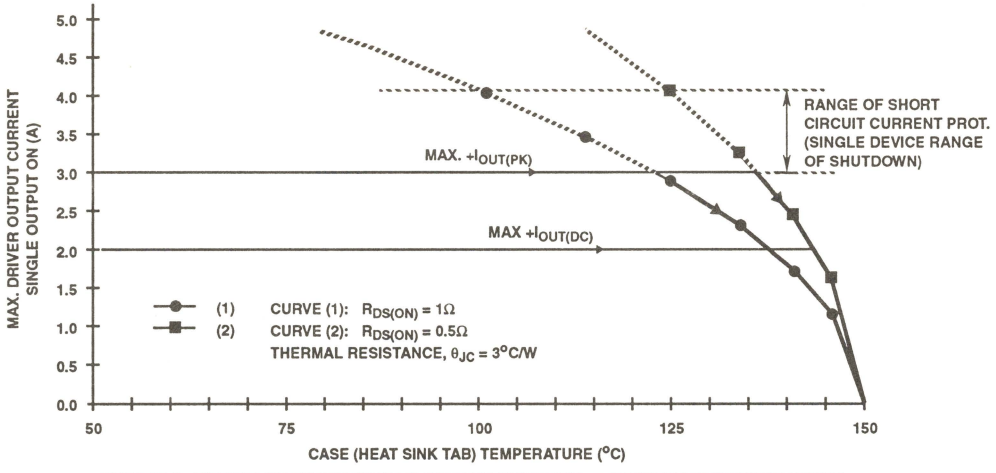


FIGURE 4. HIP0081 MAXIMUM SINGLE OUTPUT CURRENT vs CASE (TAB) TEMPERATURE

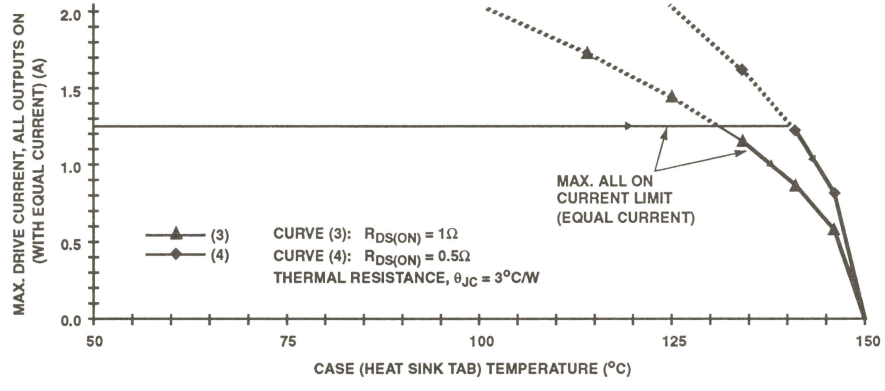


FIGURE 5. HIP0081 CURRENT vs CASE (TAB) TEMPERATURE, ALL OUTPUTS ON WITH EQUAL CURRENT

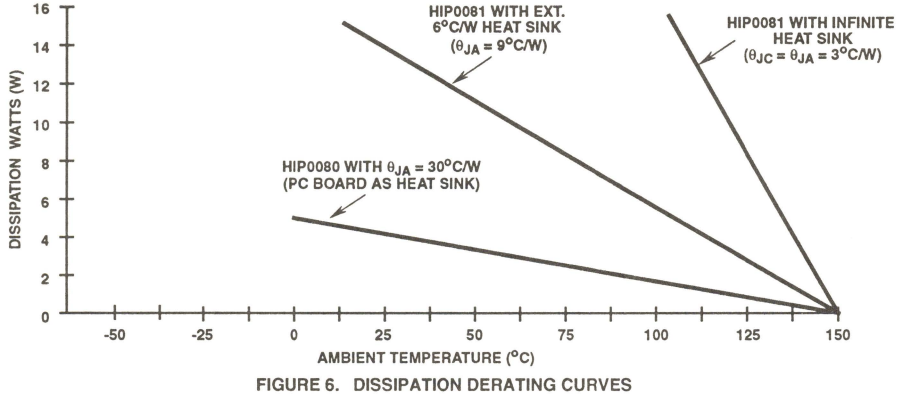


FIGURE 6. DISSIPATION DERATING CURVES

HARRIS SEMICONDUCTOR

HIP0082

PRELIMINARY

April 1994

Quad Power Driver with Serial Diagnostic Interface

Features

- Low Side Power MOSFET Output Drivers
  - Output Voltage Rating 75V
  - Maximum Output Current Switching 2A
  - Max. Output R_{DSON} (T_J = +150°C) 0.57Ω/0.62Ω
- Programmable Output Current Limiting
  - Bit Select 2A or 5A on Outputs 3 and 4
- Output Protection
  - Output Over-Current Shutdown
  - Output Over-Voltage Clamp
  - Over-Temperature Diagnostic Feedback
- Diagnostics for Shorts, Opens and Over-Temperature
- Synchronous Serial Interface with
  - 22-Bit Serial Diagnostic Register
  - SPI Compatible Interface
- Single 5V Supply Operation with CMOS Logic Inputs
- Low I_{CC} Supply Current with Full Load 10mA
- Low θ_{JC} Power SIP Package . . . . . .3°C/W
- -40°C to +125°C Operating Temperature

Description

The HIP0082 Quad Power Driver contains four individually protected NDMOS transistor switches to drive inductive and resistive loads such as: fuel injectors, relays, solenoids, etc. The outputs are low-side switches driven by active-low CMOS logic inputs. Each output is protected against excessive current due to a short-circuit. Internal drain-to-gate zener diodes provide output clamping for over-voltage. An integrated charge pump allows operation from a single 5V logic supply. Diagnostic circuits provide ground short (SG), supply short (SC) and open load (OL) detection for each of the four output stages and indicate over-temperature. Diagnostic information may be read via a synchronous serial interface. Six bits of write/store data controls the OL fault delay time or sets Outputs 3 and 4 to the 2A or 5A mode.

The HIP0082 is fabricated in a Power BiMOS IC process and is intended for use in automotive and other applications with a wide range of temperature and electrical stress. It is particularly suited for driving high-current inductive loads requiring high breakdown voltage and high output current.

The HIP0082 is supplied in a 15 Lead Power SIP package with lead form options for either vertical or surface mount.

Applications

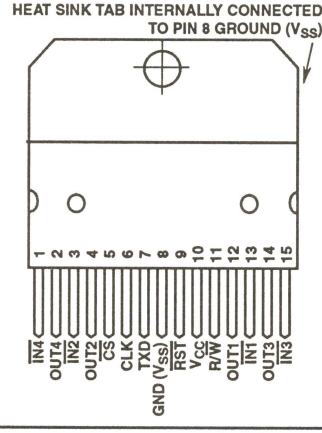
- Drivers For
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use
  - Automotive
  - Appliances
  - Industrial
  - Robotics

Ordering Information

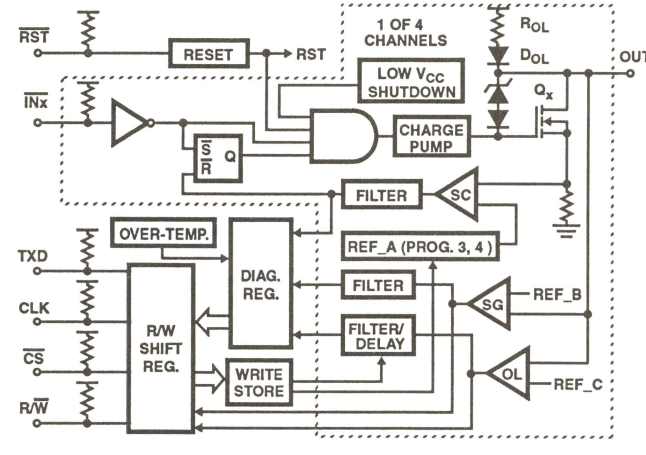
PART NUMBER	TEMPERATURE RANGE	PACKAGE AND LEAD FORM
HIP0082AS1	-40°C to +125°C	15 Lead Plastic SIP Staggered Vertical Mount
HIP0082AS2	-40°C to +125°C	15 Lead Plastic SIP Surface Mount

Pinout

HIP0082 (SIP)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3643

Absolute Maximum Ratings

Supply Voltage (Logic and Control), V_{CC} . . . . . -0.3V to 7V
Power MOSFET Drain Voltage, V_O (Note 1) . . . . . -0.7 to V_{CLAMP}
Output Clamp Energy, E_{OK} . . . . . TBDmJ
Input Voltage (Logic and Driver Inputs), V_{IN} . . . .-0.5V to V_{CC} +0.5V
Maximum Output Current, Outputs 1 and 2 . . . . . +2A
Maximum Output Current, Outputs 3 and 4 . . . . . +5A
Maximum Total Output Current, All Outputs ON . . . . . +8A
Maximum Peak Output Current, $I_{O(MAX)}$, (Note 2) . . . . . -5A to I_{SC}
Operating Ambient Temperature Range . . . . . -40°C to +125°C
Operating Junction Temperature Range . . . . . -40°C to +150°C
Storage Temperature Range, T_{STG} . . . . . -55°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic 15 Lead SIP Power Package	45°C/W	3°C/W

Power Dissipation
Up to +125°C without heat sink 0.56W
Above +125°C without Heat Sink . . .Derate Linearly at 22mW/°C
Up to +125°C with Infinite Heat Sink 8.33W
Above +125°C with
Infinite Heat Sink . . . . . .Derate Linearly at 333mW/°C
Lead Temperature (During Soldering)
At a Distance 1/16 inch ±1/32 inch (1.59mm ±0.79mm)
from Case for 10s Max. . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = 5V ±10%, T_A = -40°C to +125°C; Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER OUTPUTS						
Output ON Resistance (Normal Mode)	R_{DSON1}, R_{DSON2}	Outputs 1 and 2, One Output ON, I_{OUT} = 2A, T_J = +150°C	-	-	0.62	Ω
	R_{DSON3}, R_{DSON4}	Outputs 3 and 4, One Output ON, I_{OUT} = 2A, T_J = +150°C	-	-	0.57	Ω
Output ON Resistance, Open-Load Detection Mode	$R_{DSON1OL}$, $R_{DSON2OL}$	Outputs 1 and 2, One Output ON, I_{OUT} = 10mA, T_J = +150°C	-	-	6.2	Ω
	$R_{DSON3OL}$, $R_{DSON4OL}$	Outputs 3 and 4, One Output ON, I_{OUT} = 10mA, T_J = +150°C	-	-	5.7	Ω
Output Clamp Voltage	V_{CLAMP}	I_{OUT} = 40mA	72	-	90	V
Current Limit, Outputs 3 and 4	$I_{SC(H)}$	ISC Bit Low	5.1	-	7.4	A
Current Limit, Outputs 1, 2, 3 and 4	$I_{SC(L)}$	ISC Bit High	2.1	-	3.4	A
Over-Current Shutdown Time, Outputs 1 and 2	t_{SC1}, t_{SC2}	$I_{OUTX} = I_{SC(L)}$, From 30% of INx to 30% of OUTx	-	-	1	µs
Over-Current Shutdown Time, Outputs 3 and 4	t_{SC3}, t_{SC4}	$I_{OUTX} = I_{SC(L)}$, From 20% of INx to 20% of OUTx	-	-	1	µs
Output Positive Voltage Ramp Rate		V_{CC} = 12V, Ind. Load 120mH with 6Ω in Series; Measure 25% to 75%	5	-	40	V/µs
Output Negative Voltage Ramp Rate		V_{CC} = 12V, Ind. Load 120mH with 6Ω in Series; Measure 75% to 25%	2	-	12	V/µs
Output Negative Voltage Ramp Time at Maximum Load		V_{CC} = 12V, Resistive Load, I_{OUTX} = 2A, Measure 90% to 10%	-	-	25	µs
Turn-Off Delay	$t_{d(OFF)}$	V_{CC} = 12V, R_L = 6Ω From 50% of $\overline{INx}$ to 10% of OUTx	0.5	-	3	µs
Output Leakage Current	I_{LK}	$\overline{INx}$ = High, V_{OUTX} = 72V	-	-	5	µA
Maximum Current in Open-Load Detection Mode.	$I_{OL(MAX)}$	$R_{DSON(MAX)}$ = 5.7Ω or 6.2Ω	90	-	180	mA
Minimum Current in Normal Mode	$I_{NM(MIN)}$	$R_{DSON(MAX)}$ = 0.57Ω or 0.62Ω	0.4 X $I_{OL(MAX)}$	-	0.95 X $I_{OL(MAX)}$	mA
SUPPLY						
Power Supply Current	I_{CC}	Standby, No Load	-	7.5	15	mA
Low V_{CC} Shutdown Threshold	$V_{CC(LOW)}$	(Note 3)	3.4	-	4.1	V
Active Supply Range for $\overline{RST}$ Pin	$V_{CC(RST)}$		3.5	-	5.5	V

Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to +125°C; Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS ($\overline{INx}$, $\overline{CS}$, CLK, $\overline{RST}$, R/$\overline{W}$, TXD)						
Low-Level Input Voltage	V_{IL}		-	-	0.2 X V_{CC}	V
High-Level Input Voltage	V_{IH}		0.7 x V_{CC}	-	V_{CC} + 0.3	V
Input Hysteresis Voltage	V_{HYS}		0.85	-	2.25	V
Input Pull-Up Resistance	R_{IN}		20	-	300	kΩ
Input Current	I_{IN}	V_{IN} = High	-	-	2	µA
TXD Pin (R/$\overline{W}$ = High)						
Three-State Leakage Current	I_{L_TXD}	$\overline{CS}$ = High, V_{TXD} = V_{CC}	-5	-	+5	µA
Logic High Output Voltage	V_{TXDH}	I_{OH} = -4mA, $\overline{CS}$ = Low	V_{CC} - 0.4	-	-	V
Logic Low Output Voltage	V_{TXDL}	I_{OL} = 3.2mA, $\overline{CS}$ = Low	-	-	0.42	V
DIAGNOSTIC AND PROTECTION						
Over-Temperature Detection Threshold	T_{TMP}		-	165	-	°C
Over-Temperature Hysteresis	T_{HYS}		-	15	-	°C
Output Short-to-Gnd Threshold	V_{SG}		2.4	-	2.9	V
Short-to-Gnd Filter Time	t_{SG}		150	-	350	µs
Open-Load Threshold for High R_{DSON}	I_{OLH}		3	-	20	mA
Pull-up Resistance for Open-Load Detection	R_{OL}		2	-	6.5	KΩ
Open-Load Delay Time after $\overline{INx}$ H→L	t_{DOLL}	Td_OLx Bit = Low	3	-	5.2	ms
Open-Load Delay Time after $\overline{INx}$ H→L	t_{DOLH}	Td_OLx Bit = High (Note 4)	190	-	690	µs
SERIAL INTERFACE (See Figure 3)						
Serial Clock Frequency	f_{CLK}	50% Duty Cycle, C_{EXT} = 50pF	-	-	3	MHz
Propagation Delay CLK to Data Valid	t_{PCLKDV}		-	-	150	ns
Setup Time, $\overline{CS}$ to CLK	t_{CSLCLK}		150	-	-	ns
$\overline{CS}$ Low to Data Valid	t_{CSLDV}		-	-	100	ns
Hold Time $\overline{CS}$ after CLK	t_{CLKCSH}		150	-	-	ns
$\overline{CS}$ High to Output High Z	t_{CSHDZ}		-	-	100	ns
Minimum Time CLK = High	t_{CLKH}		100	-	-	ns
Minimum Time CLK = Low	t_{CLKL}		100	-	-	ns
Setup Time R/$\overline{W}$ Low to CLK	t_{RWLCLK}		150	-	-	ns
R/$\overline{W}$ Low to Output High Z	t_{RWLDZ}		-	-	100	ns
Setup Time Data Valid to CLK Low	t_{DVCLKL}		20	-	-	ns
Setup Time R/$\overline{W}$ High to CLK	t_{RWHCLK}		100	-	-	ns
Time R/$\overline{W}$ High to Data Valid	t_{RWHDV}		-	-	100	ns

NOTES:

1. The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns on the MOSFET to hold the Drain at the V_{CLAMP} voltage. Refer to the Electrical Specifications Table for the V_{CLAMP} voltage limits.
2. Each Output has Over-Current Shutdown protection in the positive current direction. The maximum peak current rating is set equal to the minimum Over-Current Shutdown as detailed in the Electrical Specification Table. In the event of an Over-Current Shutdown the input drive is latched OFF. The output short must be removed and the input toggled OFF and ON to restore the output drive.
3. The "Low V_{CC} Shutdown" is an internal control that switches off all power drive stages when V_{CC} is less than $V_{CC(LOW)}$.
4. Measurement includes the Filter Time.

Functional Description

Reset Operation

There are two ways to reset the IC. The first is at power-up, when the on-chip reset circuitry ensures that all counters and registers are reset and that the programmable functions are in their default states. The second way occurs when the $\overline{RST}$ pin is switched active low.

After a reset (and after power-up) the short-circuit current (3, 4) is set to the higher value and the delay times for the open-load circuits are set to the higher value between 3ms and 5.2ms.

Low Power Drive Shutdown

There is a low voltage power drive shutdown when the supply voltage, V_{CC} drops below the voltage threshold, $V_{CC(LOW)}$. During the low voltage condition the output stages are held off.

Over-Voltage Clamp Operation

A drain-to-gate zener diode on each output driver internally clamps an over-voltage pulse, including the kick pulse generated when turning off an inductive load. While providing over-voltage protection, it is not part of the diagnostic feedback via the Diagnostic Register.

Short-Circuit Protection

If the output current is above the current limit for a time greater than t_{SC} the output is switched off and the corresponding bit in the diagnostic register set. The current level for shutdown on outputs 3 and 4 is programmable between 2A and 5A with the ISC bit. After shutdown, the output remains off until the corresponding input is taken high and again low.

Open-Load Detection

Load currents are monitored while the outputs are ON. If a load current is below the I_{OL} threshold, an open-load condition is detected. After a delay time t_{DOL} (which is programmable between two levels) the condition is stored in the diagnostic register. The outputs of the open-load comparators (OL) are also connected directly to the diagnostic register so that they can be monitored via the serial interface.

Output Short-to-Ground Detection

When the voltage on an output pin is below V_{SG} and the output is off, a ground short is detected and stored in the diagnostic register after a delay t_{SG}. The outputs of the short-to-ground (SG) comparators are also connected directly to the diagnostic register so that they can be monitored via the serial interface.

Serial Interface Operation

Microprocessor communication to the diagnostic/control registers is via a 4 wire serial interface. Data control is bidirectional, the direction of data transfer being dependent on the state of the R/$\overline{W}$ pin (See Figure 1).

Diagnostic Read Operation

When $\overline{CS}$ goes from high to low (while CLK is high), the TXD pin exits three-state and outputs the FSB bit which indicates whether any of the other bits in the shift register are set. All data can be read on the high-to-low transition of the clock input (see Figure 2). The bit descriptions are as follows:

FSB Bit - Indicates that one or more of the bits in the diagnostic register are set.

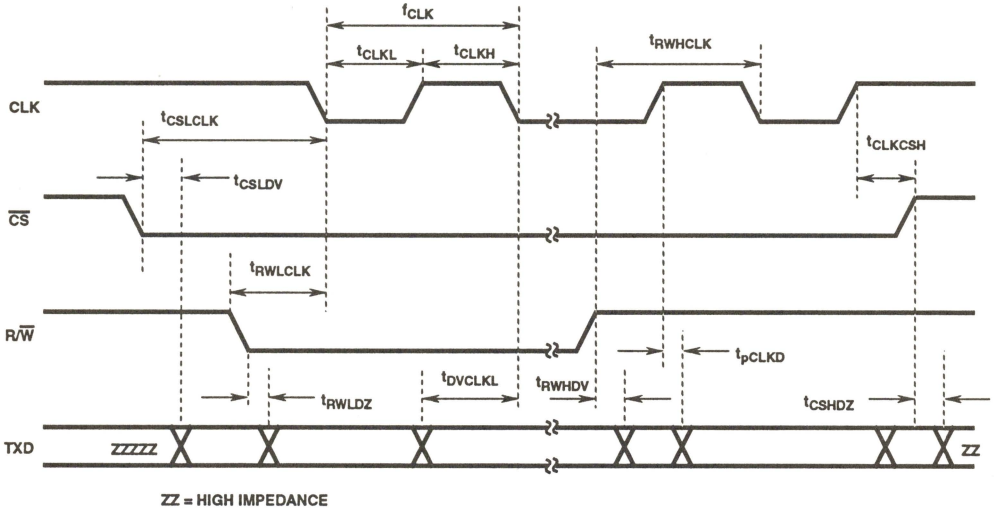


FIGURE 1. SERIAL INTERFACE TIMING DIAGRAM

TMP Bit - Indicates that the chip temperature has exceeded the limit T_{TMP}. The outputs are not switched off when this occurs; the condition is indicated by the setting of the TMP bit. Sensors for the TMP bit are located near the power drivers and are OR'd to provide a single bit for the chip.

SCx Bits - Indicate a short-circuit to battery or over-current on the corresponding output.

OLx Bits - Indicate that no load (or a high resistance load) is connected to the corresponding output.

SGx Bits - Indicate that the voltage on the corresponding output is below the V_{SG} limit.

The final 8 bits (most significant bits) of the diagnostic word indicate the states of the open-load and short-to-ground comparators when the $\overline{CS}$ pin went from high to low. Using this feature, an external microprocessor can monitor the status of the OL and SG comparators directly.

Diagnostic Write Operation

When the R/$\overline{W}$ pin is in the low state it is possible to write six bits to the IC to influence its mode of operation. The write operation is illustrated in Figure 3. The programmable bits are as follows:

Test Bit - Used to put the IC in test mode (not recommended). This bit should be low for normal operation.

ISC Bit - This bit programs the short-circuit level for outputs 3 and 4. When this bit is set high the lower value for the current shutdown threshold is set.

Td_OLx Bits - These bits set the delay times for the open-load measurements individually for each of the four outputs. A logical high sets the open-load delay time to its shorter value.

Pin Descriptions

V_{CC} and GND - 5V Supply and Ground connections. A charge pump is used to boost the Power MOSFET gate drive. This allows a single 5V supply to satisfy all logic and drive requirements.

OUT1 - OUT4 - Low-side output drivers with 0.62Ω (OUT1 and OUT2) or 0.57Ω (OUT3 and OUT4) on resistance. The outputs are provided with over-current shutdown and over-voltage clamping. Additionally open-load and short-to-ground detection is carried out when the outputs are ON.

$\overline{IN1}$ - $\overline{IN4}$ - Active-low CMOS logic inputs which control the output stages OUT1 - OUT4. These inputs are provided with pull-up resistors.

$\overline{RST}$ - Active-low logic-level reset input with internal pull-up resistor. When $\overline{RST}$ is in the low state all outputs are off and all registers and counters are reset. When the reset pin is taken high the IC remains in reset mode for a time t_{RST}.

CLK - Clock input for synchronous serial interface with internal pull-up resistor. This input must be high when $\overline{CS}$ transitions from high to low.

$\overline{CS}$ - Active-low chip select input for serial interface. This input has an internal pull-up resistor.

R/$\overline{W}$ - Read/write control pin for serial interface. This input controls whether the TXD pin is an input or output.

TXD - Bidirectional data pin for serial interface. When R/$\overline{W}$ is high diagnostic data can be read from HIP0082. When R/$\overline{W}$ is low, 6 bits may be written to the internal program register.

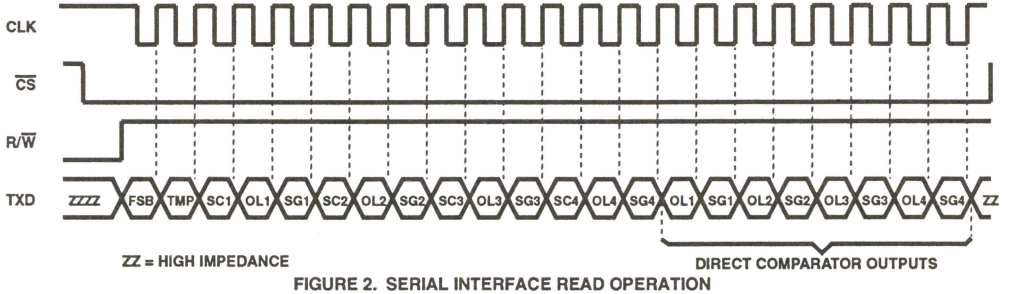


FIGURE 2. SERIAL INTERFACE READ OPERATION

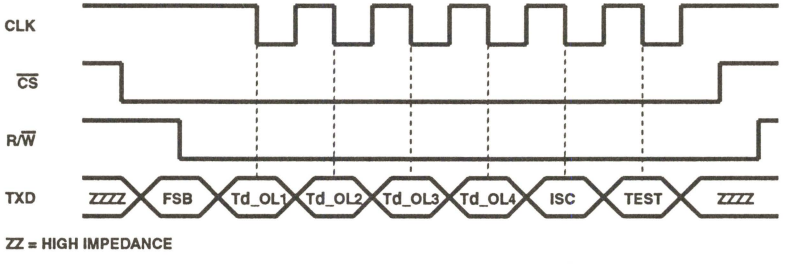


FIGURE 3. SERIAL INTERFACE WRITE OPERATION

INTELLIGENT POWER ICs

3

HIGH SIDE SWITCHES

		PAGE
HIGH SIDE SWITCHES SELECTION GUIDE		3-2
HIGH SIDE SWITCHES DATA SHEETS		
CA3273	High-Side Driver	3-3
HIP1030	1A High Side Driver with Overload Protection	3-6
HIP1031	Half Amp High Side Driver with Overload Protection	3-10
HIP1090	Protected High Side Power Switch with Transient Suppression	3-13
HV400	High Current MOSFET Driver	3-18
HV400MJ/883	High Current MOSFET Driver	3-28
ICL7667	Dual Power MOSFET Driver	3-38

High Side Switches Selection Guide

TYPE	FUNCTION	MAX SUPPLY	DC SUPPLY RANGE	PEAK MAX CURRENT	DC MAX CURRENT	PACKAGE	RECOMMENDED APPLICATIONS
PROTECTED POWER SWITCHES							
CA3273	Single Power	40V	4V to 24V	1.2A	0.6A	3 Lead Mod. TO-202	Solenoid, Relay, Lamp and Motor
HIP1030	Single Power	35V	4.5V to 25V	2.5A	1.1A	5 Lead TS-001AA	Solenoid, Relay, Lamp and Motor
HIP1031	Single Power	35V	4.5V to 25V	1.7A	0.7A	5 Lead TS-001AA	Solenoid, Relay, Lamp and Motor
HIP1090	Single Power	±90V, 15ms	4V to 16V	2A	1A	3 Lead TO-220	Solenoid, Relay, Lamp and Motor

TYPE	FUNCTION	MAX SUPPLY	DC SUPPLY RANGE	PEAK MAX CURRENT	MAX FREQUENCY	PACKAGE	RECOMMENDED APPLICATIONS
MOSFET DRIVERS							
HV400	Single High Speed	35VDC	15V to 30V	6A (Source) 30A Sink (Pulsed)	20kHz (MC) 200kHz (SMPS)	8 Lead PDIP and SOIC	SMPS, FET Drivers., and Motor Controllers
ICL7667	Dual Power	15V	4.5V to 15V	1.5A (Pulsed Gate)	200kHz	8 Lead TO-99, PDIP, CerDIP, and SOIC	SMPS, FET Drivers, and Motor Controllers

HARRIS SEMICONDUCTOR

CA3273

April 1994

High-Side Driver

Features

- Equivalent High Pass P-N-P Transistor
- Current Limiting.....0.6A to 1.2A
- Over-Voltage Shutdown.....+25V to +40V
- Junction Temperature Thermal Limit.....+150°C
- Equivalent Beta of 25.....400mA/0.5V
- Internal Bandgap Voltage and Current Reference

Applications

- Fuel Pump Driver
- Relay Driver
- Solenoid Driver
- Stepper Motor Driver
- Remote Power Switch
- Logic Control Switch

Description

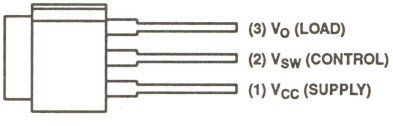
The CA3273 is a power IC equivalent of a P-N-P pass transistor operated as a high-side-driver current switch in either the saturated (ON) or cutoff (OFF) modes. The CA3273 incorporates circuitry to protect the pass currents, excessive input voltage, and thermal overstress. The high-side driver is intended for general purpose, automotive and potentially high-stress applications. If high-stress conditions exist, the use of an external zener diode of 35V or less between supply and load terminals may be required to prevent damage due to severe conditions (such as load dump, reverse battery and positive or negative transients). The CA3273 is designed to withstand a nominal reverse-battery (VBAT = 13V) condition without permanent damage to the IC. The CA3273 is supplied in a modified 3-lead TO-202 plastic power package.

Ordering Information

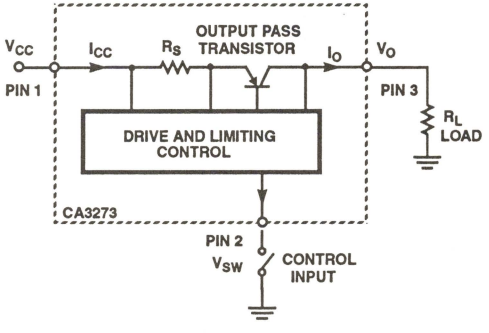
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3273	-40°C to +85°C	TO-202 Modified SIP

Pinout

CA3273 (SIP)
TOP VIEW



Block Diagram



3 HIGH SIDE SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2113.4**

Absolute Maximum Ratings

Fault Max, Supply Voltage, V_{CC} 40V
Maximum Operating V_{CC}:
At I_O=400mA (-40°C to +85°C Ambient) 16V
At I_O=600mA (-40°C to +25°C Ambient) 24V
Max. Positive Output Peak Pulse, V_{SW} Open .....V_{CC}+12V
Max. Operating Output Load Current 600mA
Short Circuit Load Current, I_{SC} .....Internal Limiting
Reverse Battery ..... -13V

Thermal Information

Thermal Resistance θ_{JA}
Plastic SIP Package .....+70°C/W
Maximum Power Dissipation, P_D
At +25°C Ambient, T_A (Note 1).....1.8W
Derate above +25°C (No Heat Sink) .....14.3mW/°C
Maximum Junction Temperature, T_J (Note 2) ..... 150°C
Ambient Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-40°C to +150°C
Lead Temperature (Soldering 10s max) .....+265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +85°C, Unless Otherwise Noted, See Block Diagram for Test Pin Reference

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	V_{CC} Reference to V_{SW}	4	-	24	V
Saturation Voltage(V_{CC} - V_O)	V_{SAT}	I_O = -400mA, V_{SW} = 0V, V_{CC} = 16V	-	-	0.5	V
Operating Load	R_L	V_{SW} = 0V (Switch ON)				
		T_A = +85°C, V_{CC} = 16V	40	-	-	Ω
		T_A = +25°C,V_{CC} = 24V	40			Ω
Over-Voltage Shutdown Threshold	$V_{CC(THD)}$	V_{SW} = 0V,R_L = 1kΩ, Increase V_{CC}, (V_O goes low)	25	33	40	V
Over-Current Limiting	$I_{O(LIM)}$	V_{CC} =16V,V_{SW} = 1V (Switch ON)	-	-	1.2	A
Over-Temperature Limiting	T_{LIM}		-	150	-	°C
Control Current, Switch ON	I_{SW}	V_{CC} =16V, V_{SW} = 0V				
		I_O = 0mA	-	-15	-	mA
		I_O = -400mA	-	-22	-	mA
Control Current, Max. Load, Switch ON		V_{CC} = 24V,V_{SW} = 0V, I_O = -600mA	-	-33	-	mA
Max. Control Current,High and Low V_{CC}	$I_{SW(MAX)}$	R_L = 40Ω, V_{SW} =1V				
		V_{CC} = 24V	-50	-	-	mA
		V_{CC} = 7V	-50	-	-	mA
Min. Control Current, No Load, Switch OFF	$I_{SW(NL)}$	V_O = Open,(Switch OFF)				
		V_{CC} = 24V,V_{SW} = 23V	-200	-	+50	µA
		V_{CC} = 7V, V_{SW} = 6V	-200	-	+50	µA
Output Current Leakage	$I_{O(LEAK)}$	V_O = 0V, V_{CC} = 16V, (Switch OFF)				
		V_{SW} =16V	-100	-	+100	µA
		V_{SW} =15V	-100	-	+100	µA

NOTES:

1. The calculation for dissipation and junction temperature rise due to dissipation is: $P_D = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{SW}$ and $T_J = T_A + P_D \times \theta_{JA}$ where T_J is device junction temperature, T_A is ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance.
2. Thermal limiting occurs at +150°C on the chip.

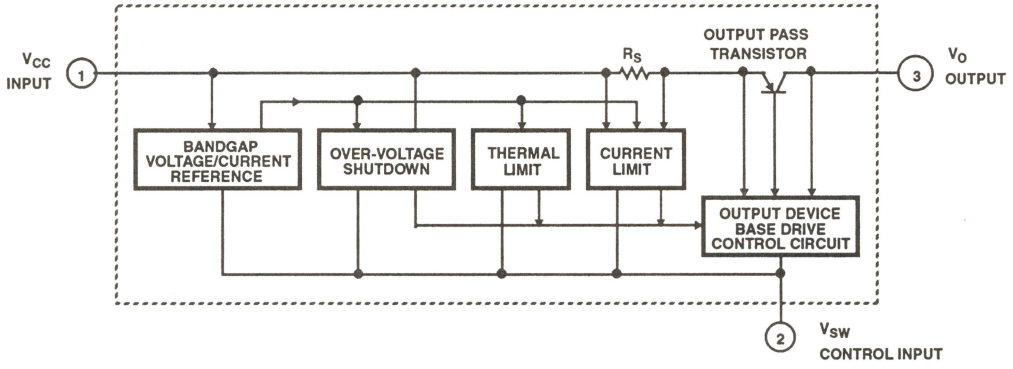


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF CA3273

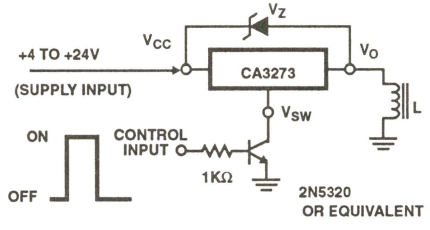


FIGURE 2. TYPICAL APPLICATION WITH ZENER DIODE FOR OVER-VOLTAGE PROTECTION WITH INDUCTIVE LOAD SWITCHING. V_Z SHOULD BE LESS THAN 35V. WHEN CURRENT IS SWITCHED OFF IN THE OUTPUT LOAD (L), THE INDUCTIVE KICK PULSE GOES NEGATIVE. THE CLAMPED CLAMP LEVEL OF THE NEGATIVE GOING PULSE IS V_{CC} - V_Z.

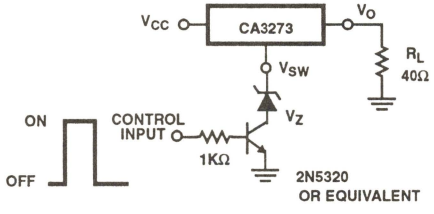


FIGURE 3. OPTIONAL RANGE SHIFTING OF THE V_{CC} INPUT VOLTAGE USING A ZENER DIODE TO OFFSET THE V_{SW} CONTROL PIN. (I.E.,THE OVER-VOLTAGE SHUTDOWN THRESHOLD WILL BE INCREASED TO $V_{CC(THD)}$ + V_Z AND THE MINIMUM V_{CC} OPERATING VOLTAGE IS V_Z + 4V).

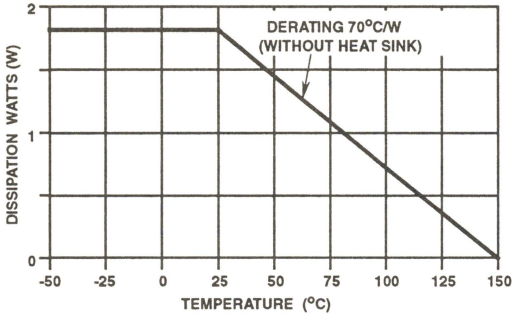


FIGURE 4. DISSIPATION DERATING CURVES

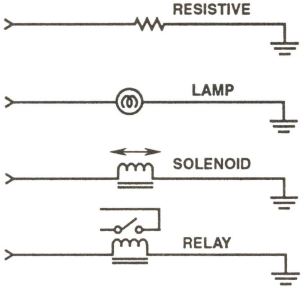


FIGURE 5. TYPICAL LOADS

HARRIS SEMICONDUCTOR

HIP1030

PRELIMINARY

April 1994

1A High Side Driver with Overload Protection

Features

- Over Operating Temperature Range -40°C to +125°C
  - 1V Max V_{SAT} at 1A
  - 1A Current Switching Capability
  - 4.5V to 25V Power Supply Range
- Over-Voltage Shutdown Protected
- Over-Current Limiting
- Thermal Limiting Protection
- 60V_{PK} Load Dump
- Reverse Battery Protection to -16V

Applications

- Motor Driver/Controller
- Driver for Solenoids, Relays and Lamps
- MOSFET and IGBT Driver
- Driver for Temperature Controller

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP1030AS	-40°C to +125°C	5 Lead TS-001AA SIP

Description

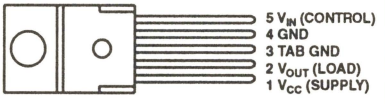
The HIP1030 is a High Side Driver Power Integrated Circuit designed to switch power supply voltage to an output load. It is the equivalent of a PNP pass transistor operated as a protected high side current switch in the saturated ON state with low forward voltage drop at the maximum rated current. The HIP1030 has low output leakage and low idle current in the OFF state.

The Functional Block Diagram for the HIP1030 shows the protection control circuit functions of over-current, overvoltage and over-temperature. A small metal resistor senses over-current in the power supply path of the pass transistor and load. Overvoltage detection and shutdown of the output driver occurs when a comparator determines that the supply voltage has exceeded a comparator reference level. Over-temperature is sensed from a V_{BE} differential sense element that is thermally close to the output drive transistor. In addition to the input detected overvoltage protection, negative peak voltage of a switched inductive load is clamped with an internal zener diode. An internal bandgap voltage source provides a stable voltage reference over the operating temperature range, providing bias and reference control for the protection circuits.

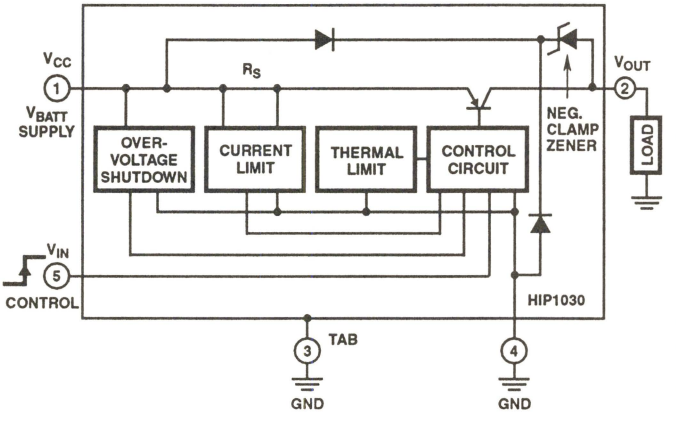
The HIP1030 is particularly well suited for driving lamps, relays, and solenoids in automotive and industrial control applications where voltage and current overload protection at high temperatures is required. The HIP1030 is supplied in a 5 lead TS-001AA Power SIP package.

Pinout

HIP1030 (SIP)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
Copyright © Harris Corporation 1994

File Number **2788.5**

Absolute Maximum Ratings

Max. Supply Voltage V_{CC} . . . . . See O.V. Shutdown Limit, V_{OVSD}
Input Voltage, V_{IN} (Note 1) . . . . . -1V to (V_{CC} - 0.5V)
Load Current, I_{OUT} . . . . . Internal Limiting
Load Dump (Survival) . . . . . $\pm 60V_{PK}$
Reverse Battery . . . . . -16V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic SIP Package	50°C/W	4°C/W

Maximum Power Dissipation (Note 2)
At T_A = +125°C, Infinite Heat Sink 6.25W
Maximum Junction Temperature, T_J . . . . . 150°C
Ambient Operating Temperature . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -40°C to +150°C
Lead Temperature (Soldering 10s max) . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +125°C, V_{IN} = 2V, V_{CC} = +12V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		4.5	-	25	V
Over-Voltage Shutdown	V_{OVSD}	R_L = 1KΩ; V_{IN} = 2V	26	33	38	V
Over-Temperature Limiting	T_{SD}		-	150	-	°C
Negative Pulse Output Clamp Voltage	V_{CL}	I_{CL} = -100mA; V_{CC} = 4.5V to 25V	(V_{CC} - 35)	(V_{CC} - 30.5)	(V_{CC} - 28)	V
Short Circuit Current Limiting	I_{SC}	(Note 4)	1.1	1.6	2.5	A
Input Control ON	V_{IH}		2.0	-	-	V
Input Control OFF	V_{IL}		-	-	0.8	V
Input Current High	I_{IH}	V_{IN} = 5.5V, V_{CC} = 6V to 24V	6	-	40	µA
Input Current Low	I_{IL}	V_{IN} = 0.8V, V_{CC} = 6V to 24V	6	-	30	µA
Supply Current, Full Load Input Control ON	I_{CCMAX}	V_{IN} = 2V; I_{OUT} = 1.0A;	-	1.05	1.1	A
Supply Current, No Load Input Control OFF	I_{CCMIN}	V_{IN} = 0V; I_{OUT} = 0A;	-	55	100	µA
Input-Output Forward Voltage Drop (V_{CC} - V_{OUT})	V_{SAT}	I_{OUT} = 1A; V_{CC} = 4.5V to 25V	-	0.6	1	V
Output Leakage	I_{OUT_LK}	V_{IN} = 0.8V; V_{CC} = 6V to 24V	-	4	50	µA
Turn ON Time	t_{ON}	R_L = 80Ω; (Note 3)	-	5	20	µs
Turn OFF Time	t_{OFF}	R_L = 80Ω; (Note 3)	-	25	65	µs

NOTES:

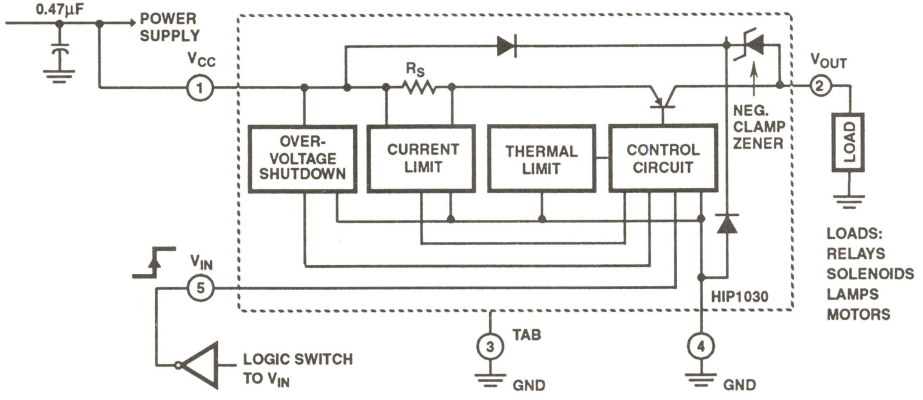
1. The Input Control Voltage, V_{IN} shall not be greater than (V_{CC} - 0.5V) and shall not exceed +7V when V_{CC} is greater than 7.5V.
2. The worst case thermal resistance, θ_{JC} for the SIP TS-001AA 5 lead package is 4°C/W. The calculation for dissipation and junction temperature rise due to dissipation is:

   $P_D = (V_{CC}\text{-}V_{OUT})(I_{OUT}) + (V_{CC})(I_{CCMAX} - I_{OUT})$ or $(V_{CC})(I_{CCMAX}) - (V_{OUT})(I_{OUT})$

   $T_J = T_{AMBIENT} + (P_D)(\theta_{JC})$ for an infinite Heat Sink.

   Refer to Figure 2 for Derating based on Dissipation and Thermal Resistance. Derating from +150°C is based on the reciprocal of thermal resistance, $\theta_{JC} + \theta_{HS}$. For example: Where θ_{JC} = 4°C/W and given θ_{HS} = 6°C/W as the thermal resistance of an external Heat Sink, the junction-to-air thermal resistance, θ_{JA} = 10°C/W. Therefore, for the maximum allowed dissipation, derate 0.1W/°C for each degree from T_{AMB} to the maximum rated junction temperature of +150°C. If T_{AMB} = +100°C, the maximum P_D is (150 - 100) x 0.1W/°C = 5W.
3. Refer to Figure 3A and 3B for typical switching speeds with a 20Ω Load.
4. Short circuit current will be reduced when thermal shutdown occurs. Testing of short circuit current may require a short duration pulse. See Figure 7.

Typical Application



Typical Performance Curves

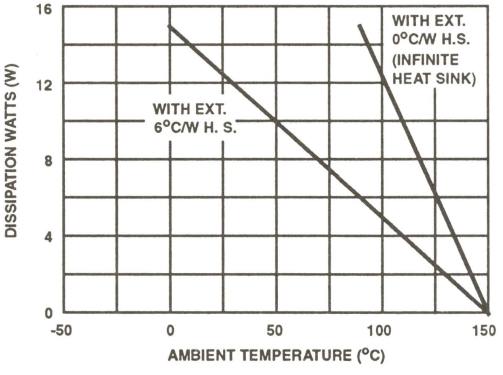


FIGURE 1. DISSIPATION DERATING CURVES

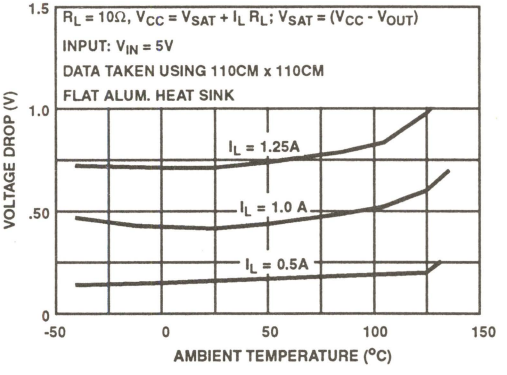


FIGURE 2. TYPICAL FORWARD VOLTAGE DROP, V_{SAT} CHARACTERISTICS vs AMBIENT OPERATING TEMPERATURE

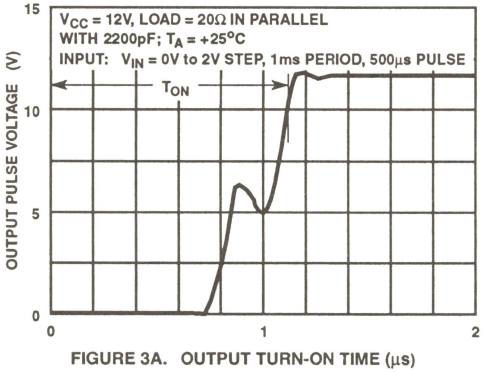


FIGURE 3A. OUTPUT TURN-ON TIME (µs)

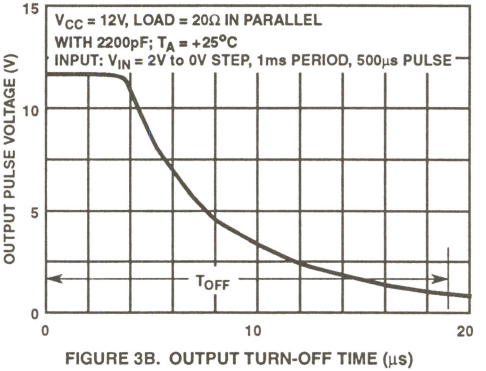


FIGURE 3B. OUTPUT TURN-OFF TIME (µs)

FIGURE 3. TYPICAL RISE TIME AND FALL TIME CHARACTERISTICS OF THE HIP1030 WITH A RESISTIVE AND CAPACITIVE LOAD. THE TURN-ON TIME OF APPROXIMATELY 1.1µs IS PRIMARILY DETERMINED BY THE V_{CC} SUPPLY. THE OUTPUT FALL TIME IS LIMITED BY RC TIME CONSTANT OF THE LOAD.

Typical Performance Curves (Continued)

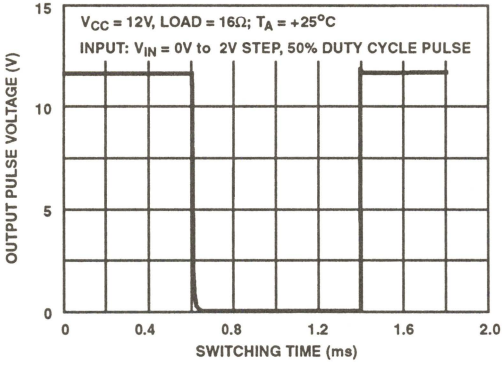


FIGURE 4. TYPICAL SWITCHING CHARACTERISTIC OF THE HIP1030 WITH AN OUTPUT RESISTIVE LOAD

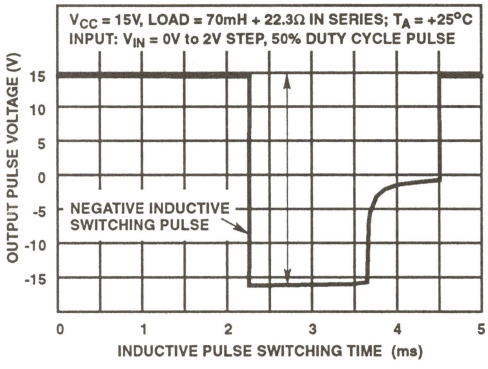


FIGURE 5. TYPICAL OUTPUT INDUCTIVE LOAD SWITCHING PULSE. THE NEGATIVE CLAMP VOLTAGE (V_{CC} -31V) FOR THE INDUCTIVE KICK PULSE IS REFERENCED TO THE V_{CC} SUPPLY INPUT

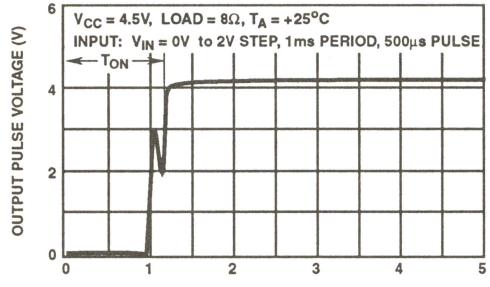


FIGURE 6A. TURN-ON TIME (µs)

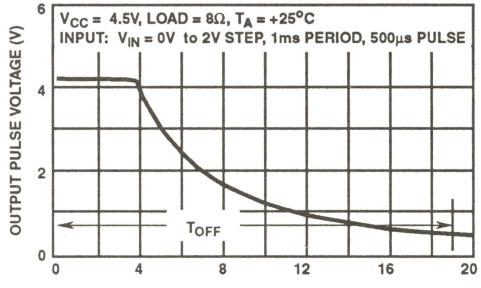


FIGURE 6B. TURN-OFF TIME (µs)

FIGURE 6. TYPICAL LOW SUPPLY VOLTAGE SWITCHING CHARACTERISTICS OF THE HIP1030. THE TURN-ON AND TURN-OFF CHARACTERISTICS ARE SHOWN FOR V_{CC} = 4.5V.

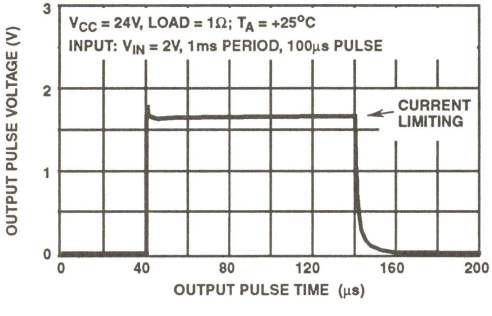


FIGURE 7. TYPICAL OUTPUT CURRENT PULSE WHEN SWITCHING INTO A LOW IMPEDANCE (1Ω), OR SHORTED LOAD. FOR THE CONDITIONS SHOWN, OUTPUT CURRENT LIMITING IS ~1.7A

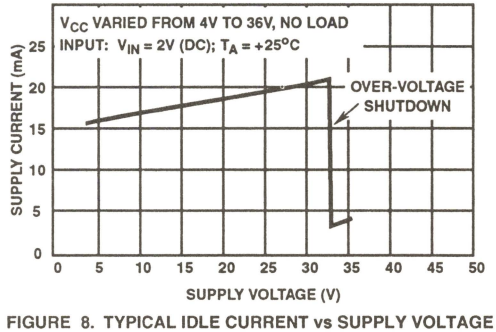


FIGURE 8. TYPICAL IDLE CURRENT vs SUPPLY VOLTAGE WITH NO LOAD

HARRIS SEMICONDUCTOR

HIP1031

PRELIMINARY

March 1994

Half Amp High Side Driver with Overload Protection

Features

- Over Operating Range: -40°C to +125°C
  - 1.0V Max V_{SAT} at 0.6A
  - 4.5V to 25V Power Supply Range
- Over-Voltage Shutdown Protected
- Over-Current Limiting
- Thermal Limiting Protection
- 60V_{PK} Load Dump
- Reverse Battery Protection to -16V

Applications

- Motor Driver/Controller
- Driver for Solenoids, Relays & Lamps
- MOSFET and IGBT Driver
- Driver for Temperature Controller

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP1031AS	-40°C to +125°C	5 Lead TS-001AA SIP

Description

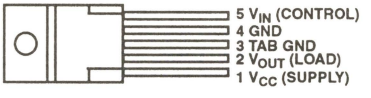
The HIP1031 is a High Side Driver Power Integrated Circuit designed to switch power supply voltage to an output load. It is the equivalent of a PNP pass transistor operated as a protected high side current switch in the saturated ON state with low forward voltage drop at the maximum rated current. It has low output leakage and low idle current in the OFF state.

The Functional Block Diagram for the HIP1031 shows the protection control circuit functions of over-current, overvoltage and over-temperature. A small metal resistor senses overcurrent in the power supply path of the pass transistor and load. Overvoltage detection and shutdown of the output driver occurs when a comparator determines that the supply voltage has exceeded a comparator reference level. Over-temperature is sensed from a V_{BE} differential sense element that is thermally close to the output drive transistor. In addition to the input detected overvoltage protection, negative peak voltage of an inductive load is clamped with an internal zener diode. An internal bandgap supply voltage source provides a stable voltage reference over the chip operating temperature range, providing bias and reference control for the protection circuits.

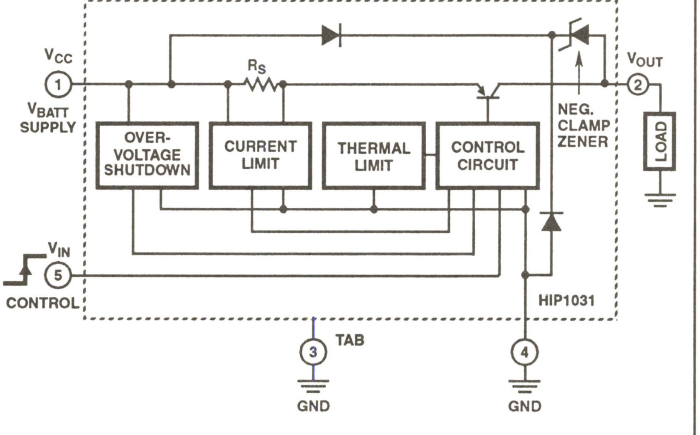
The HIP1031 is particularly well suited for driving lamps, relays, and solenoids in automotive and industrial control applications where voltage and current overload protection at high temperatures is required. The HIP1031 is supplied in a 5 lead TS-001AA Power SIP package.

Pinout

HIP1031 (SIP)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3596.2

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . See O.V. Shutdown Limit, V_{OVSD}
Input Voltage, V_{IN} (Note 1) . . . . . -0.8V to +7V
Load Current, I_{OUT} . . . . . Internally Limiting
Load Dump (Survival) . . . . . $\pm 60V_{PK}$
Reverse Battery . . . . . -16V

Thermal Information

Maximum Thermal Resistance	θ_{JA}	θ_{JC}
Plastic SIP Package	50°C/W	4°C/W

Maximum Power Dissipation, (Note 2)
At T_A = +125°C, Infinite Heat Sink 6.25W
Maximum Junction Temperature, T_J . . . . . 150°C
Ambient Operating Temperature . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -40°C to +150°C
Lead Temperature (Soldering 10s max) . . . . . 265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +125°C, V_{IN} = 2V, V_{CC} = +12V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		4.5	-	25	V
Over-Voltage Shutdown	V_{OVSD}	R_L = 1KΩ, V_{IN} = 2V	26	33	38	V
Over-Temperature Limiting	T_{SD}		-	150	-	°C
Negative Pulse Output Clamp Voltage	V_{CL}	I_{CL} = -100mA, V_{CC} = 4.5V to 25V, V_{IN} = 0.8V	(V_{CC} - 62)	(V_{CC} - 37)	(V_{CC} - 28)	V
Short Circuit Current Limiting	I_{SC}	Note 3	0.7	1.1	1.7	A
Input Control ON	V_{IH}		2.0	-	-	V
Input Control OFF	V_{IL}		-	-	0.8	V
Input Current High	I_{IH}	V_{IN} = 5.5V, V_{CC} = 6V to 24	10	-	40	µA
Input Current Low	I_{IL}	V_{IN} = 0.8V, V_{CC} = 6V to 24V	10	-	30	µA
Supply Current, Full Load, Input Control ON	I_{CCMAX}	V_{IN} = 2V; I_{OUT} = 0.55A	-	-	0.6	A
Supply Current, No Load, Input Control OFF	I_{CCMIN}	V_{IN} = 0V; I_{OUT} = 0A	-	55	100	µA
Input-Output Forward Voltage Drop (V_{CC} - V_{OUT})	V_{SAT}	I_{OUT} = 0.6A, V_{CC} = 4.5V to 25V	-	-	1.0	V
Output Leakage	I_{OUT_LK}	V_{IN} = 0.8V, V_{CC} = 6V to 24V	-	-	50	µA
Turn-On Time	t_{ON}	R_L = 80Ω, T_A = +125°C	-	6	20	µs
Turn-OFF Time	t_{OFF}	R_L = 80Ω, T_A = +125°C	-	17	65	µs

NOTES:

1. The Input Control Voltage, V_{IN} may range from -0.85V to +7V for a V_{CC} supply voltage of 0V to +25V.
2. The worst case thermal resistance, θ_{JC} for the SIP TO-220 5 pin package is 4°C/W. The calculation for dissipation and junction temperature rise due to dissipation is:

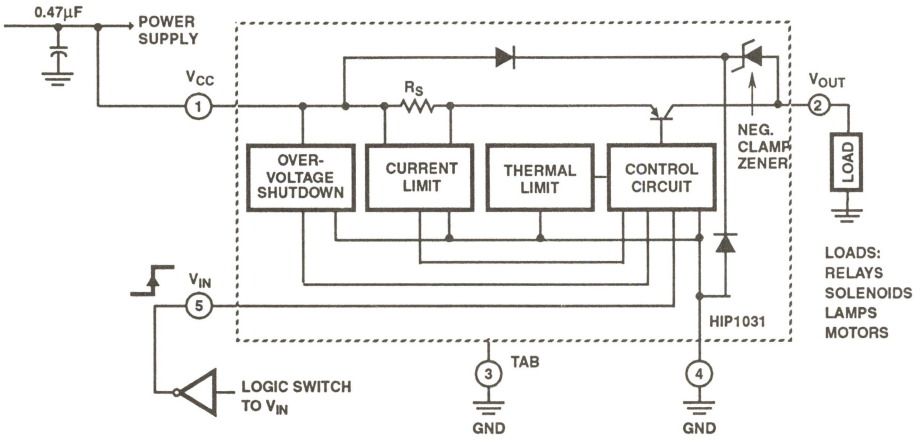
   $P_D = (V_{CC}\text{-}V_{OUT})(I_{OUT}) + (V_{CC})(I_{CCMAX} - I_{OUT})$ or $(V_{CC})(I_{CCMAX}) - (V_{OUT})(I_{OUT})$

   $T_J = T_{AMBIENT} + (P_D)(\theta_{JC})$ for an infinite Heat Sink.

   Refer to Figure 1 for Derating based on Dissipation and Thermal Resistance. Derating from 150°C is based on the reciprocal of thermal resistance, $\theta_{JC}+\theta_{HS}$. For example: Where θ_{JC} = 4°C/W and given θ_{HS} = 6°/W as the thermal resistance of an external Heat Sink, the junction-to-air thermal resistance, θ_{JA} = 10°C/W. Therefore, for the maximum allowed dissipation, derate 0.1W/°C for each degree from T_{AMB} to the maximum rated junction temperature of 150°C. If T_{AMB} = 100°C, the maximum P_D is (150 - 100) x 0.1W/°C = 5W.
3. Short Circuit current will be reduced when Thermal Shutdown occurs. Testing of a short circuit current may require a short duration pulse.

Typical Application

HIP1031 HIGH SIDE DRIVER



Typical Performance Curves

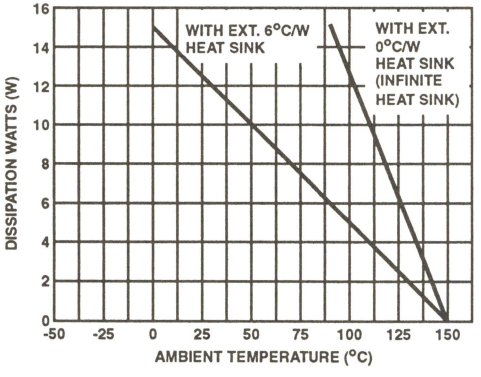


FIGURE 1. DISSIPATION DERATING CURVES

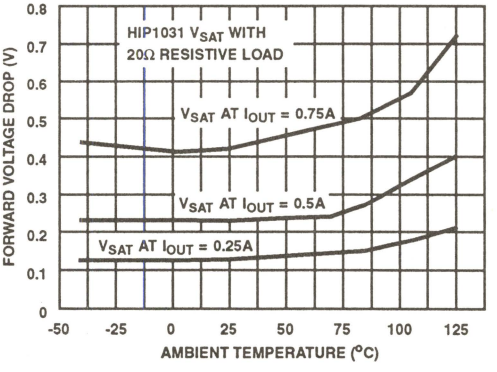


FIGURE 2. TYPICAL V_{SAT} CHARACTERISTIC vs TEMPERATURE

HARRIS SEMICONDUCTOR

HIP1090

Protected High Side Power Switch with Transient Suppression

April 1994

Features

- ±90V Transient Suppression
- 4V to 16V Operating Voltage
- 1A Current Load Capability
- Low Input-Output Voltage Drop With Controlled Saturation Detector for
  - Fast Low Current Turn-OFF
  - Reduced No-Load Idle Current
- Over-Voltage Shutdown Protection
- Short Circuit Current Limiting
- Over-Temperature Limiting Protected
- Thermal Limiting at T_J = +150°C
- -40°C to +105°C Operating Temperature Range

Applications

- Electronic Circuit Breaker
- Transient Suppressor
- Over-Voltage Monitor
- High Side Driver Switch for
  - Relays
  - Solenoids
  - Heaters
  - Motors
  - Lamps

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP1090AS	-40°C to +105°C	TO-220AB SIP

Description

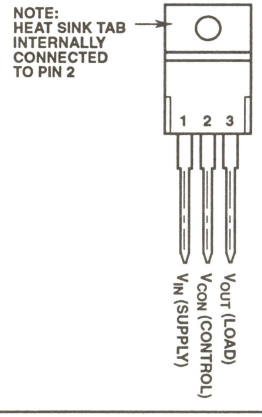
The HIP1090 is a Protected Power Interface Switch designed to suppress potentially damaging overvoltage transients with peak voltage source inputs ranging up to ±90V in amplitude. It is designed to be operated in a 'hard-wired' pass-thru mode or as a high side power switch which controls the current flow through a PNP pass transistor of the IC. In either mode The HIP1090 has a low saturated forward voltage drop. The protected load circuit is connected to the output of the IC. As such, the HIP1090 operates as a transient suppressor where the PNP drive transistor is switched off when V_{IN} is greater than the Overvoltage Shutdown range of 16V to 19V. Shutdown also occurs when V_{IN} is less than the forward turn-on threshold of approximately 2.5V, including the negative voltage range.

The merits of transient suppression depend on the required integrity of the applications load elements. Instrument panel signal warning lights for critical functions such as over temperature or low fluid levels can be protected by the HIP1090 against high level transient voltages and double battery conditions that may potentially cause bulb burnouts. The HIP1090 may be used to protect the power supplies of small signal or logic circuits with voltages ranging from 4V to 16V, effectively blocking higher peak voltages.

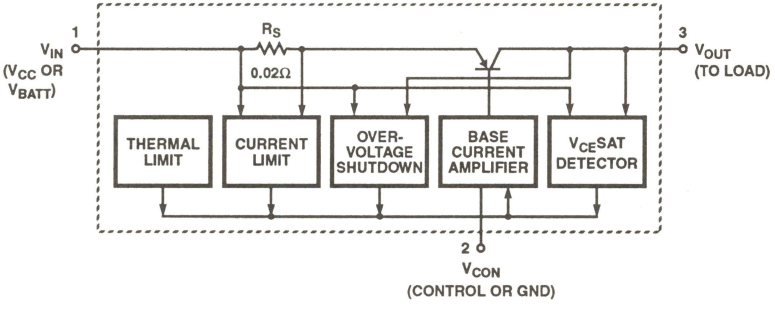
The HIP1090 has internal current limiting protection in the range of 1A to 2A for short circuit to ground conditions and thermal shutdown protection when the junction temperature is greater than 150° C It is capable of driving resistive, inductive or lamp loads (such as lamps No. 168 or 194) with minimum risk of damage under harsh environmental stress conditions. The HIP1090 is supplied in a 3 lead TO-220AB package.

Pinout

HIP1090 (SIP)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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Absolute Maximum Ratings

Input (Supply) Voltage, V_{IN} (Control Pin Reference) . . . . . ±24V
Transient Max Voltage, V_{IN} (15ms) . . . . . ± 90V
Load Current, I_{OUT} . . . . . Short Circuit Protected

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic SIP Package	50°C/W	4°C/W

Maximum Power Dissipation, (Note 4)
At T_A = +105°C, Infinite Heat Sink 11.25W
Junction Temperature . . . . . +150°C
Ambient Temperature Range . . . . . -40°C to +105°C
Storage Temperature Range . . . . . -40°C to +150°C
Lead Temperature (Soldering During) . . . . . +265°C
1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s maximum

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = -40°C to +105°C; V_{IN} = 4V to 16V; V_{CON} = GND or 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input (Supply) Voltage Operating Range	V_{IN}	(Note 1); Also, see Figure 4 for Expanding V_{IN} Range	4	-	16	V
Input Voltage Threshold for Forward Turn-On to Load	V_{THD}	Load = 1kΩ	-	2.5	-	V
Input Voltage for Output Shutdown	V_{SHSD}	(Note 2)	16	-	19	V
Output Shutdown Leakage	I_{LEAK1}	V_{IN} = 19V and 24V; Load = 1kΩ	-	-	100	µA
Output Cutoff Leakage	I_{LEAK2}	V_{IN} = 16V; Control Open; Load = 1kΩ	-	1	-	µA
Thermal Shutdown Temperature	T_{SD}		-	150	-	°C
Maximum Output Transient Pulse Current	I_{OUT}(Tran)	V_{IN} = ±90V for 15ms, V_{OUT} = 14V	-20	-	+20	mA
Maximum Control Transient Pulse Current	I_{CON}(Tran)	V_{IN} = ±90V for 15ms, V_{OUT} = 14V	-50	-	+50	mA
Short Circuit Current	I_{SC}		1	-	2	A
Input-to-Output Voltage Drop		V_{IN} = 4V, I_{OUT} = 175mA	-	-	0.25	V
		V_{IN} = 9V, I_{OUT} = 500mA	-	-	0.65	V
		V_{IN} = 16V, I_{OUT} = 800mA	-	-	1.05	V
		V_{IN} = 16V, I_{OUT} = 1A	-	0.8	-	V
Control Current	I_{CON}	V_{IN} = 16V, I_{OUT} = 100mA	-	-	25	mA
		V_{IN} = 16V, I_{OUT} = 800mA	-	-	50	mA
		V_{IN} = 16V, I_{OUT} = 1A	-	50	-	mA
Turn ON (Rise Time); "Pass-Thru" mode	t_{ON}	Switch V_{IN} 0V(GND) to 5.5V; Measure V_{OUT} (to 90%); Load = 1kΩ (Note 3)	-	-	20	µs
Turn OFF (Fall Time); "Pass-Thru" mode	t_{OFF}	Switch V_{IN} 5.5V to 0V(GND); Measure V_{OUT} (to 90%); Load = 1kΩ (Note 3)	-	-	20	µs
Turn ON (Rise Time); High Pass Switch mode	t_{ON}	See Figure 3 and Figure 4 (Note 3)	-	15	-	µs
Turn OFF (Fall Time); High Pass Switch mode	t_{OFF}	See Figure 3 and Figure 4 (Note 3)	-	15	-	µs

NOTES:

1. The Input Operating Voltage is not limited by the threshold of Shutdown. The V_{IN} voltage may range to ±24V while the normal functional switching range is typically +2.5V to +17.5V (reference to V_{CON}).
2. The Output Drive is switched-off when the Input voltage(Supply pin), referenced to the Control pin exceeds the threshold shutdown VSHSD or the input voltage is less than the forward turn-on threshold (Including negative voltages within the transient peak ratings).
3. T_{ON} and T_{OFF} times include Prop Delay and Rise/Fall time.
4. The worst case thermal resistance,θ_{JC} for the SIP TO-220 is 4°C/W. The calculation for dissipation and junction temperature rise due to dissipation is:

   $P_D = (V_{IN} - V_{OUT}) + (V_{IN})(I_{CON})$

   $T_J = T_{AMBIENT} + (P_D)(\theta_{JC})$ for an infinite Heat Sink.

   Derating from 150°C is based on the reciprocal of thermal resistance, $\theta_{JC}+\theta_{HS}$. For example: Where θ_{JC} = 4°C/W and given θ_{HS} = 6°/W as the thermal resistance of an external Heat Sink, the junction-to-air thermal resistance, θ_{JA} = 10°C/W. Therefore, for the maximum allowed dissipation, derate 0.1W/°C for each degree from T_{AMB} to the maximum rated junction temperature of 150°C. If T_{AMB} = 100°C, the maximum P_D is (150 - 100) x 0.1W/°C = 5W.

Applications

The HIP1090 may be used as a "hard-wired pass-thru" device to protect the load from source voltage transients or may be used as an active high side power interface switch with up to 1A of Load current capability. An ON state condition of (V_{IN} - 4V) ≤ V_{CON} ≤ (V_{IN} - 16V) is the normal range required to activate the high pass switch, allowing the supply source to conduct through the PNP to the load. When the control terminal, V_{CON} is open, the high pass switch is open (no conduction). Figure 2 shows an HIP1090 application example with a switch in the V_{CON} terminal. In comparison to the hard wired circuit of Figure 1 where pin 2 is fixed at ground, pin 2 in the circuit of Figure 2 is switched from open to ground to turn-ON the high pass switch. Used in this mode, the HIP1090 is both an effective transient suppressor and a high pass switch. The switch in the V_{CON} terminal may be active or passive and conducts typically less than 50mA of current. The HIP1090 used in the controlled switching mode retains all of the protected features of the device. In either circuit the output capacitor may be increased in size to hold charge longer during transient interruptions at the input. The charge duration for larger capacitors or for lamp loads is tolerated because of the internal short circuit current limiting protection. Sustained short circuits may cause the junction temperature to reach the thermal shutdown temperature (150° C).

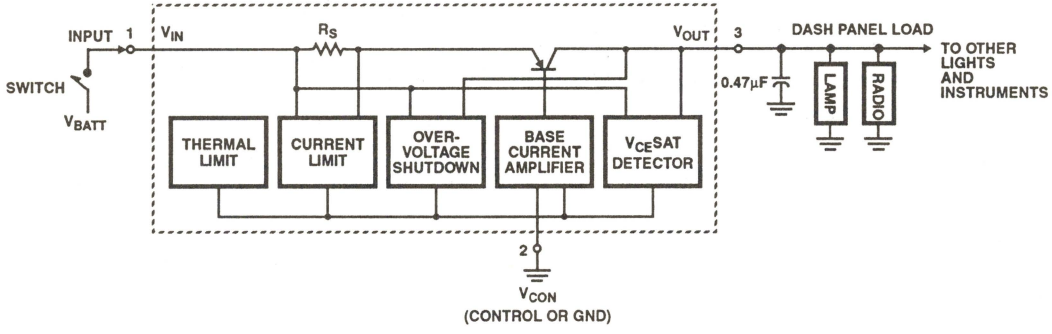


FIGURE 1. TYPICAL APPLICATION OF THE HIP1090 AS A TRANSIENT SUPPRESSOR IN A "PASS-THRU" MODE

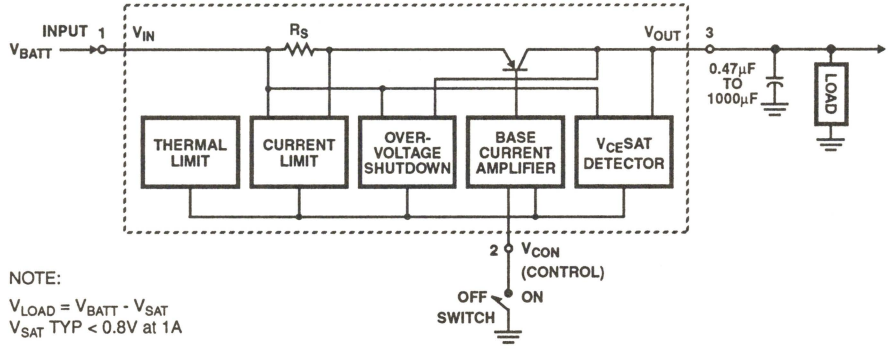
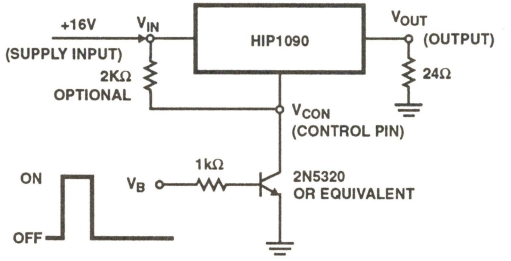


FIGURE 2. TYPICAL APPLICATIONS OF THE HIP1090 AS A TRANSIENT SUPPRESSOR IN A HIGH PASS SWITCH MODE

Figure 3 shows the pulsed output switching characteristics of the HIP1090 as a high side driver. A small delay step is noted on the rising edge due to the hold-off of a $V_{CE}SAT$ detector circuit. The $V_{CE}SAT$ circuit senses the saturation level of the PNP pass transistor and controls the drive as a ratio of load current. As the load current is reduced, the drive current to the output transistor is reduced. Under low current operation, the saturation level is controlled and the turn-OFF switching time is much faster. The control switching element is shown as a 2N5320 NPN transistor but may be any open collector or MOS gate. A pull-up resistor of 2kΩ is used for a slight improvement in the turnoff fall time but is not an essential requirement. The V_{CON} terminal may be controlled with a mechanical switch or may be controlled from any driver output that can sink the worst case condition of pin 2 current, I_{CON} when the output load current is increased to 1A (typically 50mA).



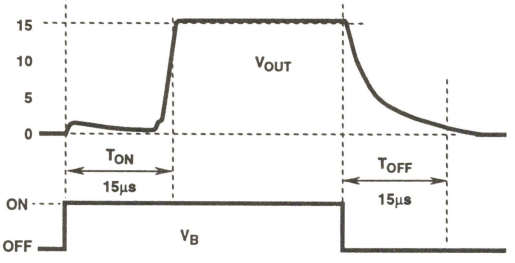


FIGURE 3. TYPICAL ON-OFF SWITCHING CHARACTERISTIC OF THE HIP1090 USING AN NPN TRANSISTOR TO SWITCH THE V_{CON} INPUT TERMINAL

The circuit of Figure 4 shows how the HIP1090 transient suppression voltage shutdown threshold may be increased by using a zener diode from the V_{CON} terminal to the collector terminal of the transistor switch. The preferred method is to use a zener diode for a fixed level shift. While a resistor in place of the zener diode having the same voltage drop will work well, the parametric variation of the I_{CON} current will cause variations of the Over-Voltage Shutdown Threshold. In this circuit, a 10V zener provides a typical overvoltage threshold shift to ~27V. The threshold for overvoltage shutdown is referenced to the (V_{IN} - V_{CON}) voltage difference.

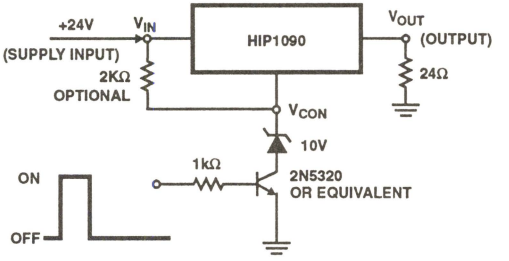


FIGURE 4. A TYPICAL APPLICATION CIRCUIT THAT USES A ZENER TO THE V_{CON} TRANSISTOR SWITCH TO RAISE THE OVERVOLTAGE SHUTDOWN THRESHOLD

Also, it is important to note that high peak current values may be reached when driving nonlinear and inductive loads. The peak output current of the HIP1090 is self limiting in the 1A to 2A range to protect against short circuit conditions. Sustained high peak current may increase the junction temperature to 150°C and cause thermal shutdown. When this happens, the output current will fall off briefly before recovering, unless the over-temperature condition is sustained. Internally, both input and output overvoltage conditions are sensed to protect the circuit, making the high levels of transient voltage ratings possible. Sustained voltage ratings of ±24VDC with transient ratings to ±90V allow a wide variety of applications in high stress environments.

Except for the $V_{CE}SAT$ detector circuit, the HIP1090 is a higher current version of the CA3273 high side driver, which turns-on without the delayed step on the leading edge of the output pulse; switching with a typical T_{ON} time of ~0.5µs. The CA3273 has a higher transient suppression threshold.

Typical Performance Curves

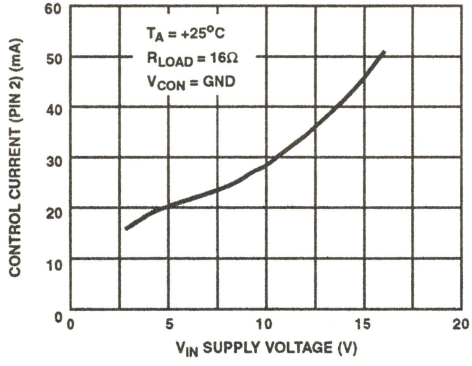


FIGURE 5. CONTROL (QUIESCENT) CURRENT CHARACTERISTIC WITH LOAD

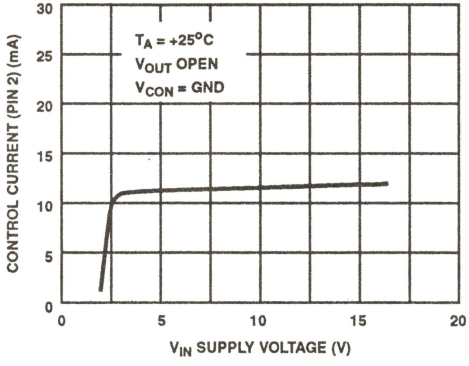


FIGURE 6. CONTROL (QUIESCENT) CURRENT CHARACTERISTIC WITH NO LOAD

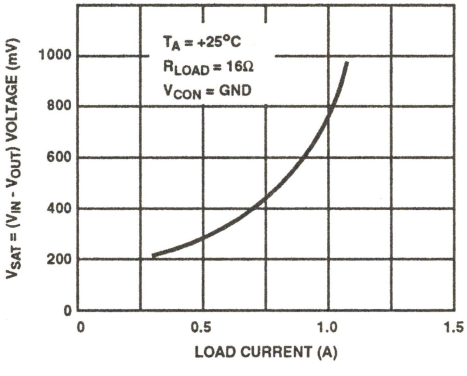


FIGURE 7. SATURATION (V_{IN} - V_{OUT}) CHARACTERISTIC

HARRIS SEMICONDUCTOR

HV400

April 1994

High Current MOSFET Driver

Features

- Fast Fall Times . . . . . .16ns at 10,000pF
- No Supply Current in Quiescent State
- Peak Source Current 6A
- Peak Sink Current 30A
- High Frequency Operation 300kHz

Applications

- Switch Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Uninterruptible Power Supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HV400IP	-40°C to +85°C	8 Lead Plastic DIP
HV400IB	-40°C to +85°C	8 Lead Plastic SOIC (N)
HV400MJ/883	-55°C to +125°C	8 Lead Ceramic SBDIP

Description

The HV400 is a single monolithic, non-inverting high current driver designed to drive large capacitive loads at high slew rates. The device is optimized for driving single or parallel connected N-channel power MOSFETs with total gate charge from 5nC to >1000nC. It features two output stages pinned out separately allowing independent control of the MOSFET gate rise and fall times. The current sourcing output stage is an NPN capable of 6A. An SCR provides over 30A of current sinking. The HV400 achieves rise and fall times of 54ns and 16ns respectively driving a 10,000pF load.

Special features are included in this part to provide a simple, high speed gate drive circuit for power MOSFETs. The HV400 requires no quiescent supply current, however, the input current is approximately 15mA while in the high state. With the internal current steering diodes (pin 7) and an external capacitor, both the timing and MOSFET gate power come from the same pulse transformer; no special external supply is required for high side switches. No high voltage diode is required to charge the bootstrap capacitor.

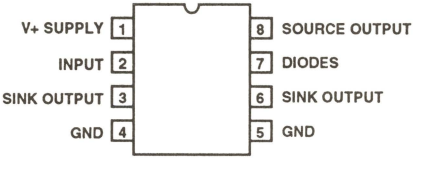
The HV400 in combination with the MOSFET and pulse transformer makes an isolated power switch building block for applications such as high side switches, secondary side regulation and synchronous rectification. The HV400 is also suitable for driving IGBTs, MCTs, BJTs and small GTOs.

The HV400 is a type of buffer; it does not have input logic level switching threshold voltages. This single stage design achieves propagation delays of 20ns. The output NPN begins to source current when the voltage on pin 2 is approximately 2V more positive than the voltage at pin 8.

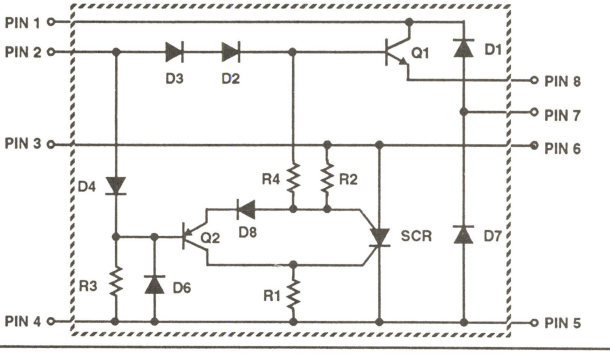
The output SCR switches on when the input pin 2 voltage is 1V more negative than the voltage at pins 3/6. Due to the use of the SCR for current sinking, once the output switches low, the input must not go high again until all the internal SCR charge has dissipated, 0.5µs - 1.5µs later.

Pinout

HV400 (PDIP, SBDIP, SOIC)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2850.1**

Absolute Maximum Ratings

Voltage Between Pin1 and Pin 4/5 ..... 35V
Input Voltage Pin 7 (Max) ..... Pin 1 + 1.5V
Input Voltage Pin 7 (Min) ..... Pin 4/5 -1.5V
Input Voltage Pin 2 to Pin 4/5 ..... +/- 35V
Input Voltage Pin 2 to Pin 6 ..... -35V
Maximum Clamp Current (Pin 7) ..... ±300mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
PDIP	150°C/W	-
SOIC	170°C/W	-
SBDIP	91°C/W	25°C/W

Power Dissipation at T_A = +25°C
PDIP 0.8W
SOIC 0.7W
SBIP 2.33W
Operating Temperature Range
HV400IP/IB ..... -40°C < T_A < +85°C
HV400MJ/883 ..... -55°C < T_A < +125°C
Lead Temperature (Soldering 10s) ..... +265°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C < T_A < +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{SUPPLY} = 15V

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	MIN	TYP	MAX	UNITS
INPUT (PIN 2)							
Input High Differential Voltage (Pin 2 - Pin 8)	V_{IH}	V_{OUT} = 0V, I_{OUT} HI = 10mA	+25°C	0.6	1.7	2.8	V
			Full	0.5	-	3.5	V
Input Low Differential Voltage (Pin 2 - Pin 3/6)	V_{IL}	V_{OUT} = 12V, I_{OUT} LO = -3mA	+25°C	-1.1	-0.9	-0.8	V
			Full	-1.26	-	-0.65	V
Input High Current	I_{IH}	$V_{PIN\ 1,2}$ = 30V, I_{SOURCE} = 0	+25°C	15	18	20	mA
			Full	15		22	mA
Input High Current Peak	I_{IHP}	I_{SOURCE} = 6A, 1µs pulse, V_{IN} = 9V, V_{OUT} = 0V	+25°C		700		mA
Input Low Current	I_{IL}	$V_{PIN\ 2}$ = -30V	+25°C	-80	-50		µA
			Full	-120			µA
SOURCE OUTPUT (PIN 8)							
High Output Voltage	V_{OH}	V_{IN} = +V, I_{OUT} = 150mA	+25°C	12.1	12.8	13.4	V
			Full	12.0		13.5	V
Peak Output Current	I_{OP8}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0V	+25°C		6		A
Output Low Leakage	I_{OL}	V_{OUT} = 0V, V_{IN} = 0V	+25°C	0	10	50	µA
			Full			55	µA
SINK OUTPUT (PIN 3/6)							
Low Output Voltage	V_{OL}	V_{IN} = 0V, I_{OUT} = -150mA	+25°C	0.8	0.89	1.0	V
			Full	0.8		1.05	V
Peak Output Current	I_{OP6}	V_{IN} = 0V, 5µs Pulse, V_{OUT} = 4V	+25°C		30		A
Output High Leakage	I_{OH}	V_{IN} = 15V	+25°C	0	0.3	2	µA
			Full	0		13.5	µA
DIODES D1 AND D7 (PIN 7)							
Forward Voltage	V_F	I_D = 100mA	+25°C	0.8	1.03	1.4	V
			Full	0.8		1.6	V
Reverse Leakage Current	I_R	V_R = 30V	+25°C	0	0.1	1	µA
			Full	0		1	µA
Diode (Pin 7) Stored Charge	Q_{RR}	I_D = 100mA	+25°C		6.5		nC

NOTE: Limits are 100% tested at +25°C; limits over the full temperature range are guaranteed but not tested.

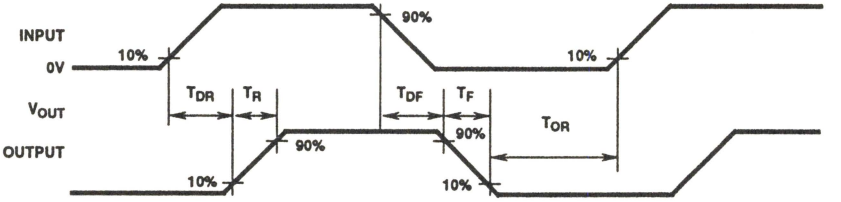
Switching Time Specifications V_{SUPPLY} = 15V

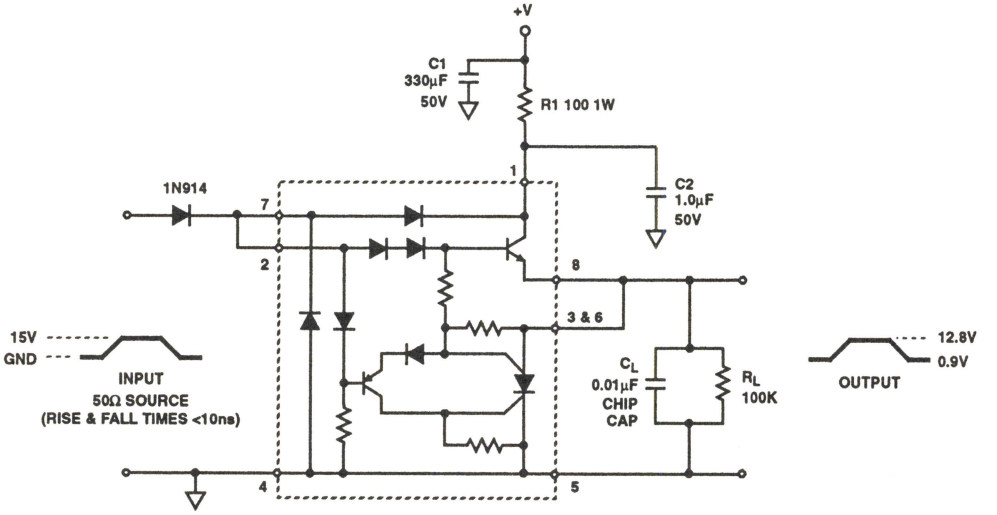
PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	MIN	TYP	MAX	UNITS
Rise Time	T_R	See Switching Test Circuit	Full		50	66	ns
Fall Time	T_F	See Switching Test Circuit	Full		15	24	ns
Delay Time (Lo to Hi)	T_{DR}	See Switching Test Circuit	Full		20	25	ns
Delay Time (Hi to Lo)	T_{DF}	See Switching Test Circuit	Full		17	28	ns
Minimum Off Time	T_{OR}	See Switching Test Circuit	Full		900	1500	ns

NOTES:

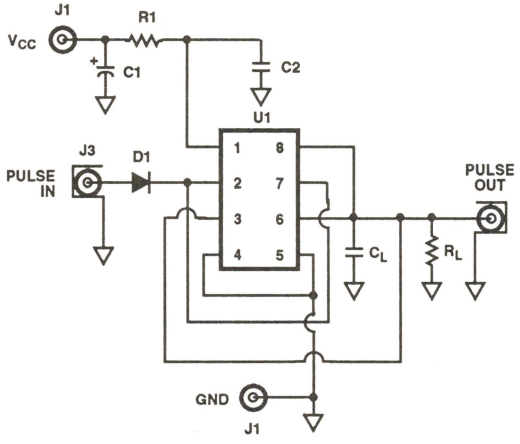
1. Switching times are guaranteed but not tested
2. Typical values are for +25°C

Switching Diagram and Test Circuit



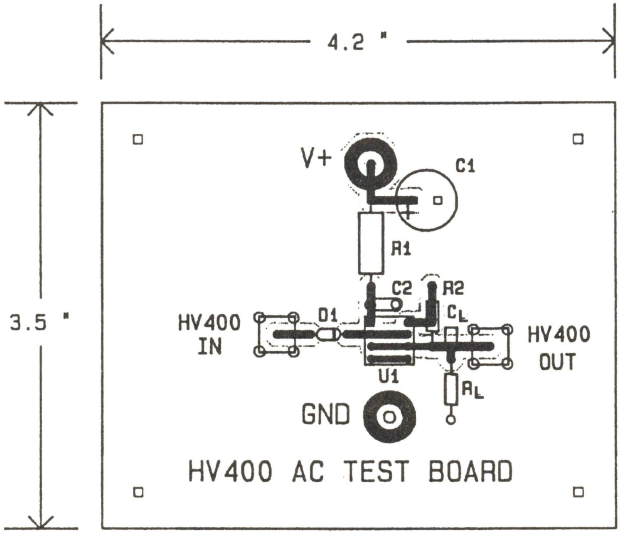


HV400 Switching Test Circuit



Parts List

R1 100Ω, 1W Carbon Resistor
R2 Wire
R_L 100KΩ, 1/8W Carbon Resistor
C1 330µF, 50V Capacitor
C2 1µF, 50V Capacitor
C_L 0.01µF, 50V Chip Capacitor
D1 1N914 Diode
J1, J2 PC Mount Banana Jack Johnson 108-0740-001
J3, J4 PC Mount SMA Connector Johnson EFJ142
U1 Harris HV400 I.C.



Pin Descriptions

SYMBOL	DESCRIPTION
DC INPUT PARAMETERS	
V_{IH}	The differential voltage between the input (Pin 2) to the output (Pin 8) required to source 10mA
V_{IL}	The differential voltage between the input (Pin 2) to the output (Pins 3, 6) required to sink 3mA
I_{IH}	The current required to maintain the input (Pin 2) high with I_{OUT} = 0A
I_{IHP}	The input (Pin 2) current for a given pulsed output current
I_{IL}	The current require to maintain the input (Pin 2) low
DC OUTPUT PARAMETERS	
V_{OH}	The output (Pin 8) voltage with input (Pin 2) = V+
I_{OP8}	The pulsed peak source current form output (Pin 8)
I_{OL}	The output (Pin 8) leakage current with the input (Pin 2) = Ground
V_{OL}	The output (Pins 3, 6) voltage with the input (Pin 2) = Ground
I_{OP6}	The pulsed peak sink current into output (Pins 3, 6)
I_{OH}	The output (Pins 3, 6) leakage current with the input (Pin 2) = V+
V_F	The forward voltage of diode D1 or D7
I_R	The reverse leakage current of diode D1 or D7
Q_{RR}	The time integral of the reverse current at turn off
AC PARAMETERS (See Switching Time Specifications)	
T_R	The low to high transition of the output
T_F	The high to low transition of the output
T_{DR}	The output propagation delay from the input (Pin 2) rising edge
T_{DF}	The output propagation delay from the input (Pin 2) falling edge
T_{OR}	The minimum time required after an output high to low transition before the next input low to high transition

Application Information

Circuit Operation

The HV400's operation is easily explained by referring to the schematic. The control signal is applied to pin 2. If the control signal is about 2V above pin 8, the output NPN Q1 turns on charging the MOSFET gate from a capacitor connected to pin 1. Resistor R4 helps keep the SCR off by applying a reverse bias to the SCR anode gate.

When the control input drops about 1V below pin 3/6, PNP Q2 turns on which triggers the SCR by driving both the anode and cathode gates. The SCR discharges the MOSFET gate and when its current becomes less than 10mA, it turns off. Transistor Q2 conducts any gate leakage currents, through resistors R1 and R2, once the SCR turns off. Figure 7 shows the output characteristics before the SCR turns on and after it turns off. When the SCR turns on, resistor R4 provides a path to remove Q1 base charge. Resistor R3 provides the base current for Q2 to reduce the turn off delay time. Resistors R1 and R2 reduce the SCR recovery time.

The two diodes connected to the diode input pin 7 provide some operation flexibility. With pins 2 and 7 connected together, diode D1 provides a path to recharge the storage capacitor once the MOSFET gate is pulled high and, along with diodes D2 and D3, keeps Q1 from going into hard saturation which would increase delay times. Diode D7 would clamp the input near ground and provide a current path if an input DC blocking capacitor is used.

Alternatively, pin 7 can be connected to pin 6 so that the SCR and NPN Q1 don't have to pass reverse current if the output "rings" above the supply or below ground. When high performance diodes are required, pin 7 can be left disconnected and external diodes substituted.

The diodes in series with pin 2 decouple the input from the output during negative going transitions. The absence of input current turns off Q1 and allows Q2 to trigger the SCR. Diode D8 turns off Q2 once the SCR turns on pulling the output low, otherwise Q2 would saturate and slow down circuit operation. In addition, the diodes D2, D3 and D8 improve noise immunity by adding about 2.5V of input hysteresis.

The HV400 is capable of large output currents but only for brief durations due to power dissipation.

Circuit Board Layout

PC board layout is very important. Pins 3 and 6 should be connected together as should pins 4 and 5. Otherwise the internal interconnect impedance is doubled and only half of the bond wires are used which would degrade the reliability.

The bootstrap capacitor should hold at least 10x the charge of the MOSFET and should be connected between pins 1 and 4/5 with minimum lead lengths and spacings. Likewise, the HV400 should be as close to the MOSFET as possible. Any long PC traces (parasitic inductances) between the MOSFET gate and pins 8 or 3/6 or between the source and pins 4/5 should be avoided. Inductance between the HV400 and the MOSFET limit the MOSFET switching time. If they are too large, the HV400 may operate erratically as discussed below.

Cross Conduction Faults

It is possible to have both Q1 and the SCR on at the same time resulting in very large cross conduction currents. The SCR has larger current capacity so the output goes low and the storage capacitor is discharged. The conditions that cause cross conduction and precautions are discussed below.

Minimum Off Time

The SCR requires a recovery time before voltage can be reapplied without it switching back on. Figure 13 shows how this SCR recovery time, called "minimum off time" (T_{OR}), is a function of the load capacitance. If the input voltage goes high before this recovery time is complete, the SCR will switch back on.

Note that reverse current flowing through the SCR, for example due to load inductance ringing, extends the minimum off time. Since the minimum off time is really dependent upon how much stored charge remains in the SCR when the anode (pin 3/6) is taken positive, it may vary for different applications. Figure 13 indirectly shows that the minimum off time increases with larger currents. It also increases at elevated temperatures as shown in Figure 14. Excessive ringing increases the minimum off time since the stored charge doesn't begin to dissipate until the current drops below 10mA for the last time. Rising anode voltage acts on the internal SCR capacitance to generate its own triggering current. The excess stored charge increases this capacitance. Faster rise times and/or higher voltages also increase the amount of internal trigger current from the internal capacitance so applications with larger dV/dt require longer minimum off times.

The minimum off time must be considered for all occurrences of SCR current. For example, in a half bridge switch mode power supply, there are two MOSFET's connected to the transformer primary. Assume that the high side MOSFET switch is off. When the low side MOSFET switch is turned on, the HV400 driving the high side MOSFET will have to sink gate current from C_{gd} and will have to source gate current when the low side MOSFET switches back off. Both of these current pulses will try to flow through pin 3/6 since the pin 8 output is turned off. Sourcing current from pins 3/6 through the SCR is possible, the pin 3/6 voltage becoming negative with respect to pins 4/5 (See Figure 8). But a better practice would be to connect a Schottky diode between pins 4/5 (anode) and 3/6 (cathode) so reverse current does not flow through the SCR.

False SCR Triggering

The SCR may be triggered inadvertently. The output may overshoot the input due to inductive loading or over driving the output NPN (allowing it to saturate). Whenever pin 6 is more positive than pin 2 by 1V, the SCR is triggered on. Also,

if the output rises too rapidly, greater than 0.5V/nS, the SCR may self trigger. Both issues are resolved by minimizing the load inductance and inserting sufficient resistance, usually 0.1 to 10 ohms, between pin 8 and the load.

A very fast negative going input voltage can result in minimum off times of about 2.5µs. If the output can not keep up with the falling input, the stored charge of diode D4 is transferred into the base of Q2. This excess charge in Q2 must have time to dissipate. Otherwise, when pin 3/6 goes positive, Q2 will turn on and trigger the SCR. An external diode in series with pin 2, as shown in Figure 1, will prevent D4 from discharging into the base of Q2 but that will also reduce the output voltage by the forward voltage of that diode.

Internal Diodes

The internal diodes connected to pin 7 are provided for convenience but may not be suitable for large currents. Since they are part of the integrated circuit, they are physically small, operate at high current densities, and have long recovery times. Figure 15 shows that their forward characteristics degrade above 100mA. In addition, Figure 16 shows their reverse recovery charge as a function of forward current. The product of this charge, the applied reverse voltage and the frequency is the additional power dissipation due to the diodes. For stored charge calculations, use the peak forward current within 100ns of the application of reverse bias. In addition to the extra power dissipation, the capacitance of these diodes may extend the switching delay times.

Power Dissipation Calculations

The power required to drive the MOSFET is the product of its total gate charge times the gate supply voltage (maximum voltage on HV400 pin 1, 2 or 7) times the frequency. Assuming that the MOSFET gate resistance is negligible, this power is dissipated within the HV400. If resistors are placed between the HV400 and the MOSFET, then some of the power is dissipated in the resistors, the percentage depending upon the ratio of resistors to HV400 output impedance.

There are two other sources of power dissipation to consider. First there is the power in R3 which is the product of the input pin 2 current and voltage (with no output current) times the duty cycle. Second is the product of the pin 7 diode stored charge, which is dependent upon the forward current, times the applied diode reverse voltage times the frequency. This information is available from figures 3 and 16 in this data sheet.

Applications Circuits

The HV400 was designed to interface a pulse transformer to a power MOSFET. There must be some means to balance the transformer volt-second product over a cycle. The unipolar drive shown in Figure 1 lets the core magnetization inductance reverse the primary and secondary voltages. The zener diode on the primary side limits this voltage and must be capable of dissipating the energy stored in the transformer. The load may be connected to either the power MOSFET drain or source.

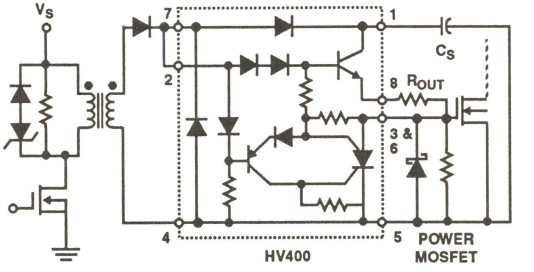


FIGURE 1. UNIPOLAR DRIVE

A diode is added in series with pins 2 and 7 to allow the transformer secondary to go negative. The charge storage of the pin 7 diode may cause the turn off delay time to be too long. Alternatively, pin 7 could be left disconnected and a second external diode connected between the transformer (anode) and pin 1 (cathode). In some applications the diode in series with pin 2 may be unnecessary but the -35V input to output or ground maximum rating should be observed.

Sometimes the volt-second balance is achieved by a push-pull drive on the pulse transformer primary. This is especially useful if there are two secondary windings driving two HV400's out of phase such as in a half-bridge configuration

Other times it is more convenient to achieve volt-second balance by using capacitors to block DC in the primary and secondary windings as shown in Figure 2. The pin 7 diodes provide a path for discharging the secondary side DC blocking capacitor. Both capacitors, C_{IN} and C_S, should be at least 10 times the equivalent MOSFET gate capacitance.

The HV400 can be used as a current booster for low side switches by connecting directly to the PWM output. The circuit would be similar to the switching time test circuit.

It is worth restating that some consideration (and experimentation) should be given to the choice of external components, i.e. resistors, capacitors and diodes, to optimize performance in a given application.

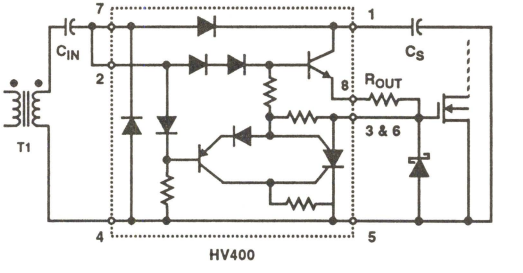


FIGURE 2. BIPOLAR DRIVE WITH DC BLOCKING CAPACITOR

Typical Performance Curves T_A = +25°C Unless Otherwise Specified

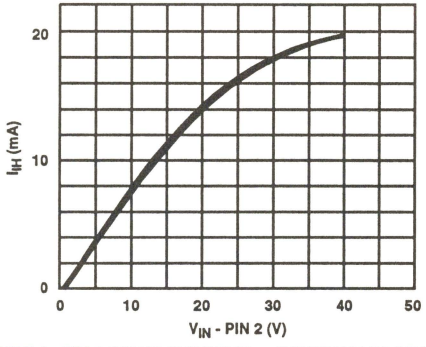


FIGURE 3. PIN 2 INPUT CURRENT vs INPUT VOLTAGE WITH ZERO OUTPUT CURRENT

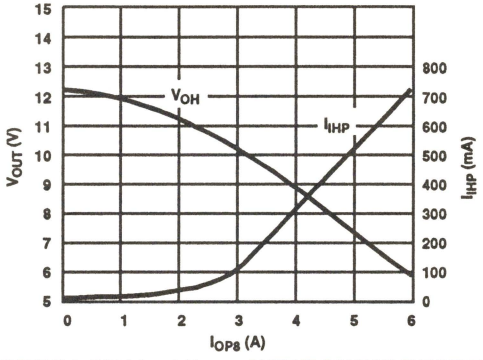


FIGURE 4. PIN 2 I_{IHP} & V_{OH} vs OUTPUT SOURCE CURRENT

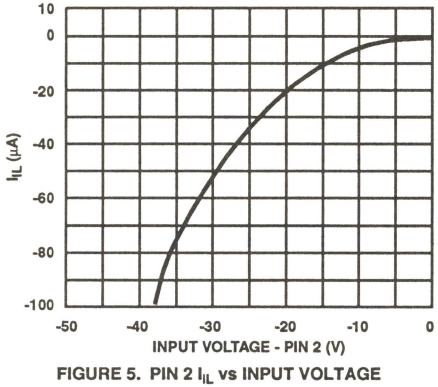


FIGURE 5. PIN 2 I_{IL} vs INPUT VOLTAGE

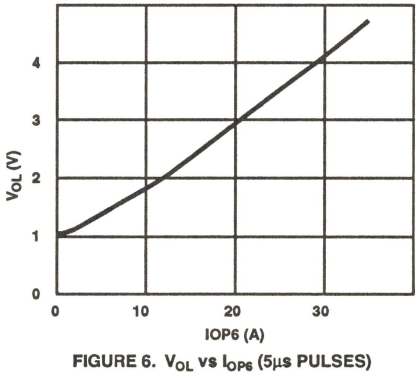


FIGURE 6. V_{OL} vs I_{OP6} (5µs PULSES)

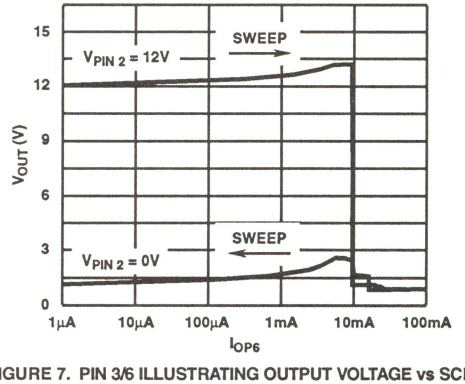


FIGURE 7. PIN 3/6 ILLUSTRATING OUTPUT VOLTAGE vs SCR OUTPUT SINK LATCHING AND HOLDING CURRENT

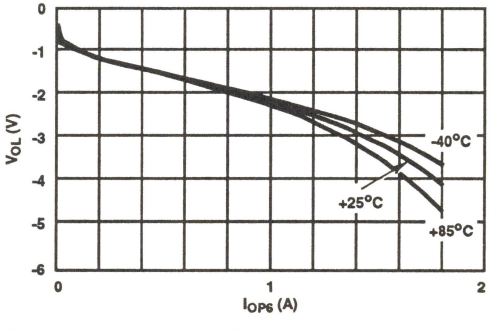


FIGURE 8. PIN 3/6 VOLTAGE vs REVERSE CURRENT 300µs PULSES

Typical Performance Curves T_A = +25°C Unless Otherwise Specified (Continued)

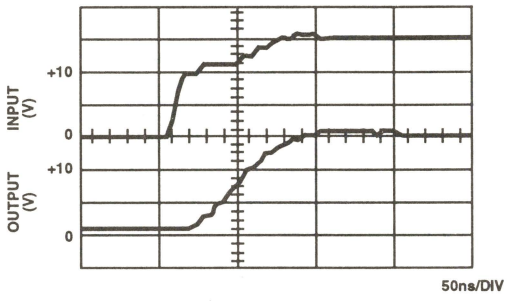


FIGURE 9. LOW TO HIGH TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

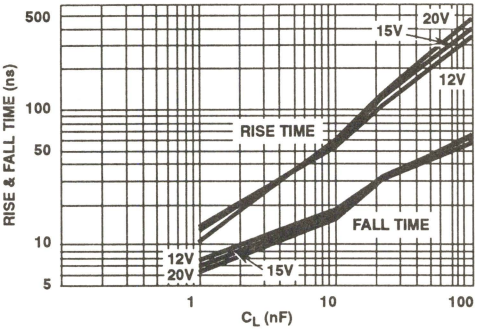


FIGURE 10. RISE AND FALL TIMES vs C_L (V+ = 12V, 15V, 20V)

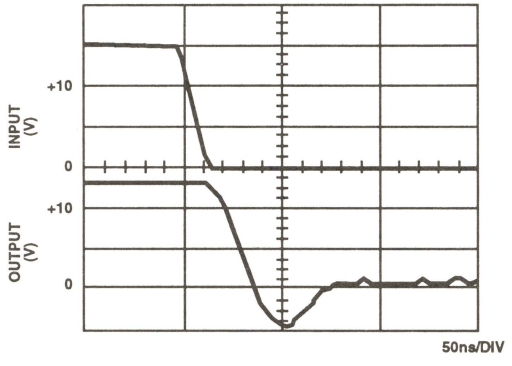


FIGURE 11. HIGH TO LOW TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

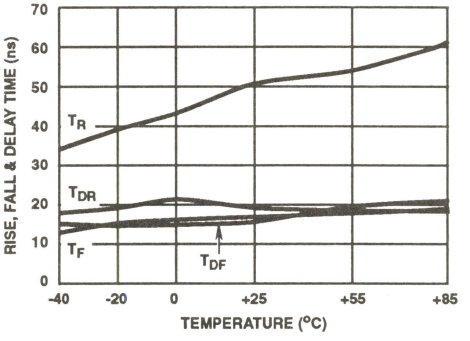


FIGURE 12. RISE, FALL AND DELAY TIMES vs TEMPERATURE

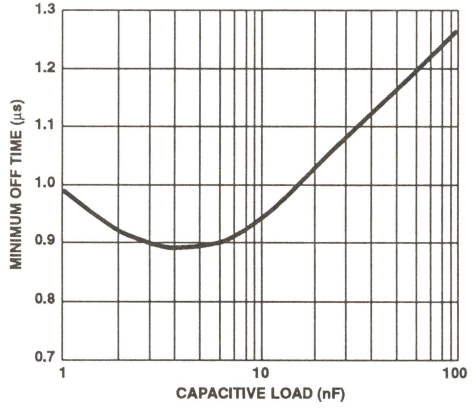


FIGURE 13. MINIMUM OFF TIME (T_{OR}) vs C_L AT +25°C

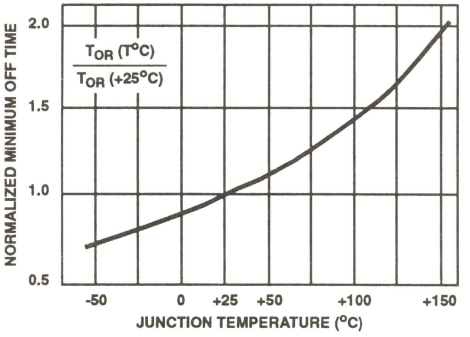


FIGURE 14. NORMALIZED MINIMUM OFF TIME (T_{OR}) vs TEMPERATURE (C_L = 10nF)

Typical Performance Curves T_A = +25°C Unless Otherwise Specified (Continued)

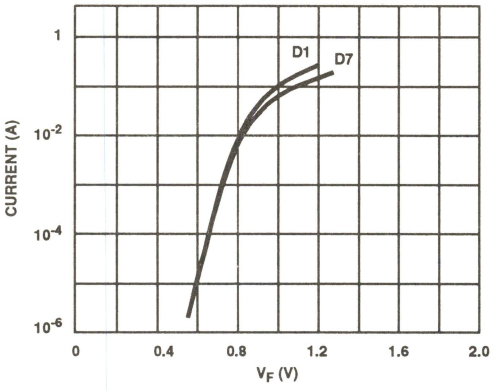


FIGURE 15. DIODE D1 AND D7 CURRENT vs V_F

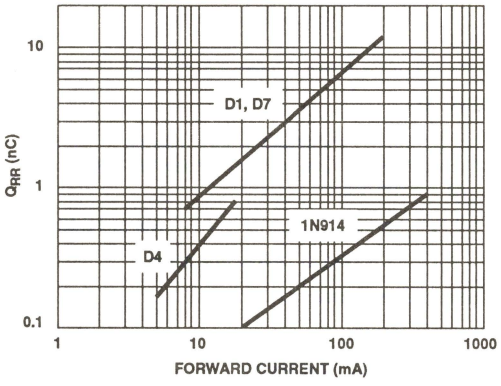
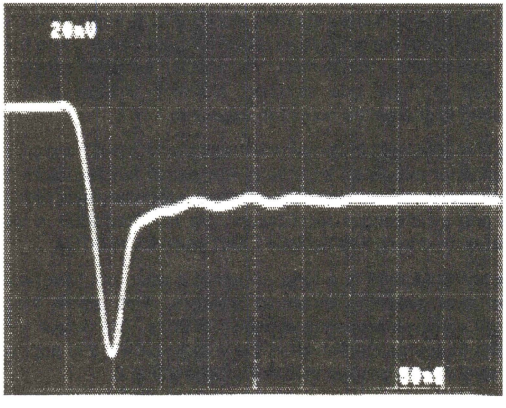


FIGURE 16. DIODE Q_{RR} vs FORWARD CURRENT



Vertical 100mA/div
Horizontal 50ns/div

FIGURE 17. DIODE D1 REVERSE RECOVERY WAVEFORM
I_F = 200mA, 20V REVERSE BIAS

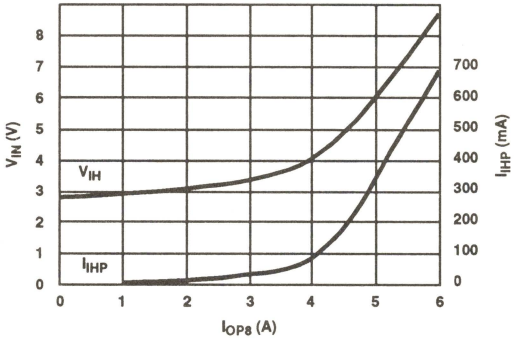


FIGURE 18. V_{IH} AND I_{IHP} vs I_{OP8} [V_{OUT} (PIN 8) = 0, V+ = 15V, 1µs PULSE]

HARRIS SEMICONDUCTOR

HV400MJ/883

April 1994

High Current MOSFET Driver

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Fall Times . . . . . 16ns at 10,000pF**
- **No Supply Current in Quiescent State**
- **Peak Source Current 6A**
- **Peak Sink Current 30A**
- **High Frequency Operation 300kHz**

Applications

- **Switch Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Uninterruptible Power Supplies**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HV400MJ/883	-55°C to +125°C	8 Lead Ceramic SBDIP

Description

The HV400MJ/883 is a single monolithic, non-inverting high current driver designed to drive large capacitive loads at high slew rates. The device is optimized for driving single or parallel connected N-channel power MOSFETs with total gate charge from 5nC to >1000nC. It features two output stages pinned out separately allowing independent control of the MOSFET gate rise and fall times. The current sourcing output stage is an NPN capable of 6A. An SCR provides over 30A of current sinking. The HV400MJ/883 achieves rise and fall times of 54ns and 16ns respectively driving a 10,000pF load.

Special features are included in this part to provide a simple, high speed gate drive circuit for power MOSFETs. The HV400MJ/883 requires no quiescent supply current, however, the input current is approximately 15mA while in the high state. With the internal current steering diodes (Pin 7) and an external capacitor, both the timing and MOSFET gate power come from the same pulse transformer; no special external supply is required for high side switches. No high voltage diode is required to charge the bootstrap capacitor.

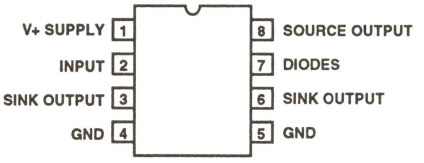
The HV400MJ/883 in combination with the MOSFET and pulse transformer makes an isolated power switch building block for applications such as high side switches, secondary side regulation and synchronous rectification. The HV400MJ/883 is also suitable for driving IGBTs, MCTs, BJTs and small GTOs.

The HV400MJ/883 is a type of buffer; it does not have input logic level switching threshold voltages. This single stage design achieves propagation delays of 20ns. The output NPN begins to source current when the voltage on Pin 2 is approximately 2V more positive than the voltage at Pin 8.

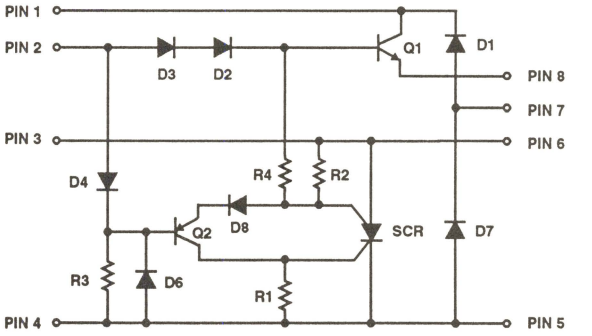
The output SCR switches on when the input Pin 2V is 1V more negative than the voltage at Pins 3/6. Due to the use of the SCR for current sinking, once the output switches low, the input must not go high again until all the internal SCR charge has dissipated, 0.5µs - 1.5µs later.

Pinout

HV400MJ/883 (SBDIP)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3584.1**

Absolute Maximum Ratings

Voltage Between Pin 1 and Pins 4/5 ..... 35V
Input Voltage Pin 7 (Max) ..... Pin 1 + 1.5V
Input Voltage Pin 7 (Min) ..... Pin 4/5 -1.5V
Input Voltage Pin 2 to Pin 4/5 ..... +/- 35V
Input Voltage Pin 2 to Pin 6 ..... -35V
Maximum Clamp Current (Pin 7) ..... ±300mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Sidebrazed DIP	91°C/W	25°C/W

Power Dissipation at T_A = +25°C 2.33W
Operating Temperature Range
HV400MJ/883 ..... -55°C < T_A < +125°C
Maximum Junction Temperature ..... +200°C
Storage Temperature Range ..... -65°C < T_A < +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... +10V to +35V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = +15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	MIN	MAX	UNITS
Input High Differential Voltage (Pin 2 - Pin 8)	V_{IH}	V_{OUT} = 0V, I_{OUT} HI = 10mA	1	+25°C	0.6	2.8	V
			2	+125°C	0.1	2.3	V
			3	-55°C	1.0	3.2	V
Input Low Differential Voltage (Pin 2 - Pin 3/6)	V_{IL}	V_{OUT} = 12V, I_{OUT} LO = -3mA	1	+25°C	-1.1	-0.8	V
			2	+125°C	-0.95	-0.6	V
			3	-55°C	-1.2	-0.9	V
Input High Current	I_{IH}	$V_{PIN\ 1,2}$ = 30V, I_{SOURCE} = 0	1	+25°C	15.0	20.0	mA
			2	+125°C	13.0	18.0	mA
			3	-55°C	18.0	25.0	mA
Input Low Current	I_{IL}	$V_{PIN\ 2}$ = -30V	1	+25°C	-80	0	µA
			2, 3	+125°C, -55°C	-80	0	µA
High Output Voltage	V_{OH}	V_{IN} = +V, I_{OUT} = 150mA	1	+25°C	12.1	13.4	V
			2	+125°C	12.2	13.5	V
			3	-55°C	11.0	13.0	V
Output Low Leakage	I_{OL}	V_{OUT} = 0V, V_{IN} = 0V	1	+25°C	0	50	µA
			2, 3	+125°C, -55°C	0	60	µA
Low Output Voltage	V_{OL}	V_{IN} = 0V, I_{OUT} = -150mA	1	+25°C	0.8	1.0	V
			2	+125°C	0.65	0.85	V
			3	-55°C	0.9	1.1	V
Output High Leakage	I_{OH}	V_{IN} = 15V	1	+25°C	0	2.0	µA
			2	+125°C	0	100	µA
			3	-55°C	0	2.0	µA
Forward Voltage	V_F	I_D = 100mA	1	+25°C	0.8	1.4	V
			2	+125°C	0.8	1.25	V
			3	-55°C	0.8	1.6	V
Reverse Leakage Current	I_R	V_R = 30V	1	+25°C	-1.0	1.0	µA
			2, 3	+125°C, -55°C	-1.0	1.0	µA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

This Table Intentionally Left Blank. See AC Parameter on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	MIN	MAX	UNITS
Input High Current fPeak	I_{IHP}	I_{SOURCE} = 6A, 1µs Pulse, V_{IN} = 9V, V_{OUT} = 0V	+25°C	500	900	mA
Peak Output Current	I_{OP8}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0	+25°C	4	8	A
Peak Output Current	I_{OP6}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0	+25°C	25	35	A
Diode (Pin 7) Stored Charge	Q_{RR}	I_D = 100mA	+25°C	6	7	nC
Rise Time	T_R	See Switching Diagram and Test Circuit	+25°C	37	62	ns
Fall Time	T_F	See Switching Diagram and Test Circuit	+25°C	14	21	ns
Delay Time (Lo to Hi)	T_{DR}	See Switching Diagram and Test Circuit	+25°C	6	13	ns
Delay Time (Hi to Lo)	T_{DF}	See Switching Diagram and Test Circuit	+25°C	7	16	ns
Minimum Off Time	T_{OR}	See Switching Diagram and Test Circuit	+25°C	400	1140	ns

NOTE:

1. Switching times are guaranteed but not tested.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-IN)	1,
Final Electrical Test Parameters	1 (Note 1), 2
Group A Test Requirements	1, 2
Groups C and D Endpoints	1,

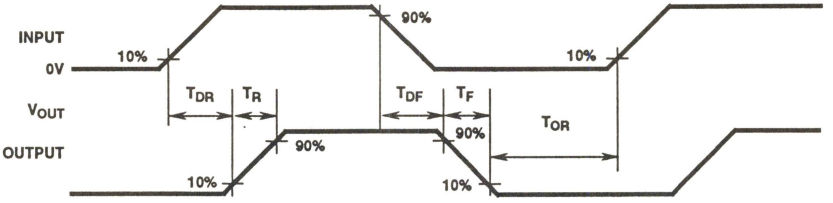
NOTE:

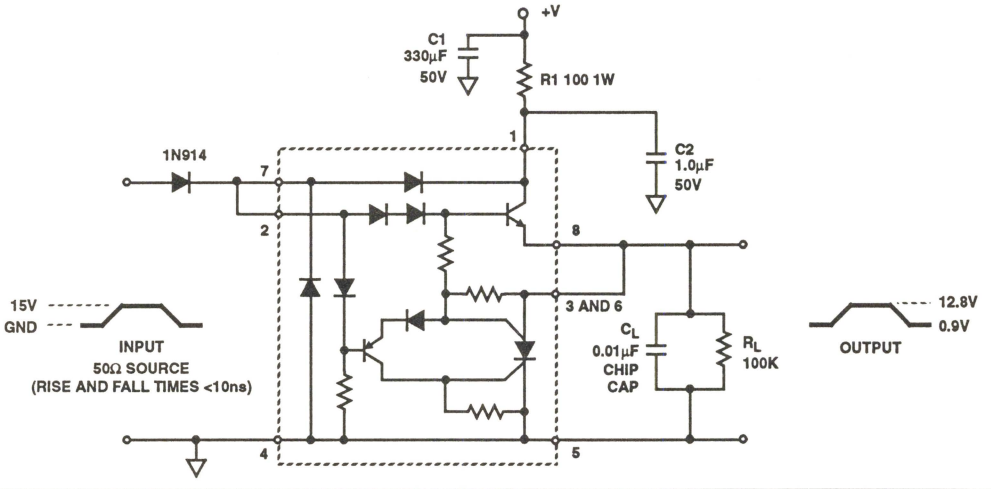
1. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Descriptions

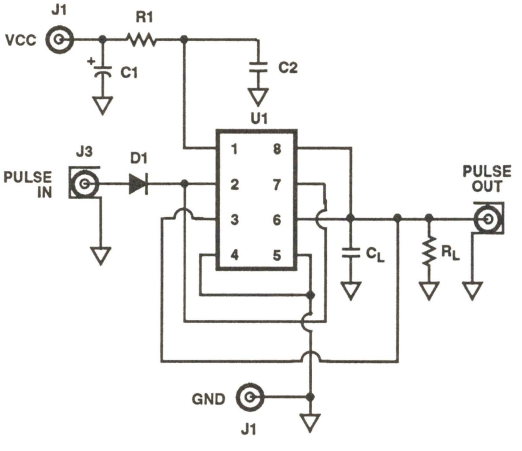
SYMBOL	DESCRIPTION
DC INPUT PARAMETERS	
V_{IH}	The differential voltage between the input (pin 2) to the output (pin 8) required to source 10mA
V_{IL}	The differential voltage between the input (pin 2) to the output (pins 3, 6) required to sink 3mA
I_{IH}	The current required to maintain the input (pin 2) high with I_{OUT} = 0A
I_{IHP}	The input (pin 2) current for a given pulsed output current
I_{IL}	The current require to maintain the input (pin 2) low
DC OUTPUT PARAMETERS	
V_{OH}	The output (pin 8) voltage with input (pin 2) = V+
I_{OP8}	The pulsed peak source current form output (pin 8)
I_{OL}	The output (pin 8) leakage current with the input (pin 2) = Ground
V_{OL}	The output (pins 3, 6) voltage with the input (pin 2) = Ground
I_{OP6}	The pulsed peak sink current into output (pins 3, 6)
I_{OH}	The output (pins 3, 6) leakage current with the input (pin 2) = V+
V_F	The forward voltage of diode D1 or D7
I_R	The reverse leakage current of diode D1 or D7
Q_{RR}	The time integral of the reverse current at turn off
AC PARAMETERS (See Switching Time Specifications)	
T_R	The low to high transition of the output
T_F	The high to low transition of the output
T_{DR}	The output propagation delay from the input (pin 2) rising edge
T_{DF}	The output propagation delay from the input (pin 2) falling edge
T_{OR}	The minimum time required after an output high to low transition before the next input low to high transition

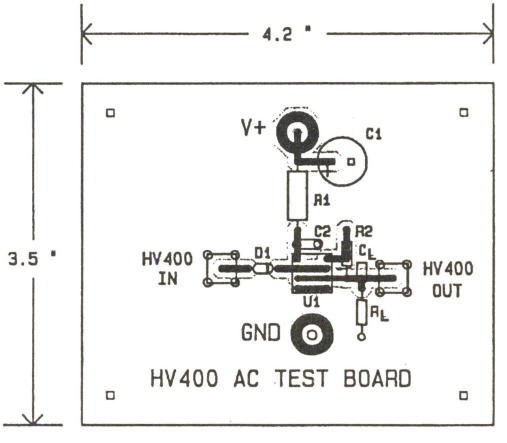
Switching Diagram and Test Circuit





HV400MJ/883 Switching Test Circuit

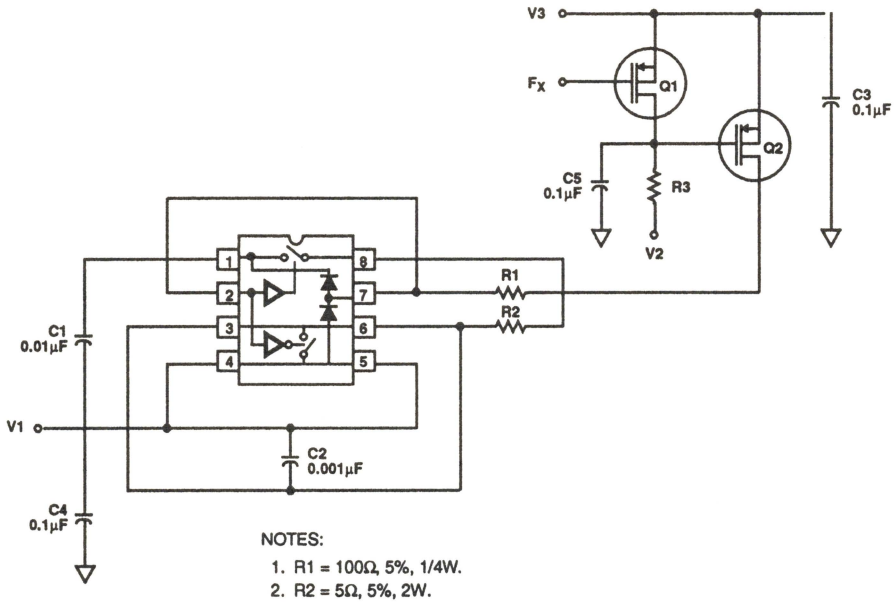




Parts List

R1 100Ω, 1W Carbon Resistor
R2 Wire
R_L 100kΩ, 1/8W Carbon Resistor
C1 330µF, 50V Capacitor
C2 1µF, 50V Capacitor
C_L 0.01µF, 50V Chip Capacitor
D1 1N914 Diode
J1, J2 PC Mount Banana Jack Johnson 108-0740-001
J3, J4 PC Mount SMA Connector Johnson EFJ142
U1 Harris HV400MJ/883 I.C.

Burn-In Circuit (Dynamic)



NOTES:

1. R1 = 100Ω, 5%, 1/4W.
2. R2 = 5Ω, 5%, 2W.
3. R3 = 100Ω, 5%, 2W.
4. C1 = 0.01µF, 10%, 30V.
5. C2 = 0.001µF, 10%, 30V.
6. C3, C4, C5 = 0.1µF, 20%, 50V.
7. V1 = -15.5V, ± 0.5V.
8. V2 = -5.5V, ± 0.5V.
9. V3 = +5.5V, ± 0.5V.
10. Q1, Q2 = SK9505 or Equivalent. (One Pair Per Board Column)
11. F_X = 12.5kHz, 50% Duty Cycle.
    V_{IL} = 0.8V (Max)
    V_{IH} = +4V (Min)

Metallization Topology

DIE DIMENSIONS:
1700 x 1820 x 483µm

METALLIZATION:
Type: 1% Cu, 99% Al
Thickness: 16kÅ ± 2kÅ

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

WORST CASE CURRENT DENSITY:
8.2 x 10^4 A/cm^2 during 1µs pulse with -35A output current, through 8µm wide line 14kA thick.

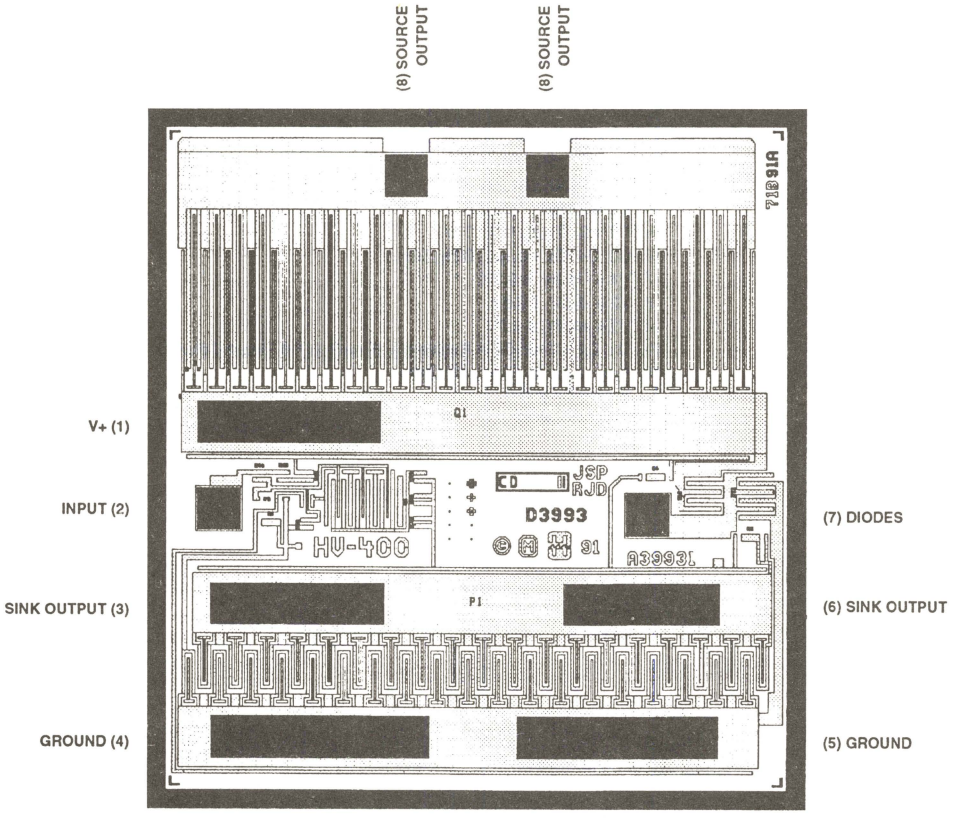
GLASSIVATION:
Type: Silox
Thickness: 12kÅ ± 2kÅ
Type: Nitride
Thickness: 3.5kÅ ± 2.5kÅ

TRANSISTOR COUNT: 3

PROCESS: HFSB Linear Dielectric Isolation

Metallization Mask Layout

HV400MJ/883



HV400MJ

DESIGN INFORMATION

April 1994

High Current MOSFET Driver

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design informiation only. No guarantee is implied.

Circuit Operation

The HV400MJ/883s operation is easily explained by referring to the schematic. The control signal is applied to Pin 2. If the control signal is about 2V above Pin 8, the output NPN Q1 turns on charging the MOSFET gate from a capacitor connected to Pin 1. Resistor R4 helps keep the SCR off by applying a reverse bias to the SCR anode gate.

When the control input drops about 1V below Pin 3/6, PNP Q2 turns on which triggers the SCR by driving both the anode and cathode gates. The SCR discharges the MOSFET gate and when its current becomes less than 10mA, it turns off. Transistor Q2 conducts any gate leakage currents, through resistors R1 and R2, once the SCR turns off. Figure 7 shows the output characteristics before the SCR turns on and after it turns off. When the SCR turns on, resistor R4 provides a path to remove Q1 base charge. Resistor R3 provides the base current for Q2 to reduce the turn off delay time. Resistors R1 and R2 reduce the SCR recovery time.

The two diodes connected to the diode input Pin 7 provide some operation flexibility. With Pins 2 and 7 connected together, diode D1 provides a path to recharge the storage capacitor once the MOSFET gate is pulled high and, along with diodes D2 and D3, keeps Q1 from going into hard saturation which would increase delay times. Diode D7 would clamp the input near ground and provide a current path if an input DC blocking capacitor is used.

Alternatively, Pin 7 can be connected to Pin 6 so that the SCR and NPN Q1 don't have to pass reverse current if the output "rings" above the supply or below ground. When high performance diodes are required, Pin 7 can be left disconnected and external diodes substituted.

The diodes in series with Pin 2 decouple the input from the output during negative going transitions. The absence of input current turns off Q1 and allows Q2 to trigger the SCR. Diode D8 turns off Q2 once the SCR turns on pulling the output low, otherwise Q2 would saturate and slow down circuit operation. In addition, the diodes D2, D3 and D8 improve noise immunity by adding about 2.5V of input hysteresis.

The HV400MJ/883 is capable of large output currents but only for brief durations due to power dissipation.

Circuit Board Layout

PC board layout is very important. Pins 3 and 6 should be connected together as should Pins 4 and 5. Otherwise the internal interconnect impedance is doubled and only half of the bond wires are used which would degrade the reliability.

The bootstrap capacitor should hold at least 10x the charge of the MOSFET and should be connected between Pins 1 and 4/5 with minimum pin lengths and spacings. Likewise, the HV400MJ/883 should be as close to the MOSFET as possible. Any long PC traces (parasitic inductances) between the MOSFET gate and Pins 8 or 3/6 or between the source and Pins 4/5 should be avoided. Inductance between the HV400MJ/883 and the MOSFET limit the MOSFET switching time. If they are too large, the HV400MJ/883 may operate erratically as discussed below.

Cross Conduction Faults

It is possible to have both Q1 and the SCR on at the same time resulting in very large cross conduction currents. The SCR has larger current capacity so the output goes low and the storage capacitor is discharged. The conditions that cause cross conduction and precautions are discussed below.

Minimum Off Time

The SCR requires a recovery time before voltage can be reapplied without it switching back on. Figure 13 shows how this SCR recovery time, called "minimum off time" (T_{OR}), is a function of the load capacitance. If the input voltage goes high before this recovery time is complete, the SCR will switch back on.

Note that reverse current flowing through the SCR, for example due to load inductance ringing, extends the minimum off time. Since the minimum off time is really dependent upon how much stored charge remains in the SCR when the anode (Pin 3/6) is taken positive, it may vary for different applications. Figure 13 indirectly shows that the minimum off time increases with larger currents. It also increases at elevated temperatures as shown in Figure 14. Excessive ringing increases the minimum off time since the stored charge doesn't begin to dissipate until the current drops below 10mA for the last time. Rising anode voltage acts on the internal SCR capacitance to generate its own triggering current. The excess stored charge increases this capacitance. Faster rise times and/or higher voltages also increase the amount of internal trigger current from the internal capacitance so applications with larger dV/dt require longer minimum off times.

The minimum off time must be considered for all occurrences of SCR current. For example, in a half bridge switch mode power supply, there are two MOSFETs connected to the transformer primary. Assume that the high side MOSFET switch is off. When the low side MOSFET switch is turned

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design informiation only. No guarantee is implied.

on, the HV400MJ/883 driving the high side MOSFET will have to sink gate current from C_{GD} and will have to source gate current when the low side MOSFET switches back off. Both of these current pulses will try to flow through Pin 3/6 since the Pin 8 output is turned off. Sourcing current from Pins 3/6 through the SCR is possible, the Pin 3/6 voltage becoming negative with respect to Pins 4/5 (See Figure 8). But a better practice would be to connect a Schottky diode between Pins 4/5 (anode) and 3/6 (cathode) so reverse current does not flow through the SCR.

False SCR Triggering

The SCR may be triggered inadvertently. The output may overshoot the input due to inductive loading or over driving the output NPN (allowing it to saturate). Whenever Pin 6 is more positive than Pin 2 by 1V, the SCR is triggered on.

Also, if the output rises too rapidly, greater than 0.5V/ns, the SCR may self trigger. Both issues are resolved by minimizing the load inductance and inserting sufficient resistance, usually 0.1Ω to 10Ω, between Pin 8 and the load.

A very fast negative going input voltage can result in minimum off times of about 2.5µs. If the output can not keep up with the falling input, the stored charge of diode D4 is transferred into the base of Q2. This excess charge in Q2 must have time to dissipate. Otherwise, when Pin 3/6 goes positive, Q2 will turn on and trigger the SCR. An external diode in series with Pin 2, as shown in Figure 1, will prevent D4 from discharging into the base of Q2 but that will also reduce the output voltage by the forward voltage of that diode.

Internal Diodes

The internal diodes connected to Pin 7 are provided for convenience but may not be suitable for large currents. Since they are part of the integrated circuit, they are physically small, operate at high current densities, and have long recovery times. Figure 15 shows that their forward characteristics degrade above 100mA. In addition, Figure 16 shows their reverse recovery charge as a function of forward current. The product of this charge, the applied reverse voltage and the frequency is the additional power dissipation due to the diodes. For stored charge calculations, use the peak forward current within 100ns of the application of reverse bias. In addition to the extra power dissipation, the capacitance of these diodes may extend the switching delay times.

Power Dissipation Calculations

The power required to drive the MOSFET is the product of its total gate charge times the gate supply voltage (maximum voltage on HV400MJ/883 Pin 1, 2 or 7) times the frequency. Assuming that the MOSFET gate resistance is negligible, this power is dissipated within the HV400MJ/883. If resistors are placed between the HV400MJ/883 and the MOSFET, then some of the power is dissipated in the resistors, the percentage depending upon the ratio of resistors to HV400MJ/883 output impedance.

There are two other sources of power dissipation to consider. First there is the power in R3 which is the product of the input Pin 2 current and voltage (with no output current) times the duty cycle. Second is the product of the Pin 7 diode stored charge, which is dependent upon the forward current, times the applied diode reverse voltage times the frequency. This information is available from Figure 3 and Figure 16 in this data sheet.

Applications Circuits

The HV400MJ/883 was designed to interface a pulse transformer to a power MOSFET. There must be some means to balance the transformer volt-second product over a cycle. The unipolar drive shown in Figure 1 lets the core magnetization inductance reverse the primary and secondary voltages. The zener diode on the primary side limits this voltage and must be capable of dissipating the energy stored in the transformer. The load may be connected to either the power MOSFET drain or source.

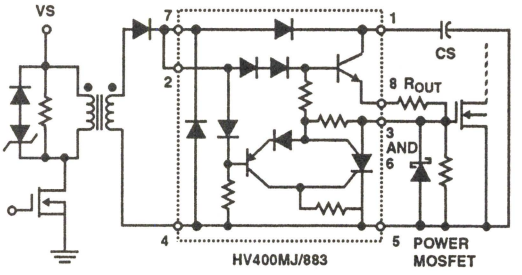


FIGURE 1. UNIPOLAR DRIVE

A diode is added in series with Pins 2 and 7 to allow the transformer secondary to go negative. The charge storage of the Pin 7 diode may cause the turn off delay time to be too long. Alternatively, Pin 7 could be left disconnected and a second external diode connected between the transformer (anode) and Pin 1 (cathode). In some applications the diode in series with Pin 2 may be unnecessary but the -35V input to output or ground maximum rating should be observed.

Sometimes the volt-second balance is achieved by a push-pull drive on the pulse transformer primary. This is especially useful if there are two secondary windings driving two HV400MJ/883s out of phase such as in a half-bridge configuration.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design informiation only. No guarantee is implied.

Other times it is more convenient to achieve volt-second balance by using capacitors to block DC in the primary and secondary windings as shown in Figure 2. The Pin 7 diodes provide a path for discharging the secondary side DC blocking capacitor. Both capacitors, C_{IN} and C_S, should be at least 10 times the equivalent MOSFET gate capacitance.

The HV400MJ/883 can be used as a current booster for low side switches by connecting directly to the PWM output. The circuit would be similar to the switching time test circuit.

It is worth restating that some consideration (and experimentation) should be given to the choice of external components, i.e. resistors, capacitors and diodes, to optimize performance in a given application.

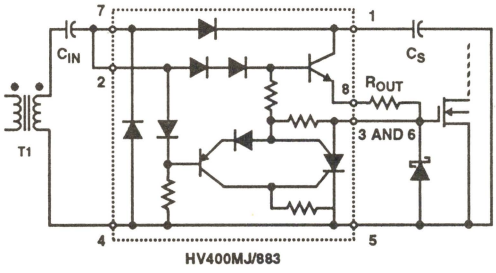


FIGURE 2. BIPOLAR DRIVE WITH DC BLOCKING CAPACITOR

HARRIS SEMICONDUCTOR

ICL7667

April 1994

Dual Power MOSFET Driver

Features

- Fast Rise and Fall Times
  - 30ns with 1000pF Load
- Wide Supply Voltage Range
  - V_{CC} = 4.5V to 15V
- Low Power Consumption
  - 4mW with Inputs Low
  - 20mW with Inputs High
- TTL/CMOS Input Compatible Power Driver
  - R_{OUT} = 7Ω Typ
- Direct Interface with Common PWM Control ICs
- Pin Equivalent to DS0026/DS0056; TSC426

Typical Applications

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Description

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667s high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667s input are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

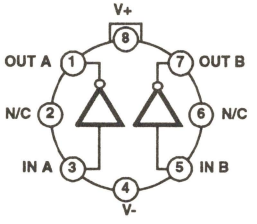
Order Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7667CBA	0°C to +70°C	8 Lead SOIC (N)
ICL7667CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7667CJA	0°C to +70°C	8 Lead Ceramic DIP
ICL7667CTV	0°C to +70°C	8 Pin Metal Can
ICL7667MTV (Note 1)	-55°C to +125°C	8 Pin Metal Can
ICL7667MJA (Note 1)	-55°C to +125°C	8 Lead CerDIP

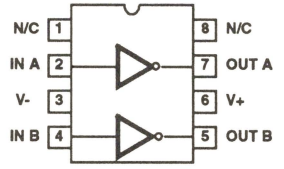
NOTE: 1. Add /883B to Part Number for 883B Processing

Pinouts

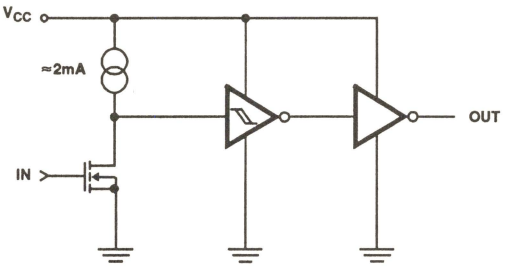
ICL7667 (CAN)
TOP VIEW



ICL7667 (PDIP, SOIC, CERDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2853.2**

Absolute Maximum Ratings

Supply Voltage V+ to V- 15V
Input Voltage ..... V- -0.3V to V+ +0.3V
Package Dissipation, T_A +25°C 500mW

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
PDIP Package	150°C/W	-
SOIC Package	170°C/W	-
Metal Can Package	156°C/W	68°C/W
CerDIP Package	115°C/W	30°C/W

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Temperature Range

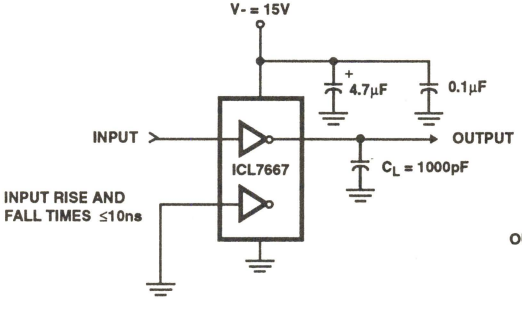
ICL7667C ..... 0°C to +70°C
ICL7667M ..... -55°C to +125°C

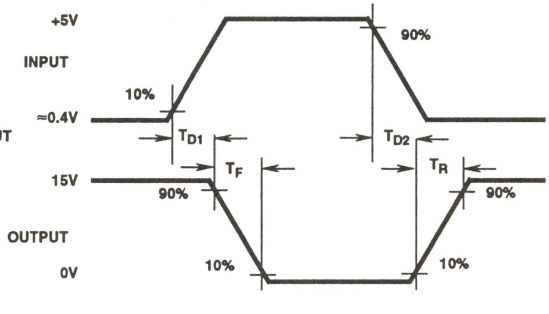
Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	ICL7667C, M T_A = +25°C MIN	TYP	MAX	ICL7667M -55°C ≤ T_A ≤ +125°C MIN	TYP	MAX	UNITS
DC SPECIFICATIONS									
Logic 1 Input Voltage	V_{IH}	V_{CC} = 4.5V	2.0	-	-	2.0	-	-	V
Logic 1 Input Voltage	V_{IH}	V_{CC} = 15V	2.0	-	-	2.0	-	-	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 4.5V	-	-	0.8	-	-	0.5	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 15V	-	-	0.8	-	-	0.5	V
Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V and 15V	-0.1	-	0.1	-0.1	-	0.1	µA
Output Voltage High	V_{OH}	V_{CC} = 4.5V and 15V	V_{CC} -0.05	V_{CC}	-	V_{CC} -0.1	V_{CC}	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V and 15V	-	0	0.05	-	-	0.1	V
Output Resistance	R_{OUT}	V_{IN} = V_{IL}, I_{OUT} = -10mA, V_{CC} = 15V	-	7	10	-	-	12	Ω
Output Resistance	R_{OUT}	V_{IN} = V_{IH}, I_{OUT} = 10mA, V_{CC} = 15V	-	8	12	-	-	13	Ω
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 3V both inputs	-	5	7	-	-	8	mA
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 0V both inputs	-	150	400	-	-	400	µA
SWITCHING SPECIFICATIONS									
Delay Time	T_{D2}	Figure 3	-	35	50	-	-	60	ns
Rise Time	T_R	Figure 3	-	20	30	-	-	40	ns
Fall Time	T_F	Figure 3	-	20	30	-	-	40	ns
Delay Time	T_{D1}	Figure 3	-	20	30	-	-	40	ns

NOTE: All typical values have been characterized but are not tested.

Test Circuits





Typical Performance Curves

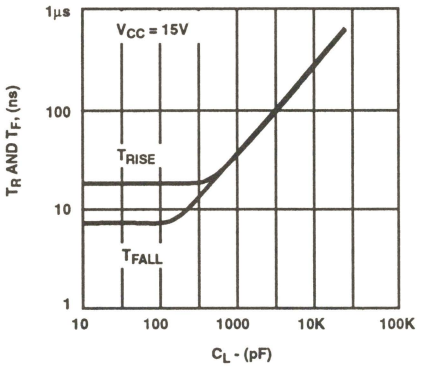


FIGURE 1. RISE AND FALL TIMES vs C_L

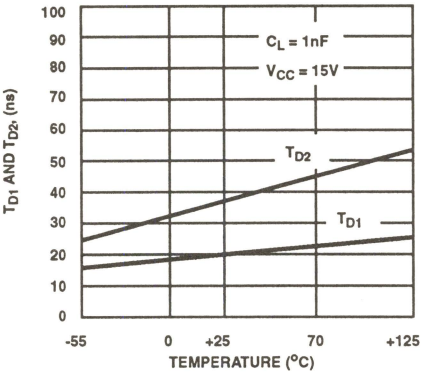


FIGURE 2. T_{D1}, T_{D2} vs TEMPERATURE

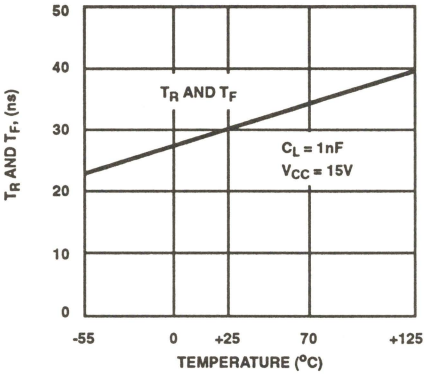


FIGURE 3. T_R, T_F vs TEMPERATURE

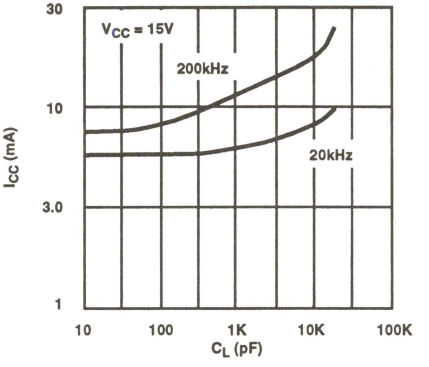


FIGURE 4. I_{CC} vs C_L

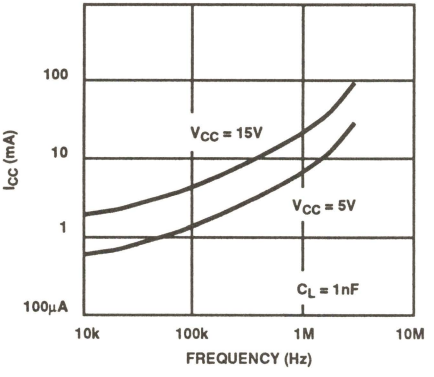


FIGURE 5. I_{CC} vs FREQUENCY

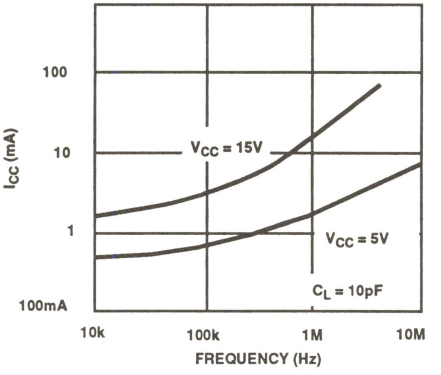


FIGURE 6. NO LOAD I_{CC} vs FREQUENCY

Typical Performance Curves (Continued)

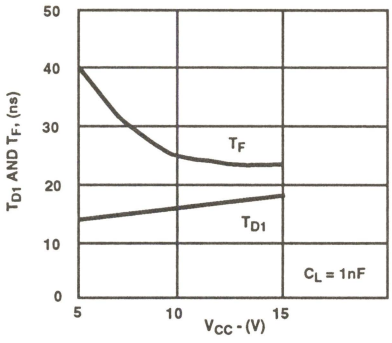


FIGURE 7. DELAY AND FALL TIMES vs V_{CC}

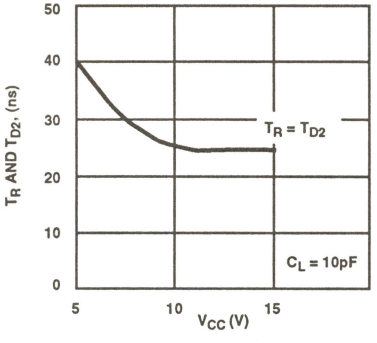


FIGURE 8. RISE TIME vs V_{CC}

Detailed Description

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at V_{CC} = 15V, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

Input Stage

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the VCC voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5V - 15V V_{CC} range. Being CMOS, the inputs draw less than 1µA of current over the entire input voltage range of ground to V_{CC}. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50mV to 100mV at the input, is generated by positive feedback around the second stage.

Output Stage

The ICL7667 output is a high-power CMOS inverter, swinging between ground and VCC. At V_{CC} = 15V, the output impedance of the inverter is typically 7Ω. The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N-channel and P-channel output devices (from V_{CC} to ground) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1µs.

Application Notes

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the ground pin, it is very important to minimize and common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7µF tantalum capacitor in parallel with a low inductance 0.1µF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1. Reduce inductance by making printed circuit board traces as short as possible.
2. Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3. Use a 10Ω to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
4. Use good bypassing techniques to prevent supply voltage ringing.

Power Dissipation

The power dissipation of the ICL7667 has three main components:

1. Input inverter current loss
2. Output stage crossover current loss
3. Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.1mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N-channel and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2f$$

where C = Load Capacitance, f = Frequency

In cases where the load is a power MOSFET and the gate drive requirement are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}f$$

where Q_G = Charge required to switch the gate, in Coulombs,
f = Frequency.

Power MOS Driver Circuits

Power MOS Driver Requirements

Because it has a very high peak current output, the ICL7667 the at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 9 is a typical curve of charge vs gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

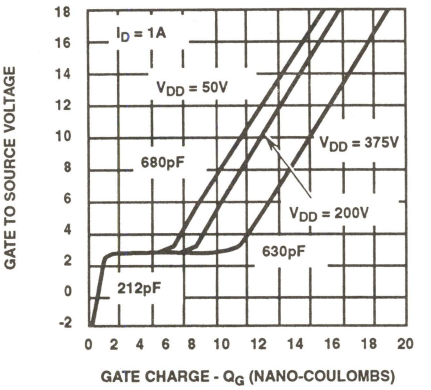


FIGURE 9. MOSFET GATE DYNAMIC CHARACTERISTICS

Direct Drive of MOSFETs

Figure 11 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speedup capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The SG1527 IC is the same as the SG1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

Transformer Coupled Drive of MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 11 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low output can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

Buffered Drivers for Multiple MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 13 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{GS} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

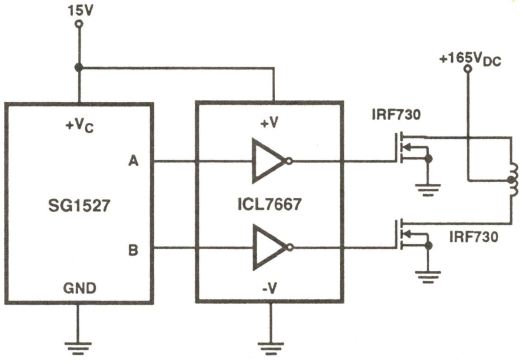


FIGURE 10A.

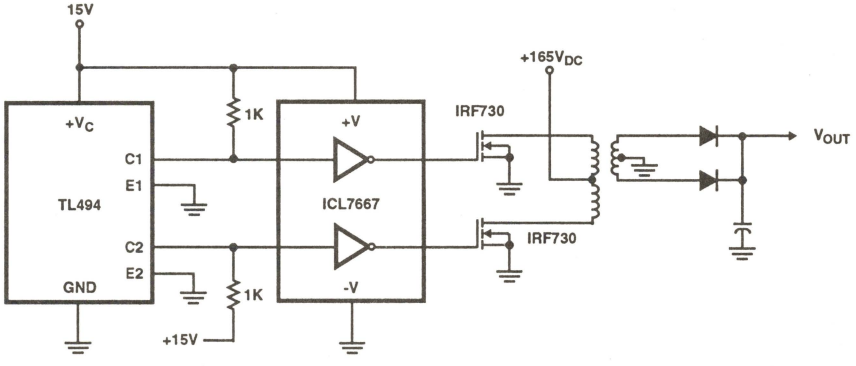


FIGURE 10B.

FIGURE 10. DIRECT DRIVE OF MOSFET GATES

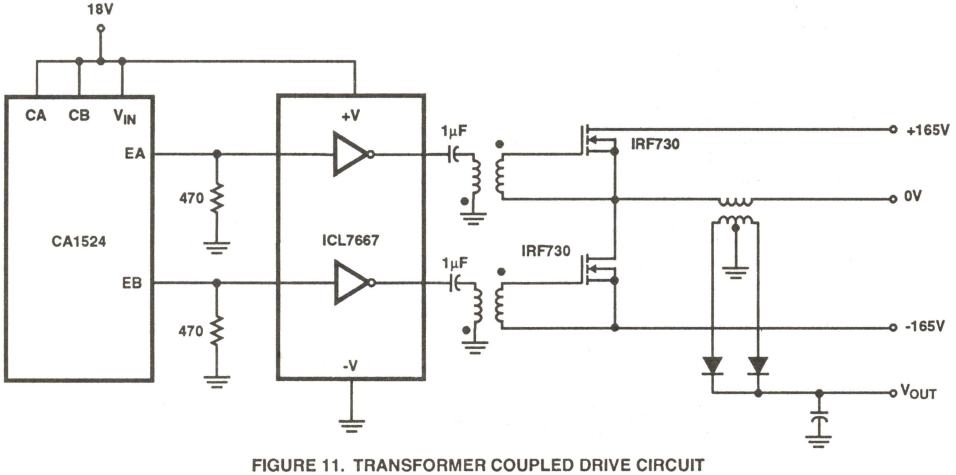


FIGURE 11. TRANSFORMER COUPLED DRIVE CIRCUIT

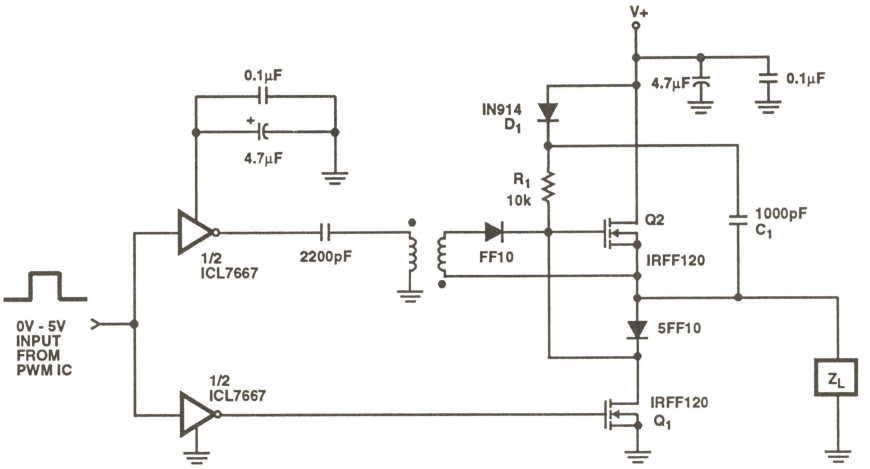


FIGURE 12. VERY HIGH SPEED DRIVER

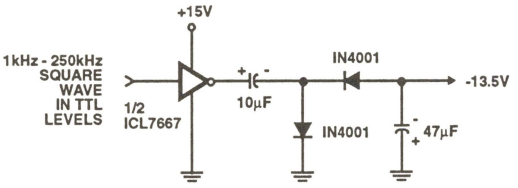


FIGURE 13A.

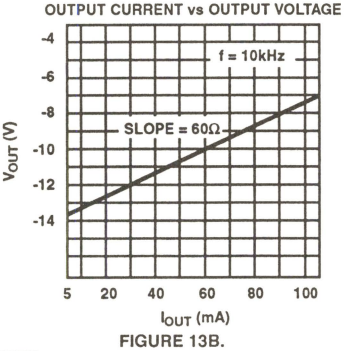


FIGURE 13B.

FIGURE 13. VOLTAGE INVERTER

Other Applications

Relay and Lamp Drivers

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

Charge Pump or Voltage Inverters and Doublers

The low output impedance and wide VCC range of the ICL7667 make it well suited for charge pump circuits. Figure 13A shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 14, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 13 would be to supply the higher voltage needed for EEPROM or EPROM programming.

Clock Driver

Some microprocessors (such as the CDP68HC05 families) use a clock signal to control the various LSI peripherals of the family. The ICL7667s combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

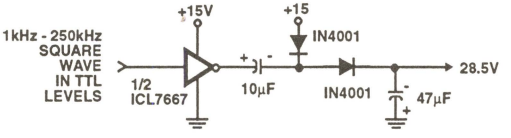


FIGURE 14. VOLTAGE DOUBLER

INTELLIGENT POWER ICs 4

HALF BRIDGES

		PAGE
HALF BRIDGES SELECTION GUIDE		4-2
HALF BRIDGES DATA SHEETS		
HIP2030	30V MCT/IGBT Gate Driver	4-3
HIP2500	Half Bridge 500V_{DC} Driver	4-10
SP600	Half Bridge 500V_{DC} Driver	4-16
SP601	Half Bridge 500V_{DC} Driver	4-23

Half Bridges Selection Guide

MOSFET Driver Circuits

TYPE	FUNCTION	MAX BUS VOLTAGE	RECOMMENDED SUPPLY VOLTAGE	MAX PULSED GATE CURRENT	MAX PWM FREQUENCY	SHOOTTHRU PROTECTION	PACKAGE	RECOMMENDED APPLICATION
HIP2030	P-Channel Power Driver	$30V_{DC}$	$8V_{DC}$ to $15V_{DC}$	6A	180kHz	Yes	28 Lead PLCC	Motor Control
HIP2500	N-Channel Half Bridge	$500V_{DC}$	$10V_{DC}$ to $15V_{DC}$	2A	400kHz	No	14 Lead PDIP 16 Lead PDIP Wafer, Die 16 Lead SOIC	Motor Control SMPS
HIP5500	N-Channel Half Bridge	$500V_{DC}$	$10V_{DC}$ to $15V_{DC}$	2.3A	300kHz	Yes	20 Lead PDIP 20 Lead SOIC	SMPS
SP600	N-Channel Half Bridge	$500V_{DC}$	$14.5V_{DC}$ to $16.5V_{DC}$	0.5A	20kHz	Yes	22 Lead PDIP	Motor Control
SP601	N-Channel Half Bridge	$500V_{DC}$	$14.5V_{DC}$ to $16.5V_{DC}$	0.5A	20kHz	Yes	22 Lead PDIP	Motor Control
HIGH SIDE DRIVERS THAT CAN BE USED IN HALF BRIDGE CONFIGURATION								
HV400	N-Channel Power Driver	$35V_{DC}$	$15V_{DC}$ to $30V_{DC}$	6A (ON) Source 30A(OFF) Sink	20kHz(MC) 200kHz (SMDS)	N/A	8 Lead PDIP 8 Lead SOIC	Motor Control SMPS
ICL7667	N-Channel Dual Driver	$15V_{DC}$	$4.5V_{DC}$ to $15V_{DC}$	1.5A	100kHz	No	TO-99, PDIP, CerDIP and SOIC	Motor Control SMPS, and MOSFET Driver

HARRIS SEMICONDUCTOR

HIP2030

PRELIMINARY

April 1994

30V MCT/IGBT Gate Driver

Features

- +/- Polarity Gate Drive
- High Output Voltage Swing.....30V
- Peak Output Current 6.0A
- Fast Rise Time .....200ns at 60,000pF
- Ability to Interface and Drive P-MCTs
- Programmable Minimum ON/OFF Time
- Gate Output Inhibit Latch
- 5V Reference .....Sinks Up to 30mA
- High Side Charge Pump
- 120kHz Operation.....at 15,000pF

Applications

- Motor Controllers
- Uninterruptible Power Supplies
- Resonant Inverters
- Static Circuit Breakers
- Inverters
- Converters
- Arc Welders

Description

The HIP2030 is a medium voltage integrated circuit (MVIC) capable of driving large capacitive loads at high voltage slew rates (dV/dts). This device is optimized for driving 60nF of MOS gate capacitance at 30V peak to peak in less than 200ns. The half bridge gate driver is ideal for driving MOS Controlled Thyristor (MCT) and IGBT modules.

The architecture of the HIP2030 includes four comparator input channels, a 5V reference, a 12V regulator, and a high side charge pump. The device provides the user with the ability to control minimum low time (MLT) and minimum high time (MHT) at the gate channel output (GO) by varying two external capacitances. In addition, the device contains two uncommitted comparator channels (channels A and B) that can be used as monitors (temperature sensing), indicators (LEDs or opto-couplers), input signal conditioning (both contain Schmitt triggers), or oscillators.

The power requirements of the HIP2030 are low. The driver can be easily configured to operate in one of three power configurations. This allows the use of a small PCB mountable transformer or battery to provide isolated power to the driver chip.

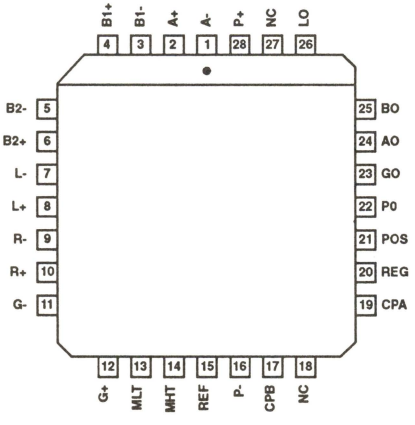
The HIP2030 supplies high output current drive to large capacitive loads and requires few external components to implement a wide variety of MOS gate driver circuits.

Ordering Information

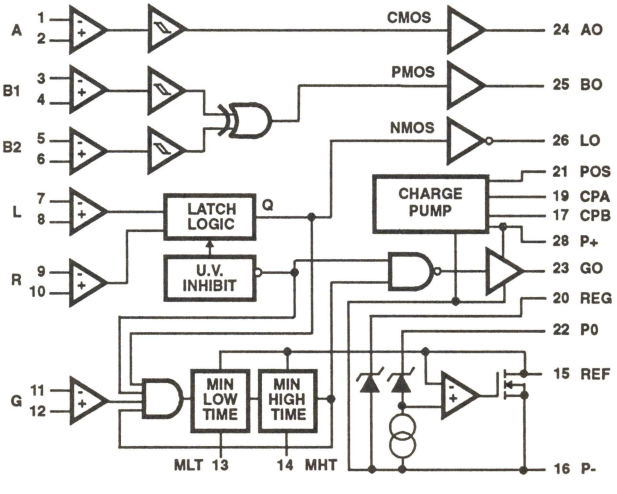
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP2030IM	-40°C to +85°C	28 Lead PLCC

Pinout

HIP2030 (PLCC)



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3691

Absolute Maximum Ratings

Gate Channel Supply Voltage, VP+ to VP- ..... -0.5V to 32V
Logic Supply Voltage, VP0 to VP- ..... 7V to 18V
All Other Pin Voltages
(A+, A-, B1+, B1-, B2+, B2-, L+, L-, R+, R-) ... (VP-)-0.5 to (VP+)+0.5

Thermal Information

Thermal Resistance ..... θ_{JA}
PLCC Package ..... 60°C/W
Lead Temperature (Soldering 10s) ..... +265°C
Storage Temperature Range ..... -40°C to +150°C
Junction Temperature ..... +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions (T_J = -40°C to +125°C Unless Otherwise Noted, All Voltages Referenced to VP-)

Gate Channel Supply Voltage, VP+ to VP- ..... -0.5V to 30V
Logic Supply Voltage, VP0 to VP- ..... 10 to 15V
All Other Pin Voltages
(A+, A-, B1+, B1-, B2+, B2-, L+, L-, R+, R-) ... (VP-)+2V to (VP0)+2V

Max Output Source Current, Channels A, B 10mA
Max Output Sink Current, Channels A, L 10mA
Min Load Current, Ref to P- 2mA

Static Electrical Specifications VP0 to VP- = 15V, VP+ to VP- = 30V, VP- = 0V and T_J = +25°C, Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	T_J = +25°C			UNITS
			MIN	TYP	MAX	
I_{QP0}	Quiescent V_{P0} Supply		-	2.75	-	mA
I_{QPP}	Quiescent V_{PP} Supply	VPP to VP- = 30V	-	1.5	-	µA
I_{QPOS}	Quiescent V_{POS} Supply	Osc Freq = 100kHz	-	3.5	-	mA
I_{SWP0}	VP0 Switching Current	A, B, and G Input Freq = 10kHz	-	3.0	-	mA
I_{SWPP}	VPP Switching Current	A, B, and G Input Freq = 10kHz	-	525	-	µA
BV_{PP}	VPP-VPM Breakdown Voltage		30	35	-	V
V_{REG}	Regulator Voltage, P0 to Ref	IREF = 2mA	-	5	-	V
R_{REG}	Regulator Impedance, P0 to Ref	IREF = 10mA, 30mA	-	5	-	Ω
V_{CLMP}	Clamp Voltage, REG to P-	I_{CLMP} = 15mA	-	12	-	V
R_{CLMP}	Clamp Impedance, REG to P-	I_{CLMP} = 15mA, 30mA	-	15	-	Ω
FQ_{PMP}	Charge Pump Frequency		-	100	-	kHz
DQ_{PMP}	Charge Pump Duty Cycle		-	50	-	%
VoQ_{PMP}	Charge Pump V_{OUT}, VP+ to VP-	IP+ = 500µA	-	28.5	-	V
VoQ_{PMP}	Charge Pump V_{OUT}, VP+ to VP-	IP+ = 5mA	-	27.5	-	V
IIN_{CMP}	Comparator input Leakage	VIN_{CMP} = VP0/2	-	10	-	nA
VOS_{CMP}	Comparator offset Voltage	Vcm = VP0/2	-	15	-	mV
VCM_{CMP}	Comparator Common Mode Voltage Range		(VP-)+2		VP0+2	V
RDS_{SRC}	AO, BO Output RDS, Sourcing	I_{SRC} = 10mA	-	75	-	Ω
RDS_{SRC}	GO Output RDS, Sourcing	I_{SRC} = 6A	-	2	-	Ω
RDS_{SNK}	AO, LO Output RDS, Sinking	I_{SNK} = 10mA	-	75	-	Ω
RDS_{SNK}	GO Output RDs, Sinking	I_{SRC} = 6A	-	1	-	Ω

Dynamic Electrical Specifications VP0 to VP- = 15V, VP+ to VP- = 30V, VP- = 0V, VIN- = 7.5V, VIN+ = (VIN-) ± 2V and T_J = +25°C, Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	T_J = +25°C			UNITS
			MIN	TYP	MAX	
$TGOH_{MIN}$	Min GO Output High Duration	MHT Open	-	750	-	ns
$TGOL_{MIN}$	Min GO Output Low Duration	MLT Open	-	1200	-	ns
TP_{LH}	Prop Delay, Low To High, Channels A, B	C_{LOAD} = 300pF	-	100	-	ns
TP_{LH}	Prop Delay, Low To High, Channel L	C_{LOAD} = 300pF	-	120	-	ns
TP_{HL}	Prop Delay, Low To High, Channel A	C_{LOAD} = 300pF	-	150	-	ns
TR_{AB}	Rise Time, Channels A, B	C_{LOAD} = 300pF	-	50	-	ns
TF_{AL}	Fall Time Channels A, L	C_{LOAD} = 300pF	-	50	-	ns
TP_{LH}	Prop Delay, Low To High, Channel G	C_{LOAD} = 60nF	-	150	-	ns
TP_{HL}	Prop Delay, High To Low, Channel G	C_{LOAD} = 60nF	-	300	-	ns
TR_G	Rise Time, Channel G	C_{LOAD} = 60nF	-	250	-	ns
TF_{AL}	Fall Time Channel G	C_{LOAD} = 60nF	-	200	-	ns

HIP2030 Application Information

The **Harris Photo-Coupled Isolated Gate Drive** (HPCIGD) circuit, illustrated in Figure 1, contains four subcircuits: a Single Supply DC bias, a Regulated voltage divider reference, a Local Energy Source Capacitance, and a Photo-Couple Receiver.

The **Single Supply DC Bias Circuit**, shown in Figure 1, consists of a single external dropping resistor (R1) connected between pins P+ (U1-28) and P0 (U1-22). When an input voltage of 30V is applied across pins P+ and P- (U1-16), R1 forms a resistive divider network with the input impedance located between pins P0 and P- (RVP0). This allows the circuit designer to adjust the value of R1 to obtain a desired bias voltage between pins P0 and P- (VP0.). The value of RVP0 can be calculated by evaluating the equivalent Quiescent Input Impedance (RQ) and the 5V reference impedance (RR) as parallel resistances. The values for R1, RQ, RR, and RVP0 can be determined by using equations 1(A, B, C, D) as shown in appendix A, exercise 1.1.

The **Regulated Voltage Divider Reference** is comprised of two resistors (R3 and R4) connected in series and are located across pins P0 and REF. This voltage divider provides a stable voltage reference to all of the HIP2030 comparator inputs. Resistors R3 and R4 are selected equal in value to create a midpoint bias reference between the peak to peak input signal of U2. Also, the midpoint bias method ensures that input signals generated from U2 and midpoint bias reference voltages are within a safe common mode voltage range of the comparators.

The **Local Energy Source Capacitances**, C2 and C3, are needed to supply the charge required to drive large capacitance loads at high dV/dts. The HPCIGD circuit uses low cost "oversized" tantalum capacitors (C = 10µF) that are used for C2 and C3. If rise times and overshoot are critical, ceramic capacitors with low ESL and ESR should be used to improve gate drive signals. In a power circuit, where the gate driver is exposed to high dV/dts, the network of C2 and C3 directs noise current away from the HIP2030. This allows the HFOIGD circuit to operate well in half bridge power circuits that use a transformer coupled power source.

The **Photo-Coupled Receiver** subcircuit consists of U2, R5, C4, and R6. U2 is a photocoupler which combines an infrared emitter diode (IRED)and a high speed photo detector to translate light pulses to low voltage input signals. These signals are routed to the G channel and are used to control the output GO. Component R5 is used to limit the DC current through the IRED when the input signal voltage switches to its most positive level. A wide range of input voltages may be accommodated by varying R5 to limit the IRED current to 25mA. C4 is a speed up capacitor and is selected to match the forward bias capacitance of the IR diode. The last component, R6, is an optional part and is intended to be a termination resistor with the value set by the user.

The Harris HIP2030 Driver Board (HIP2030DB) is a printed circuit board (PCB) developed to help evaluate the performance of the HIP2030 MCT/IGBT Driver IC in power switching circuits. The component layout of the HIP2030DB circuit enables the user to conveniently populate the PCB for either Photo-Coupled or fiber-optic receivers. In addition, the PCB layout has provisions for "on board prototyping" and special function components. This facilitates the gate drive circuit design and allows the user to exercise the internal architecture and special functions of the HIP2030. The schematic of the HIP2030DB, illustrated in Figure 2, uses the basic HPCIGD circuitry and has provisions for "on board prototyping" and special function components.

TABLE 1. LOGIC

INPUTS			OUTPUTS	
G	L	R	LO	GO
0	0	0	LS	H
0	0	1	H	H
0	1	0	L	H
0	1	1	L	H
1	0	0	LS	U
1	0	1	H	L
1	1	0	L	H
1	1	1	L	H

1 = Input True
0 = Input False

U = Undefined
LS = Last State

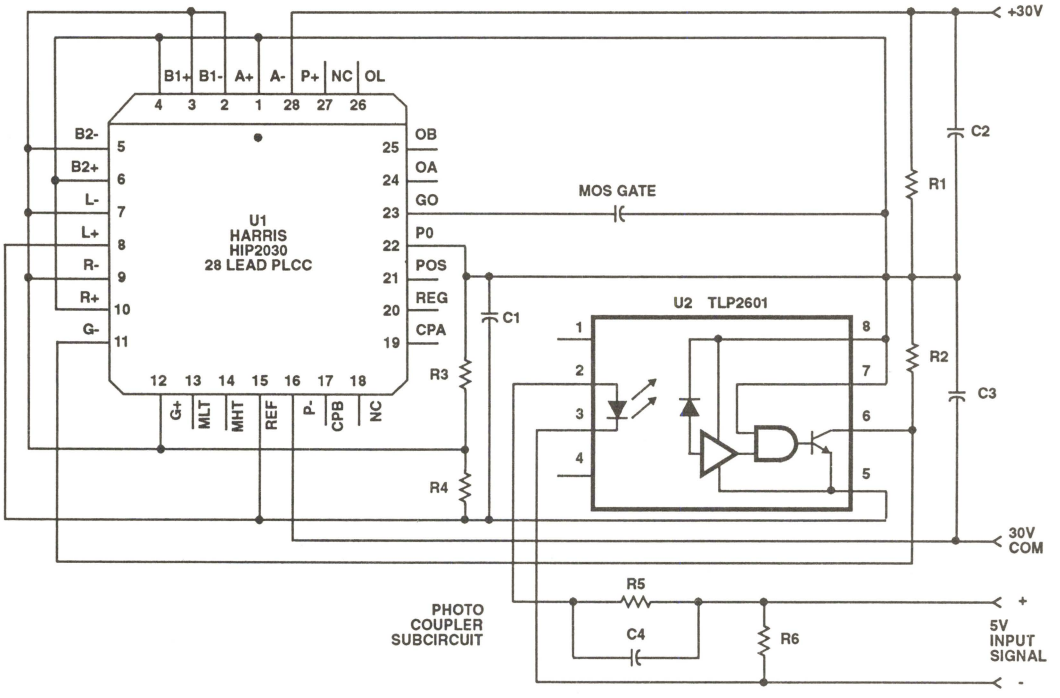


FIGURE 1. HARRIS PHOTO-COUPLED ISOLATED GATE DRIVE

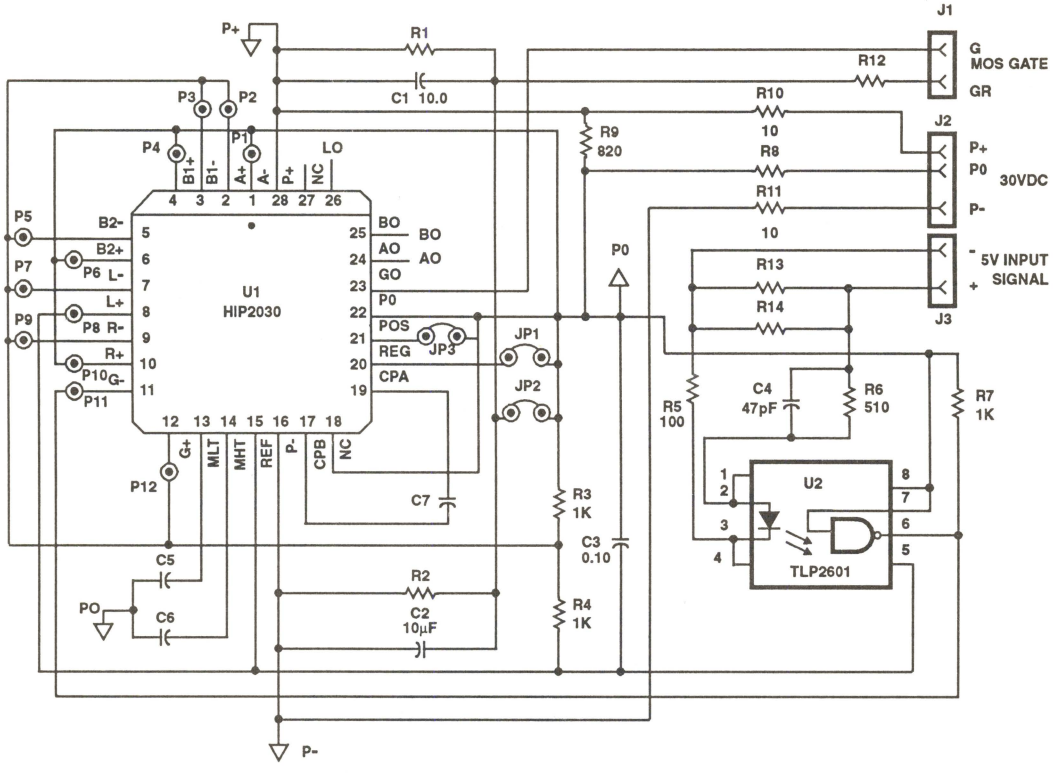


FIGURE 2. HARRIS HIP2030 DRIVER BOARD

NOTES:

1. Capacitors C5 and C6 are special function components which control MLT and MHT.
2. Asymmetrical gate drive may be obtained by opening J2 and adjusting R1 and R2 for the desired voltage ratio.
3. Insert C7 for charge pump operation.
4. Open J3 to disable the charge pump oscillator.
5. Open J1 to disable the internal 12V regulator.
6. R5 is added for noise rejection at CdV/dts.
7. The internal 5V reference (REF) must be operational for MHT and MLT functions to work properly.
8. P1 - P12 are access pads for all comparitor inputs.

Printed Circuit Board

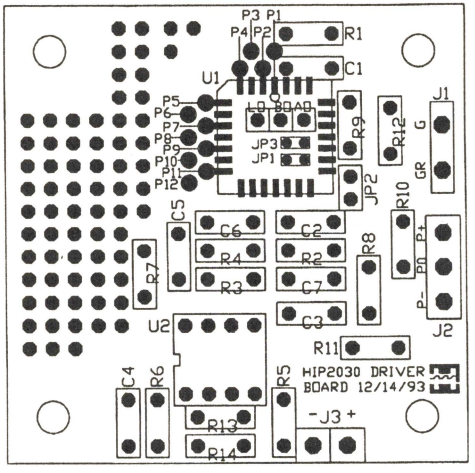


FIGURE 3A. ASSEMBLY LAYER

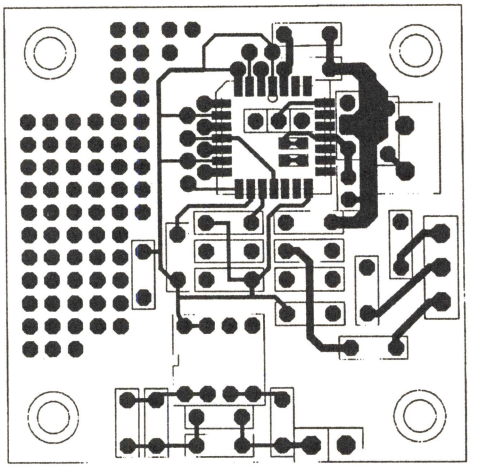


FIGURE 3B. BOTTOM LAYER

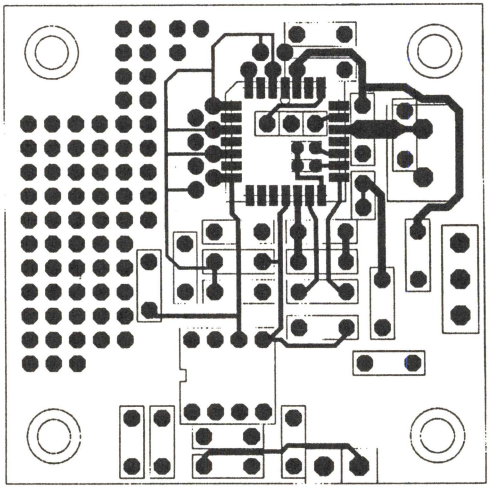


FIGURE 3C. TOP LAYER

Appendix A Exercises

Exercise 1.1

Q: How do I calculate the value of the series dropping resistor R1, shown in Figure 1?

A: The values for R1, R_Q, R_R and R_{VPO} can be determined by using equations 1 (A, B, C, D).

$$R_Q = \frac{V_{PO}}{I_{QPO}} \qquad \text{EQ1(A)}$$

$$R_R = \frac{V_{PO}}{I_{OPTO} + I_{VDR} + I_{RP}} \qquad \text{EQ1(B)}$$

$$R_{VPO} = \frac{1}{\frac{1}{R_Q} + \frac{1}{R_R}} \qquad \text{EQ1(C)}$$

Where: V_{PO} = Voltage between pins P0 and P- (U1 - U22 and U1 - U16)

I_{QPO} = Quiescent current flowing into pin P0.

I_{QPTO} = Quiescent current of the HBR-2521 fiber-optic receiver.

I_{VDR} = Current flowing through R3 and R4 (voltage divider reference).

I_{RP} = Current flowing through pull up resistor R2 (in "ON" or "OFF" state)

The maximum value of R1 can easily be determined in four design steps:

1. Assume the following values:

V_{IN} = 30V DC
I_{QPO} = 2.75mA at V_{P0} = 15V
I_{OPTO} = 5mA
I_{VDR} = 2.5mA
$I_{RP(ON)}$ = 5mA, R2 = 1K, VR2 = 5V

2. Select a usable value of V_{P0} between 7V and 15V DC.

   Use V_{P0}=15V

3. Solve for R_{VP0} using EQ1(A, B, C):

$$R_Q = \frac{15V}{2.75mA} = 5.45K$$

$$R_R = \frac{15V}{(5mA + 2.5mA + 5mA)} = 1.20K$$

$$R_{VP0} = \frac{1}{\frac{1}{5.45K} + \frac{1}{1.20K}} = 984$$

4. Solve for R1 using EQ1(D):

$$R1 = \frac{R_{VP0}(V_{IN} - V_{P0})}{V_{P0}} \qquad \text{EQ1(D)}$$

$$R1 = \frac{984\,(30V - 15V)}{15V} = 984$$

HARRIS SEMICONDUCTOR

HIP2500

April 1994

Half Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive N-Channel Power Devices
- Floating Bootstrap Power Supply for Upper Rail Drive
- CMOS Schmitt-Triggered Inputs with Hysteresis and Pull-Down
- Up to 400kHz Operation
- Single Low Current Bias Supply
- Latch-Up Immune CMOS Logic
- Peak Drive.....Up to 2.0A
- Gate Drive Rise Time (+125°C)..... < 25ns (Typ)

Applications

- High Frequency Switch-Mode Power Supply
- Induction Heating and Welding
- Switch Mode Amplifiers
- AC and DC Motor Drives
- Electronic Lamp Ballasts
- Battery Chargers
- UPS Inverters
- Noise Cancellation in Amplifier Systems

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP2500IP	-40°C to +85°C	14 Lead Plastic DIP
HIP2500IP1	-40°C to +85°C	16 Lead Plastic DIP
HIP2500IB	-40°C to +85°C	16 Lead Plastic SOIC (W)

Description

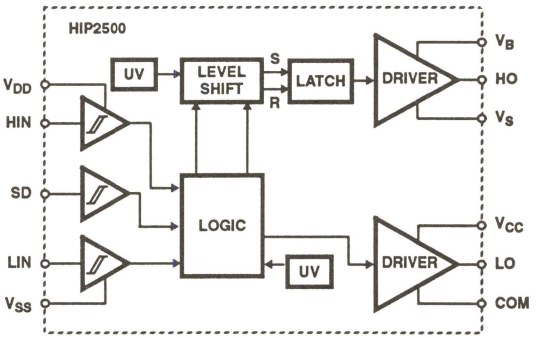
The HIP2500 is a high voltage integrated circuit (HVIC) optimized to drive N-Channel MOS gated power devices in half bridge topologies. It provides the necessary control for PWM motor drive, power supply, and UPS applications. The SD pin allows external shutdown of gate drive to both upper and lower gate outputs. Undervoltage lockout will not allow gating when the bias voltage is too low to drive the external switches into saturation.

The HIP2500IP is pin and function compatible to the International Rectifier IR2110. The HIP2500 has superior ability to accept negative voltages from the V_S pin to the COM pin due to forward recovery of the lower flyback diode.

The HIP2500IB is a SOIC or small outline IC form of the HIP2500. The HIP2500IB drives high side and low side referenced power switches just like the HIP2500IP.

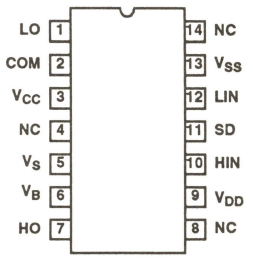
The HIP2500IP1 is a 16 pin Plastic DIP form of the HIP2500. Pins 4 and 5 removed from lead frame to provide extra creepage and strike distances in high voltage applications.

Functional Block Diagram

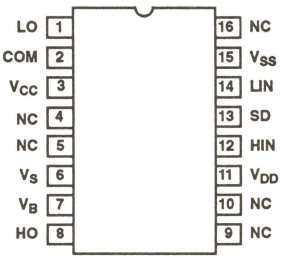


Pinouts

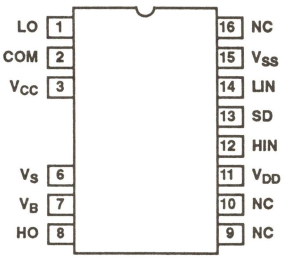
HIP2500 (PDIP)
TOP VIEW



HIP2500 (SOIC)
TOP VIEW



HIP2500 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2801.6**

Absolute Maximum Ratings

Full Temperature Range Unless Otherwise Noted, All Voltages Referenced to V_{SS} Unless Otherwise Noted.

Floating Supply Voltage, V_B . . . . . V_S-0.5V to V_S+18.0V (Positive Terminal)
Floating Supply Voltage, V_S . . . . . 500V (Common Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . -0.5V to V_B+0.5V
Fixed Supply Voltage, V_{CC} . . . . . -0.5V to 18.0V
Low Side Channel Output Voltage, V_{LO} . . . . . -0.5V to V_{CC}+0.5V
Logic Supply Voltage, V_{DD} . . . . . -0.5V to 18.0V
Logic Input Voltage, V_{IN} . . . . . -0.5V to V_{DD}+0.5V [HIN, LIN & SD (Shutdown)]

Thermal Information

Thermal Resistance	θ_{JA}
HIP2500IP	75°C/W
HIP2500IP1	80°C/W
HIP2500IB	90°C/W

See Maximum Power Dissipation vs Temperature Curve
Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range, T_S . . . . . -40°C to +150°C
Operating Ambient Temperature Range, T_A . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended DC Operating Conditions

Floating Supply Voltage, V_B . . . . . V_S+10V to V_S+15V (Floating Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . 10V to V_B (With Respect to V_S)
Fixed Supply Voltage, V_{CC} . . . . . 10V to 15V
Low Side Channel Output Voltage, VLO . . . . . 0V to V_{CC}
Logic Supply Voltage, V_{DD} . . . . . 4V to V_{CC}
Floating Supply Voltage, V_S . . . . . -4.0V to 500V (Common Terminal)

Electrical Specifications

$V_{CC} = (V_B - V_S) = V_{DD} = 15V$, $C_{OM} = V_{SS} = 0$, Unless Otherwise Noted

PARAMETER	SYMBOL	T_J = +25°C			T_J = -40°C TO +125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Quiescent V_{CC} Current	I_{QCC}	-	1.5	1.9	-	-	2.0	mA
Quiescent V_{BS} Current	I_{QBS}	-	300	400	-	300	435	µA
Quiescent V_{DD} Current	I_{QDD}	-	0.1	1	-	-	1.8	µA
Quiescent Leakage Current	I_S (500V)	-	0.4	3.0	-	-	-	µA
Logic Input Pulldown Current, $V_{IN} = V_{DD}$ (HIN, LIN, SD)	IN+	-	12	20	-	-	22	µA
Logic Input Leakage Current, $V_{IN} = V_{SS}$ (HIN, LIN, SD)	IN-	-	0	1	-	0	1	µA
Logic Input Positive Going Threshold	V_{TH}+	7.5	8.0	8.5	7.5	8.0	8.6	V
Logic Input Negative Going Threshold	V_{TH}-	5.5	5.9	6.3	5.5	5.9	6.4	V
Undervoltage Positive Going Threshold	UV+	8.0	9.35	9.99	7.8	-	9.99	V
Undervoltage Negative Going Threshold	UV-	7.7	9.05	9.69	7.5	-	9.69	V
Undervoltage Hysteresis (V_{CC})	UVHYS (V_{CC})	250	-	450	170	-	530	mV
Undervoltage Hysteresis (V_{BS})	UVHYS (V_{BS})	250	-	450	170	-	530	mV
Output High Open Circuit Voltage (HO, LO)	V_{OUT}+	14.95	15	-	14.95	15	-	V
Output Low Open Circuit Voltage (HO, LO)	V_{OUT}-	-	-	0.05	-	-	0.05	V
Output High Short Circuit Current (Sourcing)	I_{OUT}+	1.65	2.1	-	1.15	1.6	-	A
Output Low Short Circuit Current (Sinking)	I_{OUT}-	1.85	2.3	-	1.35	1.7	-	A

Switching Specifications

PARAMETER	SYMBOL	T_J = +25°C			T_J = -40°C TO +125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
HIGH SIDE CHANNEL WITH 500V OFFSET, C_L = 1000pF								
High Side Turn-On Propagation Delay	t_{ON}	320	420	525	230	-	725	ns
High Side Turn-Off Propagation Delay	t_{OFF}	300	385	450	230	-	625	ns
High Side Rise Time	t_R	-	25	50	-	25	50	ns
High Side Turn-Off Fall Time	t_F	-	25	50	-	25	50	ns
LOW SIDE CHANNEL, C_L = 1000pF								
Low Side Turn-On Propagation Delay	t_{ON}	250	365	450	190	-	600	ns
Low Side Turn-Off Propagation Delay	t_{OFF}	225	295	370	175	-	475	ns
Low Side Turn-On Rise Time	t_R	-	25	50	-	30	50	ns
Low Side Turn-Off Fall Time	t_F	-	25	50	-	30	50	ns
Shutdown Propagation Delay High Side Shutdown	t_{SDHO}	300	400	490	200	-	650	ns
Low Side Shutdown	t_{SDLO}	240	320	400	180	-	500	ns
HIGH SIDE CHANNEL WITH 500V OFFSET, C_L = 1000pF								
Turn-On Propagation Delay Matching (Between HO and LO)	M_t	0	-	125	0	-	185	ns
Minimum On Output Pulse Width (HO, LO)	$PW_{OUT(MIN)}$	-	35	50	-	35	55	ns
Minimum Off Output Pulse Width (HO, LO)	$PW_{\overline{OUT}MIN}$	275	440	640	250	440	650	ns
Minimum On Input Pulse Width (HIN, LIN)	$PW_{ON(MIN)}$	-	100	145	-	100	175	ns
Minimum Off Input Pulse Width (HIN, LIN)	$PW_{OFF(MIN)}$	-	110	200	-	110	220	ns
Deadtime LO Turn-Off to HO Turn-On	DHt_{ON}	-	125	-	-	125	-	ns
Deadtime HO Turn-Off to LO Turn-On	DLt_{ON}	-	-20	-	-	-20	-	ns
MAXIMUM TRANSIENT CONDITIONS								
Offset Supply Operating Transient	dV_S/dt	-	-	50	-	-	50	V/ns

Logic Truth Table

HIN	LIN	UV_H	UV_L	SD	HO	LO	COMMENTS
0	0	0	0	0	0	0	Normal Off
0	1	0	0	0	0	1	Lower On
1	0	0	0	0	1	0	Upper On
1	1	0	0	0	1	1	Both On
X	X	X	X	1	0	0	Chip Disabled
X	X	1	1	X	0	0	V_{CC} UV Lockout and V_{BS} Lockout
X	1	1	0	0	0	1	V_{BS} UV Lockout
1	X	0	1	0	1	0	V_{CC} UV Lockout

Typical Performance Curves

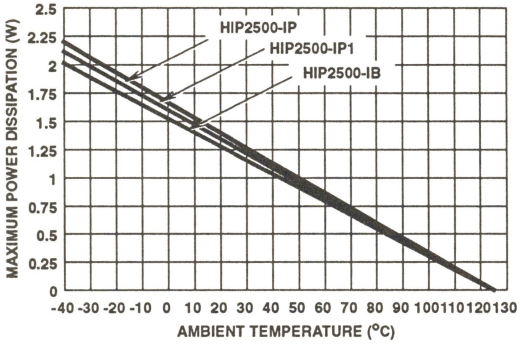


FIGURE 1. MAXIMUM POWER DISSIPATION vs TEMPERATURE

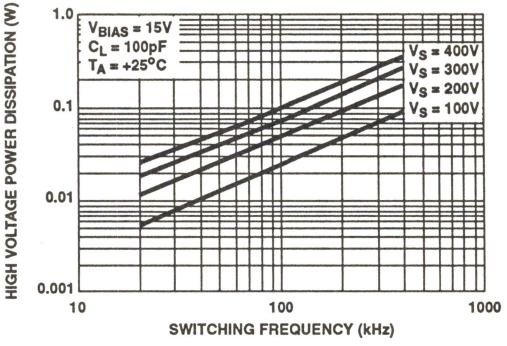
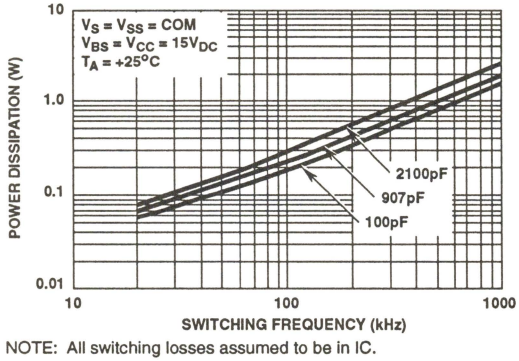


FIGURE 2. HIGH VOLTAGE POWER DISSIPATION vs SWITCHING FREQUENCY



NOTE: All switching losses assumed to be in IC.

FIGURE 3. LOW VOLTAGE POWER DISSIPATION vs FREQUENCY

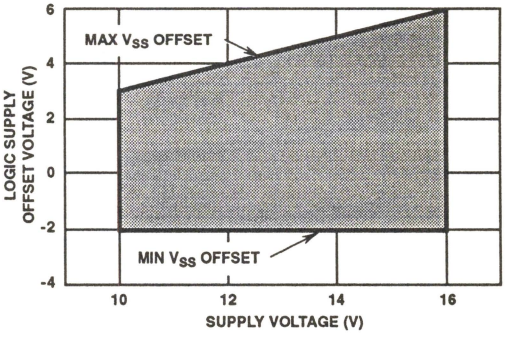


FIGURE 4. V_{SS} OFFSET vs V_{CC} SUPPLY VOLTAGE

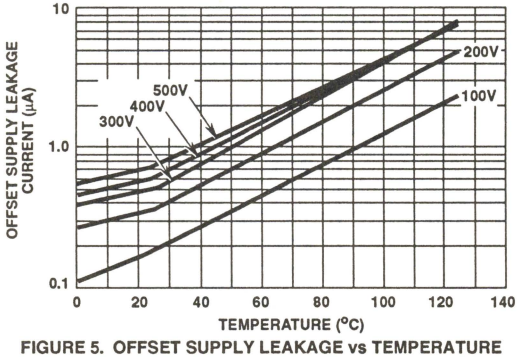


FIGURE 5. OFFSET SUPPLY LEAKAGE vs TEMPERATURE

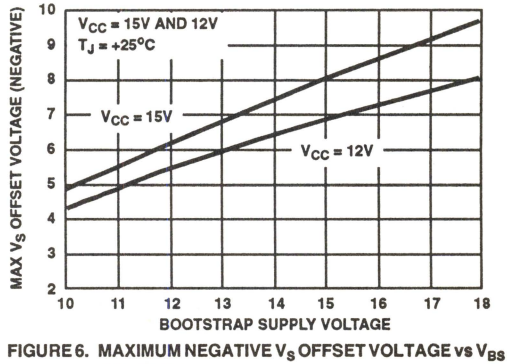


FIGURE 6. MAXIMUM NEGATIVE V_S OFFSET VOLTAGE vs V_{BS} VOLTAGE

Typical Performance Curves (Continued)

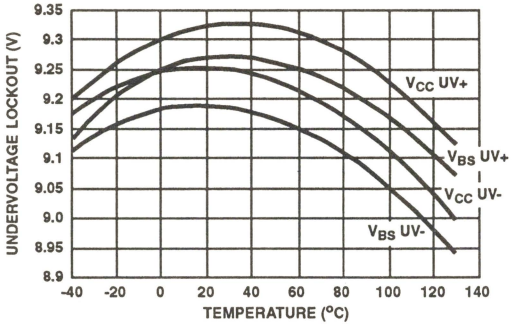


FIGURE 7. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

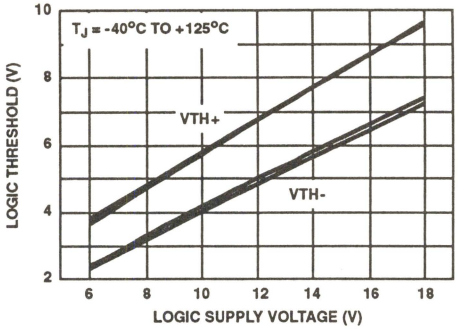


FIGURE 8. INPUT LOGIC THRESHOLD vs SUPPLY VOLTS

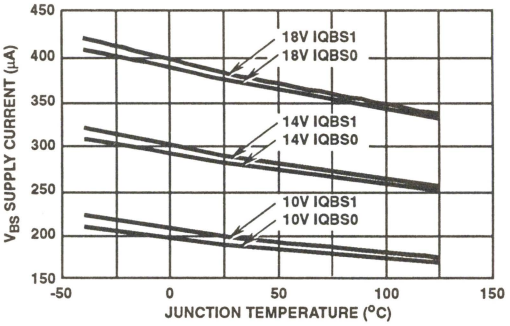


FIGURE 9. QUIESCENT V_{BS} SUPPLY CURRENT vs TEMPERATURE

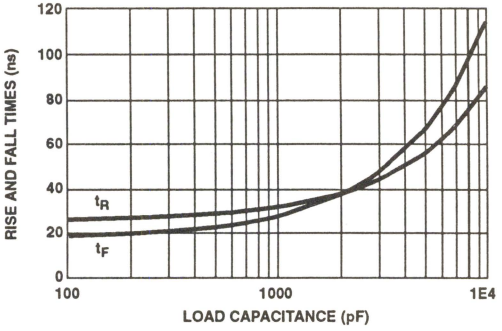


FIGURE 10. RISE AND FALL TIME vs LOAD CAPACITANCE

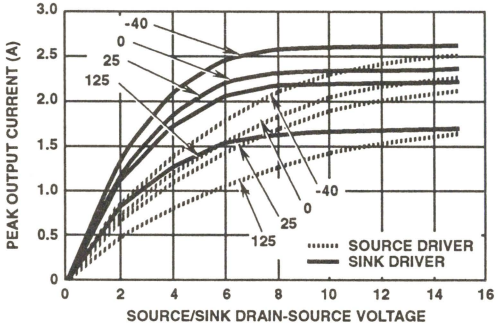


FIGURE 11. DRIVER SINK/SOURCE V-I CHARACTERISTIC

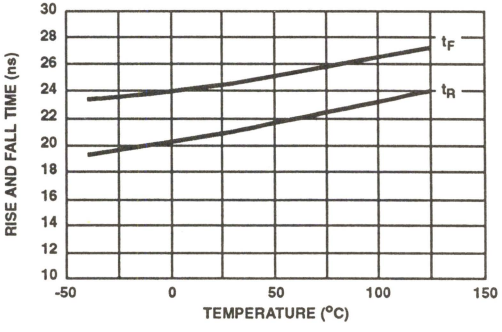


FIGURE 12. RISE AND FALL TIME vs TEMPERATURE

Typical Performance Curves (Continued)

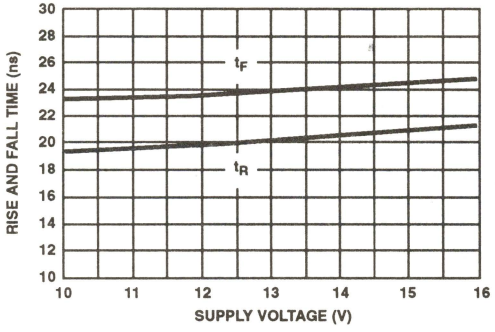


FIGURE 13. RISE AND FALL TIME vs SUPPLY VOLTAGE

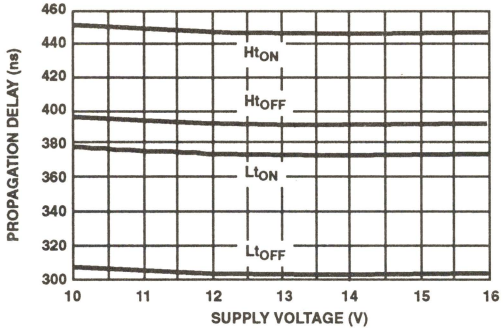


FIGURE 14. PROPAGATION DELAY vs SUPPLY VOLTAGE

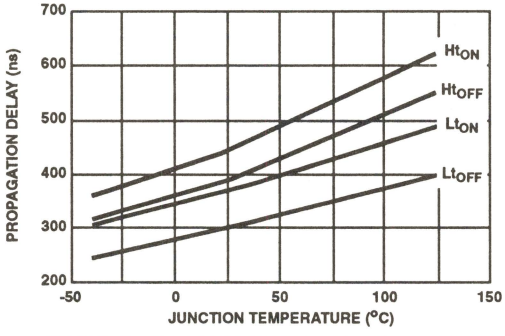
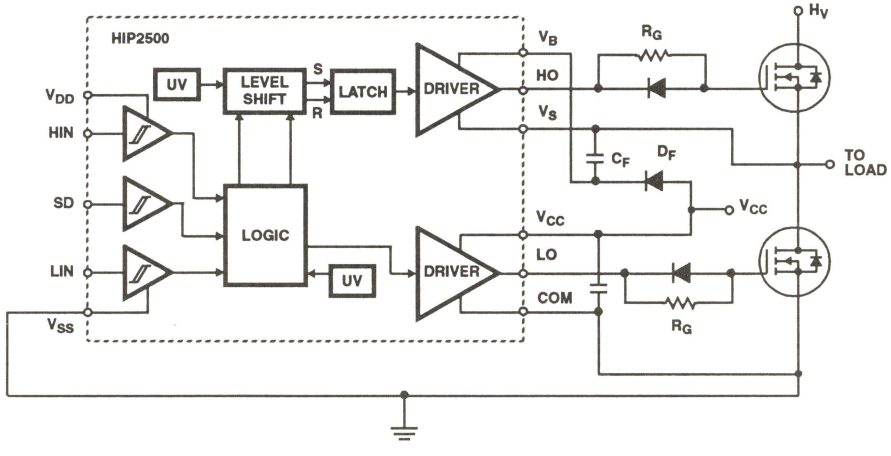


FIGURE 15. PROPAGATION DELAYS AT V_{CC} = 15V

Typical Application Diagram



HARRIS SEMICONDUCTOR

SP600

April 1994

Half Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive Standard and Current Sensing N-Channel Power MOSFET/IGBT Devices
- Creation and Management of a Floating Power Supply for Upper Rail Drive
- Simultaneous Conduction Lockout
- Overcurrent Protection
- Single Low Current Bias Supply Operation
- Latch Immune CMOS Logic
- Peak Drive in Excess of 0.5A

Description

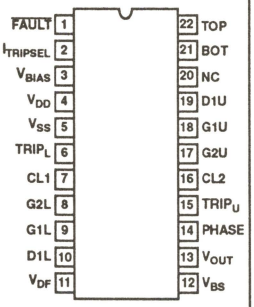
The SP600 is a smart power high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control and management for PWM motor drive, power supply, and UPS applications.

Ordering Information

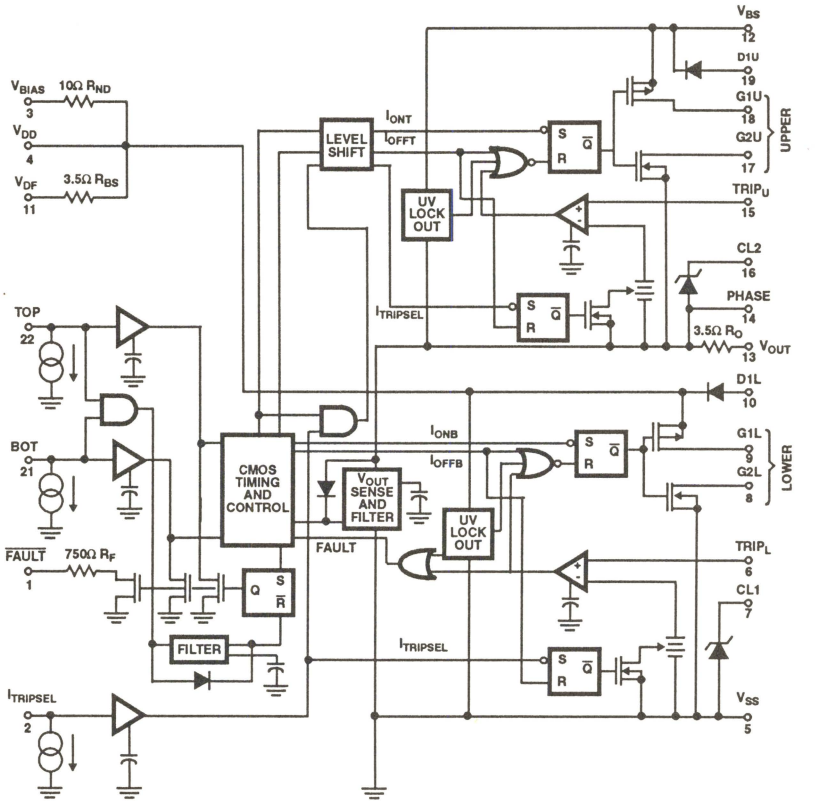
PART	TEMPERATURE	PACKAGE
SP600	-40°C to +85°C	22 Lead Plastic DIP

Pinout

SP600 (PDIP)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2428.3**

Absolute Maximum Ratings Full Temperature Range, All Voltage Referenced to V_{SS} Unless Otherwise Noted. Note 1, Note 2.

Low Voltage Power Supply, V_{BIAS} (Note 1) ..... $18V_{DC}$
Floating Low Voltage Boot Strap ..... $18V_{DC}$
Power Supply to Phase, V_{BS}
Low Voltage Signal Pins
Fault, $I_{TRIPSEL}$, V_{DD}, $TRIP_L$, CL1, G2L.....$-0.5V_{DC}$ to V_{DD} +0.5
G1L, D1L, V_{DF}, TOP, BOT
CL2, $TRIP_U$, G1U, G2U, D1U to Phase.....-0.5_{VDC} to V_{BS} +0.5
High Voltage Pins
Phase, V_{PHASE} ..... $500V_{DC}$
(V_{BS}, V_{OUT}, $TRIP_U$, CL2, G2U and D1U: 0V-18V Higher Than Phase)
Dynamic High Voltage Rating Phase,..... 10,000V/µs
$DV_{PHASE/DT}$

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package ..... 75°C/W
Maximum Package Power Dissipation at T_A = +85°C, P_O
Plastic DIP Package 500mW
Operating Ambient Temperature Range, T_A .....-25°C to +85°C
Storage Temperature Range, T_S.....-40°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C

NOTES:
1. Care must be taken in the application of V_{BIAS} as not to impose high peak dissipation demands on a relatively small metallized noise dropping resistor (R_{ND}). Prolonged high peak currents may result if $+15V_{DC}$ is applied abruptly and/or if the local bypass capacitor C_{DD} is large. It is suggested that C_{DD} be ≤ 10MFD. If it is desirable to switch the $15V_{DC}$ source or if a C_{DD} is larger, additional series impedance may be required.
2. Consult factory for additional package offerings.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, and V_{BS} Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Current (5V < V_{TOP}, V_{BOT}, $V_{TRIPSEL}$ < 15V)	I_{IN}	+25°C	-	20	30	µA
		-40°C to +85°C	-	30	33	µA
I_{BIAS} Quiescent Current (All Inputs Low)	I_{BIAS_L}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BIAS} Quiescent Current (V_{OUT} ≥ V_{BIAS}, and All Inputs Low)	I_{BIAS_H}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BS} Quiescent Current Bootstrap Supply	I_{BS}	+25°C	-	875	1000	µA
		-40°C to +85°C	-	900	1060	µA
TOP Threshold Level	V_{TOP}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
BOTTOM Threshold Level	V_{BOT}	+25°C	7	8	9	V
		-40°C to +85°C	6.9	8	9.1	V
Current TRIPSELECT Threshold Level	$V_{TRIPSEL}$	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Trip Lower and Upper Comparator Threshold Level - Normal ($I_{TRIPSEL}$ = V_{SS})	$V_{TRIP\ L/U_N}$	+25°C	90	105	125	mV
		-40°C to +85°C	90	105	127	mV
Trip Lower and Upper Comparator Threshold Level - Boost ($I_{TRIPSEL}$ = V_{DD}) % of Measured $V_{TRIP\ L/U_N}$	$V_{TRIP\ L/U_B}$	+25°C	110	130	150	%
		-40°C to +85°C	109	130	152	%
Under Voltage Lockout Thresholds (V_{DD} and V_{BS})	V_{LOCK}	+25°C	9	10	11.5	V
		-40°C to +85°C	9.7	10.5	11.8	V
Phase Out of Status Voltage Threshold (PHASE)	V_{OSVT}	+25°C	5	7	9	V
		-40°C to +85°C	4.7	7	9.6	V
Faultbar Impedance at I_{FBAR} = 1mA	RF	+25°C	500	760	1000	Ω
		-40°C to +85°C	450	760	1100	Ω

Electrical Specifications (V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, and V_{BS} Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE (Continued)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Upper/Lower Source Impedances (I_{SOURCE} = 10mA)	$R_{SO\ L/U}$	+25°C	12	17	23	Ω
		-40°C to +85°C	7	17	29	Ω
Upper/Lower Sink Impedances (I_{SINK} = 10mA)	$R_{SI\ L/U}$	+25°C	8	12	16	Ω
		-40°C to +85°C	5	12	20	Ω
Bootstrap Supply Current Limiting Impedance	R_{BS}	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω
Noise Dropping Resistor Impedance	R_{ND}	+25°C	6	10	14	Ω
		-40°C to +85°C	5.4	10	14.6	Ω
High Voltage Leakage (500V V_{BS}, V_{OUT}, PHASE, $TRIP_U$, CL2, G1U, G2U, and D1U to V_{SS}. All other Pins at V_{SS})	I_{LK}	+25°C	-	1	3	µA
Miller Clamp Diodes; D1U and D1L (I_D = 10mA)	$V_{D1U/L}$	+25°C	0.40	0.90	1.40	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 10mA)	$V_{CL2/1\text{-}LOW}$	+25°C	6.35	6.61	6.85	V
		-40°C to +85°C	6.15	6.61	7.15	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 50mA)	$V_{CL2/1\text{-}HIGH}$	+25°C	7.0	8.5	8.0	V
V_{OUT} Limiting Resistance	R_O	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω

NOTE: Maximum Steady State + $15V_{DC}$ Supply Current = $I_{BIAS_L} + I_{BS}$

Switching Specifications (All Referenced to V_{SS}, Except: $TRIP_U$, CI2, G1U, G2U, and D1U Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Refresh One Shot Timer	t_{REF}	+25°C	200	350	500	µs
		-40°C to +85°C	180	350	540	µs
Delay Time of Trip I/U Voltage ($I_{TRIPSEL}$ low) to G2U/G2L Low (50% Overdrive)	$t_{OFF_{TN}}$	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Trip I Voltage ($I_{TRIPSEL}$ low) to Faultbar Low	t_{FN}	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Phase Out of Status to Faultbar Low (TOP High)	t_{OSVF}	+25°C	500	700	900	ns
		-40°C to +85°C	400	700	1050	ns
Minimum Logic Input Pulse Width: TOP and BOTTOM	t_{MINIW}	+25°C	300	430	600	ns
		-40°C to +85°C	275	430	660	ns
Minimum G1U/G1L On Time	t_{ON}	+25°C	1.6	2.3	3.1	µs
		-40°C to +85°C	1.5	2.4	3.4	µs
Minimum Pulsed Off Time, G2U/G2L	t_{OFF}	+25°C	1.3	2.0	3.4	µs
		-40°C to +85°C	1.05	2.1	3.9	µs
Turn On Delay Time of G1U (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs
Turn On Delay Time of G1L (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs

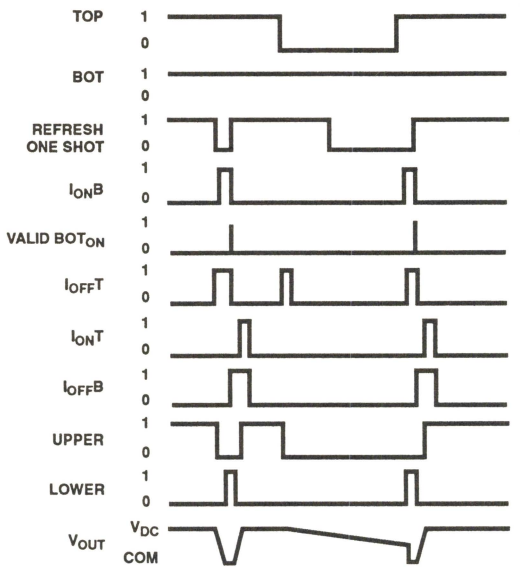
Switching Specifications (All Referenced to V_{SS}, Except: $TRIP_U$, Cl2, G1U, G2U, and D1U Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE) (Continued)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Turn On Delay Time of G1U (THREE-STATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn On Delay Time of G1L (THREE-STATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn Off Delay Time of G2U and G2L	t_{OFF_D}	+25°C	0.75	1.0	1.45	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Minimum Dead Time: G1U off to G1L on, or G1L off to G1U on (BISTATE MODE)	$t_{D.T.}$	+25°C	1.5	2.5	3.5	µs
		-40°C to +85°C	1.2	2.6	4	µs
Fault Reset Delay to Clear Faultbar	$t_{R.T.}$	+25°C	3.4	4.5	6.6	µs
		-40°C to +85°C	3.15	4.8	7.4	µs
Rise Time of Upper and Lower Driver (Load = 2000pF)	$t_{R\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns
Fall Time of Upper and Lower Driver (Load = 2000pF)	$t_{F\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns

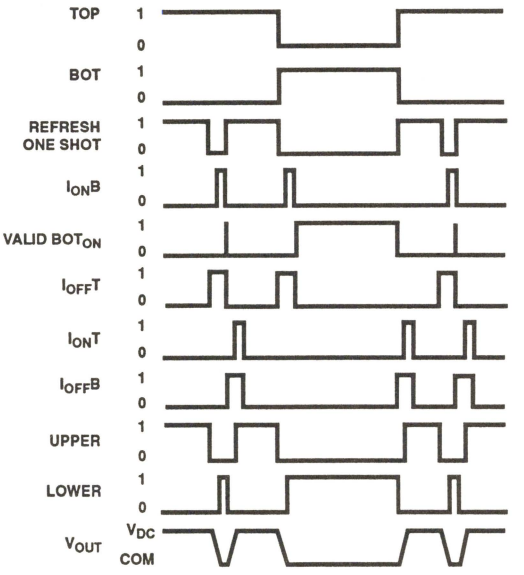
Recommended Operating Conditions and Functional Pin Description (All Voltages Referenced to V_{SS}, Unless Otherwise Noted. See Figure 1)

PARAMETER	CONDITION
FAULTBAR	Open Drain Fault Indicator Output
$I_{TRIPSELECT}$	Digital Input Command to Increase $TRIP_L$ and $TRIP_U$ Threshold by 30%
V_{BIAS}	14.5V to 16.5V with 15V nominal, ≅ 1.5mA DC BIAS Current
V_{DD}	C_{DD} to V_{SS}
V_{SS}	COMMON
TRIP I	100mV Signal to Shut Off LOWER Drive and Trigger a Fault Output
CL1	Lower Noise Clamp Zener
G2L and G1L	Low Impedance Driver Designed to Drive Power MOS Transistors (LOWER)
V_{DF}	Current Limiting Charging Resistor for Bootstrap Capacitor Power Supply
V_{BS}	Bootstrap Supply, Normally a Diode Drop Below V_{DD} Voltage with Respect to the Floating PHASE Reference
V_{OUT}	Load Connection Node
PHASE	Floating Reference Point for High Side Control Circuitry: V_{BS}, $TRIP_U$, CL2, G1U, G2U and D1U
$TRIP_U$	100mV Signal, Referenced to PHASE, to Shut Off UPPER Drive
CL2	Upper Noise Clamp Zener
G2U and G1U	Low Impedance Driver Designed to Drive Power MOS Transistors (UPPER)
TOP	Digital Input to Command the UPPER On
BOT	Digital Input to Command the LOWER On
D1U	Miller Clamp UPPER to V_{BS}
D1L	Miller Clamp LOWER to V_{DD}

Timing Diagram



THREE-STATE MODE SLOWER THAN REFRESH ONE SHOT TIMER



BISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER

NOTE: BOT switching not relevant.

Typical Circuit Configuration

TRUTH TABLE

Applicable to Typical Circuit Configuration (Figure 1)

INPUTS						OUTPUTS		
TOP	BOT	$TRIP_L$	$TRIP_U$	PHASE	V_{BIAS}	UPPER	LOWER	FAULT BAR
0	0	0	X	X	1	0	0	1
1	1	0	0	1	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	0	X	0	1	0	0	0
X	X	1	X	X	1	0	0	0
0	1	0	X	X	1	0	1	1
1	0	0	X	X	1	0	0	1
X	X	X	X	X	0	0	0	0

NOTE: 0 = False, 1 = True, X = Don't Care

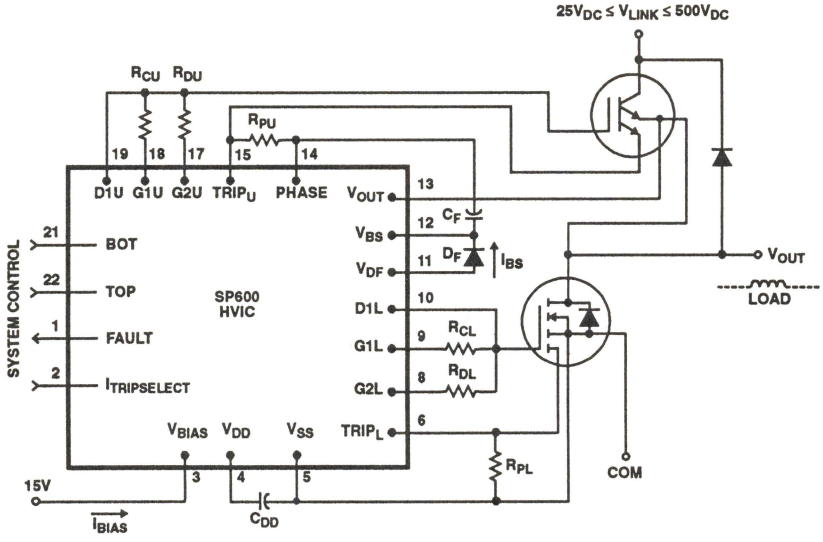


FIGURE 1. TYPICAL CIRCUIT CONFIGURATION

LEGEND		
Application Specific	R_{CU}	Upper Gate Charging Resistor
Application Specific	R_{DU}	Upper Gate Discharge Resistor
Application Specific	R_{PU}	Upper Current Pilot Resistor
Application Specific	R_{CL}	Lower Gate Charging Resistor
Application Specific	R_{DL}	Lower Gate Discharging Resistor
Application Specific	R_{PL}	Lower Current Pilot Resistor
3µF at ≥ 15DC	C_{DD}	Local LV Filter Capacitor
0.22µF Ceramic X7R at ≥ $15V_{DC}$	C_F	Flying Capacitor for Bootstrap Supply
Harris P/N A114M or Equiv PRV ≥ V_{LINK}	D_F	Flying Diode for Bootstrap Supply

NOTE: Refer to 'Additional Product Offerings' for information concerning power output devices.

Functional Description

The SP600 provides a flexible, digitally controlled power function which is intended to be used as PWM drivers of N-Channel MOSFETs and/or IGBTs for up to 240VAC line rectified totem-pole applications. The CMOS driveable inputs are filtered and captured by the control logic to determine the output state. The logic includes fixed timing to prohibit simultaneous conduction of the external power switches and, thru the V_{OUT} sense detector, verifies the output voltage state is in agreement with the controlled inputs. The >11V_{DC} floating power supply required to drive the upper rail external power device is created and managed by the HVIC through C_F and D_F. This capacitor is refreshed from the V_{DD} supply each time V_{OUT} goes low. If the upper channel is commanded on for a long period of time, the bootstrap capacitor CF is automatically refreshed by bringing V_{OUT} low. This is accomplished by turning off the upper rail MOSFET/IGBT, momentarily turning on the lower rail output device, followed by returning control back to the upper switch. Otherwise, C_F would gradually deplete its charge allowing the upper switch to come out of saturation. The upper and lower gate drivers allow for controlled charge and discharge rates as well as facilitate the use of nearly lossless current sensing power MOS devices. The over current trip level can be boosted 30% on a pulse by pulse basis by logic level '1' applied to $I_{TRIPSELECT}$. A $\overline{FAULT}$ output signal is generated when any of the following occurs:

V bias is low
Over current is detected
V phase doesn't agree with the input signal

Reset of $\overline{FAULT}$ is provided by externally removing power or by holding both TOP and BOT inputs low for the required reset time (trt_{MAX}).

Each application can be individually optimized by the selection of external components tailored to ensure proper overall system operation including:

Determining the ratings and sizing of MOSFETs and IGBTs, mixed or matched, as well as flyback diodes (FBD).

The selection of separate gate charge (R_C) and discharge (R_D) impedance chosen per the load capacitance, frequency of operation, and D_I/D_T dependent recovery characteristics of the associated FBDs. R_D should also be sized to prevent simultaneous bridge conduction by ensuring gate discharge in the allotted turn off pulse width ($t_{OFF\ MIN}$).

The selection of over current detection resistors (R_P), compatible with current sense MOSFETs/IGBTs or shunt(s) may be used.

For the floating bootstrap supply D_F and C_F must be determined. D_F must support the worse case system bus voltage and handle the charging currents of C_F. Proper selection should take into consideration T_{RR} and T_{FR} per the desired operating frequency. Proper selection of C_F is a trade off between the minimum t_{ON} time of the lower rail to charge up the capacitor, the amount of charge transfer required by the load, and cost. Due to automatic refresh the capacitor is replenished every 350µs TYP (or even sooner if input commands the TOP to switch at a faster repetition rate).

The local filter capacitor (C_{DD}) should be sized sufficiently large enough to transfer the charge to C_F without causing a significant droop in V_{DD}. As a rule of thumb it should be at least 10 times larger than C_F and be located adjacent to the V_{DD} and V_{SS} pins to minimize series resistance and inductance.

Refer to Application Note AN8829 for more details about module operation and selection of external components.

SP601

April 1994

Half Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive Standard and Current Sensing N-Channel Power MOSFET/IGBT Devices
- Creation and Management of a Floating Power Supply for Upper Rail Drive
- Simultaneous Conduction Lockout
- Overcurrent Protection
- Single Low Current Bias Supply Operation
- Latch Immune CMOS Logic
- Peak Drive in Excess of 0.5A

Description

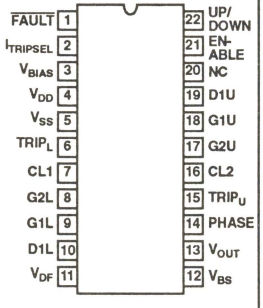
The SP601 is a smart power high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control and management for PWM motor drive, power supply, and UPS applications.

Ordering Information

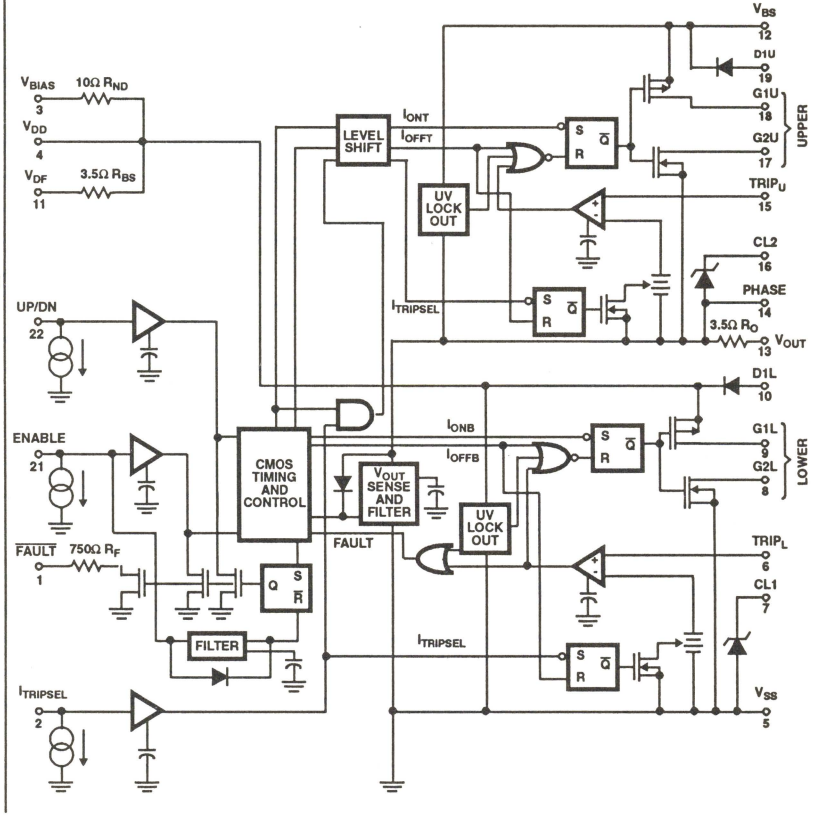
PART	TEMPERATURE RANGE	PACKAGE
SP601	-40°C to +85°C	22 Lead Plastic DIP

Pinout

SP601 (PDIP)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2429.4**

Absolute Maximum Ratings

Full Temperature Range, All Voltage Referenced to V_{SS} Unless Otherwise Noted. Note 1, Note 2.

Low Voltage Power Supply, V_{BIAS} (Note 1) ..... $18V_{DC}$
Floating Low Voltage Boot Strap ..... $18V_{DC}$
Power Supply to Phase, V_{BS}
Low Voltage Signal Pins
Fault, $I_{TRIPSEL}$, V_{DD}, $TRIP_L$, CL1, G2L ..... $-0.5V_{DC}$ to V_{DD} +0.5
G1L, D1L, V_{DF}, TOP, BOT
CL2, $TRIP_U$, G1U, G2U, D1U to Phase ..... -0.5_{VDC} to V_{BS}+0.5
High Voltage Pins
Phase, V_{PHASE} ..... $500V_{DC}$
(V_{BS}, V_{OUT}, $TRIP_U$, CL2, G2U and D1U: 0V-18V Higher Than Phase)
Dynamic High Voltage Rating Phase, ... 10,000V/µs
$DV_{PHASE/DT}$

Thermal Information

Thermal Resistance, Junction-to-Ambient θ_{JA}
Plastic DIP Package ..... 75°C/W
Maximum Package Power Dissipation at T_A = +85°C, P_O
Plastic DIP Package 500mW
Operating Ambient Temperature Range, T_A .....-25°C to +85°C
Storage Temperature Range, T_S .....-40°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C

NOTES:

1. Care must be taken in the application of V_{BIAS} as not to impose high peak dissipation demands on a relatively small metallized noise dropping resistor (R_{ND}). Prolonged high peak currents may result if +15V_{DC} is applied abruptly and/or if the local bypass capacitor C_{DD} is large. It is suggested that C_{DD} be ≤ 10MFD. If it is desirable to switch the 15V_{DC} source or if a C_{DD} is larger, additional series impedance may be required.
2. Consult factory for additional package offerings.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, and V_{BS} Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Current (5V < V_{TOP}, V_{BOT}, $V_{TRIPSEL}$ < 15V)	I_{IN}	+25°C	-	20	30	µA
		-40°C to +85°C	-	30	33	µA
I_{BIAS} Quiescent Current (All Inputs Low)	I_{BIAS_L}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BIAS} Quiescent Current ($V_{OUT} \geq V_{BIAS}$, and All Inputs Low)	I_{BIAS_H}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BS} Quiescent Current Bootstrap Supply	I_{BS}	+25°C	-	875	1000	µA
		-40°C to +85°C	-	900	1060	µA
ENABLE Threshold Level	V_{TOP}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
UP/DN Threshold Level	V_{BOT}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Current Trip Select Threshold Level	$V_{TRIPSEL}$	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Trip Lower and Upper Comparator Threshold Level - Normal ($I_{TRIPSEL}$ = V_{SS})	$V_{TRIP\ L/U_N}$	+25°C	90	105	125	mV
		-40°C to +85°C	90	105	127	mV
Trip Lower and Upper Comparator Threshold Level - Boost ($I_{TRIPSEL}$ = V_{DD}) % of Measured $V_{TRIP\ L/U_N}$	$V_{TRIP\ L/U_B}$	+25°C	110	130	150	%
		-40°C to +85°C	109	130	152	%
Under Voltage Lockout Thresholds (V_{DD} and V_{BS})	V_{LOCK}	+25°C	9	10	11.5	V
		-40°C to +85°C	9.7	10.5	11.8	V
Phase Out of Status Voltage Threshold (PHASE)	V_{OSVT}	+25°C	5	7	9	V
		-40°C to +85°C	4.7	7	9.6	V
Faultbar Impedance at I_{FBAR} = 1mA	RF	+25°C	500	760	1000	Ω
		-40°C to +85°C	450	760	1100	Ω

Electrical Specifications (V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, and V_{BS} Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE (Continued)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Upper/Lower Source Impedances (I_{SOURCE} = 10mA)	$R_{SO\ L/U}$	+25°C	12	17	23	Ω
		-40°C to +85°C	7	17	29	Ω
Upper/Lower Sink Impedances (I_{SINK} = 10mA)	$R_{SI\ L/U}$	+25°C	8	12	16	Ω
		-40°C to +85°C	5	12	20	Ω
Bootstrap Supply Current Limiting Impedance	R_{BS}	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω
Noise Dropping Resistor Impedance	R_{ND}	+25°C	6	10	14	Ω
		-40°C to +85°C	5.4	10	14.6	Ω
High Voltage Leakage (500V V_{BS}, V_{OUT}, PHASE, $TRIP_U$, CL2, G1U, G2U, and D1U to V_{SS}. All other Pins at V_{SS})	I_{LK}	+25°C	-	1	3	µA
Miller Clamp Diodes; D1U and D1L (I_D = 10mA)	$V_{D1U/L}$	+25°C	0.4	0.9	1.4	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 10mA)	$V_{CL2/1\text{-}LOW}$	+25°C	6.35	6.61	6.85	V
		-40°C to +85°C	6.15	6.61	7.15	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 50mA)	$V_{CL2/1\text{-}HIGH}$	+25°C	7.0	8.5	8.0	V
V_{OUT} Limiting Resistance	R_O	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω

NOTE: Maximum Steady State + 15V_{DC} Supply Current = I_{BIAS_L} + I_{BS}

Switching Specifications (All Referenced to V_{SS}, Except: $TRIP_U$, CI2, G1U, G2U, and D1U Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Refresh One Shot Timer	t_{REF}	+25°C	200	350	500	µs
		-40°C to +85°C	180	350	540	µs
Delay Time of Trip I/U Voltage ($I_{TRIPSEL}$ low) to G2U/G2L Low (50% Overdrive	$t_{OFF_{TN}}$	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Trip I Voltage ($I_{TRIPSEL}$ low) to Faultbar Low	t_{FN}	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Phase Out of Status to Faultbar Low (TOP High)	t_{OSVF}	+25°C	500	700	900	ns
		-40°C to +85°C	400	700	1050	ns
Minimum Logic Input Pulse Width: TOP and BOTTOM	t_{MINIW}	+25°C	300	430	600	ns
		-40°C to +85°C	275	430	660	ns
Minimum G1U/G1L On Time	t_{ON}	+25°C	1.6	2.3	3.1	µs
		-40°C to +85°C	1.5	2.4	3.4	µs
Minimum Pulsed Off Time, G2U/G2L	t_{OFF}	+25°C	1.3	2.0	3.4	µs
		-40°C to +85°C	1.05	2.1	3.9	µs
Turn On Delay Time of G1U (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs
Turn On Delay Time of G1L (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs

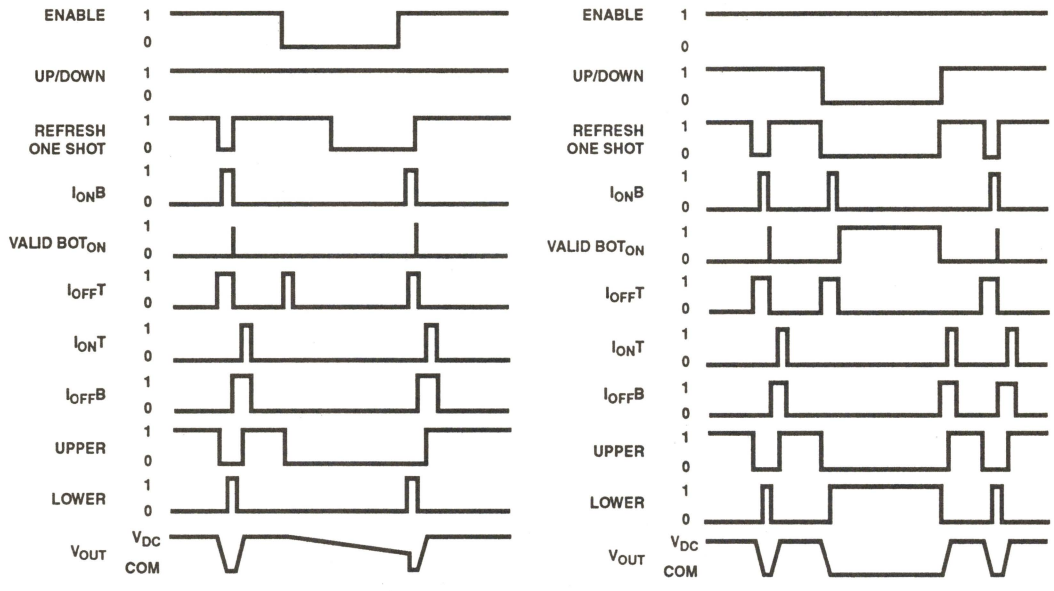
Switching Specifications (All Referenced to V_{SS}, Except: $TRIP_U$, Cl2, G1U, G2U, and D1U Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE) (Continued)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Turn On Delay Time of G1U (THREE-STATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn On Delay Time of G1L (THREE-STATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn Off Delay Time of G2U and G2L	t_{OFF_D}	+25°C	0.75	1.0	1.45	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Minimum Dead Time: G1U OFF to G1L ON, or G1L off to G1U on (BISTATE MODE)	$t_{D.T.}$	+25°C	1.5	2.5	3.5	µs
		-40°C to +85°C	1.2	2.6	4	µs
Fault Reset Delay to Clear Faultbar	$t_{R.T.}$	+25°C	3.4	4.5	6.6	µs
		-40°C to +85°C	3.15	4.8	7.4	µs
Rise Time of Upper and Lower Driver (Load = 2000pF)	$t_{R\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns
Fall Time of Upper and Lower Driver (Load = 2000pF)	$t_{F\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns

Recommended Operating Conditions and Functional Pin Description (All Voltages Referenced to V_{SS}, Unless Otherwise Noted. See Figure 1)

PARAMETER	CONDITION
FAULTBAR	Open Drain Fault Indicator Output
$I_{TRIPSELECT}$	Digital Input Command to Increase $TRIP_L$ and $TRIP_U$ Threshold by 30%
V_{BIAS}	14.5V to 16.5V with 15V nominal, ≅ 1.5mA DC BIAS Current
V_{DD}	C_{DD} to V_{SS}
V_{SS}	COMMON
TRIP I	100mV Signal to Shut Off LOWER Drive and Trigger a Fault Output
CL1	Lower Noise Clamp Zener
G2L and G1L	Low Impedance Driver Designed to Drive Power MOS Transistors (LOWER)
V_{DF}	Current Limiting Charging Resistor for Bootstrap Capacitor Power Supply
V_{BS}	Bootstrap Supply, Normally a Diode Drop Below V_{DD} Voltage with Respect to the Floating PHASE Reference
V_{OUT}	Load Connection Node
PHASE	Floating Reference Point for High Side Control Circuitry: V_{BS}, $TRIP_U$, CL2, G1U, G2U and D1U
$TRIP_U$	100mV Signal, Referenced to PHASE, to Shut Off UPPER Drive
CL2	Upper Noise Clamp Zener
G2U and G1U	Low Impedance Driver Designed to Drive Power MOS Transistors (UPPER)
ENABLE	Digital Input to ENABLE the UP/DN Command to Turn on Top/Bottom Devices
UP/DN	Digital Input to Top/Bottom Device (If ENABLE is High)
D1U	Miller Clamp UPPER to V_{BS}
D1L	Miller Clamp LOWER to V_{DD}

Timing Diagram



THREE-STATE MODE SLOWER THAN REFRESH ONE SHOT TIMER

BISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER

NOTE: BOT switching not relevant.

Typical Circuit Configuration

TRUTH TABLE

Applicable to Typical Circuit Configuration (Figure 1)

INPUTS						OUTPUTS		
UP/DN	ENABLE	$TRIP_L$	$TRIP_U$	PHASE	V_{BIAS}	UPPER	LOWER	FAULT BAR
0	0	0	X	X	1	0	0	1
1	1	0	0	1	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	0	X	0	1	0	0	0
X	X	1	X	X	1	0	0	0
0	1	0	X	X	1	0	1	1
1	0	0	X	X	1	0	0	1
X	X	X	X	X	0	0	0	0

NOTE: 0 = False, 1 = True, X = Don't Care

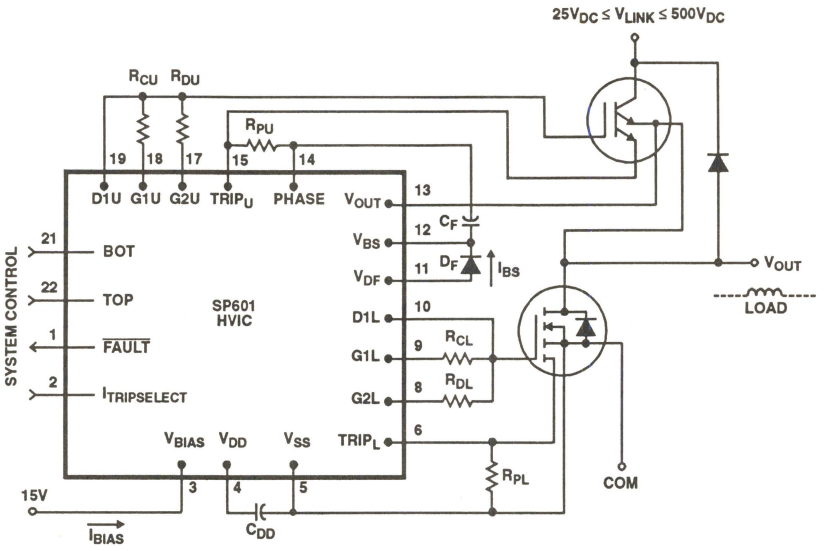


FIGURE 1. TYPICAL CIRCUIT CONFIGURATION

LEGEND		
Application Specific	R_{CU}	Upper Gate Charging Resistor
Application Specific	R_{DU}	Upper Gate Discharge Resistor
Application Specific	R_{PU}	Upper Current Pilot Resistor
Application Specific	R_{CL}	Lower Gate Charging Resistor
Application Specific	R_{DL}	Lower Gate Discharging Resistor
Application Specific	R_{PL}	Lower Current Pilot Resistor
3µF at ≥ 15DC	C_{DD}	Local LV Filter Capacitor
0.22µF Ceramic X7R at ≥ $15V_{DC}$	C_F	Flying Capacitor for Bootstrap Supply
Harris P/N A114M or Equiv PRV ≥ V_{LINK}	D_F	Flying Diode for Bootstrap Supply

NOTE: Refer to 'Additional Product Offerings' for information concerning power output devices.

Functional Description

The SP601 provides a flexible, digitally controlled power function which is intended to be used as PWM drivers of N-Channel MOSFETs and/or IGBTs for up to 240VAC line rectified totem-pole applications. The CMOS driveable inputs are filtered and captured by the control logic to determine the output state. The logic includes fixed timing to prohibit simultaneous conduction of the external power switches and, thru the V_{OUT} sense detector, verifies the output voltage state is in agreement with the controlled inputs. The > $11V_{DC}$ floating power supply required to drive the upper rail external power device is created and managed by the HVIC through C_F and D_F. This capacitor is refreshed from the V_{DD} supply each time V_{OUT} goes low. If the upper channel is commanded on for a long period of time, the bootstrap capacitor C_F is automatically refreshed by bringing V_{OUT} low. This is accomplished by turning off the upper rail MOSFET/IGBT, momentarily turning on the lower rail output device, followed by returning control back to the upper switch. Otherwise, C_F would gradually deplete its charge allowing the upper switch to come out of saturation. The upper and lower gate drivers allow for controlled charge and discharge rates as well as facilitate the use of nearly lossless current sensing power MOS devices. The over current trip level can be boosted 30% on a pulse by pulse basis by logic level '1' applied to $I_{TRIPSELECT}$. A $\overline{FAULT}$ output signal is generated when any of the following occurs:

V bias is low
Over current is detected
V phase doesn't agree with the input signal

Reset of $\overline{FAULT}$ is provided by externally removing power or by holding the ENABLE input low for the required reset time (trt_{MAX}).

Each application can be individually optimized by the selection of external components tailored to ensure proper overall system operation including:

Determining the ratings and sizing of MOSFETs and IGBTs, mixed or matched, as well as flyback diodes (FBD).

The selection of separate gate charge (R_C) and discharge (R_D) impedance chosen per the load capacitance, frequency of operation, and D_I/D_T dependent recovery characteristics of the associated FBDs. R_D should also be sized to prevent simultaneous bridge conduction by ensuring gate discharge in the allotted turn off pulse width ($t_{OFF\ MIN}$).

The selection of over current detection resistors (R_P), compatible with current sense MOSFETs/IGBTs or shunt(s) may be used.

For the floating bootstrap supply D_F and C_F must be determined. D_F must support the worse case system bus voltage and handle the charging currents of C_F. Proper selection should take into consideration T_{RR} and T_{FR} per the desired operating frequency. Proper selection of C_F is a trade off between the minimum t_{ON} time of the lower rail to charge up the capacitor, the amount of charge transfer required by the load, and cost. Due to automatic refresh the capacitor is replenished every 350µs TYP (or even sooner if the UP/DN input switches at a faster repetition rate).

The local filter capacitor (C_{DD}) should be sized sufficiently large enough to transfer the charge to C_F without causing a significant droop in V_{DD}. As a rule of thumb it should be at least 10 times larger than C_F and be located adjacent to the V_{DD} and V_{SS} pins to minimize series resistance and inductance.

Refer to Application Note AN8829 for more details about module operation and selection of external components.

INTELLIGENT POWER ICs

5

AC TO DC CONVERTERS

		PAGE
AC TO DC CONVERTER SELECTION GUIDE		5-2
AC TO DC CONVERTER DATA SHEETS		
CA3059, CA3079	Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications	5-3
HV-2405E	World-Wide Single Chip Power Supply	5-15

AC to DC Converter Selection Guide

DEVICE	DESCRIPTION	AC INPUT VOLTAGE AT 50-60Hz AND 400Hz (VAC)	MAX DC SUPPLY VOLTAGE (V)	MAX OUTPUT CURRENT (mA)	SENSOR RANGE (RX) (KΩ)	FEATURES
CA3059	Zero Voltage Switch AC Power Control System on a Chip	24V 120V 208/230V 277V	14	124	2 to 100	Contains, Power Supply Zero Crossing Detector, External Sensor Comparator and Triac Driver. (Inhibit and Protection Circuits on CA3059 only)
CA3079			10	124	2 to 50	
HV-2405E	World Wide Single Chip Power Supply	15V to 275V	Output 5V to 24V	50	-	UL Recognized E130808

NOTE:

1. Electrical Characteristics at T_A = +25°C, 14 Lead Dual-In-Line (E) Package Operating Temperature Range (T_A) -55°C to +125°C.

DEVICE	DESCRIPTION	INPUT VOLTAGE RANGE	OUTPUT VOLTAGE RANGE	MAXIMUM OUTPUT CURRENT	BIAS CURRENT	TEMPERATURE RANGE
HIP5600	High Voltage Linear Regulator	50V to 400V	1.2V to 350V	35mA	600µA	-40°C to +100°C Thermal Protection at 134°C

HARRIS SEMICONDUCTOR

CA3059, CA3079

PRELIMINARY

April 1994

Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications

Features

- Relay Control
- Valve Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator with Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control
- Heater Control
- Lamp Control

Type Features

	CA3059	CA3079
• 24V, 120V, 208/230V, 277V at 50/60 or 400Hz Operation	X	X
• Differential Input	X	X
• Low Balance Input Current (Max) - μA	1	2
• Built-In Protection Circuit for Opened or Shorted Sensor (Term 14)	X	X
• Sensor Range (Rx) - kΩ	2 - 100	2 - 50
• DC Mode (Term 12)	X	
• External Trigger (Term 6)	X	
• External Inhibit (Term 1)	X	
• DC Supply Volts (Max)	14	10
• Operating Temperature Range (°C)	-55 to +125	

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3059	-55°C to +125°C	14 Lead Plastic DIP
CA3079	-55°C to +125°C	14 Lead Plastic DIP

Description

The CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V, and 277V at 50Hz-60Hz and 400Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see the Functional Block Diagram) as follows:

1. Limiter-Power Supply - Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit - Provides high-current pulses to the gate of the power controlling thyristor.

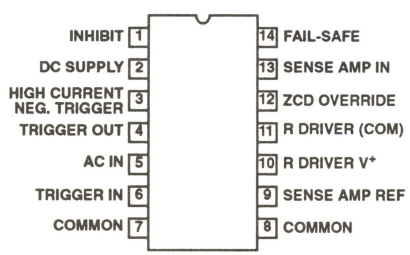
In addition, the CA3059 provides the following important auxiliary functions (see the Functional Block Diagram).

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

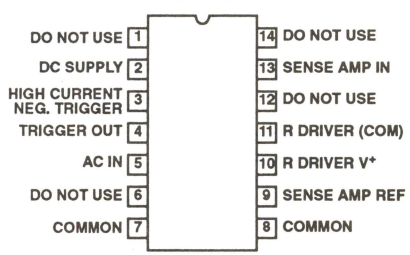
The CA3059 and CA3079 are supplied in 14 lead dual-in-line plastic packages.

Pinouts

CA3059 (PDIP)
TOP VIEW



CA3079 (PDIP)
TOP VIEW

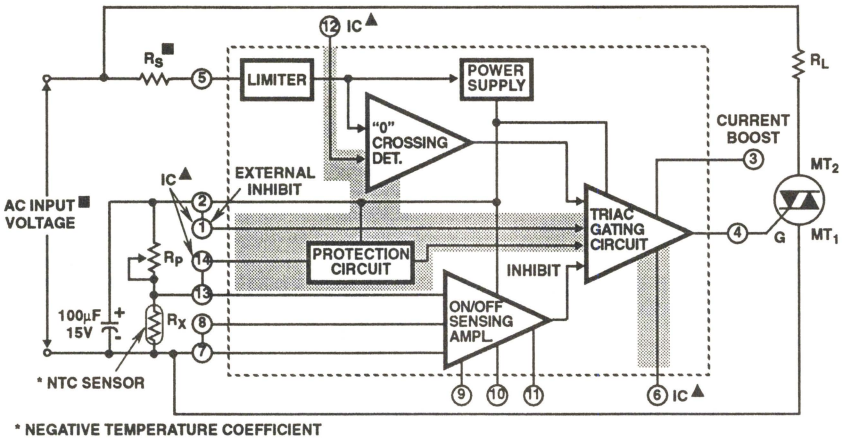


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **490.3**

Functional Block Diagram



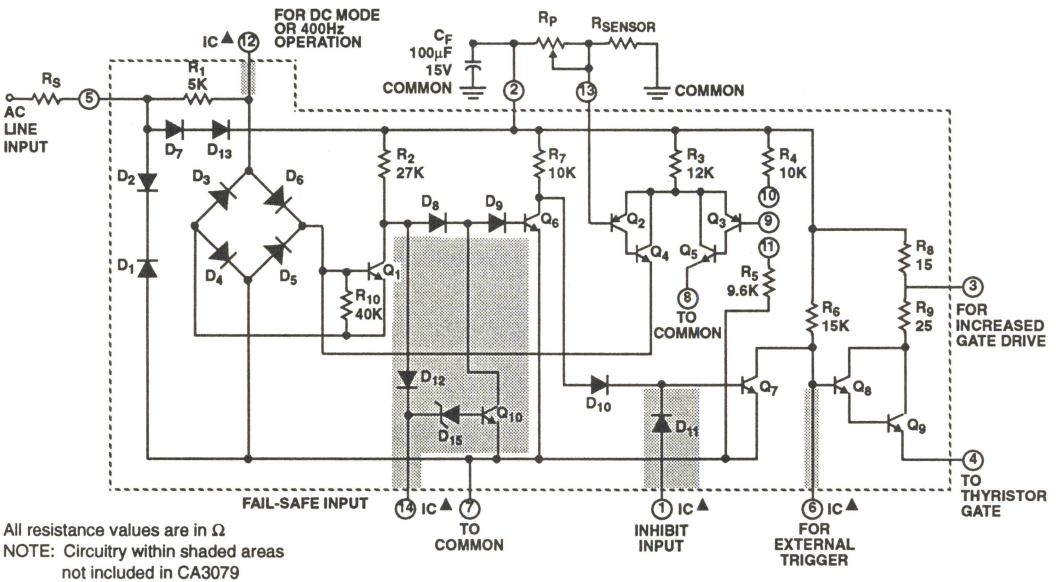
* NEGATIVE TEMPERATURE COEFFICIENT

AC INPUT VOLTAGE (50/60 OR 400Hz) V AC	INPUT SERIES RESISTOR (R_S) kΩ	DISSIPATION RATING FOR R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE: Circuitry within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)



All resistance values are in Ω

NOTE: Circuitry within shaded areas not included in CA3079

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)

FIGURE 1. SCHEMATIC DIAGRAM OF CA3059 AND CA3079

Absolute Maximum Ratings T_A = +25°C

DC Supply Voltage (Between Terminals 2 & 7)
CA3059 . . . . . 14V
CA3079 . . . . . 10V
DC Supply Voltage (Between Terminals 2 & 8)
CA3059 . . . . . 14V
CA3079 . . . . . 10V
Peak Supply Current (Terminals 5 & 7) . . . . . ±50mA
Output Pulse Current (Terminal 4) 150mA

Thermal Information

Thermal Resistance θ_{JA}
PDIP Package . . . . . 100°C/W
Power Dissipation
Up to T_A = +55°C CA3059, CA3079 . . . . . 950mW
Above T_A = +55°C CA3059, CA3079 . . Derate Linearly 10mW/°C
Ambient Temperature
Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At distance 1/16" ± 1/32" (1.59 ± 0.79) from case
for 10 seconds max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at 120V_{RMS}, 50-60Hz (AC Line Voltage) (Note 1)

PARAMETERS		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY VOLTAGE (Figure 2A, 2B, 2C)							
Inhibit Mode	At 50/60Hz	V_S	R_S = 8kΩ, I_L = 0	6.1	6.5	7	V
	At 400Hz		R_S = 10kΩ, I_L = 0	-	6.8	-	V
	At 50/60Hz		R_S = 5kΩ, I_L = 0	-	6.4	-	V
Pulse Mode	At 50/60Hz	V_S	R_S = 8kΩ, I_L = 0	6	6.4	7	V
	At 400Hz		R_S = 10kΩ, I_L = 0	-	6.7	-	V
	At 50/60Hz		R_S = 5kΩ, I_L = 0	-	6.3	-	V
Gate Trigger Current (Figures 3, 4A)		I_{GT} Terminal 4	Terminals 3 and 2 Connected, V_{GT} = 1V	-	105	-	mA
PEAK OUTPUT CURRENT (PULSED) (Figures 4, 5)							
With Internal Power Supply Figure 4a, 4b		I_{OM} Terminal 4	Terminal 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	-	mA
			Terminals 3 and 2 Connected, Gate Trigger Voltage (V_{GT}) = 0	90	124	-	mA
With External Power Supply Figure 5a, 5b, 5c		I_{OM} Terminal 4	Terminal 3 open, V+ = 12V, V_{GT} = 0	-	170	-	mA
			Terminals 3 and 2 Connected, V+ = 12V, V_{GT} = 0		240	-	mA
Inhibit Input Ratio (Figure 6)		V_9/V_2	Voltage Ratio of Terminals 9 to 2	0.465	0.485	0.520	-
TOTAL GATE PULSE DURATION (Note 2) (Figure 7A, 7B, 7C, 7D)							
For Positive dv/dt	50-60Hz	t_P	C_{EXT} = 0	70	100	140	µs
	400Hz		C_{EXT} = 0, R_{EXT} = ∞	-	12	-	µs
For Negative dv/dt	50-60Hz	t_N	C_{EXT} = 0	70	100	140	µs
	400Hz		C_{EXT} = 0, R_{EXT} = ∞	-	10	-	µs
PULSE DURATION AFTER ZERO CROSSING (50-60Hz) (Figure 7A)							
For Positive dv/dt		t_{P1}	C_{EXT} = 0, R_{EXT} = ∞	-	50	-	µs
For Negative dv/dt		t_{N1}		-	60	-	µs
OUTPUT LEAKAGE CURRENT (Figure 8)							
Inhibit Mode		I_4		-	0.001	10	µA
INPUT BIAS CURRENT (Figure 9)							
CA3059		I_I		-	220	1000	nA
CA3079				-	220	2000	nA
Common-mode Input Voltage Range		V_{CMR}	Terminals 9 and 13 Connected	-	1.5 to 5	-	V

Electrical Specifications T_A = +25°C, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at $120V_{RMS}$, 50-60Hz (AC Line Voltage) (Note 1) **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SENSITIVITY (Note 3) (Figures 4(a), 11)						
Pulse Mode	ΔV_{13}	Terminal 12 open	-	6	-	mV

NOTES:

1. The values given in the Electrical Characteristics Chart at 120V also apply for operation at input voltages of 208/230V, and 277V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in the Functional Block Diagram, for the specified input voltage.
2. Pulse Duration in 50Hz applications is approximately 15% longer than shown in Figure 7(b).
3. Required voltage change at Terminal 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

Maximum Voltage Ratings T_A = +25°C

MAXIMUM VOLTAGE RATINGS T_A = +25°C															MAXIMUM CURRENT RATINGS	
TERM. NO.	NOTE 3 1	2	3	4	NOTE 1 5	NOTE 3 6	7	8	9	10	11	NOTE 3 12	13	NOTES 2,3 14	I_{IN} mA	I_{OUT} mA
1 Note 3		Note 4	Note 4	Note 4	Note 4	15 0	10 -2	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0 Note 5 -14	0 Note 5 -14	0 -14	0 -14	0 -14	Note 4	0 -14	0 -14	150	10
3				0 -15	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
4					Note 4	2 -10	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	0.1	150
5 Note 1						Note 4	7 -7	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	50	10
6 Note 3							14 0	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
7								Note 4	14 0	Note 4	20 0	2.5 -2.5	14 0	6 -6	Note 4	Note 4
8									10 0	Note 4	Note 4	Note 4	Note 4	Note 4	0.1	2
9										Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
10											Note 4	Note 4	Note 4	Note 4	Note 4	Note4
11												Note 4	Note 4	Note 4	Note 4	Note4
12 Note 3													Note 4	Note 4	50	50
13														Note 4	Note 4	Note4
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2V to -10V.

NOTES:

1. Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50mA.
2. Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2mA.
3. For the CA3079 indicated terminal is internally connected and, therefore, should not be used.
4. Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.
5. For CA3079 (0V to -10V).

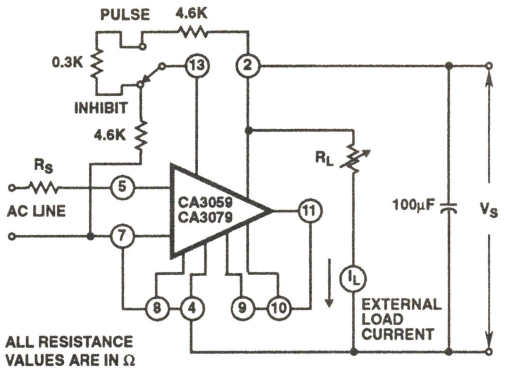


FIGURE 2A. DC SUPPLY VOLTAGE TEST CIRCUIT FOR CA3059 AND CA3079

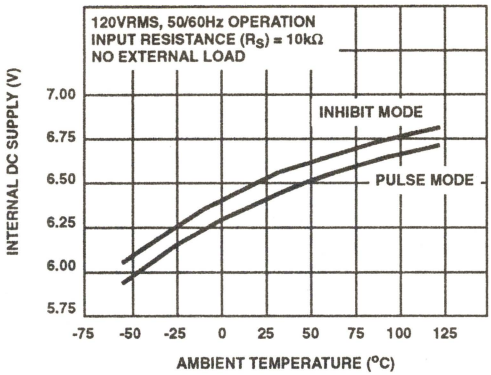


FIGURE 2B. DC SUPPLY VOLTAGE vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

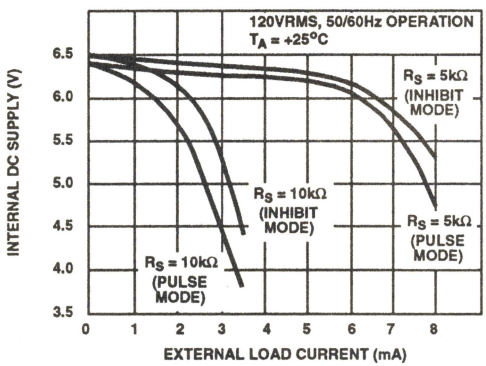


FIGURE 2C. DC SUPPLY VOLTAGE vs EXTERNAL LOAD CURRENT FOR CA3059 AND CA3079

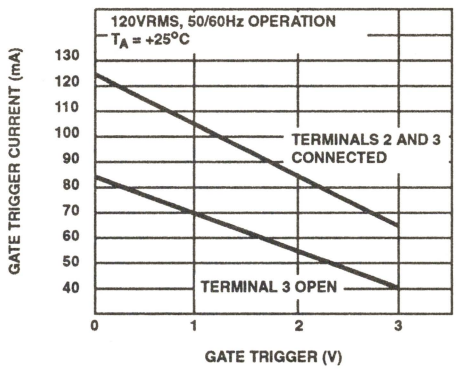


FIGURE 3. GATE TRIGGER CURRENT vs GATE TRIGGER VOLTAGE FOR CA3059 AND CA3079

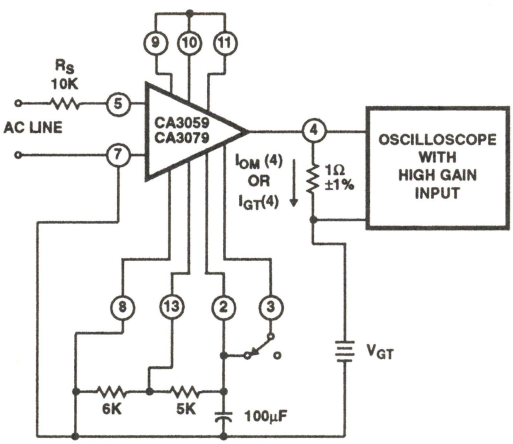


FIGURE 4A. PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059 AND CA3079

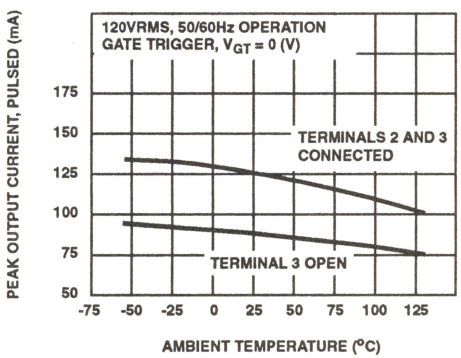


FIGURE 4B. PEAK OUTPUT CURRENT (PULSED) vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

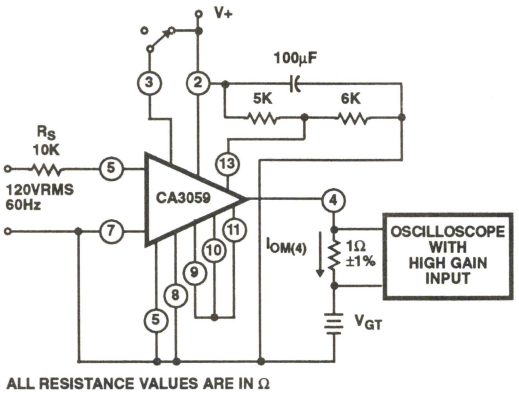


FIGURE 5A. PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059

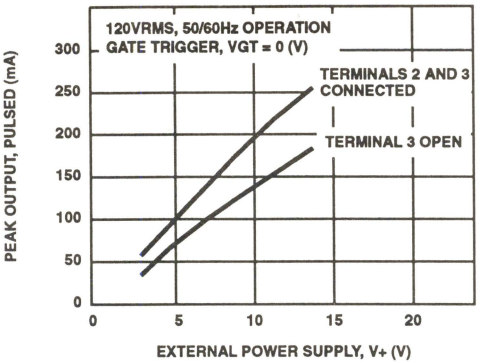


FIGURE 5B. PEAK OUTPUT CURRENT (PULSED) vs EXTERNAL POWER SUPPLY VOLTAGE FOR CA3059

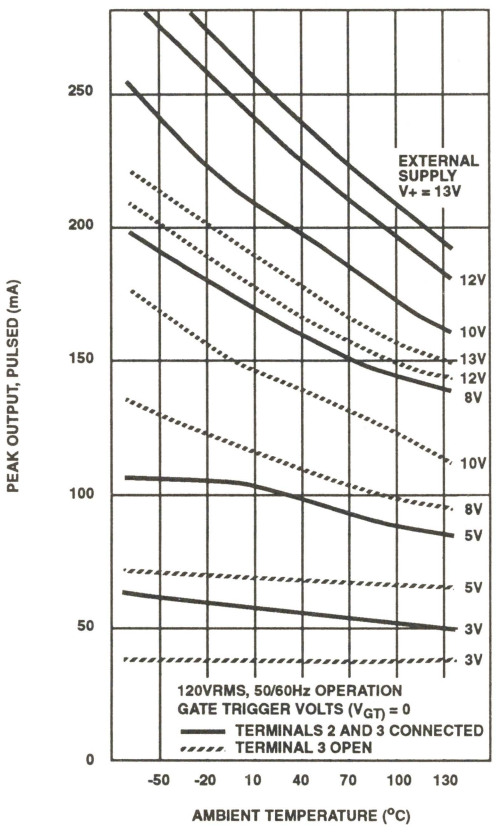


FIGURE 5C. PEAK OUTPUT CURRENT (PULSED) vs AMBIENT TEMPERATURE FOR CA3059

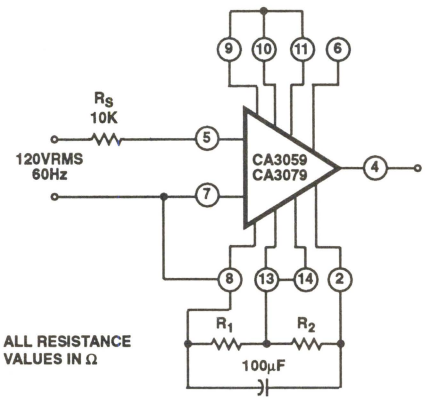


FIGURE 6(A). INPUT INHIBIT VOLTAGE RATIO TEST CIRCUIT FOR CA3059 AND CA3079

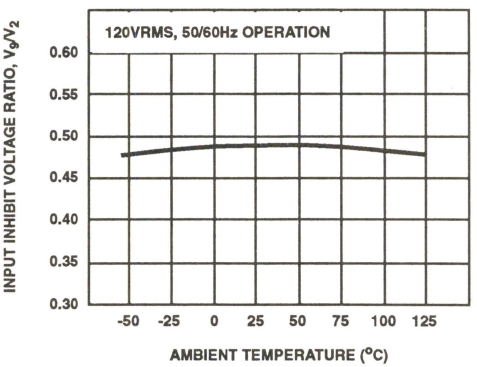
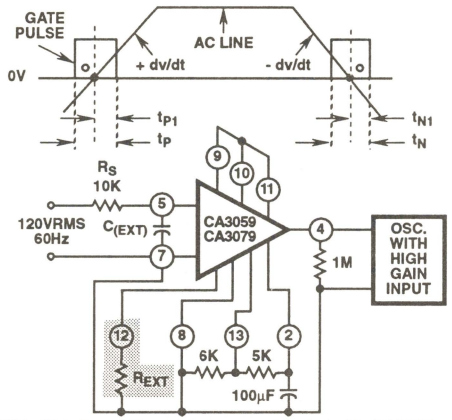


FIGURE 6B. INPUT INHIBIT VOLTAGE RATIO vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079



NOTE: Circuitry within shaded area not included in CA3079. All resistance values are in Ω

FIGURE 7A. GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM FOR CA3059 AND CA3079

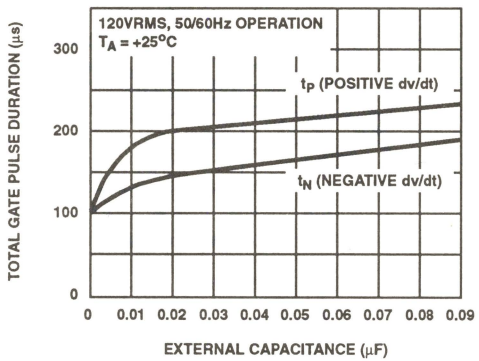


FIGURE 7B. TOTAL GATE PULSE DURATION vs EXTERNAL CAPACITANCE FOR CA3059 AND CA3079

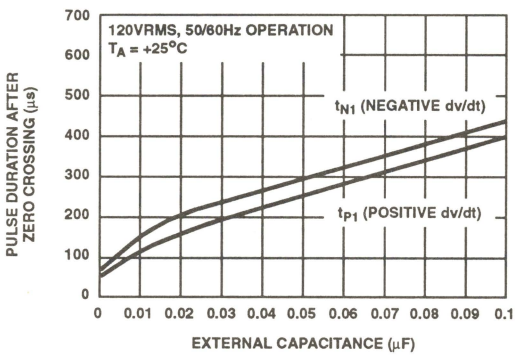


FIGURE 7C. PULSE DURATION AFTER ZERO CROSSING vs EXTERNAL CAPACITANCE FOR CA3059 AND CA3079

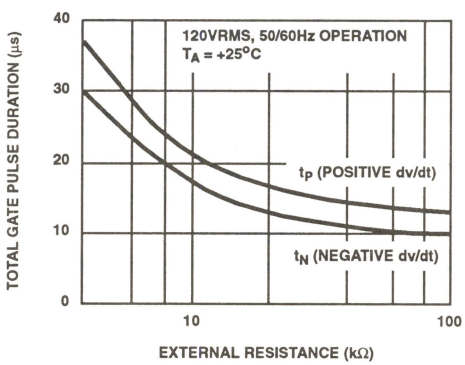


FIGURE 7D. TOTAL GATE PULSE DURATION vs EXTERNAL RESISTANCE FOR CA3059

FIGURE 7.

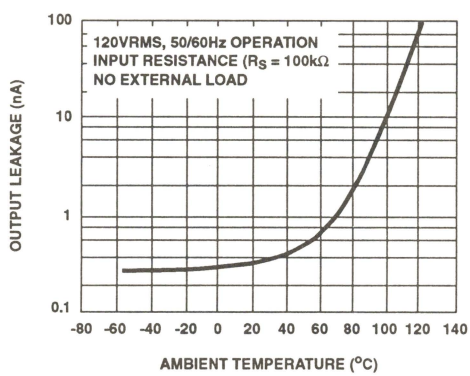


FIGURE 8. OUTPUT LEAKAGE CURRENT (INHIBIT MODE) vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

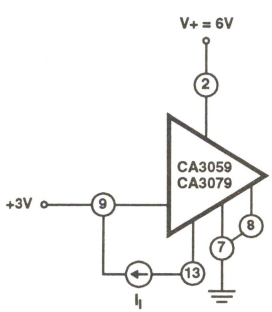


FIGURE 9. INPUT BIAS CURRENT TEST CIRCUIT FOR CA3059 AND CA3079

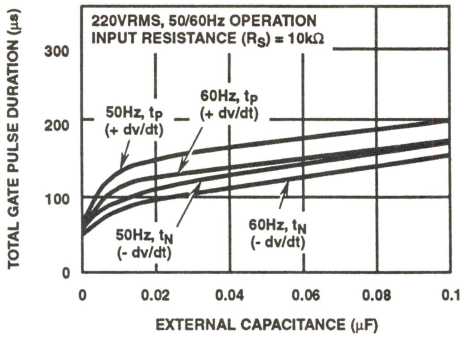


FIGURE 10A.

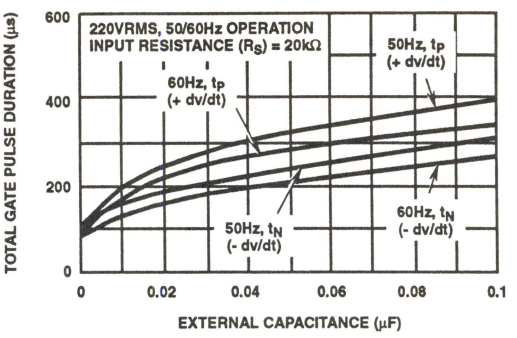


FIGURE 10B.

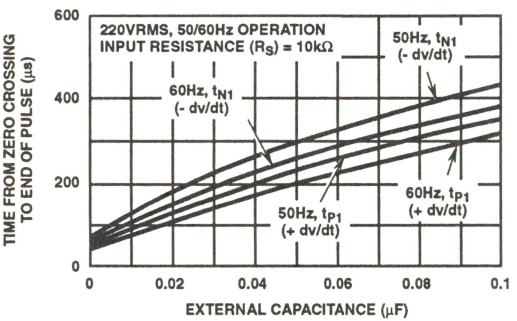


FIGURE 10C.

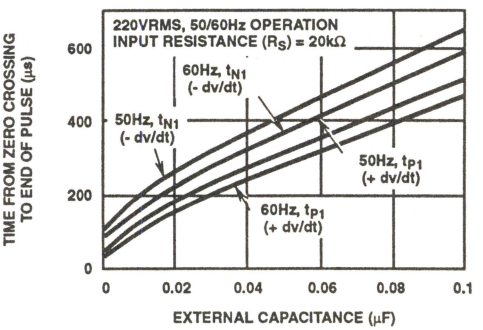


FIGURE 10D.

FIGURE 10. RELATIVE PULSE WIDTH AND LOCATION OF ZERO CROSSING FOR 220V OPERATION FOR CA3059 AND CA3079

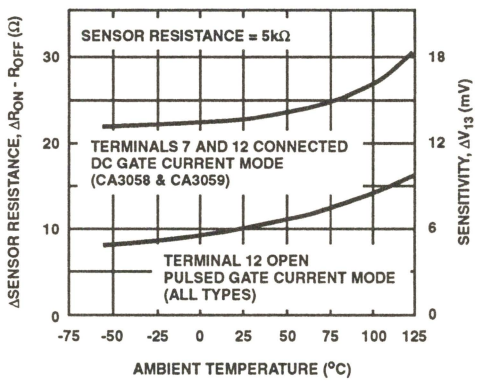


FIGURE 11. SENSITIVITY vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

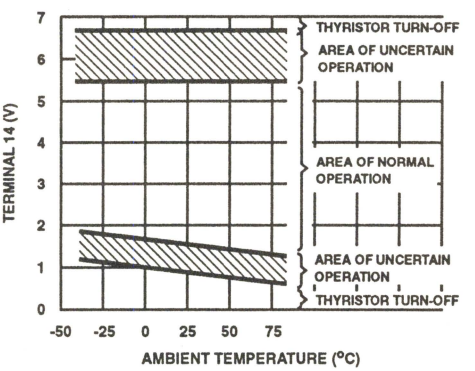
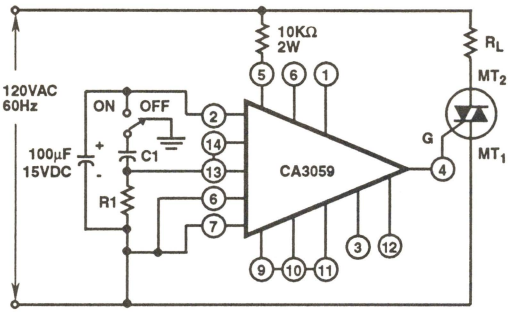


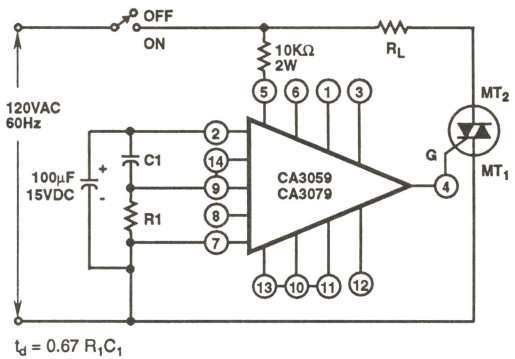
FIGURE 12. OPERATING REGIONS FOR BUILT-IN PROTECTION CIRCUIT FOR CA3059



$t_{ON} = 0.67\ R_1C_1$

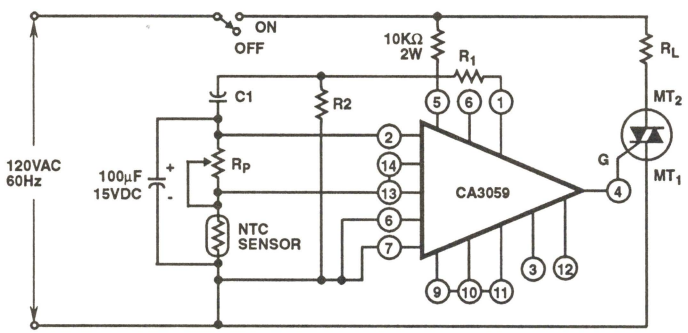
R_1(max. value allowable) = 1mΩ

FIGURE 13. LINE-OPERATED ONE-SHOT TIMER



$t_d = 0.67\ R_1C_1$

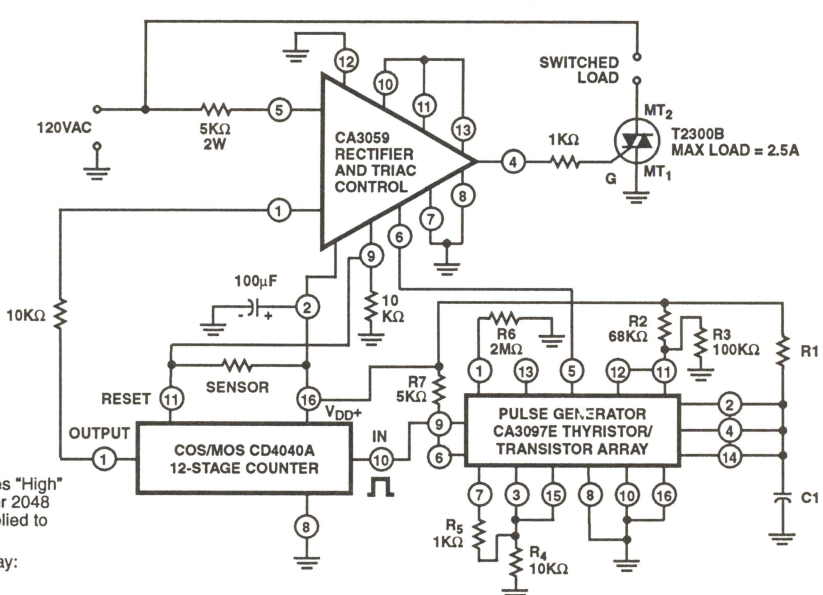
FIGURE 14. LINE-OPERATED THYRISTOR CONTROL TIME DELAY TURN-ON CIRCUIT



$t_d = R_TC_1$

$$R_T = \frac{R_1R_2}{R_1 + R_2}$$

FIGURE 15. ON/OFF TEMPERATURE CONTROL CIRCUIT WITH DELAYED TURN-ON



NOTE:

Terminal 1 goes "High" (Logic "1") after 2048 pulses are applied to Terminal 10.

For 8 hour delay:

$R_1 = 12M\Omega$

$C_1 = 2\mu F$

FIGURE 16A. LINE-OPERATED IC TIMER FOR LONG TIME PERIODS

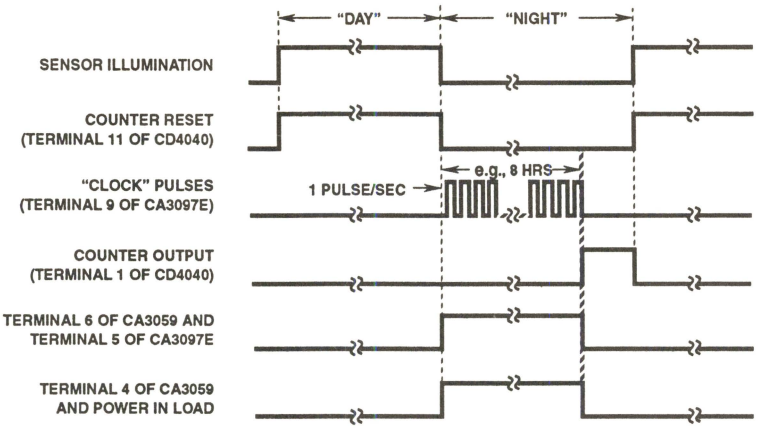


FIGURE 16B. TIMING DIAGRAM FOR FIGURE 16A

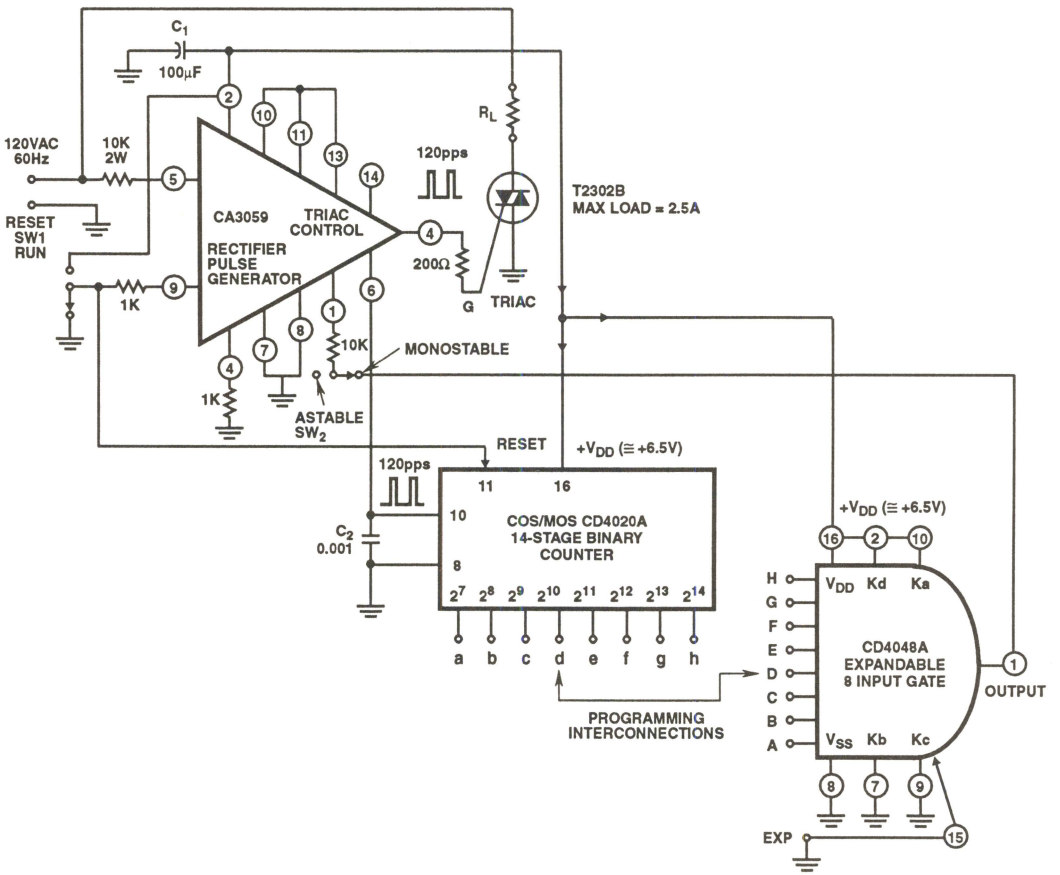


FIGURE 17A. PROGRAMMABLE ULTRA-ACCURATE LINE-OPERATED TIMER.

TIME PERIODS (t = 0.5333 s)								
1t	2t	4t	8t	16t	32t	64t	128t	t_O
CD4020A TERMINALS								
a	b	c	d	e	f	g	h	
CD4048A TERMINALS								
A	B	C	D	E	F	G	H	
C	NC	NC	NC	NC	NC	NC	NC	1t
NC	C	NC	NC	NC	NC	NC	NC	2t
C	C	NC	NC	NC	NC	NC	NC	3t
NC	NC	C	NC	NC	NC	NC	NC	4t
C	NC	C	NC	NC	NC	NC	NC	5t
NC	C	C	NC	NC	NC	NC	NC	6t
C	C	C	NC	NC	NC	NC	NC	7t
NC	NC	NC	C	NC	NC	NC	NC	8t
C	NC	NC	C	NC	NC	NC	NC	9t
NC	C	NC	C	NC	NC	NC	NC	10t
C	C	NC	C	NC	NC	NC	NC	11t
NC	NC	C	C	NC	NC	NC	NC	12t
C	NC	C	C	NC	NC	NC	NC	13t
NC	C	C	C	NC	NC	NC	NC	14t
C	C	C	C	NC	NC	NC	NC	15t
C	C	C	C	NC	C	C	NC	111t
NC	NC	NC	NC	C	C	C	NC	112t
C	NC	NC	NC	C	C	C	NC	113t
C	C	C	C	C	C	C	C	255t

NOTES:

1. t_O = Total time delay = $n_1\ t + n_2\ t + \ldots\ n_n t$.
2. C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.
3. NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to $+V_{DD}$ bus.

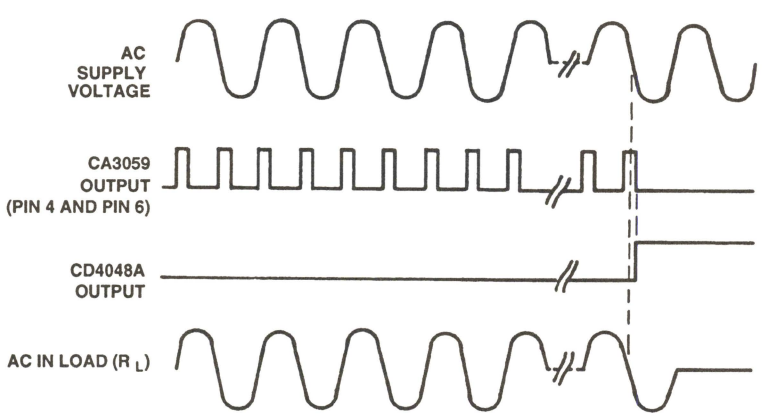


FIGURE 17B. "PROGRAMMING" TABLE FOR FIGURE 17(A).

Operating Considerations

Power Supply Considerations for CA3059 and CA3079

The CA3059 and CA3079 are intended for operation as self-powered circuits with the power supplied from and AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figures 2(b) and 2(c).

Power Supply Considerations for CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Figure 4 for the peak output current characteristics.) When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Figure 5(a).

Operation of Built-In Protection for the CA3059

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in the Functional Block Diagram. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2mA with a 5kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2kΩ and 100kΩ
3. The ratio of R_X to R_P typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

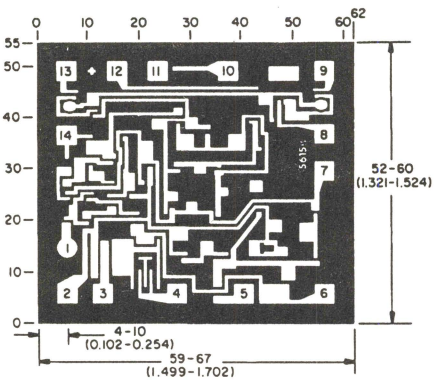
If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Figure 12.

External Inhibit Function for the CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2V at 10μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is par of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

DIMENSIONS AND PAD LAYOUT FOR CA3059H AND CA3079H

HARRIS SEMICONDUCTOR

HV-2405E

World-Wide Single Chip Power Supply

April 1994

Features

- Direct AC to DC Conversion
- Wide Input Voltage Range.....15Vrms-275Vrms
- Dual Output Voltages Available
- Output Current..... up to 50mA
- Output Voltage.....5V to 24V
- Line and Load Regulation..... <2%
- UL Recognition, File # E130808

Applications

- Power Supply for Non-Isolated Applications
- Power Supply for Relay Control
- Dual Output Supply for OFF-LINE Motor Controls
- Housekeeping Supply for Switch-Mode Power Supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HV3-2405E-5	0°C to +75°C	8 Lead Plastic DIP
HV3-2405E-9	-40°C to +85°C	8 Lead Plastic DIP

Description

The HV-2405E is a single chip off line power supply that converts world wide AC line voltages to a regulated DC voltage. The output voltage is adjustable from $5V_{DC}$ to $24V_{DC}$ with an output current of up to 50mA. The HV-2405E can operate from input voltages between 15Vrms and 275Vrms as well as input frequencies between 47Hz to 200Hz (see Table 1 in section titled "Minimum Input Voltage vs Output Current" for details).

The wide input voltage range makes the HV-2405E an excellent choice for use in equipment which is required to operate from either 240V or 120V. Unlike competitive AC-DC convertors, the HV-2405E can use the same external components for operation from either voltage. This flexibility in input voltage, as well as frequency, enables a single design for a world wide supply.

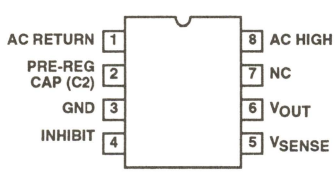
The HV-2405E has a safety feature that monitors the incoming AC line for large dv/dt (i.e. random noise spikes on AC line, initial power applied at or near peak line voltage). This inhibit function protects the HV-2405E, and subsequent circuitry, by turning off the HV-2405E during large dv/dt transients.This feature is utilized to ensure operation within the SOA (Safe Operating Area) of the HV-2405E.

The HV-2405E can be configured to work directly from an electrical outlet (see Figure 1) or imbedded in a larger system (see Figure 7). Both application circuits have components that will vary based on input voltage, output current and output voltage. It is important to understand these values prior to beginning your design.

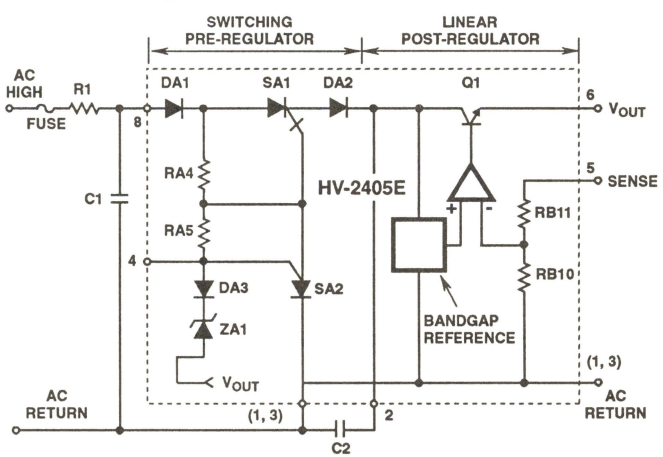
CAUTION: This Product Does Not Provide Isolation From The AC line. See "General Precautions". Failure to use a properly rated fuse may cause R1 to reach dangerously High Temperature or Cause the HV-2405E to Crack or Explode.

Pinout

HV-2405E (PDIP)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2487.5**

Absolute Maximum Ratings

Voltage Between Pin 1 and 8, Peak ..... ±500V
Voltage Between Pin 2 and 6 ..... 15V
Input Current, Peak 2A
Output Current 100mA
Output Voltage 34V

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP ..... 150°C/W
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C

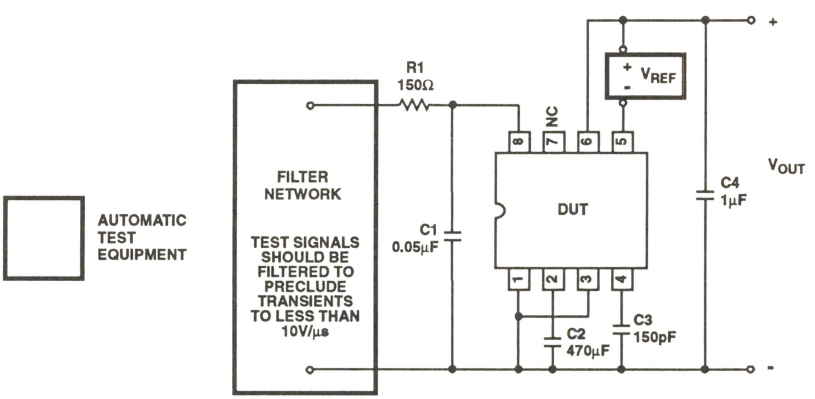
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Unless Otherwise Specified: V_{IN} = 264Vms at 50Hz, C1 = 0.05µF, C2 = 470µF, C4 = 1µF, V_{OUT} = 5V, I_{OUT} = 50mA, Source Impedance R_1 = 150Ω. Parameters are Guaranteed at the Specific V_{IN} and Frequency Conditions, Unless Otherwise Specified. See test circuit for Component Location.

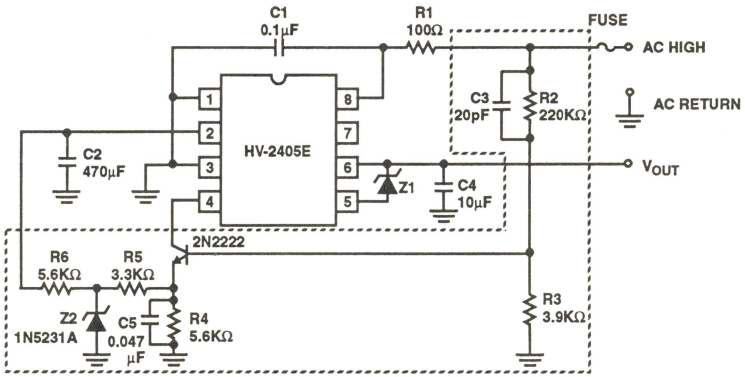
PARAMETER	CONDITIONS	TEMP	HV-2405E-5/-9			UNITS
			MIN	TYP	MAX	
Output Voltage (At Preset 5V)	V_{REF} = 0V_{DC}	+25°C	4.75	5.0	5.25	V
		Full	4.65	5.0	5.35	V
Output Voltage (At Preset 24V)	V_{REF} = 19V_{DC}	+25°C	22.8	24.0	25.2	V
		Full	22.32	24.0	25.68	V
Line Regulation	80Vrms to 264Vrms	+25°C	-	10	20	mV
		Full	-	15	40	mV
Load Regulation	(I_{OUT} = 5mA to 50mA)	+25°C	-	-	20	mV
		Full	-	-	40	mV
Output Current		Full	50	-	-	mA
Output Ripple (Vp-p)		Full	-	24	-	mV
Short Circuit Current Limit		Full	-	70	-	mA
Output Voltage TC		Full	-	0.02	-	%/°C
Quiescent Current Post Regulator	11V_{DC} to 30V_{DC} on Pin 2	+25°C	-	2	-	mA

Test Circuit



Application Information

OPERATING CONDITIONS
V_{IN} = 50Vrms TO 275Vrms
FREQUENCY = 50Hz to 60Hz
I_{OUT} = 0mA to 50mA
V_{OUT} = 5V + V_{Z1}



COMPONENT LIST

FUSE = 1/ 4A
R1 = 100Ω, 5W
R2 = 220kΩ, 1W
R3 = 3.9kΩ, 1/4W
R4 = 5.6kΩ, 1/ 4W
R5 = 3.3Ω, 1/ 4W
R6 = 5.6kΩ, 1/4 W

C1 = 0.1µF, AC RATED
C2 = 470µF, 15V + V_{OUT}, ELECTROLYTIC
C3 = 20pF, CERAMIC
C4 = 10µF, V_{OUT} + 10V, ELECTROLYTIC
C5 = 0.047µF, 10V
Z1 = V_{OUT} - 5V, 1/4W
Z2 = 5.1V, 1N5231/A OR EQUIVALENT
Q1 = 2N2222 OR EQUIVALENT

FIGURE 1. OFF LINE WORLD-WIDE SUPPLY ($I_{OUT} \geq$ 50mA)

Off line World Wide Supply ($I_{OUT} \leq$ 50mA)

Figure 1 shows the recommended application circuit for an off line world wide supply. The circuit will deliver an output voltage of 5V to 24V and an output current from 0 to 50mA. The value of C2 can be reduced for applications requiring less output current (see section titled "Optimizing Design" for details). For a basic understanding of the internal operation of the HV-2405E reference section titled "How the HV-2405E Works".

The following is a detailed explanation of this application circuit:

Basic Operation

When the input voltage goes positive an internal switch connects pin 8 to pin 2 allowing current to flow through R1 to charge up C2. When the voltage on C2 reaches a predetermined voltage the switch opens and the charging of C2 stops. R1 limits the input current and along with C1 provides a snubber for the internal switch. A linear regulator takes current from C2 further regulating the voltage and limiting the ripple at pin 6. The voltage at pin 6 is equal to V_{Z1} +5V. The linear regulator also provides output current limiting. The capacitor C4 on pin 6 is required for stability of the output.

Input Current Limiting Circuit

The external components in the shaded area of Figure 1 perform two functions. The first is to shut down the HV-2405E in the presences of a large voltage transients and the second is to provide input current limiting.

Resistors R2, R3 and capacitor C3 monitor the input voltage and turn on Q1 which shuts down the HV-2405E when the input voltage or the dv/dt is too large. This network anticipates the voltage applied to pin 8, since R1 and C1 add several micro seconds delay, and turns off the HV-2405E when a predetermined input voltage is exceeded. The difference between R3/C3 and R1/C1 time constants ensures that the HV-2405E internal switch opens before the voltage, and thereby the input current, is allowed to rise to a dangerous level at pin 8.The input voltage at which the HV-2405E is turned off, is dependent upon the voltage on C2. The higher the voltage on C2 the larger the input current that the HV-2405E can safely turn off. For a detailed explanation of why the voltage on C2 determines the maximum input current that the HV-2405E can safely turn off, reference "Start-up" in section titled "How the HV-2405E Works".

Input current limiting is provided when the voltage at the base of Q1 forward biases the base to emitter junction, turning off the internal switch. The voltage required at the base to turn on Q1 increases as the voltage on C2 increases the emitter voltage. When the voltage on C2 is >10V, the emitter voltage is held constant by Z2 and the maximum input current is set by resistors R2, R3, R4 and R5 (see section titled "Design Equations" for more details).

Operation

The circuit in Figure 1 ensures operation within the SOA of the HV-2405E by limiting the input current to <500mA when the voltage on C2 equals zero and <2A when the voltage on

Application Information (Continued)

C2 is greater than 10V. The circuits operation is illustrated in Figure 2 and Figure 3. In Figure 2 the initial current pulse is approximately 400mA when V_{C2} = 0V and gradually increases to approximately 1.8A when C2 = 10V. Also notice that after the 17th line cycle the input current is approximately 1.4A. At this point C2 is fully charged. The input current required to maintain the voltage on C2 is less than the current to charge it and the circuit has reached steady state operation. Since the steady state current is less than the input current limit, the circuit in the shaded area is off and no longer has any effect.

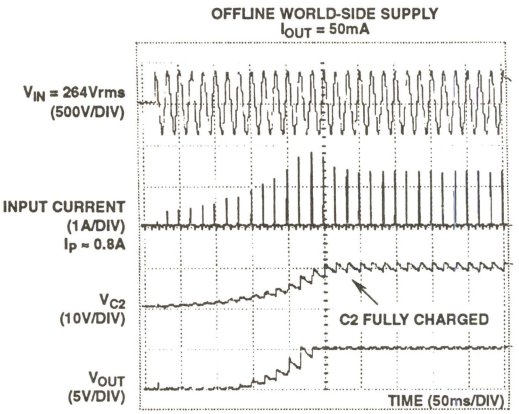


FIGURE 2. START UP OPERATION

Under short circuit operation the maximum voltage on pin 2 is less than 10V and the input current limiting circuit is invoked. Figure 3 shows that under output short circuit conditions, the input current is limited to about 800mA. The effects on the output current when the input current limiting circuit is invoked is illustrated in Figure 6.

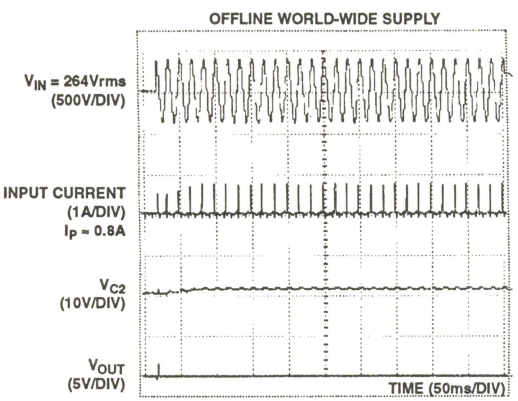


FIGURE 3. SHORT CIRCUIT OPERATION

Design Equations for Input Current Limiting

Initial Start-Up

Assume: V_{C2} = 0V, R1 = 100Ω, R2 = 220kΩ, R3 = 3.9kΩ, R4 = 5.6kΩ, R5 = 3.3kΩ, R6 = 5.6kΩ, V_{BE} = 0.54V, I_{TRIG} = 60µA, $V_{Pin\ 8}$ - $V_{Pin\ 2}$ = 3.5V at low inputs currents. V_{IN1} = Voltage on AC high when input current limit circuit is invoked (V_{C2} = 0V)

$$I_{IN(min)} = \frac{V_{IN1} - V_{Pin\ 8} - V_{Pin\ 2}}{R1} \quad \text{(EQ 1)}$$

$$V_{IN1} = \frac{R2 + R3}{R3}\left(V_{BE} + \frac{R4\,(R5 + R6)}{R4 + R5 + R6} \times I_{TRIG}\right) \quad \text{(EQ. 2)}$$

$$V_{IN1} = 57.41\,(0.54 + 3.437k\Omega \times 60\mu A) = 42.84V \quad \text{(EQ. 3)}$$

$$I_{IN(min)} = \frac{42.84 - 3.5}{100} = 393mA \quad \text{(EQ. 4)}$$

Equation 1 through Equation 4, for the given assumptions, predict that the initial input current will be limited to 393mA.

The following equations can be used to predict the maximum input current during start-up.

Assume: V_{C2} > 10V, R1 = 100Ω, R2 = 220kΩ, R3 = 3.9kΩ, R4 = 5.6kΩ, R5 = 5.6kΩ, R6 = 3.3kΩ, V_{BE} = 0.54V, I_{TRIG} = 60µA, V_Z = 5.1V, $V_{Pin\ 8}$ - $V_{Pin\ 2}$ = 6V at high inputs currents, $V_{Pin\ 2}$ - $V_{Pin\ 6}$, V_{IN2} = Voltage on AC high when input current circuit is invoked (V_{C2} > 10V).

$$I_{IN(max)} = \frac{V_{IN2} - V_{OUT} - (V_{Pin\ 8} - V_{Pin\ 2}) - (V_{Pin\ 2} - V_{Pin\ 6})}{R1} \quad \text{(EQ. 5)}$$

$$V_{IN2} = \frac{R2 + R3}{R3}\left[\left(V_{BE} + \frac{R4\ R5}{R4 + R5} \times I_{TRIG} + \frac{R4}{R4 + R5}V_{Z2}\right)\right] \quad \text{(EQ. 6)}$$

$$V_{IN2} = 57.41\,[0.54 + (2.076k\Omega \times 60\mu A) + (0.6292 \times 5.1)] \quad \text{(EQ. 7)}$$

$$I_{IN(max)} = \frac{222 - V_{OUT} - 6 - 6}{100} = 2.05A \text{ at } V_{OUT} = 5V \quad \text{(EQ. 8)}$$

$$I_{IN(max)} = \frac{222 - V_{OUT} - 6 - 6}{100} = 1.86A \text{ at } V_{OUT} = 24V \quad \text{(EQ. 9)}$$

Equation 5 through Equation 9 predict the maximum input current will be limited to less than 2.05A. In practice at 5V operation the current is less than predicted due to the low bias current through Z2.

Setting The Output Voltage

The circuit shown in Figure 1 provides a regulated 5V to 24V DC and is set by adjusting the value of Z1. The output voltage of the HV-2405E (pin 6) is set by feedback to the sense pin (pin 5). The output will rise to the voltage necessary to keep the sense pin at 5V. The output voltage is equal to the Zener voltage (V_{Z1}) plus the 5V on the sense pin. For a 5V output, pin 5 and pin 6 would be shorted together. The output voltage has the accuracy and tolerance of both the Zener diode and the band-gap of the HV-2405E (see Figure 16). The maximum output voltage is limited by Z_{B2} to ≈ $34V_{DC}$. Z_{B2} protects the output by ensuring that an overvoltage condition does not exist. Note: the output voltage can also be set by placing a resistor (1/4W) between pin 5 and pin 6. If a resistor is placed between pin 5 and pin 6 an additional 1V per kΩ (±10%) is added to the 5V output.

Application Information (Continued)

Optimizing Design (World-Wide Supply)

Selecting the Storage Capacitor C2

For applications requiring less than 50mA or the full input voltage range, the value of C2 can be reduced for a more cost effective solution. The minimum C2 capacitor value is determined by the intersection between the maximum input voltage and the output current curve in Figure 4. (Note, for 50Hz operation see Figure 19 in section titled "Typical Performance Curves".) Advantages of making C2 as small as possible are:

- Reduced total size and cost of the circuit.
- Reduced start up time.

Consideration should be given to the tolerance and temperature coefficient of the C2 value selected. (Note; momentary peak output current demands should be considered in the sizing of C2. Increasing the output capacitor C4 is another way to supply momentary peak current demands.)

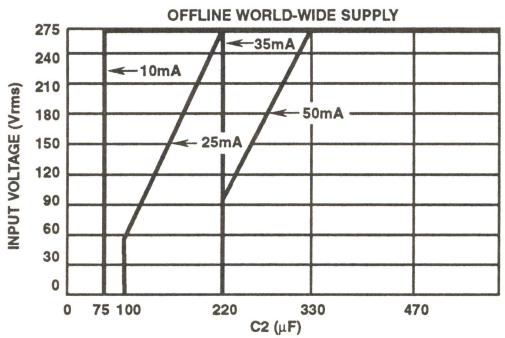


FIGURE 4. MINIMUM C2 VALUE vs INPUT VOLTAGE

The following example illustrates the method for determining the minimum C2 value required:

EXAMPLE

Requirements: V_{OUT} = 5V to 24V, I_{OUT} = 35mA, $V_{IN(max)}$ = 120Vrms, 60Hz.

For the given conditions, the minimum C2 value (from Figure 4) is determined to be 220µF.

Determining the Power Dissipation in R1

Circuit efficiency is limited by the power dissipation in R1. The power dissipation for 240Vrms and 120Vrms is shown in Figure 5.

For input voltages other than 240Vrms or 120Vrms equation 10 can be used to determine the power dissipation in R1.

$$Pd = 2.8 \sqrt{R1\ Vrms\ (I_{OUT})^3} \qquad \text{(EQ. 10)}$$

Example: R_1 = 100Ω, Input Voltage = 240Vrms, I_{OUT} = 50mA, P_D = 4.8W

NOTE: Under short circuit conditions the P_D in R1 decreases to 1.2W Due to fold back current limiting (I_{OUT} = 20mA, Reference Figure 6).

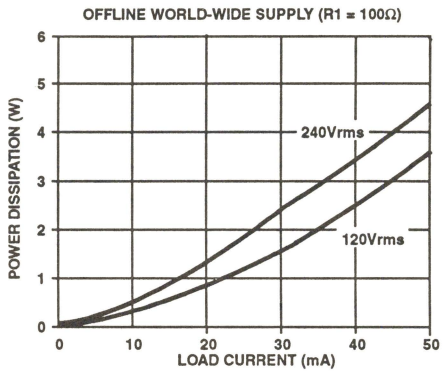


FIGURE 5. POWER DISSIPATION IN R1 vs LOAD CURRENT

Operation Information

Effects of Temperature on Output Current:

Figure 6 shows the effects of temperature on the output current for the circuit shown in Figure 1. Figure 6 illustrates operation with the output configured for 5V. Temperature effects on the output current for V_{OUT} = 24V operation is similar. The foldback current limiting is the result of reduced voltage on C2. The circuit delivers 50mA output current across the specified temperature range of -40°C to +85°C for all output voltages between 5V and 24V. The effect of decreasing the value of C2 (470µF) reduces the maximum output current (i.e. moves curve to the left). For all C2 values selected from Figure 4 (assuming tolerance and temperature coefficient are taken into account) the circuit meets the expected output current across the above mentioned temperature range.

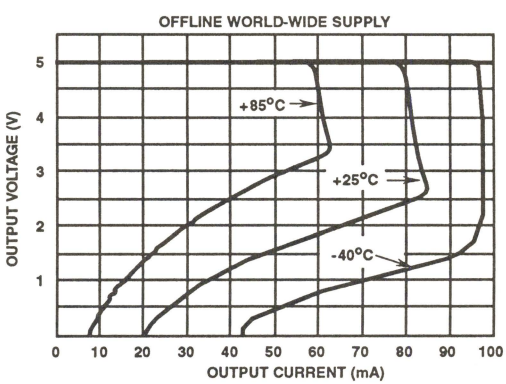


FIGURE 6. OUTPUT CURRENT vs TEMPERATURE

Application Information (Continued)

Minimum Input Voltage vs I_{OUT}

Table 1 shows the minimum input voltage range as a function of output current. Notice that the HV-2405E can deliver 5V at 10mA from a source voltage as little as 15Vrms and requires a minimum of 50Vrms to deliver 24V at 50mA.

TABLE 1. MINIMUM INPUT VOLTAGE vs OUTPUT CURRENT

	I_{OUT}			
V_{OUT}	10mA	25mA	35mA	50mA
5V	15Vrms	21Vrms	25Vrms	30Vrms
24V	31Vrms	38Vrms	41Vrms	50Vrms

Component List (World Wide Supply <50mA)

Fuse

Opens the connection to the power line.

Recommended value: 1/4AG

R1 Source Resistor

R1 limits the input current into the HV-2405E. Needs to be large enough to limit inrush current when C2 is discharged fully. The maximum inrush current needs to be limited to less than 2A (V peak / R1 <2A). The equation for power dissipation in R1 is:

$$Pd = 2.8 \sqrt{R1\ Vrms\ (I_{OUT})^3} \qquad \text{(EQ. 10)}$$

Wirewound resistors are recommended due to their superior temperature characteristics.

R1 = 100Ω (±10%)

R2, R3, R4, R5 and R6 Resistors

R2, R3, R4, R5 and R6 set the bias level for Q1 that establishes the minimum and maximum input current limit during start-up.

Resistor values (±5%):

R2 = 220kΩ, 1W
R3 = 3.9kΩ, 1/4W
R4 = 5.6kΩ, 1/4W
R5 = 3.3kΩ, 1/4W
R6 = 5.6kΩ, 1/4W

C1 Snubber Capacitor

C1 and R1 form a low pass filter that limits the voltage rate of rise across SA1 (the main current carrying SCR of the HV-2405E) and therefore its power dissipation.

C1 = 0.1µF (±10%) AC rated, metallized polyester.

C2 Pre-Regulator Capacitor

C2 is charged once each line cycle. The post regulator section of the HV-2405E is powered by C2 for most of the line cycle. If the application requires a smaller input voltage, the value of C2 can be reduced from that shown in Figure 1 (see section on "Optimizing Design" for details). Note: capacitors with high ESR may not store enough charge to maintain full load current. The voltage rating of C2 should be about 10V greater than the selected V_{OUT}.

Recommended value = 470µF electrolytic (±20%), unless otherwise specified.

C3 Feed Forward Capacitor

C3 is part of the input Current limiting circuitry shown in Figure 1. C3 detects large voltage transients on the AC line and turns off the HV-2405E by turning Q1 on.

C3 = 20pF (20%), breakdown voltage >500V.

C4 Output Filter Capacitor

C4 is required to maintain the stability of the output stage. Larger values may help in supplying short momentary current peaks to the load and improve output ripple during start-up.

C4 = 10µF (±20%)

Z1 Output Voltage Adjust

Z1 is used to set the output voltage above the 5V reference on pin 5 (see section titled "Setting The Output Voltage" for more details).

Z1= V_{OUT} - 5V,1/4W. V2 valve at 1mA.

Note, the wattage rating is different when configured as a dual supply (see dual supply section for on how to determine wattage).

Z2 Clamp Diode

Z2 clamps the voltage on Q1s emitter when the voltage on C2 >10V. This results in limiting the maximum input current to less than 2A.

Z2 = 5.1V, 1N5231A or equivalent

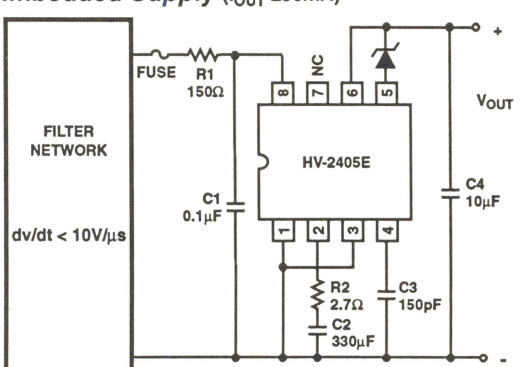
Q1 Input Current Limiting Transistor

Q1 shuts down the HV-2405E when the input voltage or dv/dt is too large.

V_{CEO} = 40V min.

Q1 = 2N2222 or equivalent

Imbedded Supply (I_{OUT} ≤30mA)



COMPONENT LIST

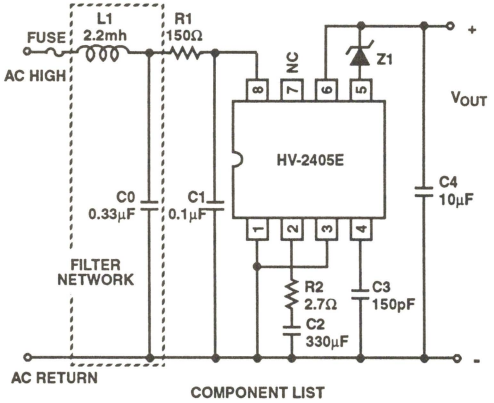
FUSE = 1/4A
R1 = 150Ω, 3W
R2 = 2.7Ω, 1/4W
C1 = 0.1µF, AC RATED
C2 = 330µF, 15V + V_{OUT}, ELECTROLYTIC
C3 = 150pF, CERAMIC
C4 = 10µF, V_{OUT} + 10V, ELECTROLYTIC
Z1 = V_{OUT} -5V, 1/4W

FIGURE 7. IMBEDDED SUPPLY I_{OUT} ≤ 30mA

Application Information (Continued)

For applications requiring 30mA or less and not directly off line (i.e. filter network preceding supply), the external transistor and associated resistors in Figure 1 can be replaced with a single 1/4W resistor R2 and capacitor C3 (Figure 7) if: (1) The filter network reduces the input dv/dt to less than 10V/μs (ensures sufficient pin 2 voltage at turn off), (2) Source resistor R1 equals 150Ω (limits the maximum input current) and (3) Inhibit Capacitor C3 equals 150pF (turns off the HV-2405E during large voltage transients).

For applications where EMI (conductive interference) is a design requirement, the circuit shown in Figure 8 is the recommended application circuit. This circuit delivers an output voltage of 5V to 24V with an output current from 0 to 30mA and passes VDE 0871 class "B" test requirements for conductive interference with a resistive load.



COMPONENT LIST

FUSE = 1/ 4A	C3 = 150pF, CERAMIC
R1 = 150Ω, 3W	C4 = 10μF, V_{OUT} + 10V, ELECTROLYTIC
R2 = 2.7Ω, 1/4W	Z1 = V_{OUT} -5V, 1/4W
C1 = 0.1μF, AC RATED	L1 = 2.2mh, μ = 2000
C2 = 330μF, 15V + V_{OUT}, ELECTROLYTIC	C0 = 0.33μF, AC RATED

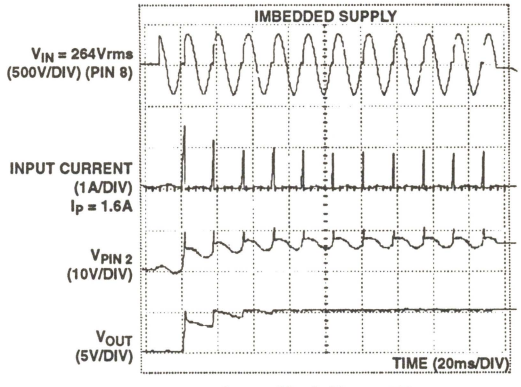
FIGURE 8. IMBEDDED SUPPLY WITH EMI FILTER ($I_{OUT} \leq 30mA$)

Basic Operation

When power is initially applied the filter network reduces the magnitude of any transient noise spikes that might result in operation outside the SOA of the HV-2405E (see Start-up in section titled "How the HV-2405E Works" for and explanation of the SOA). When the voltage on pin 8 goes positive an internal switch connects pin 8 to pin 2 and C2 starts to charge through R1 and R2. When the voltage on pin 2 reaches a predetermined voltage the switch opens and the charging of C2 stops. R1 limits the input current and along with C1 provides a snubber for the internal switch. R2 also has the effect of limiting the input current by increasing the voltage on pin 2 sooner in the cycle. A linear regulator takes current from C2 and provides a DC voltage at pin 6. The voltage at pin 6 is equal to V_{Z1}+ 5V. The inhibit capacitor (C3) provides protection from large input voltage transients by turning off the HV-2405E and the output capacitor C4 provides stabilization of the output stage.

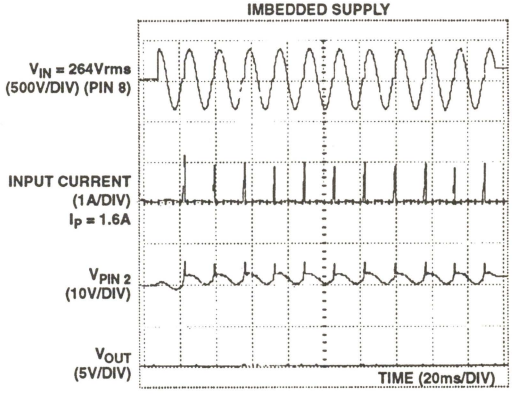
Operation

The operation of the imbedded supply is illustrated in Figure 9 and Figure 10. Figure 9 shows operation with a 30mA load and Figure 10 with the output short circuited. Notice that In both cases, the inhibit function of the HV-2405E prevents the circuit from turning on when the input voltage was applied near the peak line voltage. Also notice the initial current pulse (Figure 9) is approximately 1.6A and decreased to 1A within 40ms. This decrease in the input current results when the charging current required to maintain the voltage on C2 decreased. The effect of the series resistor (R2) is illustrated by the small voltage spike on the Vpin 2 trace. This voltage spike increases the voltage on pin 2 to the 10V trip point sooner in the cycle, thereby limiting the input current.



I_{OUT} = 30mA, V_{OUT} = 5V

FIGURE 9. START UP OPERATION



OUTPUT SHORT CIRCUITED

FIGURE 10. SHORT CIRCUIT OPERATION

Application Information (Continued)

Setting The Output Voltage

The circuits shown in Figure 7 and Figure 8 provide a regulated 5V to 24V_{DC} output voltage that is set by adjusting the value of Z1. The output voltage of the HV-2405E (pin 6) is set by feedback to the sense pin (pin 5). The output will rise to the voltage necessary to keep the sense pin at 5V. The output voltage is equal to the Zener voltage (V_{Z1}) plus the 5V on the sense pin. For a 5V output, pin 5 and pin 6 would be shorted together. The output voltage has the accuracy and tolerance of both the Zener diode and the band-gap of the HV-2405E (see Figure 16). The maximum output voltage is limited by Z_{B2} to $\approx 34V_{DC}$. Z_{B2} protects the output by ensuring that an overvoltage condition does not exist. Note: the output voltage can also be set by placing a resistor (1/4W) between pin 5 and pin 6. If a resistor is placed between pin 5 and pin 6 an additional 1V per kΩ (±10%) is added to the 5V output.

Optimizing Design (Imbedded Supply)

Selecting the storage capacitor C2

For applications requiring less than 30mA, the value of C2 can be reduced for a more cost effective solution. The minimum C2 capacitor value vs. output current is presented in Table 2. Advantages of making C2 as small as possible are:

- Reduced total size and cost of the circuit.
- Reduced start up time.

Consideration should be given to the tolerance and temperature coefficient of the C2 value selected. (Note: momentary peak output current demands should be considered in the sizing of C2. Increasing the output capacitor C4 is another way to supply momentary peak current demands.)

TABLE 2. IMBEDDED SUPPLY

R1 - 150Ω		R2 = 2.7Ω	
V_{IN}	FREQ.	C2	I_{OUT}
264Vrms	50Hz	330µF	30mA
		220µF	24mA
		100µF	14mA
		50µF	8mA
264Vrms	60Hz	330µF	30mA
		220µF	27mA
		100µF	16mA
		50µF	9mA
132Vrms	50Hz	330µF	30mA
		220µF	30mA
		100µF	16mA
		50µF	8mA
132Vrms	60Hz	330µF	30mA
		220µF	30mA
		100µF	16mA
		50µF	9mA

Determining the Power Dissipation in R1

Circuit efficiency is limited by the power dissipation in R1. The power dissipation for 240Vrms and 120Vrms is shown in Figure 11.

For input voltages other than 240Vrms or 120Vrms Equation 10 can be used to determine the power dissipation in R1.

$$Pd = 2.8 \sqrt{R1\ Vrms\ (I_{OUT})^3} \qquad \text{(EQ. 10)}$$

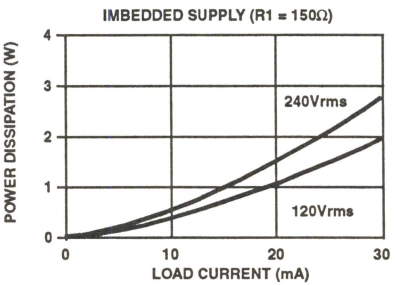


FIGURE 11. POWER DISSIPATION IN R1 vs LOAD CURRENT

Operation information

Effects of Temperature on Output Current

Figure 12 and Figure 13 show the effects of temperature on the output current for the imbedded supply (R2 = 2.7Ω). Figure 12 illustrates V_{OUT} = 5V operation and Figure 13 illustrates V_{OUT} = 24V operation. The imbedded supply (R2 = 2.7Ω) delivers 30mA output current across the specified temperature range of -40°C to +85°C for all output voltages between 5V and 24V. The effect of decreasing the value of C2 (330µF) reduces the maximum output current (i.e. moves curve to the left). For all C2 values selected from Table 2 (assuming tolerance and temperature coefficient are taken into account) the circuit meets the expected output current across the above mentioned temperature range.

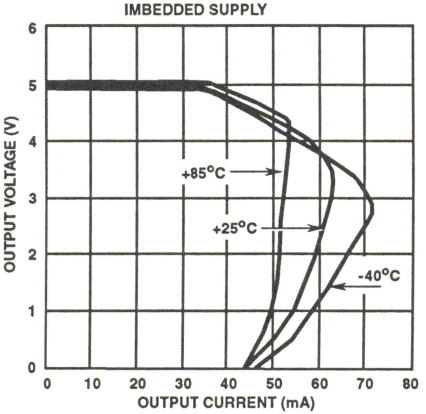


FIGURE 12. OUTPUT CURRENT vs TEMPERATURE (R1 = 150Ω, R2 = 2.7Ω, C2 = 330µF)

Application Information (Continued)

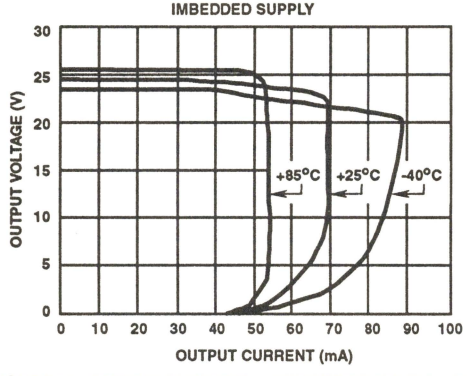


FIGURE 13. OUTPUT CURRENT vs TEMPERATURE (R1 = 150Ω, R2 = 2.7Ω, C2 = 330μF)

Component List (Imbedded Supply ≤30mA)

Fuse

Opens the connection to the power line should the system fail.

Recommended value: 1/4AG

R1 Source Resistor

R1 limits the input current into the HV-2405E. Needs to be large enough to limit inrush current when C2 is discharged fully. The maximum inrush current needs to be limited to less than 2A (Vpeak / R1 < 2A). The equation for power dissipation in R1 is:

$$Pd = 2.8 \sqrt{R1\ Vrms\ (I_{OUT})^3}$$

Wirewound resistors are recommended due to their superior temperature characteristics.

R1 = 150Ω (±10%)

R2 Series Resistor

R2 limits the input current by boosting the voltage on pin 2 sooner in the cycle.

R2 = 2.7Ω (5%), 1/4W

C1 Snubber Capacitor

C1 and R1 form a low pass filter that limits the voltage rate of rise across SA1 (the main current carrying SCR of the HV-2405E) and therefore its power dissipation.

C1 = 0.1μF (±10%) AC rated, metallized polyester.

C2 Pre-Regulator Capacitor

C2 is charged once each line cycle. The post regulator section of the HV-2405E is powered by C2 for most of the line cycle. If the application requires a smaller input voltage, the value of C2 can be reduced from that shown in Figure 7 or Figure 8 (see section on "Optimizing Design" for details. Note; capacitors with high ESR may not store enough charge to maintain full load current. The voltage rating of C2 should be about 10V greater than the selected V_{OUT}.

Recommended value = 330μF electrolytic (±20%),unless otherwise specified.

C3 Inhibit Capacitor

C3 keeps the HV-2405E from turning on during large input voltage transients.

C3 = 150pF (10%)

C4 Output Filter Capacitor

C4 is required to maintain the stability of the output stage. Larger values may help in supplying short momentary current peaks to the load and improves output ripple during start-up.

C4 = 10μF (±20%)

Z1 Output Voltage Adjust

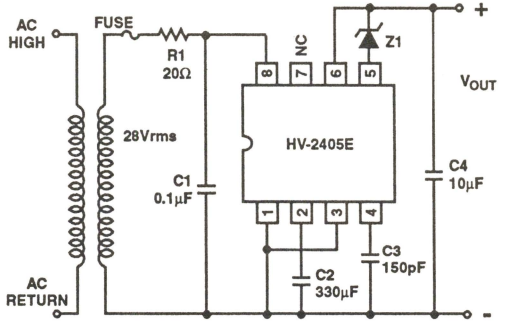
Z1 is used to set the output voltage above the 5V reference on pin 5 (see section titled "Setting The Output Voltage" for more details).

Z1 = V_{OUT} - 5V,1/4W

Note, the wattage rating is different when configured as a dual supply (see dual supply section for on how to determine wattage).

Low Input Voltage Supply (I_{OUT} <50mA)

An ideal application, taking advantage of the low voltage operation, would be thermostat controls were 28Vrms is supplied via a transformer. In this application the HV-2405E could deliver a regulated 5V at 40mA with a power dissipation in R1 (R1= 20Ω) equal to 530mw. The current limiting components, in Figure 1, are not required at this low input voltage level. See Figure 23 and Figure 24 for output vs temperature.



COMPONENT LIST

FUSE = 1/ 4A, OPTIONAL
R1 = 20Ω, 1W
C1 = 0.05μF, AC RATED
C2 = 330μF, 15V + V_{OUT}, ELECTROLYTIC
C3 = 150pF, CERAMIC
C4 = 10μF, V_{OUT} + 10V, ELECTROLYTIC
Z1 = V_{OUT} -5V, 1/4W

FIGURE 14. LOW INPUT VOLTAGE SUPPLY

Application Information (Continued)

COMPONENT LIST

FUSE = 1/ 2A
R1 = 100Ω, 5W
R2 = 220kΩ, 1W
R3 = 3.9kΩ, 1W
R4 = 5.6kΩ, 1/ 4W
R5 = 3.3Ω, 1/ 4W
R6 = 5.6kΩ, 1/4 W
C1 = 0.1μF, AC RATED
C2 = 470μF, 15V + V_{OUT}, ELECTROLYTIC
C3 = 20pF, CERAMIC
C4 = 10μF, V_{OUT} + 10V, ELECTROLYTIC
C5 = 0.047μF, 10V
Z1 = V_{OUT} - 5V, 1/4W
Z2 = 5.1V, 1N5231/A OR EQUIVALENT
Q1 = 2N2222 OR EQUIVALENT

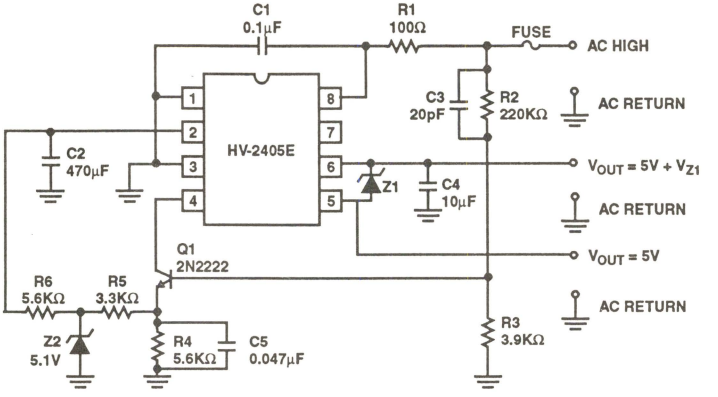


FIGURE 15. DUAL SUPPLY

Dual Supply (I_{OUT} <50mA)

Dual output voltages are available by making use of the 5V reference at pin 5. The sum of both supply currents must not exceed maximum output current limit of 50mA. The output current for the 5V supply is delivered from the output (pin 6) through the Zener diode. The wattage calculation for the Zener diode is given in Equation 11.

Wattage = (V pin 6 - V pin 5) (I_{OUT} pin 5) (EQ. 11)

General Precautions

CAUTION: This product does not provide isolation from the AC line. Failure to use a properly rated fuse may cause R1 to reach dangerously high temperatures or cause the HV-2405E to crack or explode.

Instrumentation Effects

Background:

Input to output parasitic exist in most test equipment power supplies. The inter-winding capacitance of the transformer may result in substantial current flow (mA) from the equipment ground wire to the AC and DC ground of the HV-2405E. This current can induce instability in the inhibit circuit of the HV-2405E resulting in erratic operation.

Recommendations for evaluation of the HV-2405E in the lab:

a). The use of battery powered DVMs and scopes will eliminate ground loops.

b). When connecting test equipment, locate grounds as close to pin 1 as possible.

c). Current measurements on the AC side of the HV-2405E (Pin 8, Pin 1 and Pin 2) should be made with a non-contact current probe.

If AC powered test equipment is used, then the use of an isolated plug is recommended. The isolated plug eliminates any voltage difference between earth ground and AC ground. However, even though the earth ground is disconnected, ground loop currents can still flow through transformer of the test equipment. Ground loops can be minimized by connecting the test equipment ground probe as close to pin 1 as possible.

Caution: Dangerous voltages may appear on exposed metal surfaces of AC powered test equipment.

AC Source Effects

Background:

Laboratory AC sources (such as VARIACs, step-up transformers etc.) contain large inductances that can generate damaging high voltage transients any time they are switched on or off. Switch arcing can further aggravate the effects of source inductance.

Recommendation:

Adequate protection means (such as MOV, avalanche diode, surgector, etc.) may be needed to clamp transients to within the ±500V input limit of the HV-2405E.

Output Short Circuited

For output voltages greater than 5V the maximum voltage rating from pin 2 to pin 6 (15V) could be exceeded. For a 24V output the voltage on pin 2 could be as high as 32V. Under normal operating conditions the voltage differential between pin 2 and pin 6 is maintained by DA3, DA4, DA5 and ZA1 (Figure 6) to about 6V. However, if the output (pin 6) is shorted to ground the potential difference would equal the voltage on C2 which would exceed the 15V max limit. (Note: if the output is shorted prior to initial power up, the voltage on C2 only reaches about 6.8V and therefore is not a problem.)

Recommendation:

If the possibility of the output being shorted to ground during normal operation exist, a 10V zener diode (cathode pin 2, anode pin 6) is recommended from pin 2 to pin 6.

Safe Operating Area

Ensure operation is within the SOA of the HV-2405E. Reference "Start-Up" in section titled "How the HV-2405E Works".

How The HV-2405E Works

Steady State Operation

The HV-2405E converts an AC voltage into a regulated DC voltage. This is accomplished in two functional sections (1) Switching Pre-Regulator and (2) Linear Voltage Regulator. Refer to HV-2405E schematic Figure 16.

The purpose of the Switching Pre-Regulator circuit is to capture energy from an incoming AC power line, 1/6 of every positive half cycle and store this energy in an electrolytic capacitor (C2). This energy is then transferred to the Linear Voltage Regulator.The current path for charging C2 is through DA1, SA1 and DA2. When the voltage level on C2 reaches approximately 6.8V above the output voltage, SA2 turns on turning off SA1 and the charging of C2 stops until the next positive half cycle on AC high. SA2 is triggered on when current flows out of SA2s anode gate and through the Zener diode stack (ZA1, DA3, DA4, DA5). This results in a feedback circuit that limits the peak voltage on pin 2.

The input voltage and current wave forms at pin 8 are illustrated in Photo 1. The operation of the HV-2405E is easily confirmed by noticing the clamping of the input voltage during the charging of C2. Photo 2 shows the voltage on C2 (bottom trace), along with the voltage on pin 8 as a reference. The test conditions for the wave forms are listed at the end of this section.

The Linear Voltage Regulator performs two functions. The first is to provide a reference voltage at pin 5 that is temperature independent and the second is to provide an output voltage on pin 6 that is adjustable from 5V to 24V. The band-gap (NB1, NB2, RB3 and RB4) provides a temperature independent reference voltage on the base of NB5. This reference voltage (1.21V) results in approximately 1mA through RB10 when the feedback loop from pin 6 is closed. The output voltage is adjusted by placing a Zener diode between pin 5 and pin 6. The output voltage on pin 6 is adjusted above the 5V reference on pin 5 by a value equal to the Zener voltage. The maximum output voltage is limited to ~ $34V_{DC}$ by the internal Zener diode Z_{B2}. Z_{B2} protects the output by ensuring that an overvoltage condition does not exist. The bottom trace of Photo 3 shows the output voltage ripple (worst case conditions), along with the voltage on pin 8 as a reference.

Test conditions for waveforms: T_A = +25°C, V_{AC} = 240Vrms, f = 50Hz, R1 = 150Ω, C1= 0.1µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V at 50mA.

Start-up

Start up operation is similar to that described above. Since the storage capacitor connected to pin 2 is discharged, the main SCR, SA1, has to pass more current than for steady state.

The ability of the second SCR, SA2, to turn off SA1 is a function of the voltage on C2. Due to the impedances of SA1 and SA2, the maximum input current that can be safely turned off decreases for C2 voltages below 5V. To understand why the voltage on C2 determines the maximum input current that the HV-2405E can safely turn off, its important to understand the electrical connection between SA1, SA2 and the storage capacitor C2. Figure 17(A) is a schematic representation of both SCRs and is presented to explain how SA2 turns off SA1.

Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Current into Pin 8, (0.5A/Div)

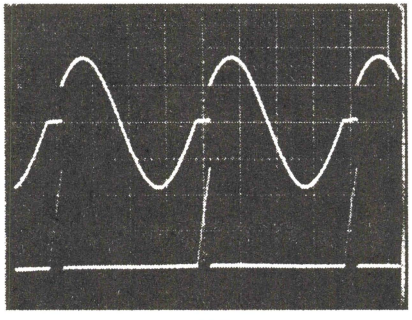


PHOTO 1

Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Pre-Regulator Capacitor Voltage, C2 (5V/Div) at Approximately $10V_{DC}$

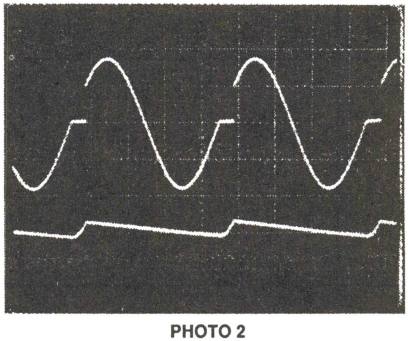


PHOTO 2

Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Ripple or Switch Spike on Regulator $5V_{DC}$ Output (50mV/Div) This is Worst Case Ripple (High Line Voltage, Maximum I_{OUT})

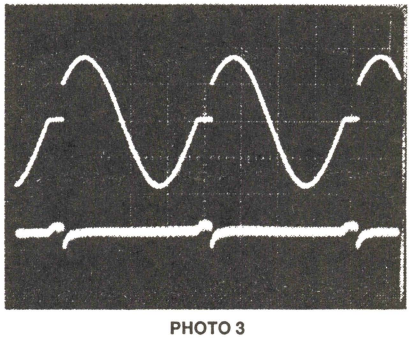


PHOTO 3

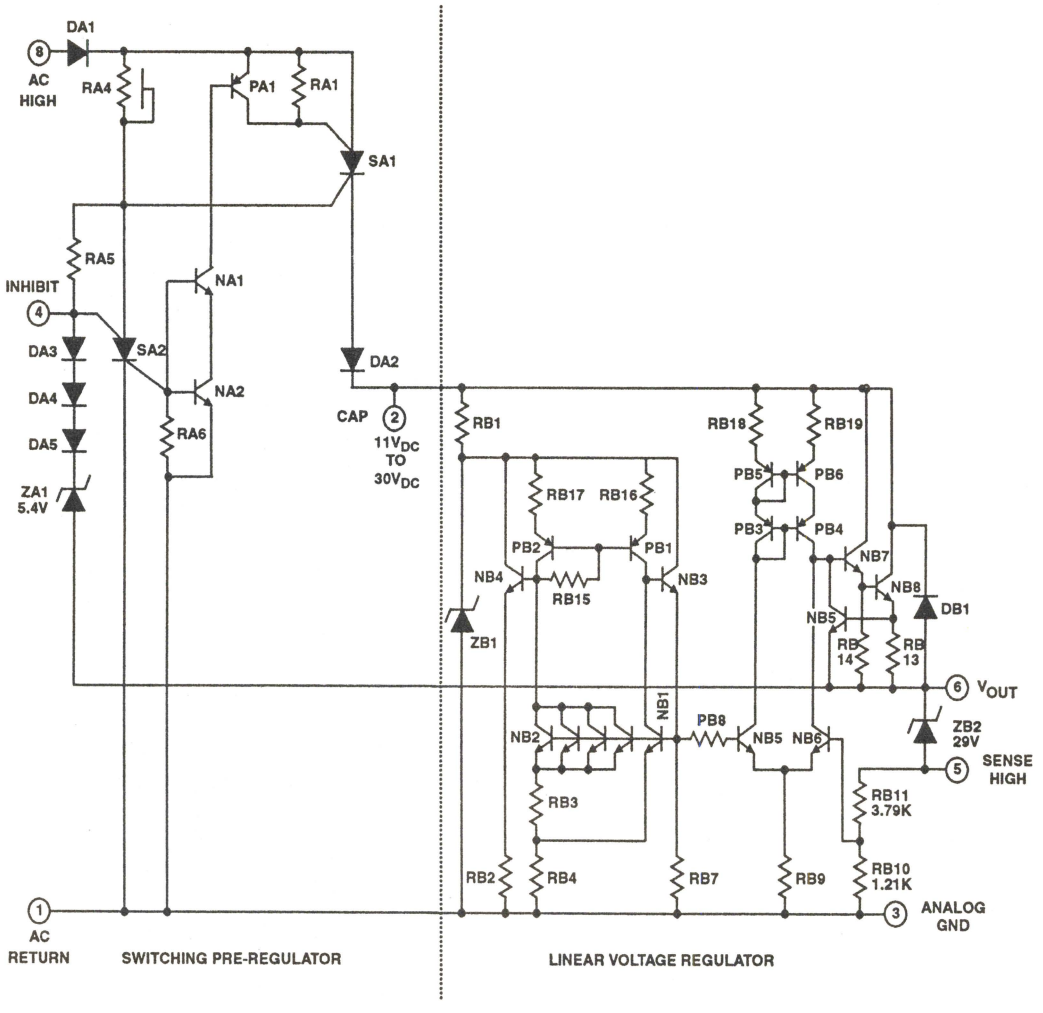


FIGURE 16. HV-2405E SCHEMATIC DIAGRAM

Assume that SA1 is on and the current path is from pin 8 to pin 2. If a small current is pulled out of the base of SA2s pnp (point 1, Figure 17A) SA2 will turn on. When SA2 turns on the collector current of SA1s pnp no longer provides base drive to its npn and SA1 turns off. Figure 17(B) shows the current relationships for both SCRs.

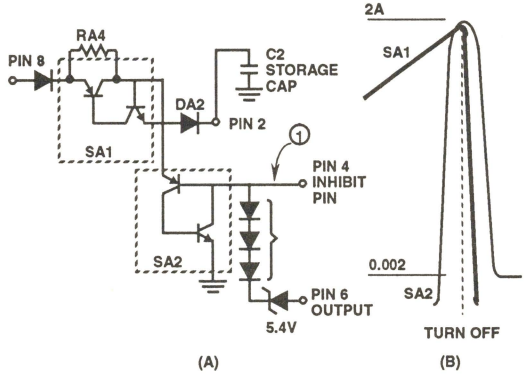


FIGURE 17 (A) (B). SCHEMATIC REPRESENTATION OF SCRs

In order for current to be pulled out of the base of SA2s pnp the voltage on the pnps emitter will have to be more positive than the voltage on the base. The voltage on the base is referenced 7.5V above the output voltage by the zener diode stack between pin 4 and pin 6. When the voltage on pin 2 reaches 6.8V (7.5V-1Vbe) above the output voltage, current flows and SA2 is gated on. With 6.8V above the output voltage on C2, there is a sufficient voltage across SA2 to turn off SA1 by sinking 100% of SA1s anode current.

SA2 could be triggered on before C2s voltage is sufficient to ensure that SA2 can sink 100% of SA1s current, by noise on pin 8. In this case SA1 goes into a high impedance state but does not turn off. This condition can exist if switch arcing triggers enough current through the inhibit capacitor to prematurely turn on SA2.

The **S**afe **O**perating **A**rea (SOA) of the HV-2405E is defined by the voltage on C2 and the magnitude of the input current. Figure 18 shows the safe operating area of the HV-2405E.

Under normal operating conditions the HV-2405E does not turn off the input current until the voltage on C2 is well above 5V. Input currents larger than the safe turn off value in Figure 10 do not present any problems as long as the HV-2405E does not attempt to interrupt them.

During start up operation, power line noise, typically generated by switch bounce/arcing, may accidently initiate input current turn off before C2 is charged. The application circuit shown in Figure 1 never permits the HV-2405E to operate outside the safe turn off current region so any false turn off signals have no effect. Also, once the capacitor is charged, noise causes no problems.

For applications where there is little noise during start up, the external transistor and associated resistors are not needed. A 150pF capacitor connected to pin 4 helps keep the HV-2405E turned off until any switching noise dies out. Also the input resistor R1 may have to be increased to limit the input current to the allowable maximum.

Some applications inherently have little start-up noise. EMI filters between the power switch and the HV-2405E greatly attenuate switch bounce noise. Likewise, the presences of large capacitors connected through bridge rectifiers act as filters. Solid-state relays that close at the line zero crossing generate little noise. Also, there is no problem if power is applied during the negative part of the line cycle. [The user is cautioned to verify the suitability of his application circuit. Contact Harris Applications for specific questions.]

If the safe turn off current is exceeded, SA1 will fail as a short circuit. However, SA2 will continue to act, temporarily, as shunt regulator to keep the voltage on pin 2 from exceeding the safe limit of the post regulator. The voltage at pin 6 will not change. Failure to use a properly rated fuse may cause R1 to reach dangerously high temperatures or cause the HV-2405E to crack or explode.

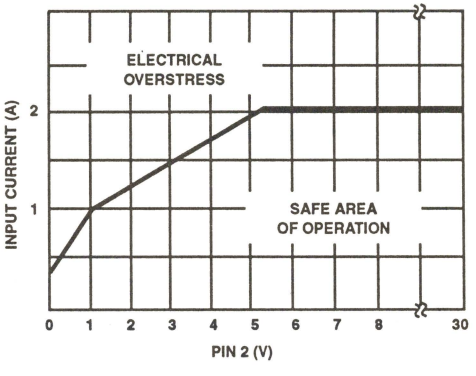


FIGURE 18. HV-2405E SAFE INTERRUPT CURRENT vs PIN 2 VOLTAGE

Typical Performance Curves

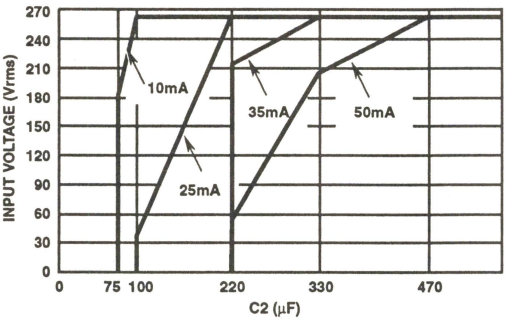


FIGURE 19. MINIMUM C2 VALUE vs INPUT VOLTAGE 50Hz

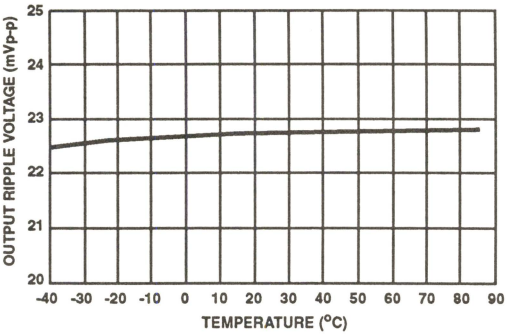


FIGURE 20. OUTPUT RIPPLE VOLTAGE vs TEMPERATURE

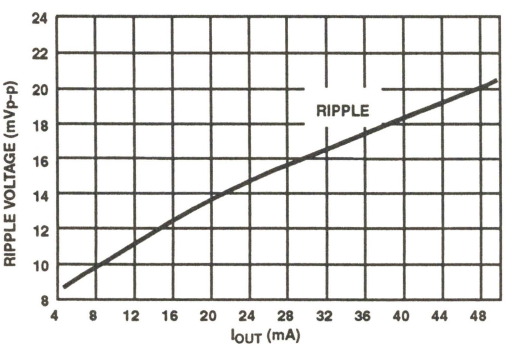


FIGURE 21. OUTPUT RIPPLE VOLTAGE vs LOAD CURRENT

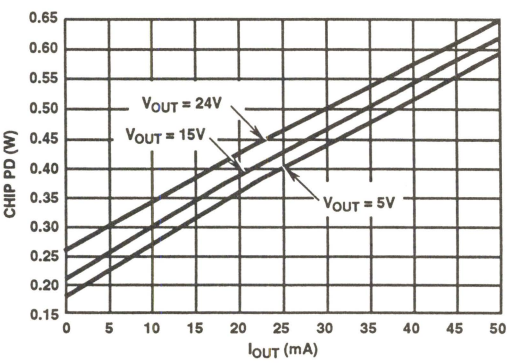


FIGURE 22. CHIP POWER DISSIPATION vs OUTPUT CURRENT

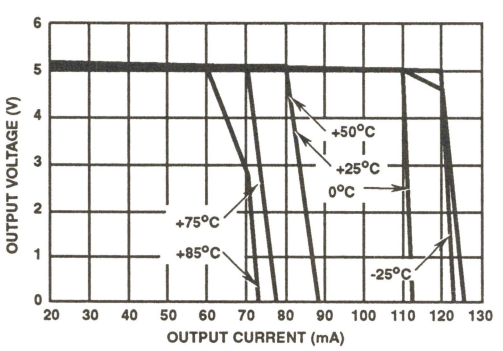


FIGURE 23. OUTPUT CURRENT LIMIT ($5V_{OUT}$) 50Hz
50mA is the Maximum Recommended Output Current

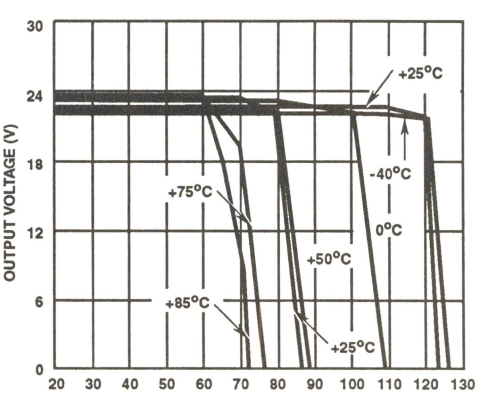


FIGURE 24. OUTPUT CURRENT LIMIT ($24V_{OUT}$) 50Hz
50mA is the Maximum Recommended Output Current

INTELLIGENT POWER ICs

6

FULL BRIDGES

		PAGE
FULL BRIDGE SELECTION GUIDE		6-2
FULL BRIDGE DATA SHEETS		
CA3275	Dual Full Bridge Driver	6-3
HIP4010	Power Full Bridge Driver for Low Voltage Motor Drive with Direction and Brake Control	6-7
HIP4011	Three Phase Brushless DC Motor Controller	6-11
HIP4080	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-14
HIP4080A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-28
HIP4081	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-41
HIP4081A	80V/2.5A Peak, High Frequency Full Bridge FET Driver	6-54
HIP4082	80V/1.25A Peak, Current Full Bridge FET Driver	6-67

Full Bridges Selection Guide

PART NUMBER	DESCRIPTION	PEAK OUTPUT CURRENT EACH DRIVE	SUPPLY VOLTAGE BIAS/BUS	NO LOAD MAXIMUM SUPPLY CURRENT	TARGETED APPLICATIONS
CA3275	Dual Full Bridge Driver	150mA	8V to 16V	20mA	Instrumentation
HIP4010	Low Voltage Motor Drive Power Full Bridge Driver	0.55A	3V to 7V	5µA (Typ)	3V - 5V Motors
HIP4011	3 Phase Motor Controller	5A	10.4V to 13.2V	15mA	Hall Effect Brushless Motors
HIP4080	Full Bridge FET Driver With Comparator, High Performance	2.5A	Bias 8V to 16V Bus 1V to 80V	18mA	Class D Amplifiers, Voice Coil, Motor Control
HIP4080A	Full Bridge FET Driver U/V, Comparator	2.5A	Bias 9.5V to 16V Bus 1V to 80V	18.5mA	Class D Amplifiers, Voice Coil, Motor Control
HIP4081	Full Bridge FET Driver, High Performance	2.5A	Bias 6V to 16V Bus 1V to 80V	16mA	DC-DC Converters, Motor Control, UPS
HIP4081A	Full Bridge FET Driver With U/V, High Performance	2.5A	Bias 9.5V to 16V Bus 1V to 80V	16.5mA	DC-DC Converters, Motor Control, UPS
HIP4082	Full Bridge FET Driver With U/V, 20kHz-200kHz	1.25A	Bias 9.5V to 16V Bus 1V to 80V	6.5mA	UPS, Motor Control

HARRIS SEMICONDUCTOR

CA3275

April 1994

Dual Full Bridge Driver

Features

- Two Full Bridge Drivers
- ± 150mA Maximum Current
- Logic Controlled Switching
- Direction Control
- PWM I_{OUT} Control
- 18V Over-Voltage Protection
- 300mA Short-Circuit Protection
- Nominal 8V to 16V Operation
- Internal Voltage Regulation With Bandgap Reference

Applications

- Dual Full Bridge Driver For Air Core Gauge Instrumentation
- µP Controlled Sensor Data Displays
- Speedometer Displays
- Tachometer Displays
- Stepper Motors
- Slave Position Indicators

Description

The CA3275 Dual Full Bridge Driver is intended for general-purpose applications requiring Dual Full Bridge drive or switching, including direction and pulse-width modulation for position control. While all features of the IC may not be utilized or required, they would normally be used in instrumentation systems with quadrature coils, such as air-core gauges, where the coils would be driven at frequencies ranging from 200Hz to 400Hz. The coils are wrapped at 90° angles for independent direction control. Coils wound in this physical configuration are controlled by pulse width modulation, where each coil drive is a function of the sine or cosine versus degrees of movement. The direction control is used to change the direction of the current in the H-Driver coil.

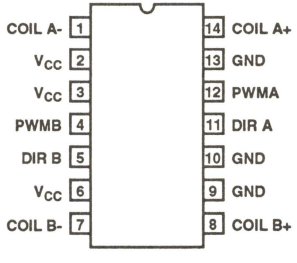
The switch rate capability of the IC is typically 30kHz regardless of the inductive load. Over-current limiting is used to limit short circuit current. Over-voltage protection (in the range of 18V to 24V) causes the device to shut down the output current drive. Thermal shutdown limits power dissipation on the chip. The CA3275 is supplied in a 14 lead dual-in-line plastic package.

Ordering Information

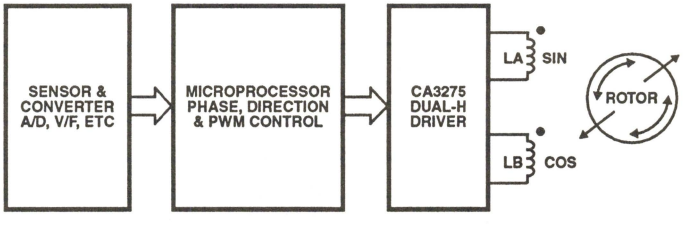
PART NO.	TEMPERATURE	PACKAGE
CA3275E	-40°C to +85°C	14 Lead Plastic DIP

Pinout

CA3275 (PDIP)
TOP VIEW



Block Diagram



6 FULL BRIDGE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 2159.3

Absolute Maximum Ratings

Operating V_{CC} 16V
Transient V_{CC}, 30 Seconds Maximum 24V
Peak V_{CC}, 0.4 Seconds Maximum 40V
Maximum Continuous Output Current, Each Drive ..... ±100mA
Maximum PWM Output Switching Current, Each Drive ..... ±150mA

Thermal Information

Thermal Resistance θ_{JA}
PDIP Package ..... 100°C/W
Power Dissipation, P_D
Up to +70°C 800mW
Above +70°C ..... Derate Linearly at 10mW/°C
Ambient Temperature Range
Operating ..... -40°C to +85°C
Storage ..... -55°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At distance 1/16 ± 1/32" (1.59 ± 0.79mm) from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = 16V Unless Otherwise Specified

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	8	-	16	V
Supply Current (Note 1)	I_{CC}	-	8	20	mA
INPUT LEVELS					
Logic Input, Low Voltage	V_{IL}	-	-	0.8	V
Logic Input, High Voltage	V_{IH}	3.5	-	-	V
Logic Input, Low Current, V_{IL} = 0V	I_{IL}	-10	-	-	µA
Logic Input, High Current, V_{IH} = 5V	I_{IH}	-	-	10	µA
OUTPUT: RLA = RLB = 138Ω					
Maximum Source Saturated Voltage	V_{SAT} - High	-	1.2	1.75	V
Maximum Sink Saturated Voltage	V_{SAT} - Low	-	0.25	0.5	V
Differential V_{SAT} Voltage, Both Outputs Saturated	Diff - V_{SAT}	-	10	100	mV

Switching Specifications

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
SOURCE CURRENT (See Figure 3)					
Turn-Off Delay	T_{SC-OFF}	-	-	2	µs
Fall Time	T_{SC-F}	-	-	2.2	µs
Turn-On Time	T_{SC-ON}	-	-	1	µs
Rise Time	T_{SC-R}	-	-	0.4	µs
SINK CURRENT (See Figure 4)					
Turn-Off Delay	T_{SK-OFF}	-	-	1.6	µs
Fall Time	T_{SK-F}	-	-	0.4	µs
Turn-On Time	T_{SK-ON}	-	-	0.6	µs
Rise Time	T_{SK-R}	-	-	0.2	µs

NOTE:

1. No load, PWMA = PWMB = 5V, DIR A = DIR B = 0V

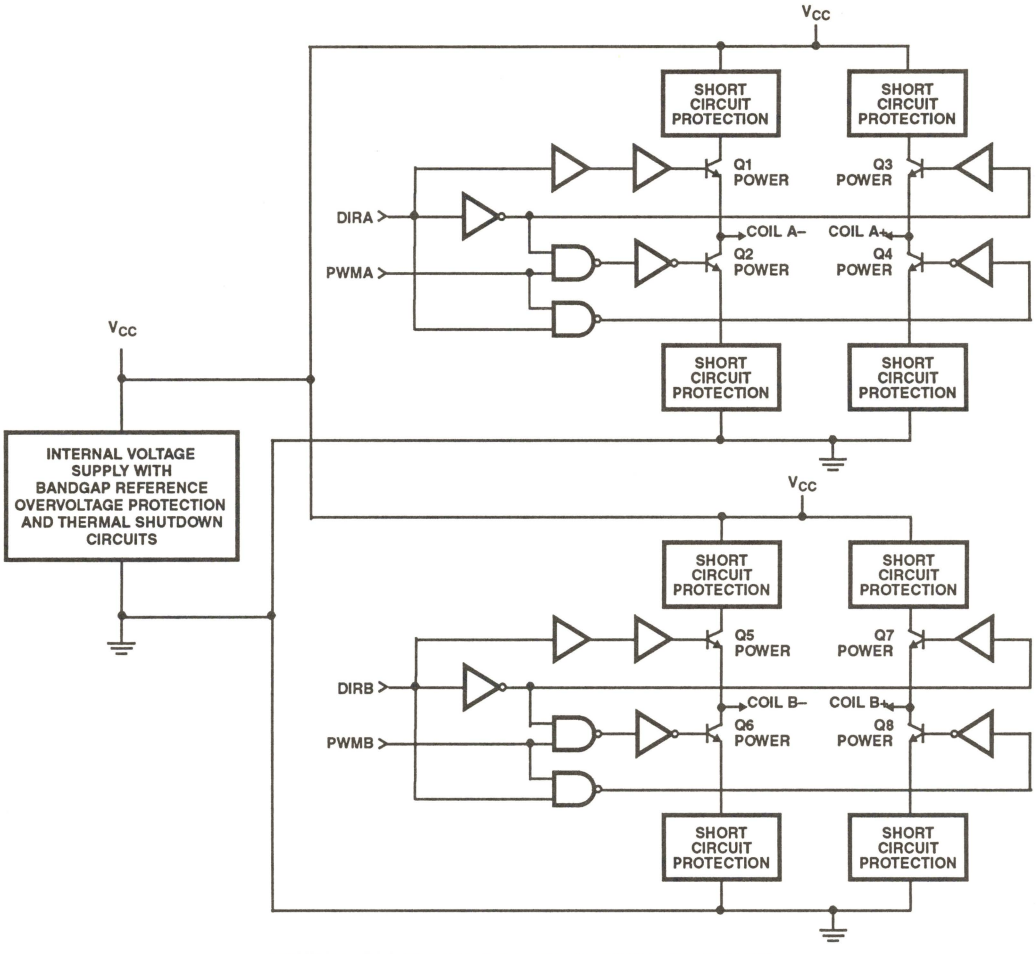


FIGURE 1. CA3275 DUAL FULL BRIDGE DRIVER SCHEMATIC

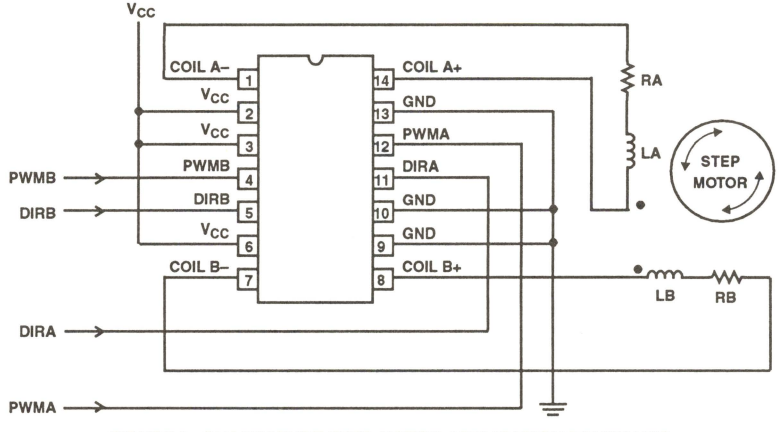
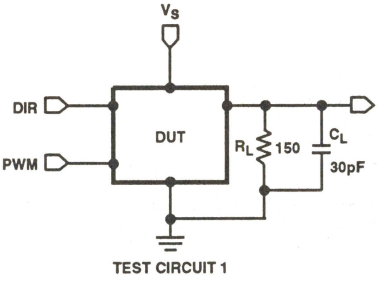


FIGURE 2. QUADRATURE STEP-MOTOR APPLICATION SCHEMATIC



TEST CONDITIONS: PWM = 0V, V_S = 16V
DIR PULSE PARAMETERS:
F = 1kHz, W = 100µs, TR = TF = 1µs, AMPL = 4V

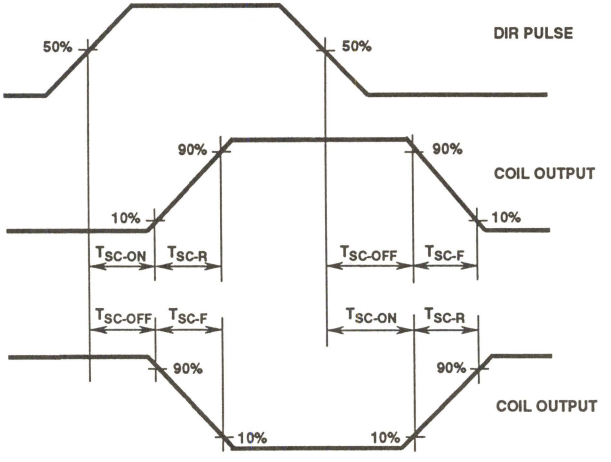
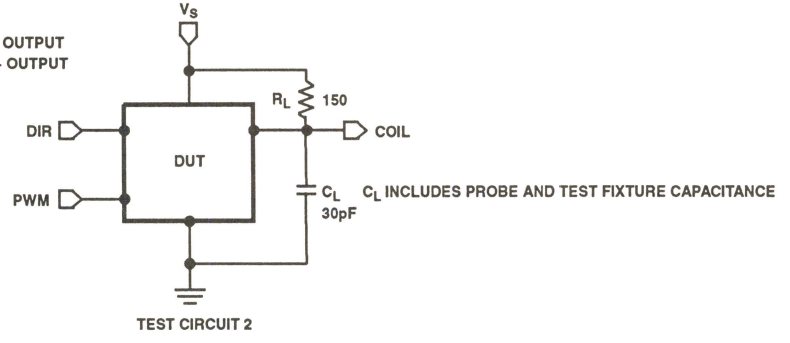


FIGURE 3. SOURCE SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

TEST CONDITIONS: V_S = 16V
DIR = 0V WHEN TESTING COIL - OUTPUT
DIR = 4V WHEN TESTING COIL + OUTPUT



PWM PULSE PARAMETERS:
F = 1kHz, W = 100µs, TR = TF = 1µs, AMPL = 4V

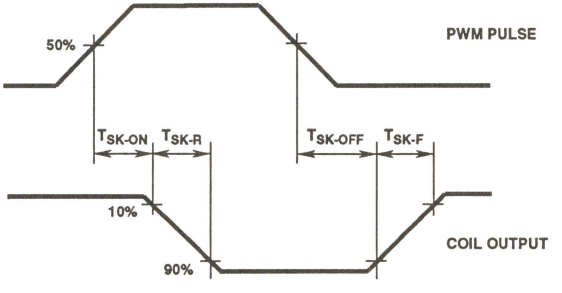


FIGURE 4. SINK SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

HIP4010

ADVANCE INFORMATION

April 1994

Power Full Bridge Driver for Low Voltage Motor Drive with Direction and Brake Control

Features

- Two Independent Complementary MOS Output Half Bridge Drivers for Operation with Low Power Supply Voltages
- Load Switching Capabilities . . . . . to 0.5A with +5V Power Supply
- Single Supply Range . . . . . +3V to +7V
- Split Supply Option with a Negative Reference for the H-Switch Power Drivers
- Low Standby Current
- CMOS/TTL Compatible Input Logic
- Over-Temperature Protection
- Current-Overload Protection
- Over-Current Fault Flag Output
- Direction, Braking and PWM Control

Applications

- DC Motor Driver
- Relay Driver
- Solenoid Driver
- Stepper Motor Controller
- Air Core Gauge Instrument Driver
- Speedometer Displays
- Tachometer Displays
- Remote Power Switch
- +3V to +6V Battery Operated Switch Circuits
- Logic and Microcontroller Operated Switch

Description

In the Functional Block Diagram of the HIP4010 the four switches and a load are arranged in an H-Configuration so that the drive voltage from terminals OUTA and OUTB can be cross-switched to change the direction of current flow in the load. This is commonly known as 4-quadrant load control. As shown in the Block Diagram, switches Q1 and Q4 are conducting or in an ON state when current flows from V_{DDA} through Q1, through the load, and then through Q4 to terminal V_{SSB}; where load terminal OUTA is at a positive potential with respect to OUTB. Switches Q1 and Q4 are operated synchronously by the control logic. The control logic switches Q3 and Q2 to an open or OFF state when Q1 and Q4 are switched ON. To reverse the current flow in the load, the switch states are reversed where Q1 and Q4 are OFF while Q2 and Q3 are ON. Consequently, current then flows from V_{DDB} through Q3, through the load, and through Q2 to terminal V_{SSA}, and load terminal OUTB is then at a positive potential with respect to OUTA.

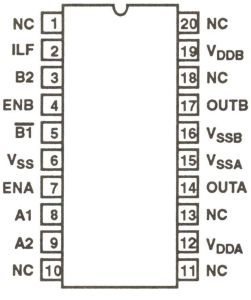
The positive power supply terminals are V_{DDA} and V_{DDB} and are internally connected on the chip. Terminals ENA and ENB are ENABLE Inputs for the Logic A and B Input Controls. The ILF output is an Over-Current Limit Fault Flag Output and indicates a fault condition for either Output A or B or both. While V_{DDA}, V_{DDB} and V_{SS} are the Power Supply reference terminals for the A and B Control Logic Inputs and ILF Output, the V_{SSA} and V_{SSB} Power Supply terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. This is accomplished with the use of level shifting in the gate drive circuitry to the NMOS (low-side) output stages.

Ordering Information

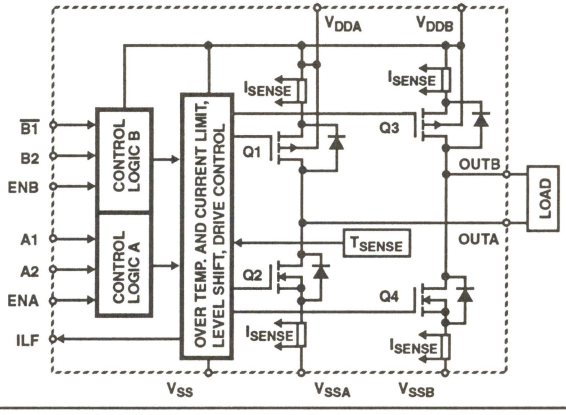
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4010IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

Pinout

HIP4010 (SOIC)
TOP VIEW



Block Diagram



6 FULL BRIDGE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3176.1

Absolute Maximum Ratings

Supply Voltage; V_{DDA} and V_{DDB} to V_{SS} or V_{SSA} or V_{SSB} ..... +7V
Neg. Output Supply Voltage, (V_{SSA},V_{SSB}) ..... (Note 1)
DC Logic Input Voltage (Each Input)
..... (V_{SS}-0.5V) to (V_{DDA}, V_{DDB} +0.5V)
DC Logic Input Current (Each Input) .....±20mA
ILF Fault Output Current.....±20mA
Output Load Current, (Self Limiting, See Elec. Spec.)..... $\pm I_{O(LIMIT)}$

Reliability Information

Thermal Resistance, θ_{JA}.....90°C/W
Power Dissipation
At +25°C (Free Air) 1.39W
Above +25°C ..... Derate Linearly at 11.1mW/°C
Storage Temperature Range.....-65°C to +150°C
Maximum Junction Temperature.....+150°C
Lead Temperature (Soldering 10s).....+265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions T_A = +25°C, V_{SUPPLY}=V_{DDA} = V_{DDB} = +5V, V_{SSA} = V_{SSB} = V_{SS} = 0V; Unless Otherwise Specified

Typical Operating Supply Voltage Range ..... +3 to +7V
Minimum Logic Supply Voltage (V_{DD}-V_{SS})..... +2V
Typical NMOS Driver $R_{DS(ON)}$, 0.5A Load 0.8Ω
Typical PMOS Driver $R_{DS(ON)}$, 0.5A Load.....1.0Ω

Input Low Voltage, V_{IL}.....0V to +0.8V
Input High Voltage, V_{IH} ..... +2.0V to V_{DD}
Input Resistance 0.5TΩ

Electrical Specifications T_A = +25°C; V_{SUPPLY}=V_{DDA} = V_{DDB} = +5V, V_{SSA} = V_{SSB} = V_{SS} = 0V; Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{LEAK}		-	40	50	pA
Input Voltage Range	V_{IN}		0	-	5	V
Low Level Input Voltage	V_{IL}		-	-	0.8	V
High Level Input Voltage	V_{IH}		2	-	-	V
ILF Output Low, Sink Current	I_{OH}	V_{OUT} = 0.4V	3	8	-	mA
ILF Output High, Source Current	I_{OL}	V_{OUT} = 4.6V	-	-4.5	-1.5	mA
ILF Output Low (Sink) Current;	I_{OH}	V_{SUPPLY}=+3V, V_{OUT} = 0.4V	1.5	3	-	mA
ILF Output High (Source) Current);	I_{OL}	V_{SUPPLY}=+3V, V_{OUT} = 2.6V	-	-1.6	-0.8	mA
Input Capacitance	C_{IN}		-	TBE	-	pF
Idle Supply Current; No Load	I_{SUPPLY}		-	0.8	1.5	mA
OUTA, OUTB Voltage High	V_{OH}	I_{SOURCE} = 0.5A	4.2	4.5	-	V
OUTA, OUTB Voltage Low	V_{OL}	I_{SINK} = 0.5A	-	0.4	0.6	V
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$		500	550	620	mA
OUTA, OUTB Sink Current Limiting	$-I_{O(LIMIT)}$		500	550	620	mA
OUTA, OUTB Voltage High	V_{OH}	V_{SUPPLY}=+3V, I_{SOURCE} = 0.3A	2.25	2.5	-	V
OUTA, OUTB Voltage Low	V_{OL}	V_{SUPPLY}=+3V, I_{SINK} = 0.3A	-	0.5	0.65	V
Response Time: V_{EN} to V_{OUT} Turn-on: Prop Delay Rise Time Turn-off: Prop Delay Fall Time	 t_{PLH} t_R t_{PHL} t_F	I_O = 0.5A (Note 2)	-	 4 TBE 0.25 TBE	-	µs

NOTES:

1. V_{SS} is the required common ground reference for the logic input switching. The load currents may be switched near the common ground reference by using a split supply for V_{DDA} and V_{DDB} to V_{SSA} and V_{SSB}. For an uneven split in the supply voltage, the Maximum Negative Output Supply Voltage to V_{SSA} and V_{SSB} is limited by the Maximum V_{DDA} and V_{DDB} to V_{SSA} and V_{SSB} ratings. For all operating conditions the required positive voltages on V_{DDA} and V_{DDB} must be equal and common.
2. Refer to the TRUTH TABLE and the V_{EN} to V_{OUT} SWITCHING WAVEFORMS. Current, I_O refers to I_{OUTA} or I_{OUTB} as the Output Load current. Note that ENA controls OUTA and ENB controls OUTB. Each Half H-Switch has independent control from the respective A1, A2, ENA or $\overline{B1}$, B2, ENB inputs. Refer to the TERMINAL INFORMATION TABLE for external pin connections to establish mode control switching. Figure 1 shows a typical application circuit used to control a DC Motor.

TERMINAL INFORMATION TABLE

V_{DDA}, V_{DDB}	Positive Power Supply pins; internally connected and must be externally connect to the same Positive Supply (V+).
V_{SSA}	Negative Power Supply pin; Negative or Ground return for Switch Driver A.
V_{SSB}	Negative Power Supply pin; Negative or Ground return for Switch Driver B.
V_{SS}	Common Ground pin for the Input Logic Control circuits.
A1, $\overline{B1}$	Input pins used to control the direction of output load current to/from OUTA and OUTB, respectively. When connected, A1 and $\overline{B1}$ can be controlled from the same logic signal to change the directional rotation of a motor.
A2, B2	Input pins used to force a low state on OUTA and OUTB, respectively. When connected, A2 and B2 can be controlled from the same logic signal to activate Dynamic Braking of a motor.
ENA, ENB	Input pins used to Enable Switch Driver A and Switch Driver B, respectively. When Low, the respective output is in a high impedance (Z) off-state. Since each Switch Driver is independently controlled, OUTA and OUTB may be a separately PWM controlled as Half H-Switch Drivers.
OUTA, OUTB	Respectively, Switch Driver A and Switch Driver B Output pins.
ILF	Current Limiting Fault Output Flag pin; when in a high logic state, signifies that Switch Driver A or B or both are in a Current Limiting Fault Mode.

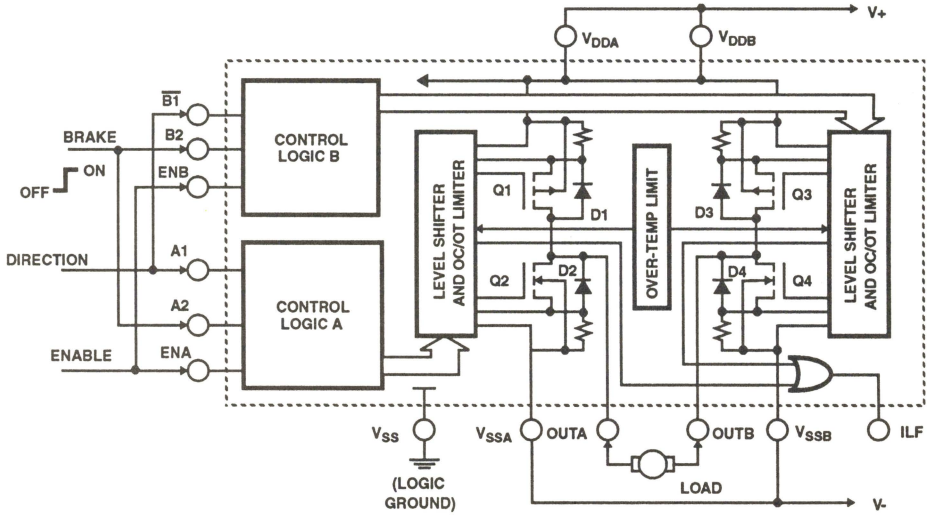
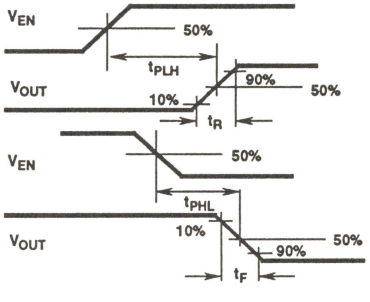


FIGURE 1. TYPICAL HIP4010 MOTOR CONTROL APPLICATION CIRCUIT SHOWING DIRECTIONAL AND BRAKING CONTROL

TRUTH TABLE

SWITCH DRIVER A				SWITCH DRIVER B			
INPUTS			OUTPUT	INPUTS			OUTPUT
A1	A2	ENA	OUTA	B1	B2	ENB	OUTB
H	L	H	OH	L	L	H	OH
L	L	H	OL	H	L	H	OL
H	H	H	OL	L	H	H	OL
L	H	H	OL	H	H	H	OL
X	X	L	Z	X	X	L	Z

L = Low logic level; H = High logic level
Z = High Impedance (off state)
OH = Output High (sourcing current to the output terminal)
OL = Output Low (sinking current from the output terminal)
X = Don't Care



SWITCHING WAVEFORMS

Applications

The HIP4010 is designed to detect load current feedback from sampling resistors of low value in the source connections of the output drivers to V_{DDA}, V_{DDB}, V_{SSA} and V_{SSB} (See Figure 1). When the sink or source current at OUTA or OUTB exceeds the preset OC (Over-Current) limiting value of 550mA typical, the current is held at the limiting value. If the OT (Over-Temperature) Protection limit is exceeded, temperature sensing BiMOS circuits limit the junction temperature to 150°C typical.

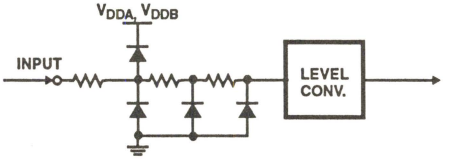
The circuit of Figure 1 shows a Low Voltage motor-driver application for the HIP4010 as a Full H-Switch. The left (A) and right (B) H-Switch's are controlled from the A and B inputs via the A and B CONTROL LOGIC to the MOS output transistors Q1, Q2, Q3 and Q4. The circuit is intended to safely start, stop, and control rotational direction for a motor requiring no more than 0.5A of supply current. The stop function includes a Dynamic Braking feature.

With the ENABLE Inputs Low, the MOS transistors Q1 and Q3 are OFF; which cuts-off supply current to OUTA and OUTB. With the BRAKE terminal Low and ENABLE Inputs High, either Q1 and Q4 or Q3 and Q2 will be driven into conduction by the DIRECTION Input Control terminal. The MOS output transistor pair chosen for conduction is determined by the logic level applied to the DIRECTION control; resulting in either clockwise (CW) or counter-clockwise (CCW) shaft rotation.

When the BRAKE terminal is switched high (while holding the ENABLE input high), the gates of both Q2 and Q4 are driven high. Current flowing through Q2 (from the motor terminal OUTA) at the moment of Dynamic Braking will continue to flow through Q2 to the V_{SSA} and V_{SSB} external connection, and then continue through diode D4 to the motor terminal OUTB. As such, the resistance of the motor winding (and the series-connected path) dissipates the kinetic energy stored in the system. Reversing rotation, current flowing through Q4 (from the motor terminal OUTB), at the moment of Dynamic Braking, would continue to flow through Q4 to the V_{SSB} and V_{SSA} tie, and then continue through diode D2 to the motor terminal OUTA, to dissipate the stored kinetic energy as previously described.

Where V_{DDA} and V_{DDB} to V_{SS} are the Power Supply reference terminals for the Control Logic, the lowest practical supply voltage for proper logic control should be no less than 2.0V. The V_{SSA} and V_{SSB} terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. However, the maximum supply level from V_{DDA} and V_{DDB} to V_{SSA} or V_{SSB} must not be greater than the Absolute Maximum Supply Voltage rating of 7V.

Terminals A1, $\overline{B1}$, A2, B2, ENA and ENB are internally connected to protection circuits intended to guard the CMOS gate-oxides against damage due to electrostatic discharge. (See Figure 3) Inputs ENA, ENB, A1, $\overline{B1}$ A2 and B2 have CD74HCT4000 Logic Interface Protection and Level Converters for TTL or CMOS input Logic. These inputs are designed to typically provide ESD protection up to 2kV. However, these devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.



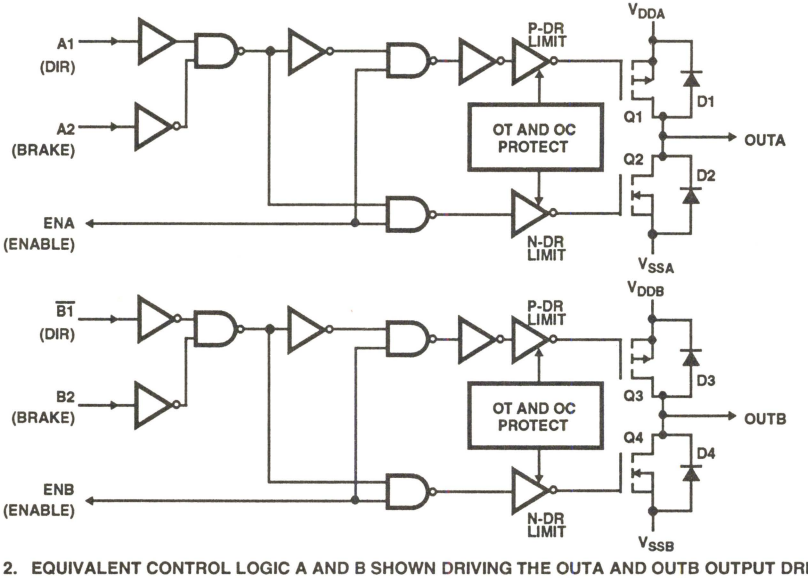


FIGURE 2. EQUIVALENT CONTROL LOGIC A AND B SHOWN DRIVING THE OUTA AND OUTB OUTPUT DRIVERS

HARRIS SEMICONDUCTOR

HIP4011

April 1994

Three Phase Brushless DC Motor Controller

Features

- 3A DC, 5A Peak Output Current
- 16V Max. Rated Supply Voltage
- Built-in "Free-Wheeling" Diodes
- Output dv/dt Limited to Reduce EMI
- External Dynamic Brake Control Switch With Undervoltage Sense
- Thermal and Current Limiting Protects Against Locked Rotor Conditions
- Provides Analog Current Sense and Reference Inputs
- Decode Logic with Illegal Code Rejection

Applications

- Drive Spindle Motor Controller
- 3 Phase Brushless DC Motor Controller
- Brushless DC Motor Driver for 12V Battery Powered Appliances
- Phased Driver for 12V DC Applications
- Logic Controlled Driver for Solenoids, Relays and Lamps

Description

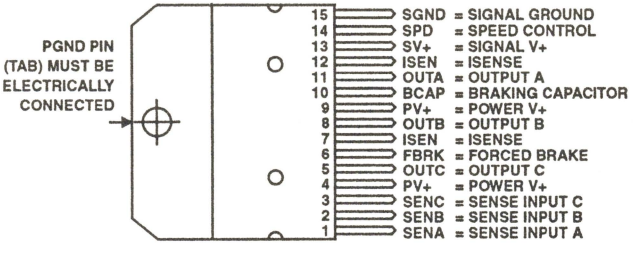
The HIP4011 motor driver is intended for three phase Brushless motor control at continuous output currents up to 3A. It accepts inputs from buffered Hall effect sensors and drives three motor windings, regulating the current through an external current sensing resistor, according to an analog control input. Output "freewheeling" diodes are built in and output dv/dt is limited to decrease the generated EMI. Thermal and current limiting are used to protect the device from locked rotor conditions. A brake control input forces all outputs to ground simultaneously to provide dynamic braking, and an internal voltage sensor does the same when the supply drops below a predetermined switch point. Power down braking energy is stored in an external capacitor.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4011IS	-40°C to +85°C	15 Pin Plastic SIP Surface Mount

Pinout

HIP4011 (SIP)
TOP VIEW



OUTPUT TRUTH TABLE

SENSOR INPUTS			FORCE BRAKE INPUT*	OUTPUTS		
A	B	C	FBRK	A	B	C
0	0	0	0	OFF	OFF	OFF
1	0	0	0	1	OFF	0
0	1	0	0	0	1	OFF
1	1	0	0	OFF	1	0
0	0	1	0	OFF	0	1
1	0	1	0	1	0	OFF
0	1	1	0	0	OFF	1
1	1	1	0	OFF	OFF	OFF
X	X	X	1	0	0	0

* Undervoltage and Force Brake logic truth table entries are identical.

"X" = Don't Care

6 FULL BRIDGE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 2939.3

Absolute Maximum Ratings

Supply Voltage, SV+ or PV+ . . . . . -1V to +16V
Referred to SGND or PGND (Note 1)
Output Current, Continuous 3A
Output Current, Peak (Note 2) 5A
Substrate (PGND) Current 1A
Logic Input Current . . . . . -20mA to +20mA
(Clamped to SV+ and SGND)

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
15 Lead SIP Power Package	45°C/W	3°C/W

Power Dissipation (Note 3) 25W
Junction Temperature Range, Operating . . . . . +150°C
Storage Temperature Range . . . . . -55°C to +150°C
Power Dissipation
Up to +125°C without heat sink 0.56W
Above +125°C without Heat Sink . . . Derate Linearly at 22mW/°C
Up to +125°C with Infinite Heat Sink 8.33W
Above +125°C with Infinite Heat Sink . . . . . .Derate Linearly at 333mW/°C
Lead Temperature (During Soldering)
At a Distance 1/16 inch ±1/32 inch (1.59mm ±0.79mm)
from Case for 10s Max. . . . . +265°C

NOTES:

1. PV+ and SV+ are to be tied together, as are PGND and SGND.
2. Operating above the continuous current rating causes a decrease in operating life.
3. Derate power dissipation above case temperature of +75°C at 0.33 Watts/°C.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNITS
SUPPLY (SV+) CURRENT					
No Drive	Outputs Off	-	-	10	mA
With Drive	Outputs On	-	-	15	mA
LOGIC INPUT CURRENT					
Sensor Inputs	SENA, SENB & SENC = 0V to 3V	-0.5	-	-1.5	mA
Brake Input	FBRK = 0.8V to 2.4V	50	-	150	µA
LOGIC INPUT THRESHOLDS					
Sensor Inputs	Logic "0" Input Voltage	-	-	1.8	V
Sensor Inputs	Logic "1" Input Voltage	3	-	-	V
Brake Input	Logic "0" Input Voltage	-	-	0.8	V
Brake Input	Logic "1" Input Voltage	2.4	-	-	V
AMPLIFIER INPUT (SPD)					
Bias Current		-	-	700	nA
Offset Voltage		-	-	3	mV
Input Range (Linear)		0	-	1	V
Input Impedance		1	-	-	MΩ
System Bandwidth	(Note 1)	-	35	-	kHz
Current Limit	Rsense = 0.20Ω	-	5	-	A
THERMAL LIMIT					
Threshold		-	155	-	°C
Hysteresis		-	40	-	°C
OUTPUT DRIVERS					
On Saturation (See Note 5)	I_{OUT} = 3A, $V_{PMOS} + V_{NMOS}$	-	-	2.2	V
On Saturation (See Note 5)	I_{OUT} = 0.6A, $V_{PMOS} + V_{NMOS}$	-	-	0.44	V
Off Leakage	PV+ > V_{OUT} > PGND or I_{SEN}	-	-	1	mA
Slew Rate	(See Note 2)	-	0.5	-	V/µS

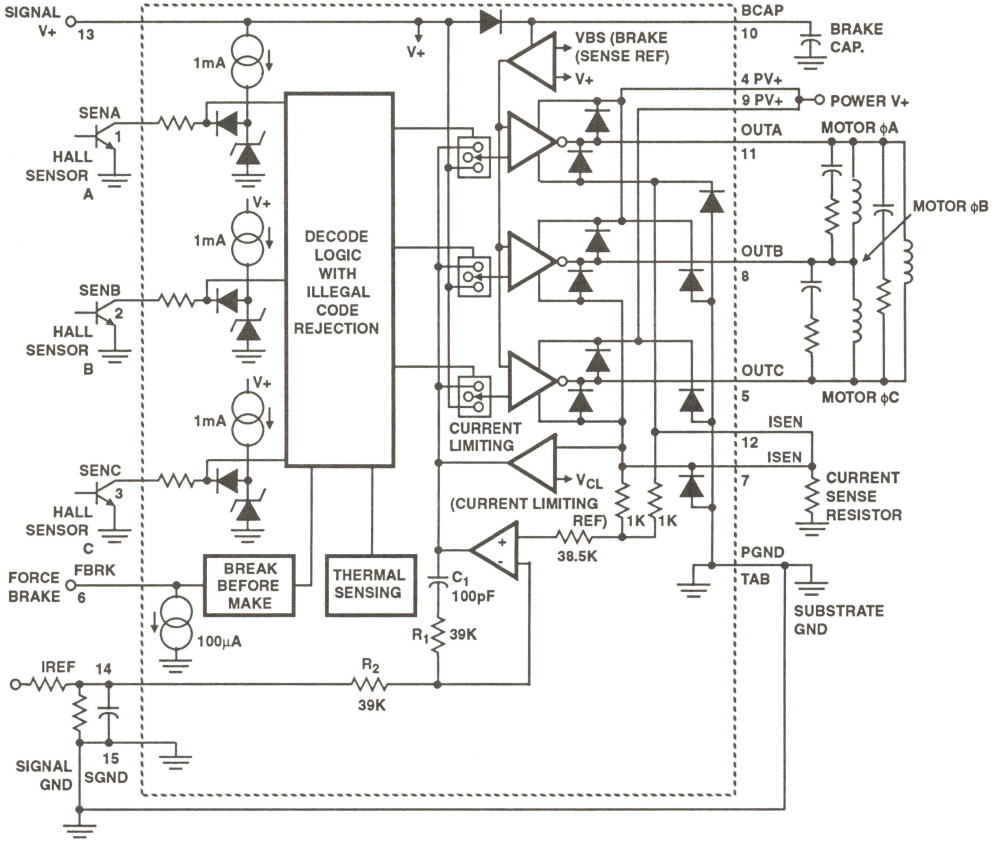
Electrical Specifications T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNITS
FREEWHEEL DIODES					
Forward Drop	I_{OUT} = 1A	-	-	1.5	V
INTERNAL BRAKE DRIVER					
Undervoltage Trip Point, PV+	(See Note 3)	2.7	-	3.3	V
Hysteresis	(See Note 4)	40	-	60	%
On Saturation	Each N_{MOS}, I_{OUT} = 3A	-	-	0.4	V
BRAKE CAPACITOR (BCAP)					
Discharge Leakage	SV+ = PV+ = 3V to 12V, BCAP = 10V	-	-	5	µA

NOTES:

1. The system bandwidth is fixed by an internal RC network around the amplifier.
2. Internal limiting of turn on and turn off drive is used to limit output dv/dt.
3. The braking action starts at the given trip point with a falling supply voltage.
4. Hysteresis causes the brake to be removed at a higher trip point with a rising supply voltage.
5. This value includes the combined voltage drops of one upper plus one lower switch at the indicated current.

Functional Block Diagram



THREE PHASE BRUSHLESS CONTROLLER

HARRIS SEMICONDUCTOR

HIP4080

80V/2.5A Peak, High Frequency Full Bridge FET Driver

April 1994

Features

- Drives N-Channel FET Full Bridge Including High Side Chop Capability
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load at 1MHz in Free Air at +50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- Charge-Pump and Bootstrap Maintain Upper Bias Supplies
- DIS (Disable) Pin Pulls Gates Low
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption

Applications

- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Class D Audio Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

Description

The HIP4080 is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4080 includes an input comparator, used to facilitate the "hysteresis" and PWM modes of operation. Its HEN (high enable) lead can force current to freewheel in the bottom two external power MOSFETs, maintaining the upper power MOSFETs off. Since it can switch at frequencies up to 1MHz, the HIP4080 is well suited for driving Voice Coil Motors, switching amplifiers in class D high-frequency switching audio amplifiers and power supplies.

HIP4080 can also drive medium voltage brush motors, and two HIP4080s can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in precise control of the driven load.

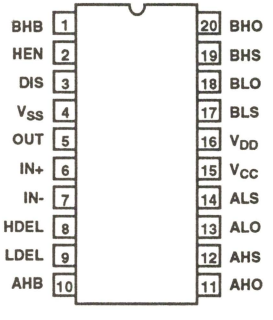
The similar HIP4081 IC allows independent control of all 4 FETs in an Full Bridge configuration.

Ordering Information

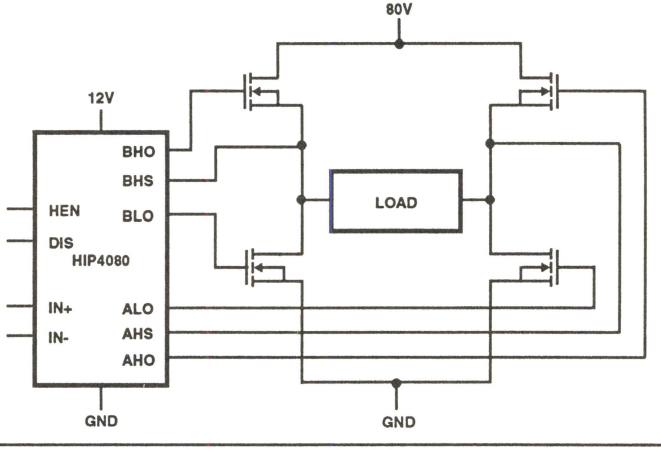
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4080IP	-40°C to +85°C	20 Lead Plastic DIP
HIP4080IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

Pinout

HIP4080 (PDIP, SOIC)
TOP VIEW



Application Block Diagram

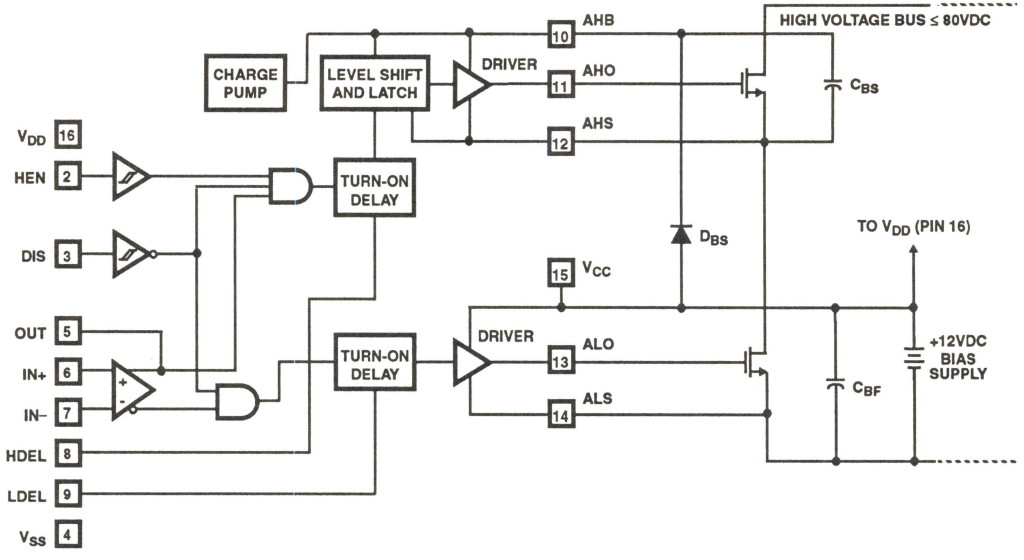


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

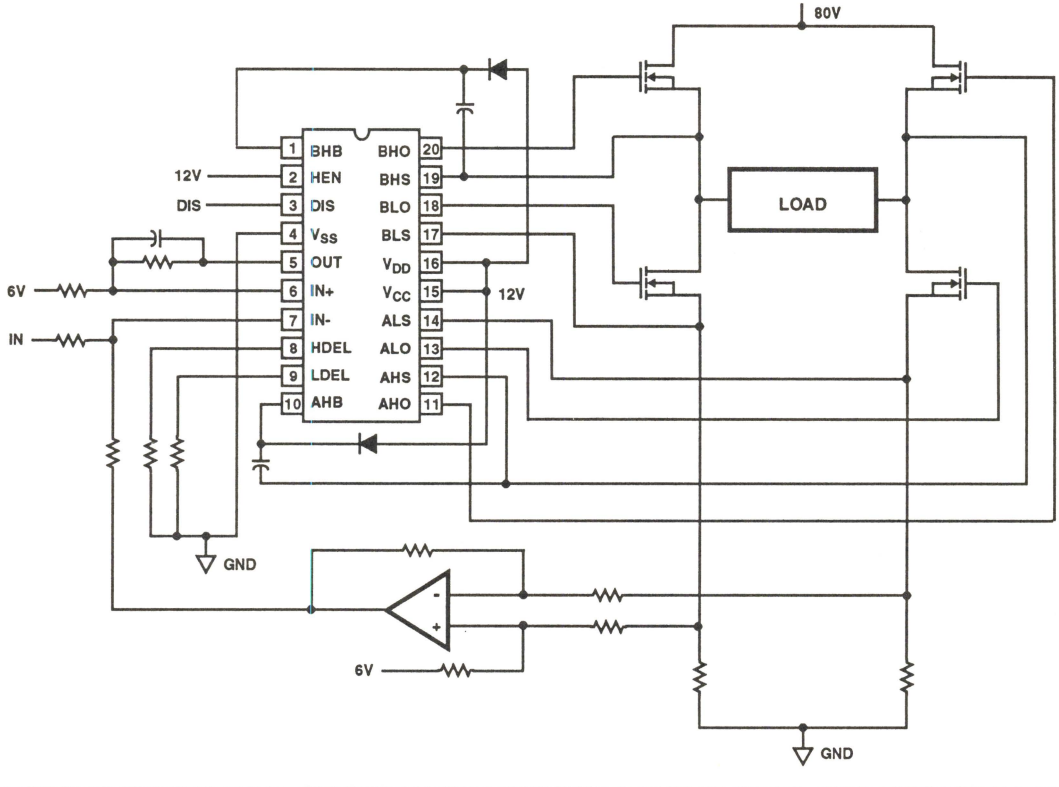
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File Number **3178.6**

Functional Block Diagram (1/2 HIP4080)



Typical Application (Hysteresis Mode Switching)



Absolute Maximum Ratings

Supply Voltage, V_{DD} and V_{CC} ..... -0.3V to 16V
Logic I/O Voltages ..... -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS ..... -6.0V (Transient) to 88V
Voltage on ALS, BLS .....-2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB ..... $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +16V, or 95V whichever is less
Voltage on ALO, BLO ..... $V_{ALS, BLS}$ -0.3V to V_{CC} +0.3V
Voltage on AHO, BHO ..... $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V
Input Current, HDEL and LDEL .....-5mA to 0mA
Phase Slew Rate 20V/ns
NOTE: All Voltages relative to pin 4, V_{SS}, unless otherwise specified.

Thermal Information

Thermal Resistance θ_{JA}
SOIC Package..... +85°C/W
DIP Package ..... +75°C/W
Maximum Power Dissipation at +85°C
SOIC Package.....470mW
DIP Package 530mW
Storage Temperature Range.....-65°C to +150°C
Operating Max. Junction Temperature .....+125°C
Lead Temperature (Soldering 10s) .....+300°C
(For SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} ..... +8V to +15V
Voltage on ALS, BLS .....-1.0V to +1.0V
Voltage on AHS, BHS.....-1V to 80V
Voltage on AHB, BHB ..... $V_{AHS, BHS}$ +5V to $V_{AHS, BHS}$ +15V
Input Current, HDEL and LDEL.....-500µA to -50µA
Operating Ambient Temperature Range .....-40°C to +85°C

Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = - 40°C TO +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND CHARGE PUMPS								
V_{DD} Quiescent Current	I_{DD}	IN- = 2.5V, Other Inputs = 0V	8	10.5	13	7	14	mA
V_{DD} Operating Current	I_{DDO}	Outputs switching f = 500kHz	9	11	14	8	15	mA
V_{CC} Quiescent Current	I_{CC}	IN- = 2.5V, Other Inputs = 0V, $I_{ALO} = I_{BLO} = 0$	-	25	80	-	100	µA
V_{CC} Operating Current	I_{CCO}	f = 500kHz, No Load	1	1.5	2.0	0.8	3	mA
AHB, BHB Quiescent Current - Qpump Output Current	I_{AHB}, I_{BHB}	IN- = 2.5V, Other Inputs = 0V, $I_{AHO} = I_{BHO} = 0$, $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V$	-50	-30	-15	-60	-10	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 500kHz, No Load	0.5	0.9	1.3	0.4	1.7	mA
AHS, BHS, AHB, BHB Leakage Current	I_{HLK}	$V_{AHS} = V_{BHS} = V_{AHB} = V_{BHB} = 95V$	-	0.02	1.0	-	10	µA
AHB-AHS, BHB-BHS Qpump Output Voltage	$V_{AHB} - V_{AHS}$ $V_{BHB} - V_{BHS}$	$I_{AHB} = I_{AHB} = 0$, No Load	11.5	12.6	14.0	10.5	14.5	V
INPUT COMPARATOR PINS: IN+, IN-, OUT								
Offset Voltage	V_{OS}	Over Common Mode Voltage Range	-10	0	+10	-15	+15	mV
Input Bias Current	I_{IB}		0	0.5	2	0	4	µA
Input Offset Current	I_{OS}		-1	0	+1	-2	+2	µA
Input Common Mode Voltage Range	CMVR		1	-	V_{DD} -1.5	1	V_{DD} -1.5	V
Voltage Gain	AVOL		10	25	-	10	-	V/mV
OUT High Level Output Voltage	V_{OH}	IN+ > IN-, I_{OH} = -300µA	V_{DD} -0.4	-	-	V_{DD} - 0.5	-	V
OUT Low Level Output Voltage	V_{OL}	IN+ < IN-, I_{OL} = 300µA	-	-	0.3	-	0.4	V
High Level Output Current	I_{OH}	V_{OUT} = 6V	-9	-7	-4	-11	-2	mA
Low Level Output Current	I_{OL}	V_{OUT} = 6V	8	10	12	5	14	mA
INPUT PINS: DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	µA

Electrical Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
INPUT PINS: HEN								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	$V_{IN} = 0V$, Full Operating Conditions	-260	-200	-150	-270	-130	µA
High Level Input Current	I_{IH}	$V_{IN} = 5V$, Full Operating Conditions	-1	-	+1	-10	+10	µA
TURN-ON DELAY PINS: LDEL AND HDEL								
LDEL, HDEL Voltage	$V_{HDEL,}V$	$I_{HDEL} = I_{LDEL} = -100µA$	4.9	5.1	5.3	4.8	5.4	V
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO								
Low Level Output Voltage	V_{OL}	$I_{OUT} = 100mA$	.70	0.85	1.0	0.5	1.1	V
High Level Output Voltage	$V_{CC} - V_{OH}$	$I_{OUT} = -100mA$	0.8	0.95	1.1	0.5	1.2	V
Peak Pull-up Current	I_O+	$V_{OUT} = 0V$	1.7	2.6	3.8	1.4	4.1	A
Peak Pull-down Current	I_O-	$V_{OUT} = 12V$	1.7	2.4	3.3	1.3	3.6	A

Switching Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, $C_L = 1000pF$, and $T_A = +25°C$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (IN+/IN- to ALO/BLO)	T_{LPHL}		-	40	70	-	90	ns
Upper Turn-off Propagation Delay (IN+/IN- to AHO/BHO)	T_{HPHL}		-	50	80	-	110	ns
Lower Turn-on Propagation Delay (IN+/IN- to ALO/BLO)	T_{LPLH}	$R_{HDEL} = R_{LDEL} = 10K$	-	45	70	-	90	ns
Upper Turn-on Propagation Delay (IN+/IN- to AHO/BHO)	T_{HPLH}	$R_{HDEL} = R_{LDEL} = 10K$	-	70	110	-	140	ns
Rise Time	T_R		-	10	25	-	35	ns
Fall Time	T_F		-	10	25	-	35	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$	$R_{HDEL} = R_{LDEL} = 10K$	50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$	$R_{HDEL} = R_{LDEL} = 10K$	40	-	-	40	-	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	45	75	-	95	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	55	85	-	105	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	T_{DLPLH}		-	35	70	-	90	ns
Refresh Pulse Width (ALO and BLO)	T_{REF-PW}		160	260	380	140	420	ns
Disable to Upper Enable (DIS - AHO and BHO)	T_{UEN}		-	335	500	-	550	ns
HEN-AHO, BHO Turn-off, Propagation Delay	$T_{HEN-PHL}$	$R_{HDEL} = R_{LDEL} = 10K$	-	35	70	-	90	ns
HEN-AHO, BHO Turn-on, Propagation Delay	$T_{HEN-PLH}$	$R_{HDEL} = R_{LDEL} = 10K$	-	60	90	-	110	ns

TRUTH TABLE

INPUT			OUTPUT			
IN+ > IN-	HEN	DIS	ALO	AHO	BLO	BHO
X	X	1	0	0	0	0
1	1	0	0	1	1	0
0	1	0	1	0	0	1
1	0	0	0	0	1	0
0	0	0	1	0	0	0

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	HEN	High-side Enable input. Logic level input that when low overrides IN+/IN- (Pins 6 and 7) to put AHO and BHO drivers (Pins 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by IN+/IN- inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold HEN high, so no connection is required if high-side and low-side outputs are to be controlled by IN+/IN- inputs.
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold DIS high if this pin is not driven.
4	V_{SS}	Chip negative supply, generally will be ground.
5	OUT	OUTput of the input control comparator. This output can be used for feedback and hysteresis.
6	IN+	Non-inverting input of control comparator. If IN+ is greater than IN- (Pin 7) then ALO and BHO are low level outputs and BLO and AHO are high level outputs. If IN+ is less than IN- then ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (Pin 3) high level will override IN+/IN- control for all outputs. HEN (Pin 2) low level will override IN+/IN- control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (Pins 8 and 9).
7	IN-	Inverting input of control comparator. See IN+ (Pin 6) description.
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (Pin 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (Pin 15). De-couple this pin to V_{SS} (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

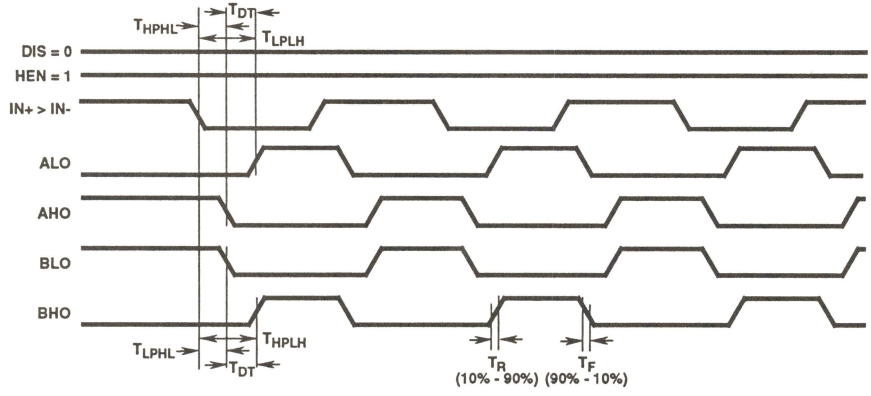


FIGURE 1. BISTATE MODE

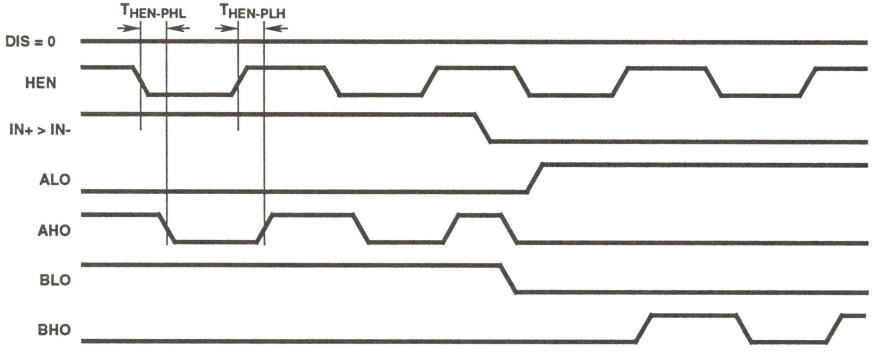


FIGURE 2. HIGH SIDE CHOP MODE

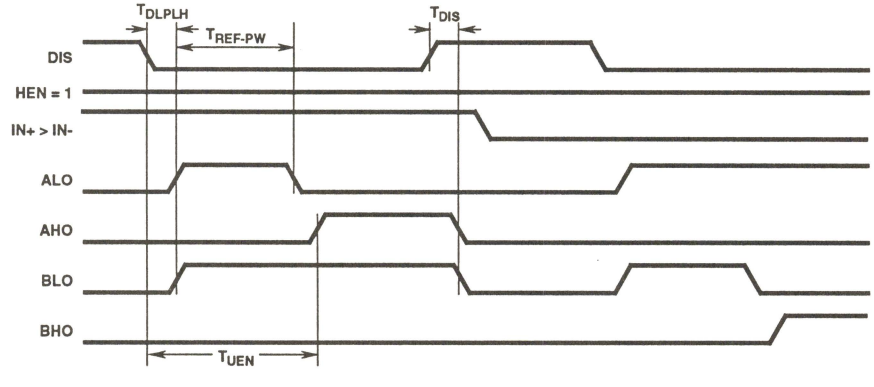


FIGURE 3. DISABLE FUNCTION

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

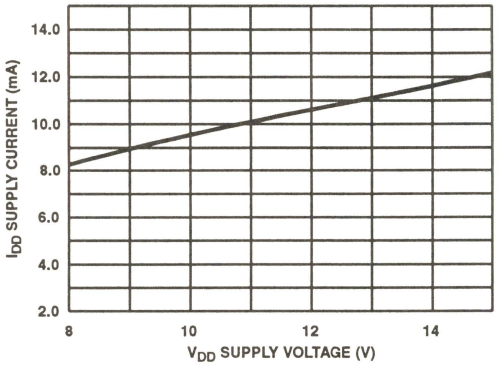


FIGURE 4. QUIESCENT I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

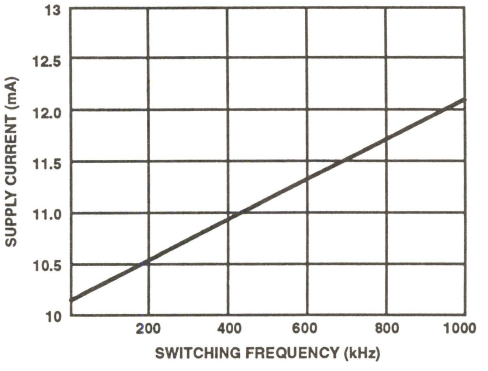


FIGURE 5. I_{DDO}, NO-LOAD I_{DD} SUPPLY CURRENT vs FREQUENCY (kHz)

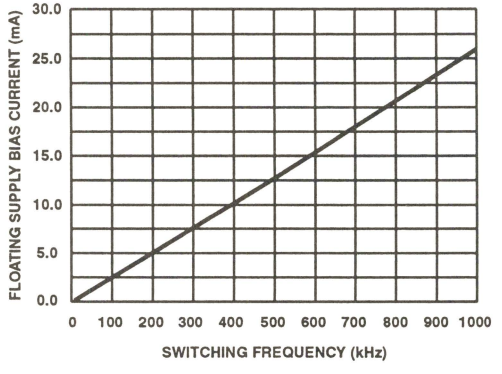


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

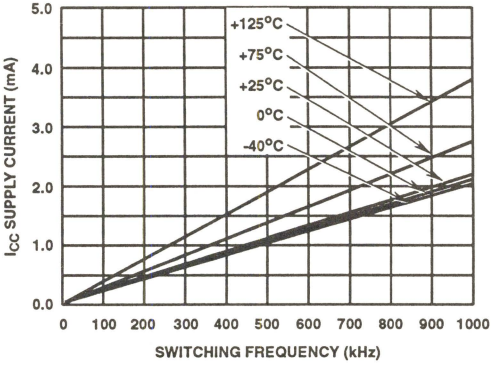


FIGURE 7. I_{CCO}, NO-LOAD I_{CC} SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

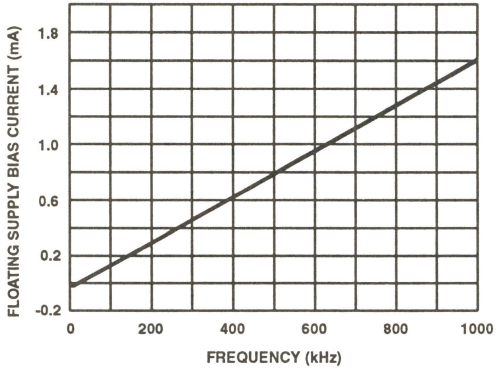


FIGURE 8. I_{AHB}, I_{BHB}, NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

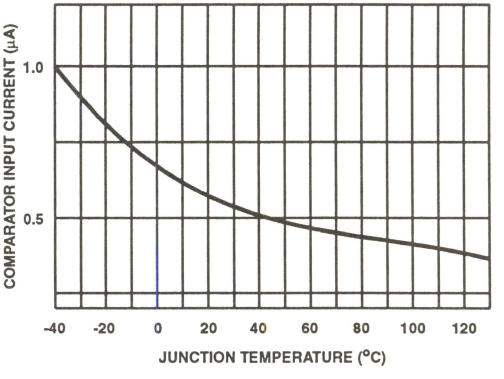


FIGURE 9. COMPARATOR INPUT CURRENT I_L vs TEMPERATURE AT $V_{CM} = 5V$

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

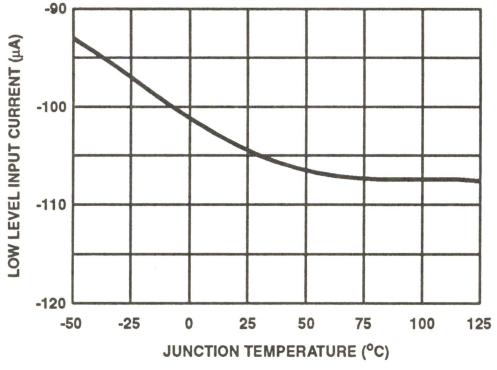


FIGURE 10. DIS LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

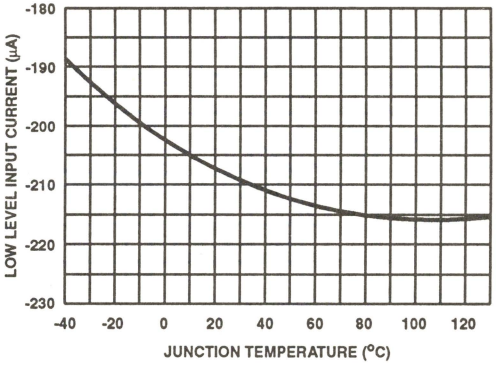


FIGURE 11. HEN LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

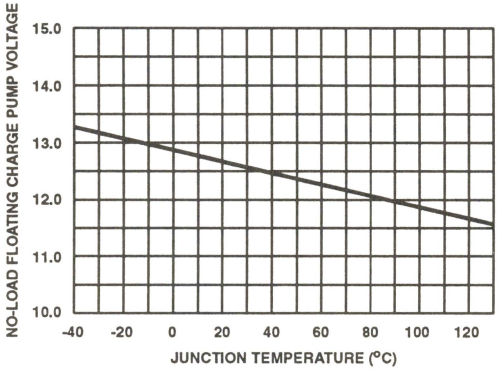


FIGURE 12. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

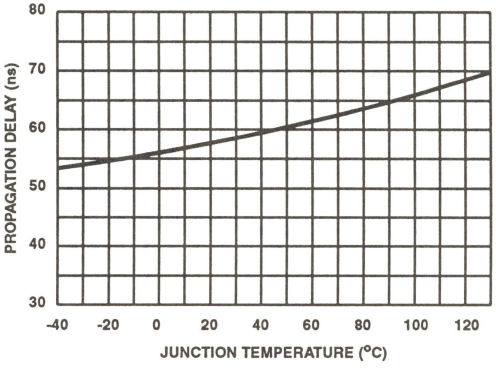


FIGURE 13. UPPER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISHIGH}$ vs TEMPERATURE

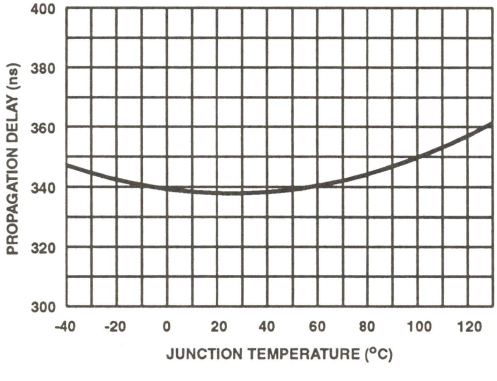


FIGURE 14. DISABLE TO UPPER ENABLE T_{UEN} PROPAGATION DELAY vs TEMPERATURE

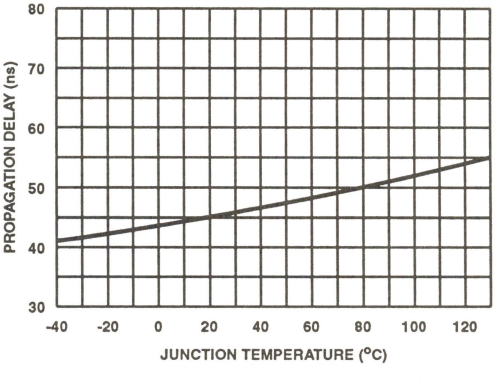


FIGURE 15. LOWER DISABLE TURN-OFF PROPAGATION DELAY T_{DISLOW} vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, $T_A = +25°C$ and $R_{HDEL} = R_{LDEL} = 10K$, Unless Otherwise Specified

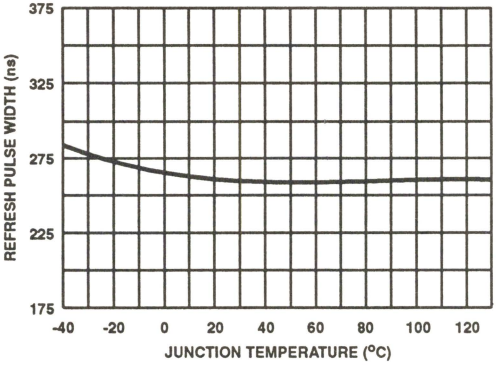


FIGURE 16. T_{REF-PW} REFRESH PULSE WIDTH vs TEMPERATURE

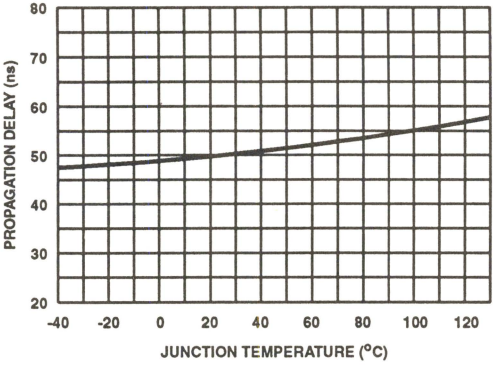


FIGURE 17. DISABLE TO LOWER ENABLE T_{DLPLH} PROPAGATION DELAY vs TEMPERATURE

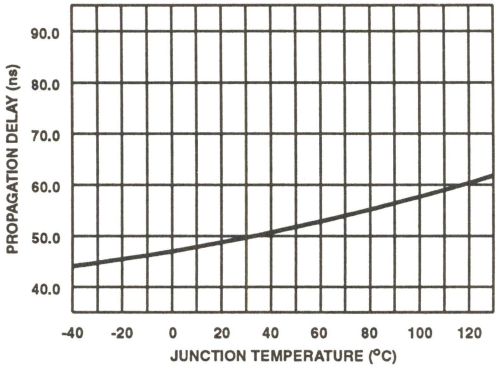


FIGURE 18. UPPER TURN-OFF PROPAGATION DELAY T_{HPHL} vs TEMPERATURE

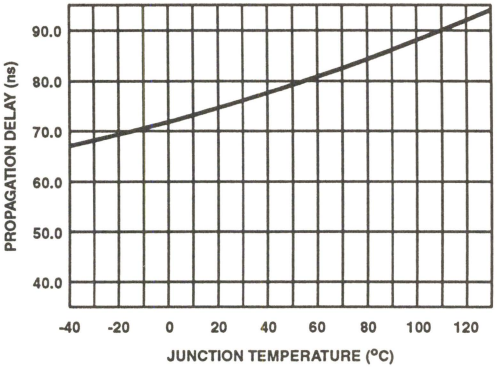


FIGURE 19. UPPER TURN-ON PROPAGATION DELAY T_{HPLH} vs TEMPERATURE

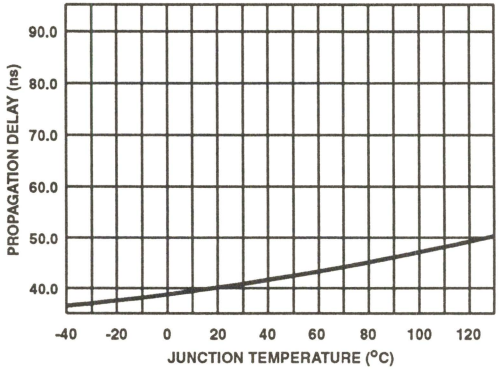


FIGURE 20. LOWER TURN-OFF PROPAGATION DELAY T_{LPHL} vs TEMPERATURE

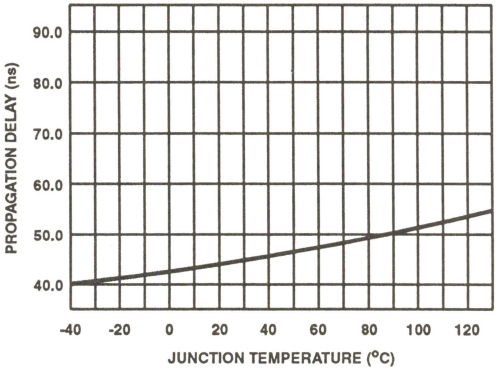


FIGURE 21. LOWER TURN-ON PROPAGATION DELAY T_{LPLH} vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = +25°C$, Unless Otherwise Specified

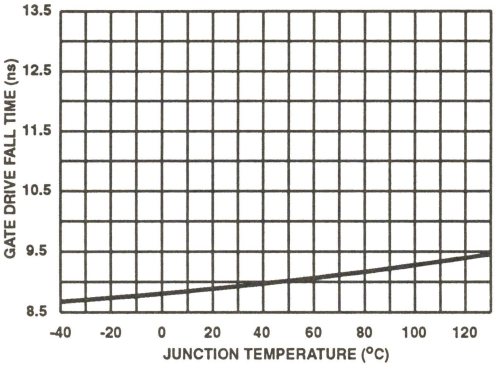


FIGURE 22. GATE DRIVE FALL TIME T_F vs TEMPERATURE

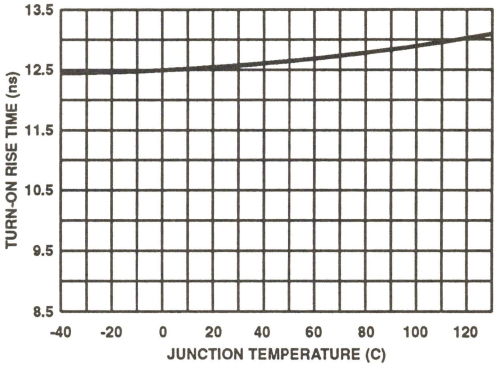


FIGURE 23. GATE DRIVE RISE TIME T_R vs TEMPERATURE

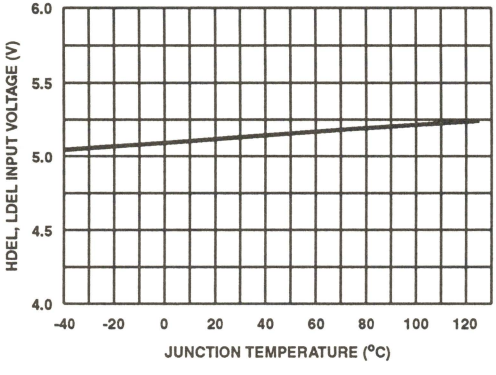


FIGURE 24. V_{LDEL}, V_{HDEL} VOLTAGE vs TEMPERATURE

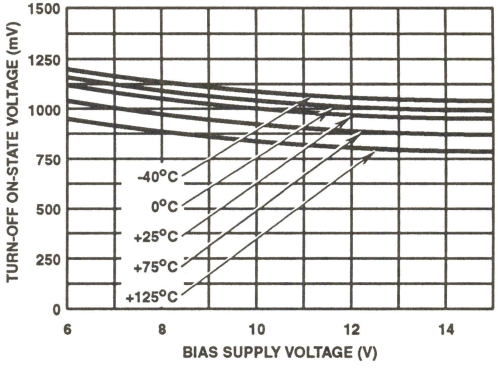


FIGURE 25. HIGH LEVEL OUTPUT VOLTAGE, $V_{CC} - V_{OH}$ vs BIAS SUPPLY AND TEMPERATURE AT 100mA

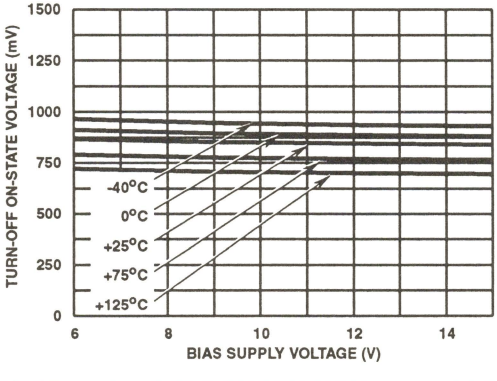


FIGURE 26. LOW LEVEL OUTPUT VOLTAGE V_{OL} vs BIAS SUPPLY AND TEMPERATURE AT 100mA

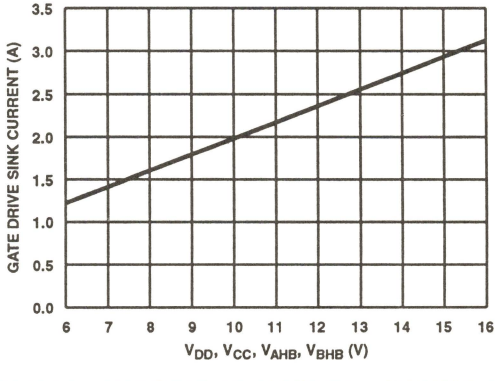


FIGURE 27. PEAK PULLDOWN CURRENT I_O vs BIAS SUPPLY VOLTAGE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

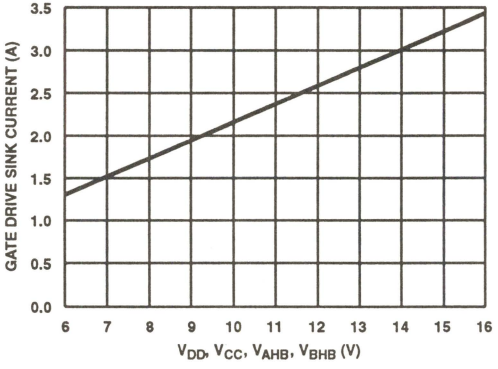


FIGURE 28. PEAK PULLUP CURRENT I_{O+} vs SUPPLY VOLTAGE

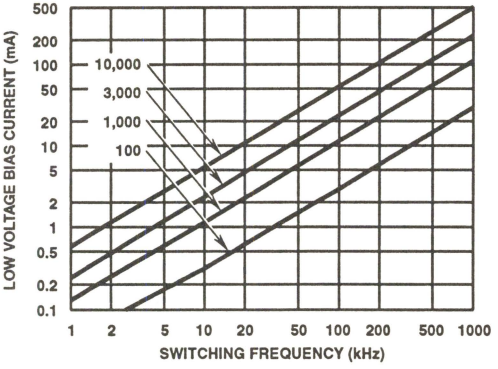


FIGURE 29. LOW VOLTAGE BIAS CURRENT I_{DD} AND I_{CC} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

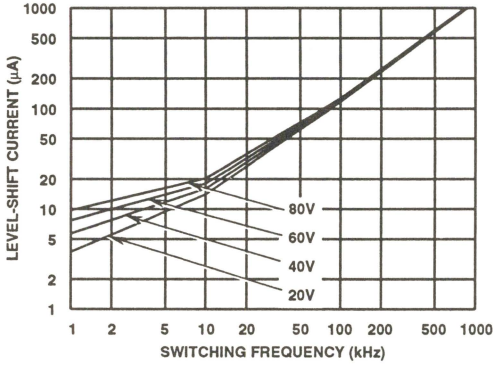


FIGURE 30. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

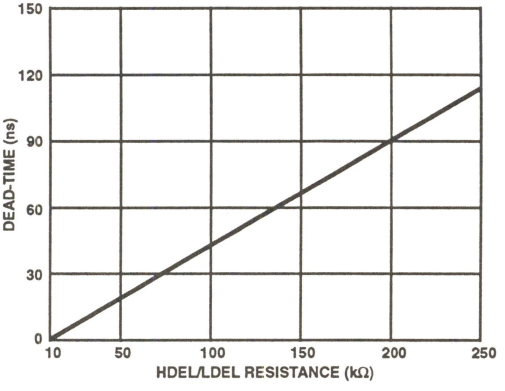


FIGURE 31. MINIMUM DEAD-TIME vs DEL RESISTANCE

HIP4080 Power-up Application Information

The HIP4080 H-Bridge Driver IC requires external circuitry to assure reliable start-up conditions of the upper drivers. If not addressed in the application, the H-Bridge power MOSFETs may be exposed to shoot-through current, possibly leading to MOSFET failure. Following the instructions below will result in reliable start-up.

The HIP4080 does not have an input protocol like the HIP4081 that keeps both lower power MOSFETs off other than through the DIS pin. IN+ and IN- are inputs to a comparator that control the bridge in such a way that only one of the lower power devices is on at a time, assuming DIS is low.

However, keeping both lower MOSFETs off can be accomplished by controlling the lower turn-on delay pin, LDEL, while the chip is enabled, as shown in Figure 32. Pulling LDEL to V_{DD} will indefinitely delay the lower turn-on delays through the input comparator and will keep the lower MOSFETs off. With the lower MOSFETs off and the chip enabled, i.e. DIS = low, IN+ or IN- can be switched through a full cycle, properly setting the upper driver outputs. Once this is accomplished, LDEL is released to its normal operating point. It is critical that IN+/IN- switch a full cycle while LDEL is held high, to avoid shoot-through. This start-up procedure can be initiated by the supply voltage and/or the chip enable command by the circuit in Figure 32.

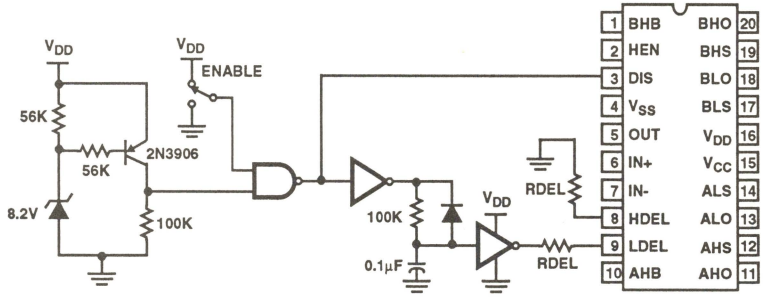
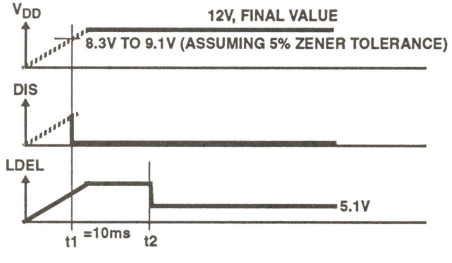


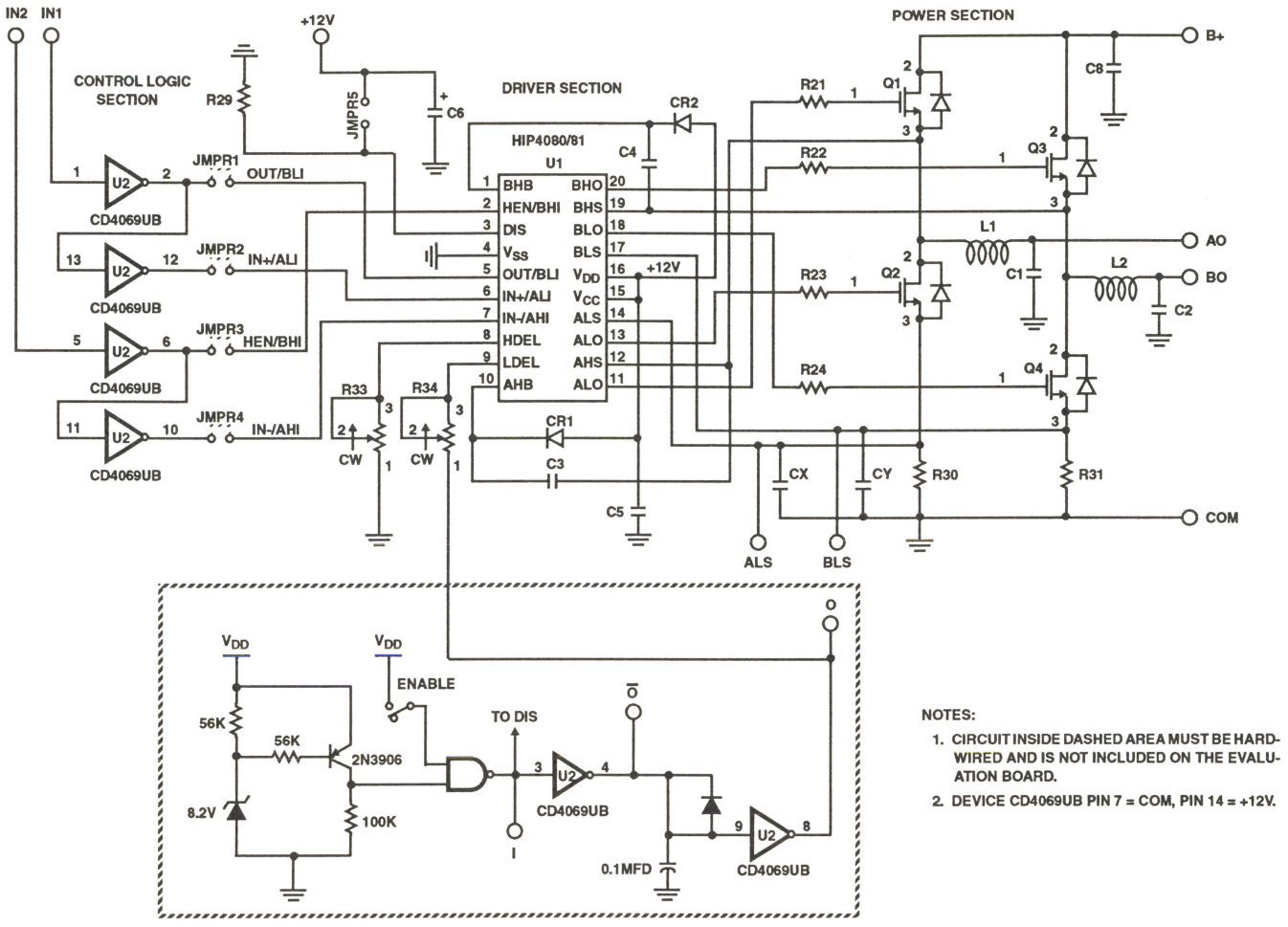
FIGURE 32.



TIMING DIAGRAM FOR FIGURE 32

NOTE:

1. Between t1 and t2 the IN+ and IN- inputs must cause the OUT pin to go through one complete cycle (transition order is not important). If the ENABLE pin is low after the under-voltage circuit is satisfied, the ENABLE pin will initiate the 10ms time delay during which the IN+ and IN- pins must cycle at least once.
2. Another product, HIP4080A, incorporates undervoltage circuitry which eliminates the need for the above power up circuitry.



NOTES:

1. CIRCUIT INSIDE DASHED AREA MUST BE HARD-WIRED AND IS NOT INCLUDED ON THE EVALUATION BOARD.
2. DEVICE CD4069UB PIN 7 = COM, PIN 14 = +12V.

FIGURE 33. HIP4080 EVALUATION PC BOARD SCHEMATIC

FIGURE 34. HIP4080 EVALUATION BOARD SILKSCREEN

HARRIS SEMICONDUCTOR

HIP4080A

PRELIMINARY

April 1994

80V/2.5A Peak, High Frequency Full Bridge FET Driver

Features

- Drives N-Channel FET Full Bridge Including High Side Chop Capability
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load at 1MHz in Free Air at +50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time,
- Charge-Pump and Bootstrap Maintain Upper Bias Supplies
- DIS (Disable) Pin Pulls Gates Low
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption
- Undervoltage Protection

Applications

- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Class D Audio Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

Description

The HIP4080A is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4080A includes an input comparator, used to facilitate the "hysteresis" and PWM modes of operation. Its HEN (high enable) lead can force current to freewheel in the bottom two external power MOSFETs, maintaining the upper power MOSFETs off. Since it can switch at frequencies up to 1MHz, the HIP4080A is well suited for driving Voice Coil Motors, switching amplifiers in class D high-frequency switching audio amplifiers and power supplies.

HIP4080A can also drive medium voltage brush motors, and two HIP4080As can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in precise control of the driven load.

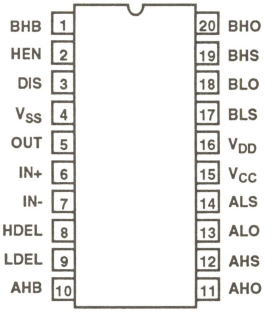
The similar HIP4081 IC allows independent control of all 4 FETs in an Full Bridge configuration.

Ordering Information

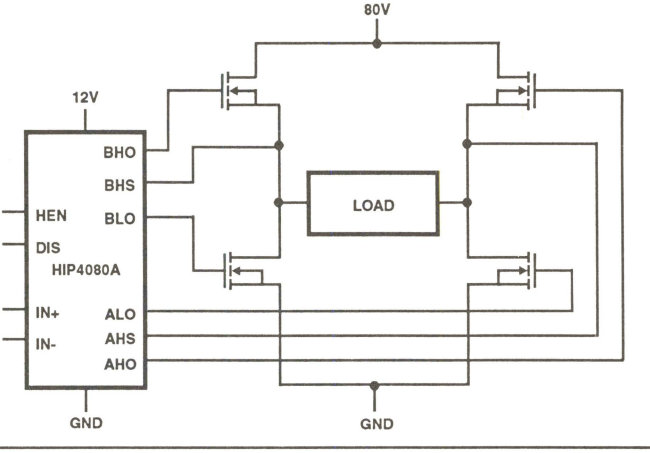
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4080AIP	-40°C to +85°C	20 Lead Plastic DIP
HIP4080AIB	-40°C to +85°C	20 Lead Plastic SOIC (W)
HIP4080AIW	-40°C to +85°C	Wafer
HIP4080AIY	-40°C to +85°C	Die

Pinout

HIP4080A (PDIP, SOIC)
TOP VIEW



Application Block Diagram

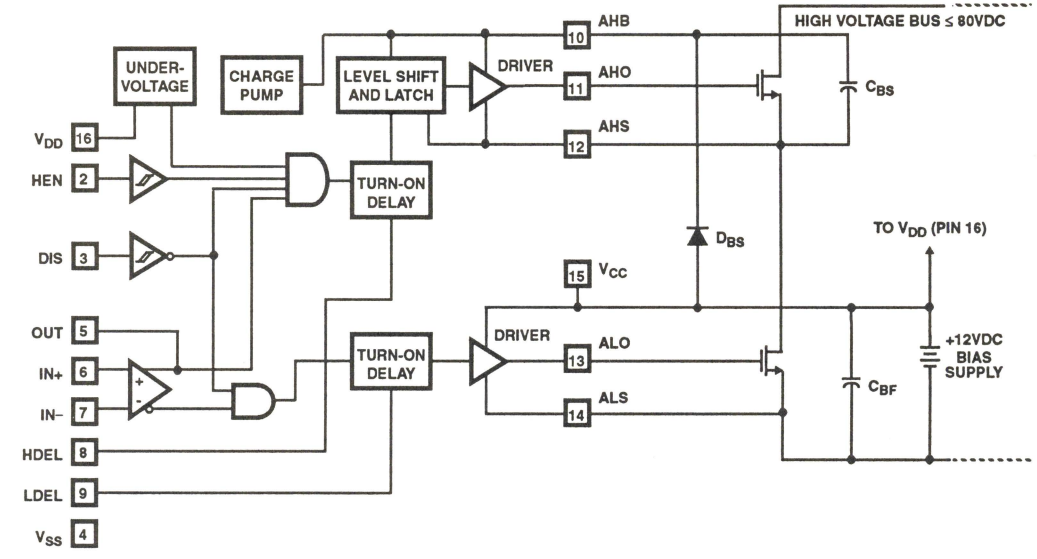


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

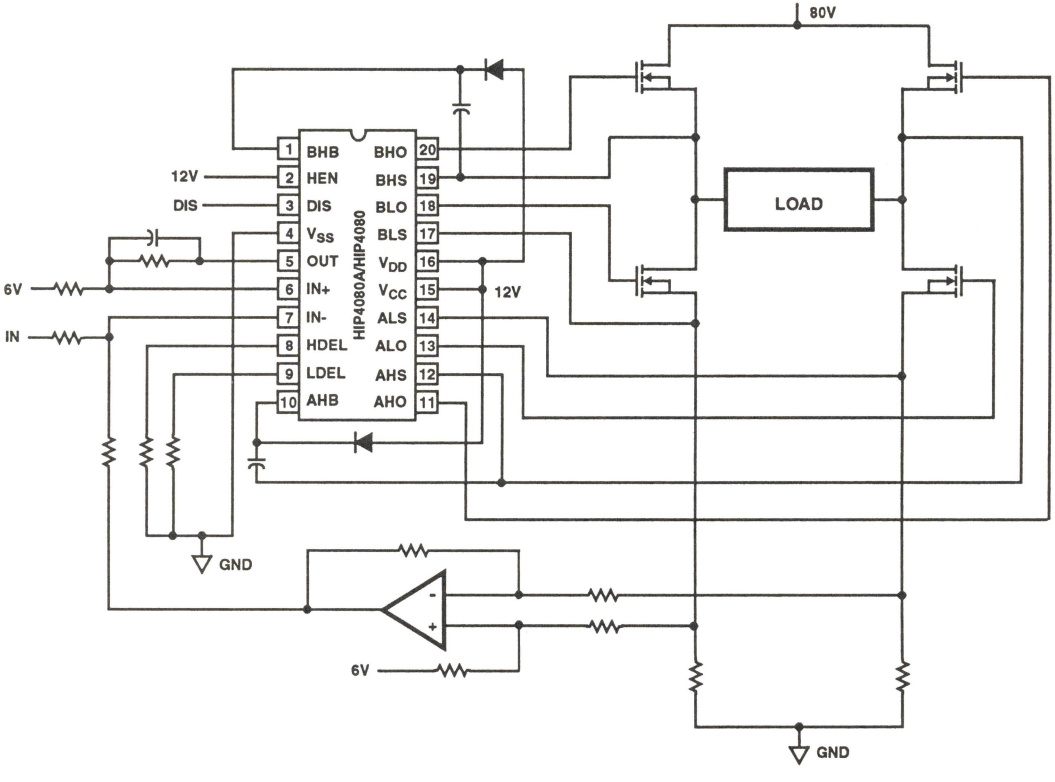
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File Number **3658.1**

Functional Block Diagram (1/2 HIP4080A)



Typical Application (Hysteresis Mode Switching)



Absolute Maximum Ratings

Supply Voltage, V_{DD} and V_{CC} ..... -0.3V to 16V
Logic I/O Voltages ..... -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS ..... -6.0V (Transient) to 88V
Voltage on ALS, BLS ..... -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB ..... $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +16V, or 95V whichever is less
Voltage on ALO, BLO ..... $V_{ALS, BLS}$ -0.3V to V_{CC} +0.3V
Voltage on AHO, BHO ..... $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V
Input Current, HDEL and LDEL ..... -5mA to 0mA
Phase Slew Rate 20V/ns
NOTE: All Voltages relative to pin 4, V_{SS}, unless otherwise specified.

Thermal Information

Thermal Resistance θ_{JA}
SOIC Package ..... +85°C/W
DIP Package ..... +75°C/W
Maximum Power Dissipation at +85°C
SOIC Package 470mW
DIP Package 530mW
Storage Temperature Range ..... -65°C to +150°C
Operating Max. Junction Temperature ..... +125°C
Lead Temperature (Soldering 10s) ..... +300°C
(For SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} ..... +9.5V to +15V
Voltage on ALS, BLS ..... -1.0V to +1.0V
Voltage on AHS, BHS ..... -1V to 80V
Voltage on AHB, BHB ..... $V_{AHS, BHS}$ +5V to $V_{AHS, BHS}$ +15V
Input Current, HDEL and LDEL ..... -500µA to -50µA
Operating Ambient Temperature Range ..... -40°C to +85°C

Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = - 40°C TO +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND CHARGE PUMPS								
V_{DD} Quiescent Current	I_{DD}	IN- = 2.5V, Other Inputs = 0V	8	11	14	7	14	mA
V_{DD} Operating Current	I_{DDO}	Outputs switching f = 500kHz, No Load	9	12	15	8	15	mA
V_{CC} Quiescent Current	I_{CC}	IN- = 2.5V, Other Inputs = 0V, $I_{ALO} = I_{BLO} = 0$	-	25	80	-	100	µA
V_{CC} Operating Current	I_{CCO}	f = 500kHz, No Load	1	1.25	2.0	0.8	3	mA
AHB, BHB Quiescent Current - Qpump Output Current	I_{AHB}, I_{BHB}	IN- = 2.5V, Other Inputs = 0V, $I_{AHO} = I_{BHO} = 0$, $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V$	-50	-25	-11	-60	-10	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 500kHz, No Load	0.62	1.2	1.5	0.5	1.9	mA
AHS, BHS, AHB, BHB Leakage Current	I_{HLK}	$V_{AHS} = V_{BHS} = V_{AHB} = V_{BHB} = 95V$	-	0.02	1.0	-	10	µA
AHB-AHS, BHB-BHS Qpump Output Voltage	$V_{AHB} - V_{AHS}$ $V_{BHB} - V_{BHS}$	$I_{AHB} = I_{AHB} = 0$, No Load	11.5	12.6	14.0	10.5	14.5	V
INPUT COMPARATOR PINS: IN+, IN-, OUT								
Offset Voltage	V_{OS}	Over Common Mode Voltage Range	-10	0	+10	-15	+15	mV
Input Bias Current	I_{IB}		0	0.5	2	0	4	µA
Input Offset Current	I_{OS}		-1	0	+1	-2	+2	µA
Input Common Mode Voltage Range	CMVR		1	-	V_{DD} -1.5	1	V_{DD} -1.5	V
Voltage Gain	AVOL		10	25	-	10	-	V/mV
OUT High Level Output Voltage	V_{OH}	IN+ > IN-, I_{OH} = -250µA	V_{DD} -0.4	-	-	V_{DD} - 0.5	-	V
OUT Low Level Output Voltage	V_{OL}	IN+ < IN-, I_{OL} = +250µA	-	-	0.4	-	0.5	V
Low Level Output Current	I_{OL}	V_{OUT} = 6V	6.5	14	19	6	20	mA
High Level Output Current	I_{OH}	V_{OUT} = 6V	-17	-10	-3	-20	-2.5	mA
INPUT PINS: DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	µA

Electrical Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
INPUT PINS: HEN								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	$V_{IN} = 0V$, Full Operating Conditions	-260	-200	-150	-270	-130	µA
High Level Input Current	I_{IH}	$V_{IN} = 5V$, Full Operating Conditions	-1	-	+1	-10	+10	µA
TURN-ON DELAY PINS: LDEL AND HDEL								
LDEL, HDEL Voltage	V_{HDEL},V	$I_{HDEL} = I_{LDEL} = -100µA$	4.9	5.1	5.3	4.8	5.4	V
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO								
Low Level Output Voltage	V_{OL}	$I_{OUT} = 100mA$	0.7	0.85	1.0	0.5	1.1	V
High Level Output Voltage	$V_{CC} - V_{OH}$	$I_{OUT} = -100mA$	0.8	0.95	1.1	0.5	1.2	V
Peak Pullup Current	I_{O+}	$V_{OUT} = 0V$	1.7	2.6	3.8	1.4	4.1	A
Peak Pulldown Current	I_{O-}	$V_{OUT} = 12V$	1.7	2.4	3.3	1.3	3.6	A
Under Voltage, Rising Threshold	UV+		8.1	8.8	9.4	8.0	9.5	V
Under Voltage, Falling Threshold	UV-		7.6	8.3	8.9	7.5	9.0	V
Under Voltage, Hysteresis	HYS		0.25	0.4	0.65	0.2	0.7	V

Switching Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, $C_L = 1000pF$, and $T_A = +25°C$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (IN+/IN- to ALO/BLO)	T_{LPHL}		-	40	70	-	90	ns
Upper Turn-off Propagation Delay (IN+/IN- to AHO/BHO)	T_{HPHL}		-	50	80	-	110	ns
Lower Turn-on Propagation Delay (IN+/IN- to ALO/BLO)	T_{LPLH}		-	40	70	-	90	ns
Upper Turn-on Propagation Delay (IN+/IN- to AHO/BHO)	T_{HPLH}		-	70	110	-	140	ns
Rise Time	T_R		-	10	25	-	35	ns
Fall Time	T_F		-	10	25	-	35	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$		50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$		40	-	-	40	-	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	45	75	-	95	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	55	85	-	105	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	T_{DLPLH}		-	45	70	-	90	ns
Refresh Pulse Width (ALO and BLO)	T_{REF-PW}		240	380	500	200	600	ns
Disable to Upper Enable (DIS - AHO and BHO)	T_{UEN}		-	480	630	-	750	ns
HEN-AHO, BHO Turn-off, Propagation Delay	$T_{HEN-PHL}$	$R_{HDEL} = R_{LDEL} = 10K$	-	40	70	-	90	ns
HEN-AHO, BHO Turn-on, Propagation Delay	$T_{HEN-PLH}$	$R_{HDEL} = R_{LDEL} = 10K$	-	60	90	-	110	ns

TRUTH TABLE

INPUT				OUTPUT			
IN+ > IN-	HEN	U/V	DIS	ALO	AHO	BLO	BHO
X	X	X	1	0	0	0	0
0	0	0	0	1	0	0	0
1	1	0	0	0	1	1	0
0	1	0	0	1	0	0	1
1	0	0	0	0	0	1	0
X	X	1	X	0	0	0	0

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	HEN	High-side Enable input. Logic level input that when low overrides IN+/IN- (Pins 6 and 7) to put AHO and BHO drivers (Pins 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by IN+/IN- inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold HEN high, so no connection is required if high-side and low-side outputs are to be controlled by IN+/IN- inputs.
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold DIS high if this pin is not driven.
4	V_{SS}	Chip negative supply, generally will be ground.
5	OUT	OUTput of the input control comparator. This output can be used for feedback and hysteresis.
6	IN+	Noninverting input of control comparator. If IN+ is greater than IN- (Pin 7) then ALO and BHO are low level outputs and BLO and AHO are high level outputs. If IN+ is less than IN- then ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (Pin 3) high level will override IN+/IN- control for all outputs. HEN (Pin 2) low level will override IN+/IN- control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (Pins 8 and 9).
7	IN-	Inverting input of control comparator. See IN+ (Pin 6) description.
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (Pin 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (Pin 15). De-couple this pin to V_{SS} (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

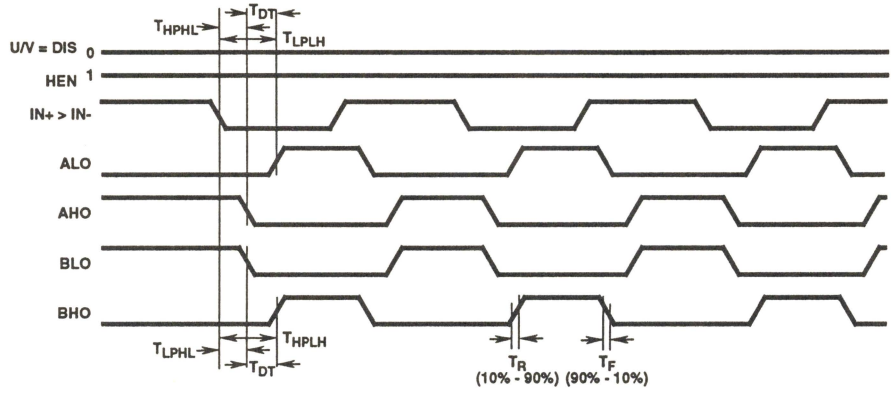


FIGURE 1. BISTATE MODE

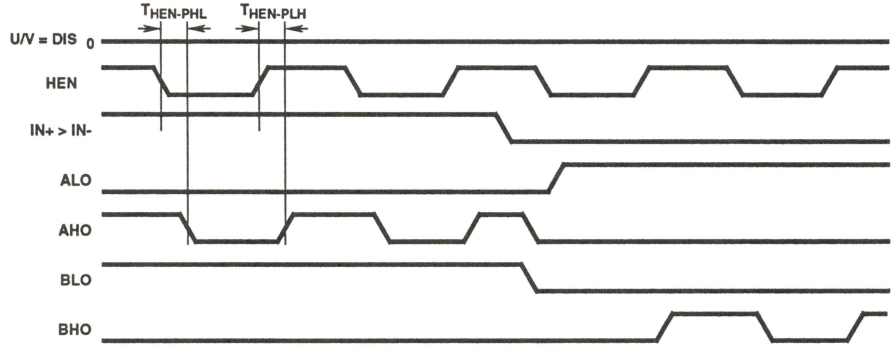


FIGURE 2. HIGH SIDE CHOP MODE

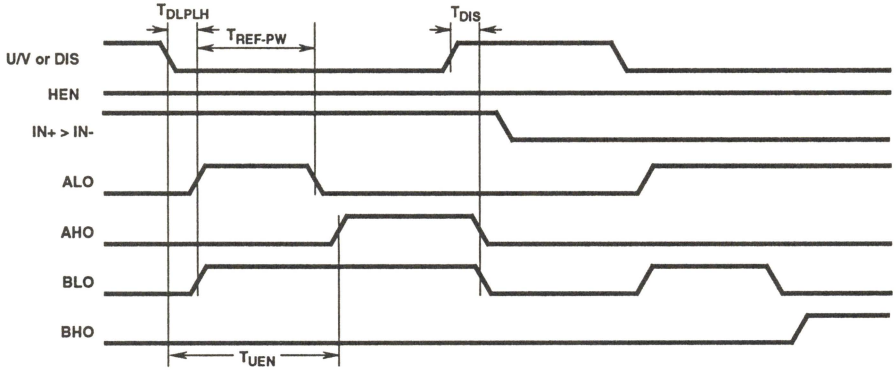


FIGURE 3. DISABLE FUNCTION

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

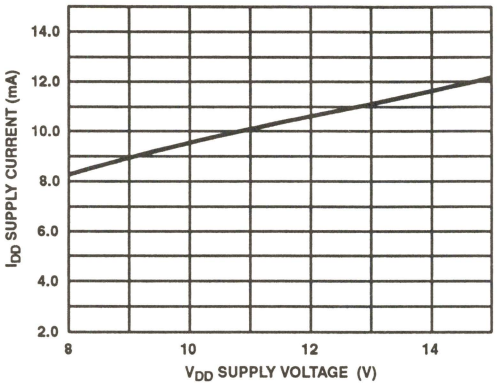


FIGURE 4. QUIESCENT I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

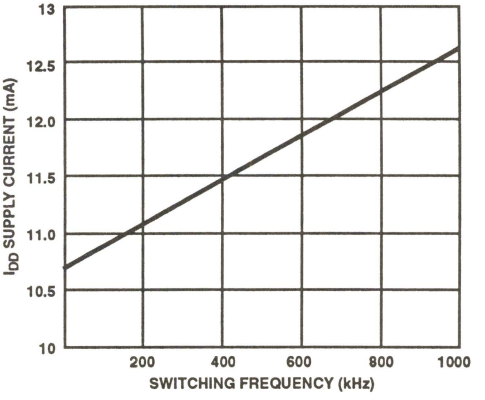


FIGURE 5. I_{DDO} NO-LOAD I_{DD} SUPPLY CURRENT vs FREQUENCY (kHz)

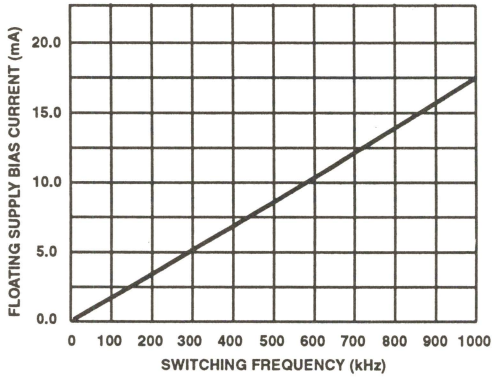


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

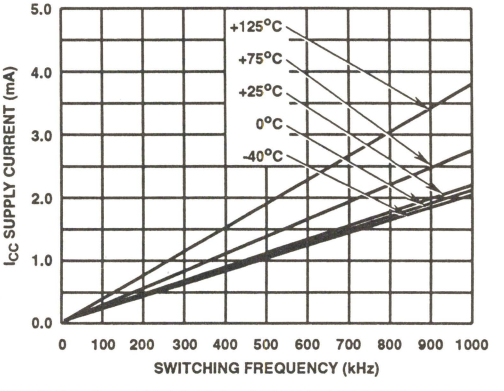


FIGURE 7. I_{CCO}, NO-LOAD I_{CC} SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

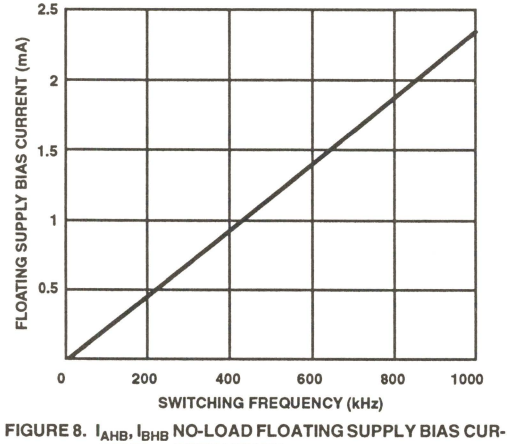


FIGURE 8. I_{AHB}, I_{BHB} NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

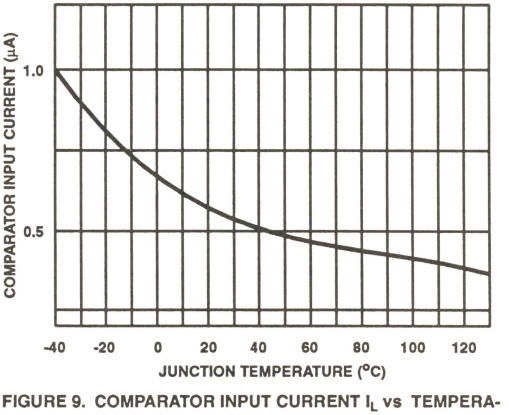


FIGURE 9. COMPARATOR INPUT CURRENT I_L vs TEMPERATURE AT $V_{CM} = 5$ V

Typical Performance Curves

V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V, V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V, R_{HDEL} = R_{LDEL} = 100K, and T_A = +25°C, Unless Otherwise Specified **(Continued)**

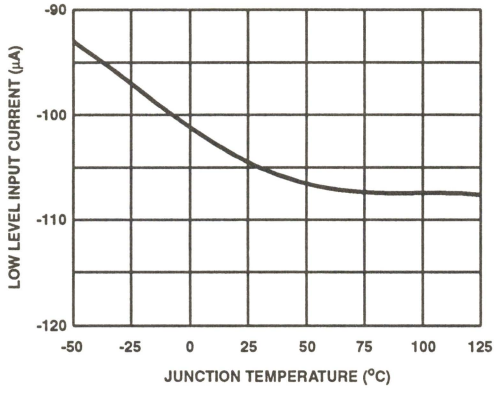


FIGURE 10. DIS LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

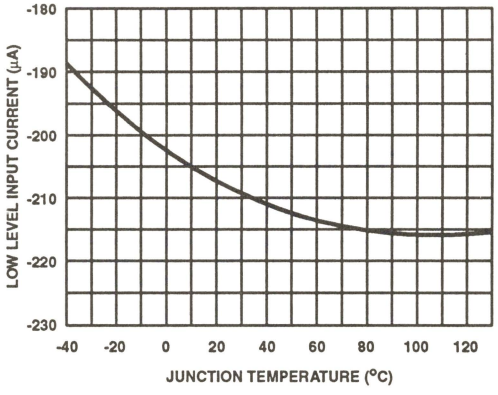


FIGURE 11. HEN LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

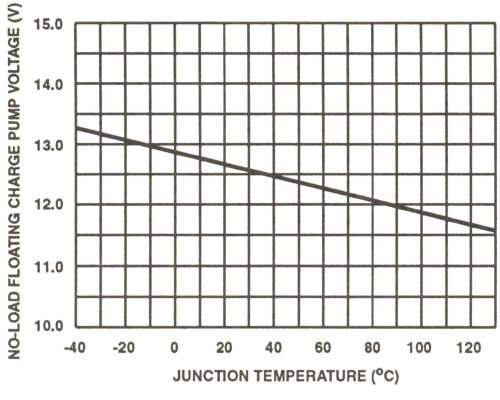


FIGURE 12. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

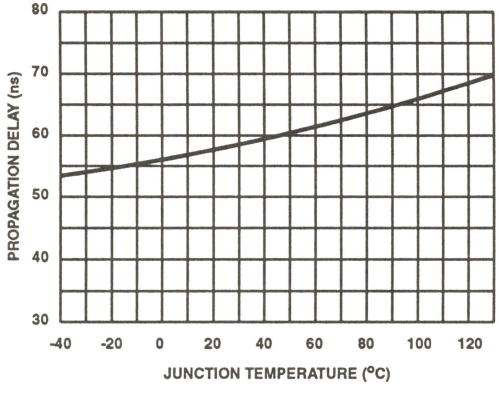


FIGURE 13. UPPER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISHIGH}$ vs TEMPERATURE

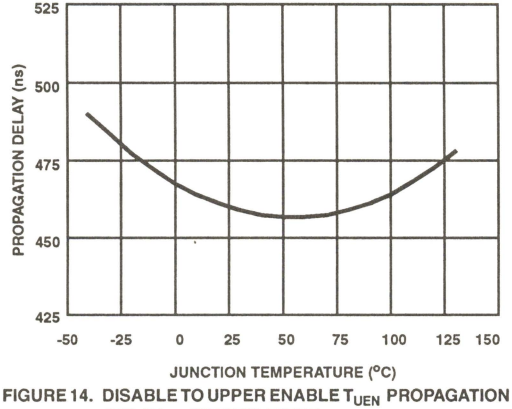


FIGURE 14. DISABLE TO UPPER ENABLE T_{UEN} PROPAGATION DELAY vs TEMPERATURE

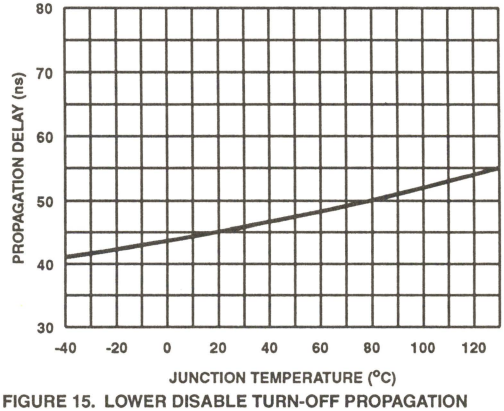


FIGURE 15. LOWER DISABLE TURN-OFF PROPAGATION DELAY T_{DISLOW} vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, and $T_A = +25°C$, Unless Otherwise Specified

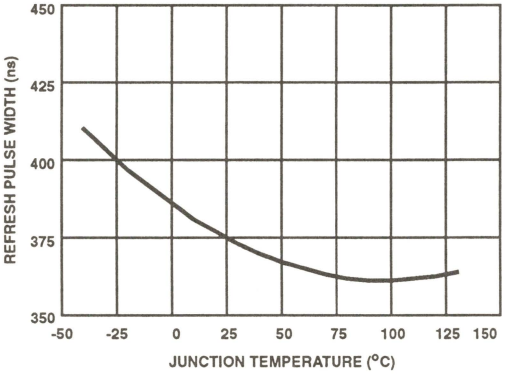


FIGURE 16. T_{REF-PW} REFRESH PULSE WIDTH vs TEMPERATURE

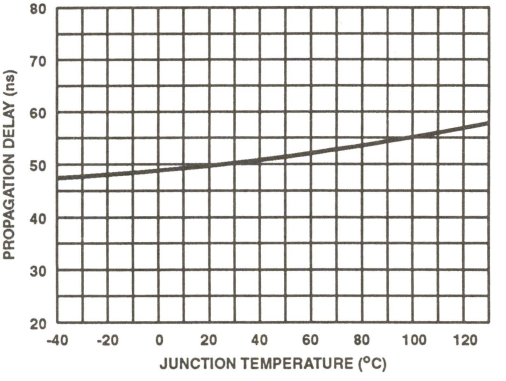


FIGURE 17. DISABLE TO LOWER ENABLE TDLPLH PROPAGATION DELAY vs TEMPERATURE

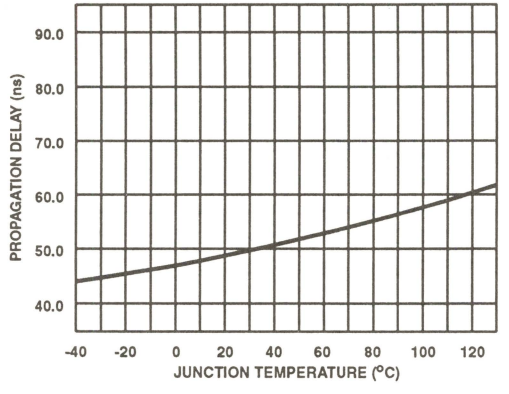


FIGURE 18. UPPER TURN-OFF PROPAGATION DELAY T_{HPHL} vs TEMPERATURE

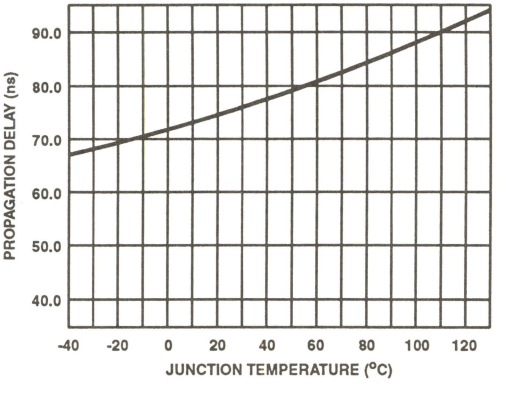


FIGURE 19. UPPER TURN-ON PROPAGATION DELAY THPLH vs TEMPERATURE

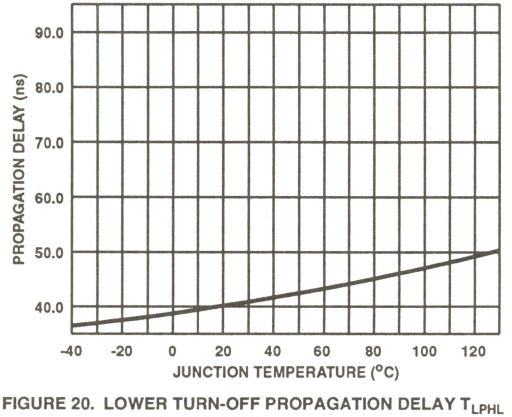


FIGURE 20. LOWER TURN-OFF PROPAGATION DELAY T_{LPHL} vs TEMPERATURE

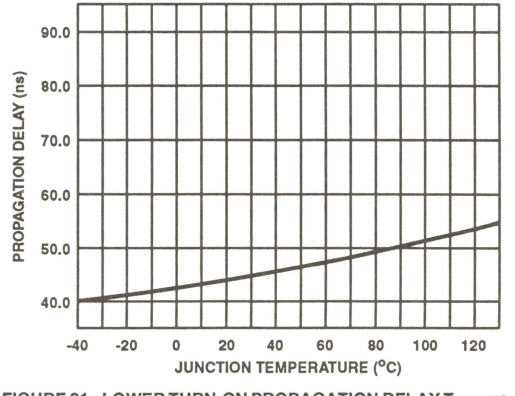


FIGURE 21. LOWER TURN-ON PROPAGATION DELAY T_{LPLH} vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

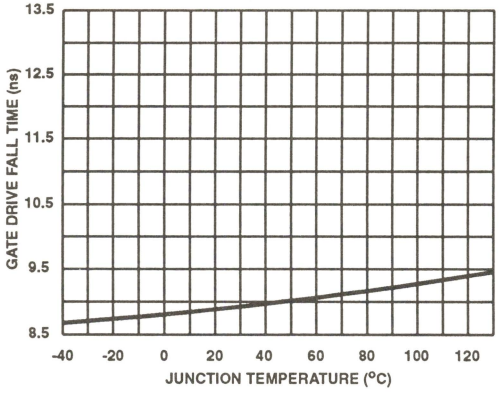


FIGURE 22. GATE DRIVE FALL TIME T_F vs TEMPERATURE

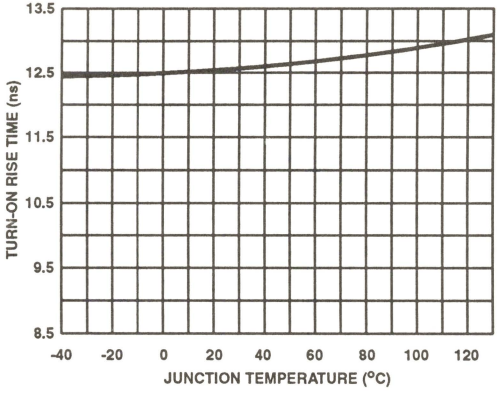


FIGURE 23. GATE DRIVE RISE TIME T_R vs TEMPERATURE

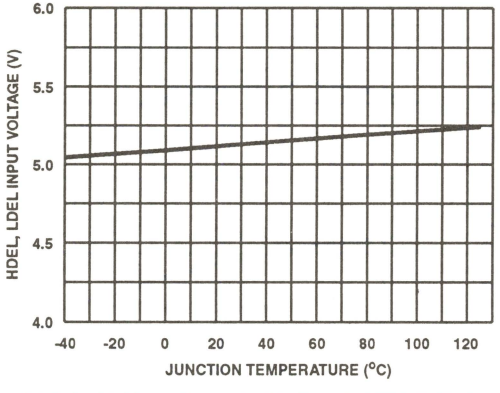


FIGURE 24. V_{LDEL}, V_{HDEL} VOLTAGE vs TEMPERATURE

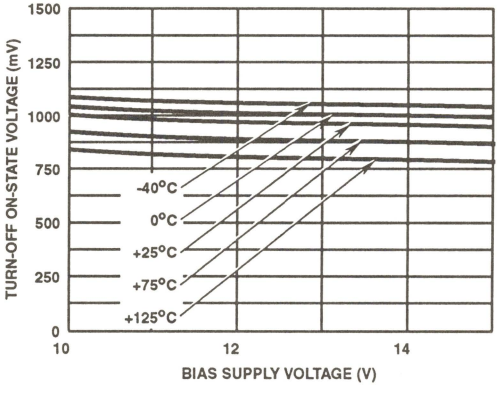


FIGURE 25. HIGH LEVEL OUTPUT VOLTAGE, $V_{CC} - V_{OH}$ vs BIAS SUPPLY AND TEMPERATURE AT 100µA

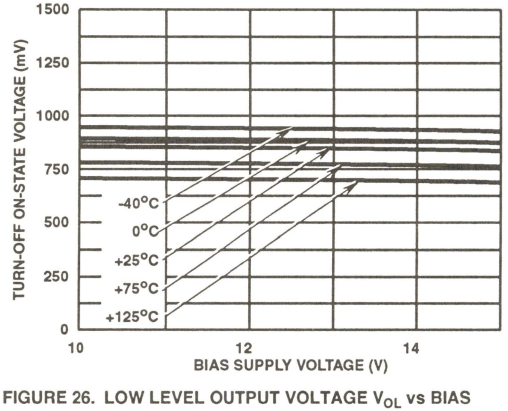


FIGURE 26. LOW LEVEL OUTPUT VOLTAGE V_{OL} vs BIAS SUPPLY AND TEMPERATURE AT 100µA

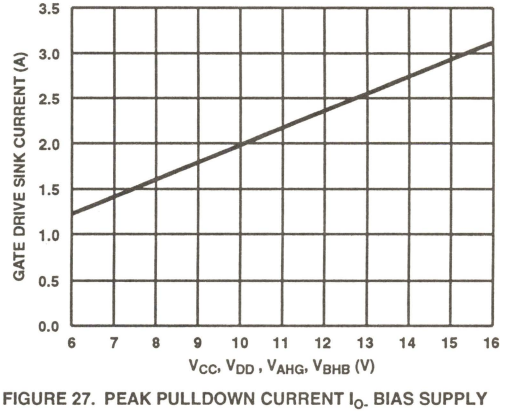


FIGURE 27. PEAK PULLDOWN CURRENT I_O. BIAS SUPPLY VOLTAGE

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K, and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

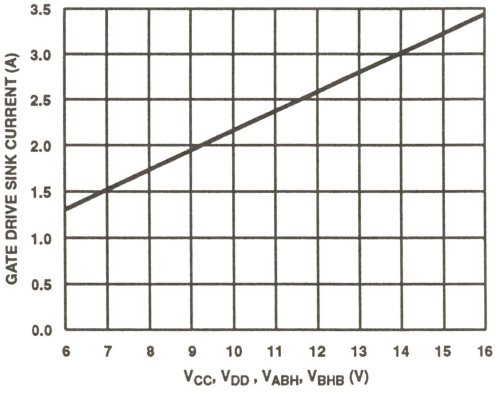


FIGURE 28. PEAK PULLUP CURRENT I_{O+} vs SUPPLY VOLTAGE

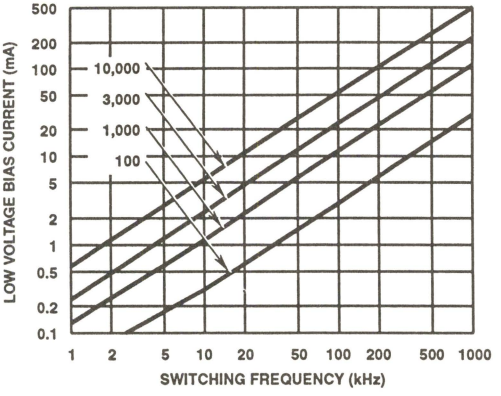


FIGURE 29. LOW VOLTAGE BIAS CURRENT I_{DD} AND I_{CC} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

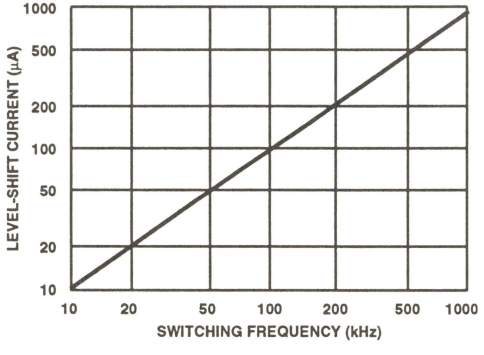


FIGURE 30. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

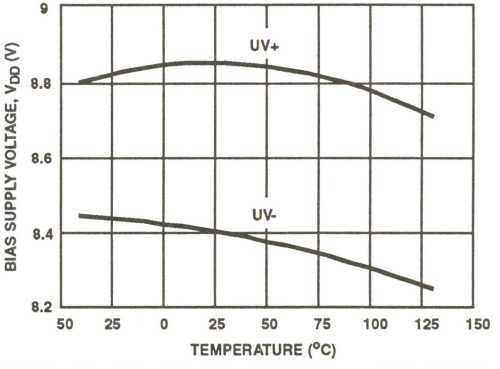


FIGURE 31. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

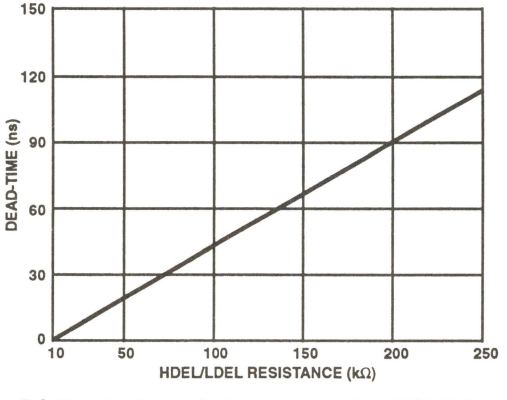
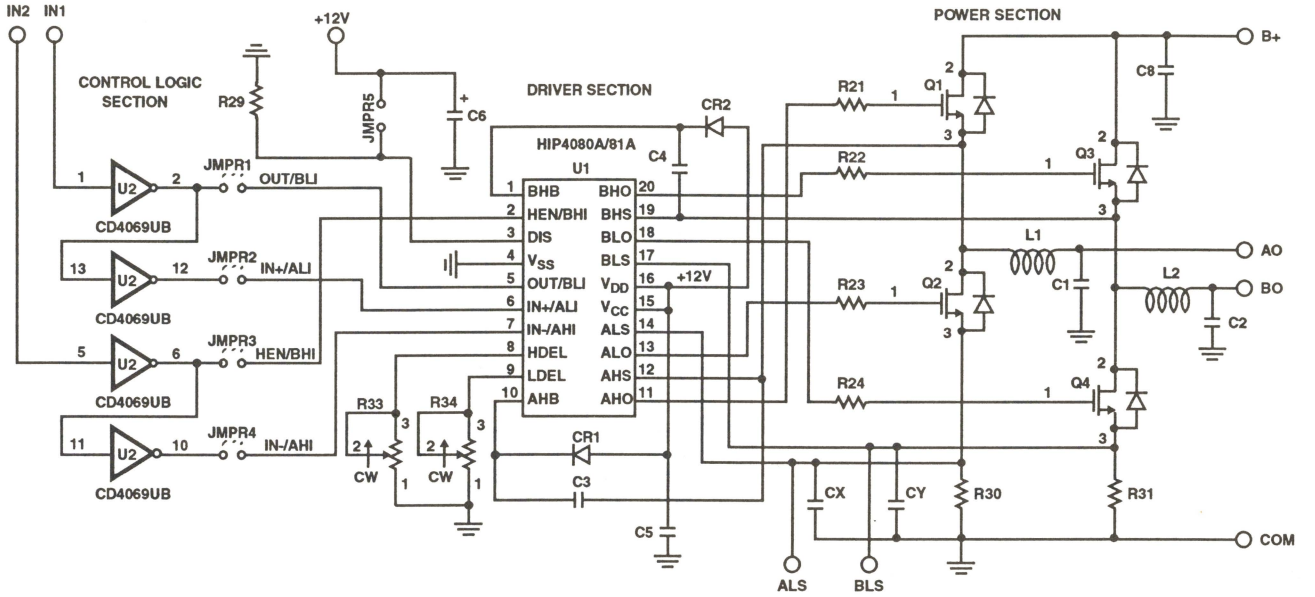


FIGURE 32. MINIMUM DEAD-TIME vs DEL RESISTANCE



NOTE:

DEVICE CD4069UB PIN 7 = COM, PIN 14 = +12V.

FIGURE 33. HIP4080A EVALUATION PC BOARD SCHEMATIC

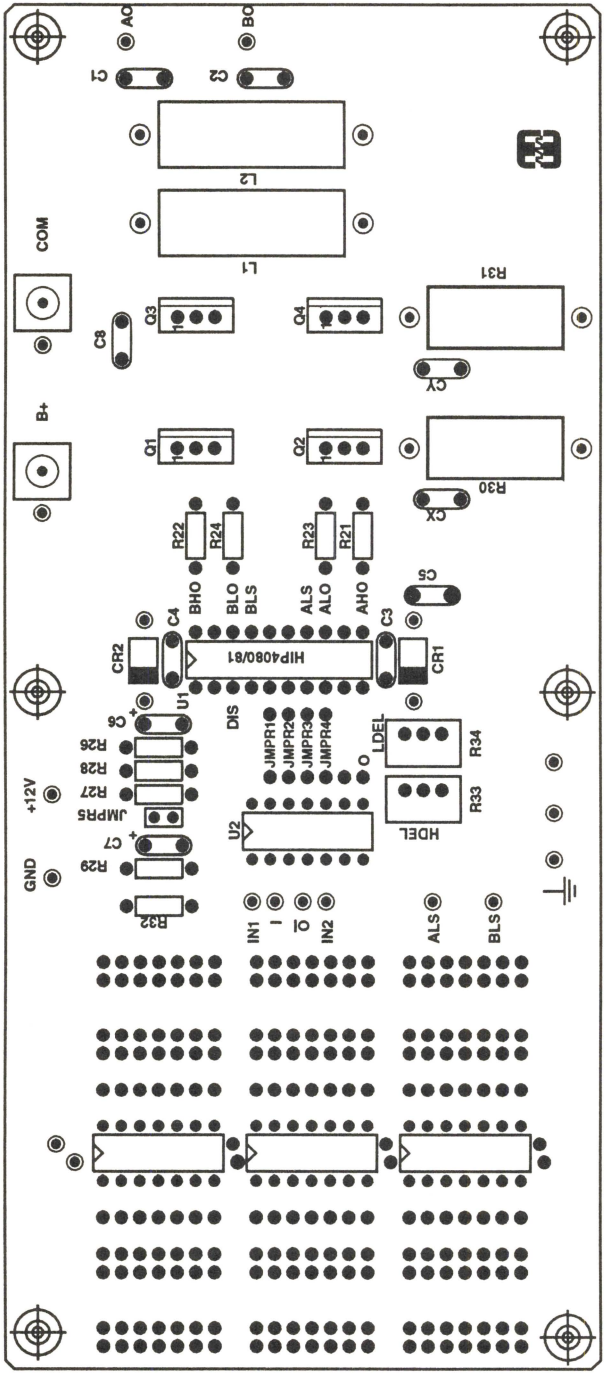


FIGURE 34. HIP4080A EVALUATION BOARD SILKSCREEN

HARRIS SEMICONDUCTOR

HIP4081

80V/2.5A Peak, High Frequency Full Bridge FET Driver

April 1994

Features

- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load at 1MHz in Free Air at +50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- On-Chip Charge-Pump and Bootstrap Upper Bias Supplies
- DIS (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption

Applications

- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Class D Audio Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

Description

The HIP4081 is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4081 can drive every possible switch combination except those which would cause a shoot-through condition. The HIP4081 can switch at frequencies up to 1MHz and is well suited to driving Voice Coil Motors, high-frequency Class D audio amplifiers, and power supplies.

For example, the HIP4081 can drive medium voltage brush motors, and two HIP4081s can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in rapid, precise control of the driven load.

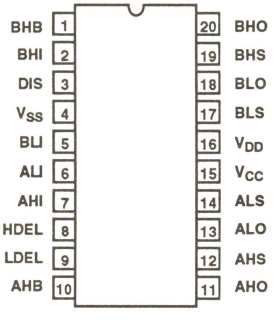
A similar part, the HIP4080, includes an on-chip input comparator to create a PWM signal from an external triangle wave and to facilitate "hysteresis mode" switching.

Ordering Information

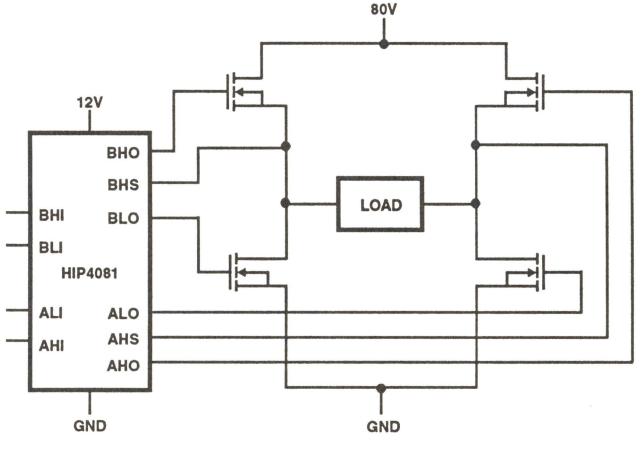
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4081IP	-40°C to +85°C	20 Lead Plastic DIP
HIP4081IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

Pinout

HIP4081 (PDIP, SOIC)
TOP VIEW



Application Block Diagram

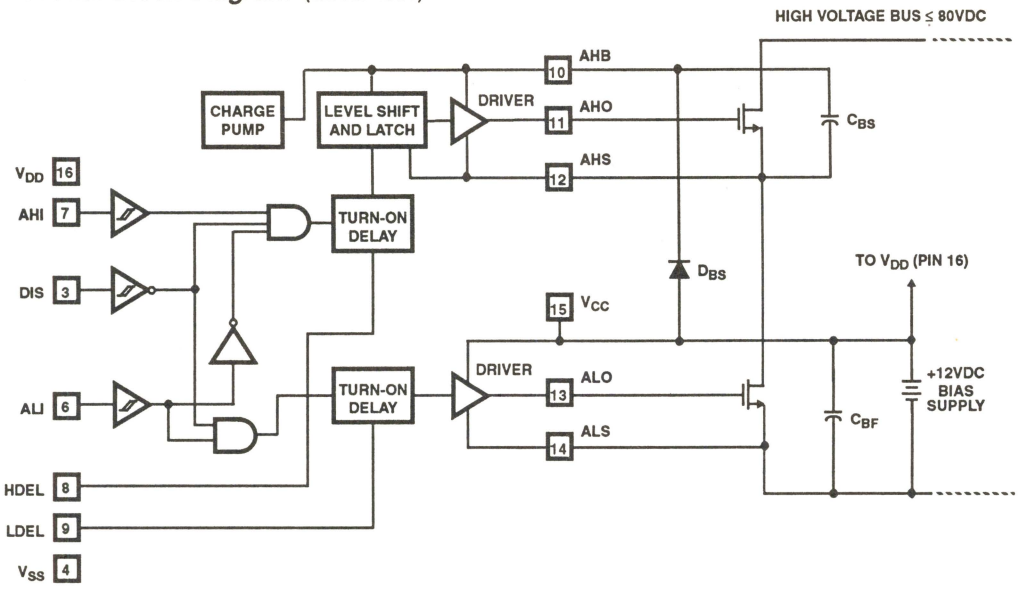


6 FULL BRIDGE

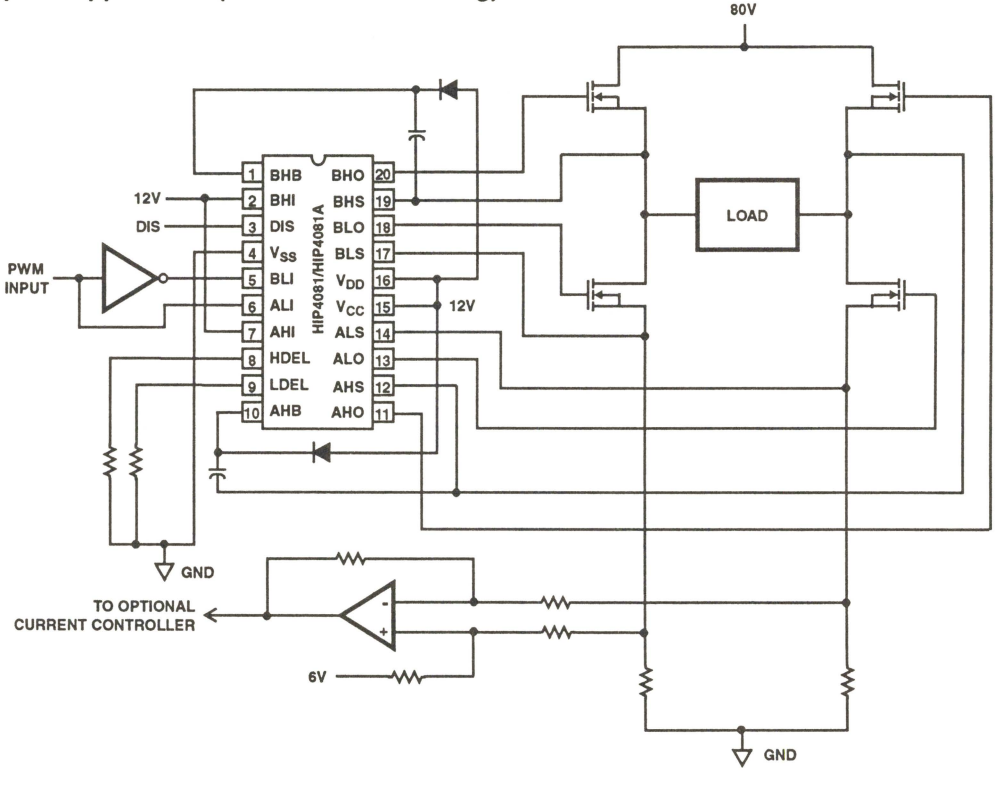
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3556.4

Functional Block Diagram (1/2 HIP4081)



Typical Application (PWM Mode Switching)



Absolute Maximum and Thermal Ratings

Supply Voltage, V_{DD} and V_{CC} ..... -0.3V to 16V
Logic I/O Voltages ..... -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS ..... -6.0V (Transient) to 88V
Voltage on ALS, BLS ..... -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB ..... $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +16V, or 95V, whichever is less
Voltage on ALO, BLO ..... $V_{ALS, BLS}$ -0.3V to V_{CC} +0.3V
Voltage on AHO, BHO ..... $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V
Input Current, HDEL and LDEL ..... -5mA to 0mA
Phase Slew Rate 20V/ns
NOTE: All voltages are relative to pin 4, V_{SS}, unless otherwise specified.

Storage Temperature Range ..... -65°C to +150°C
Operating Max. Junction Temperature ..... +125°C
Lead Temperature (Soldering 10s) ..... +300°C
(For SOIC - Lead Tips Only)
Thermal Resistance, Junction-Ambient
SOIC Package ..... 85°C/W
DIP Package ..... 75°C/W
Maximum Power Dissipation at +85°C
SOIC Package 470mW
DIP Package 530mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} ..... +6V to +15V
Voltage on ALS, BLS ..... -1.0V to +1.0V
Voltage on AHS, BHS ..... -1V to 80V
Voltage on AHB, BHB ..... $V_{AHS, BHS}$ +5V to $V_{AHS, BHS}$ +15V
Input Current, HDEL and LDEL ..... -500µA to -50µA
Operating Ambient Temperature Range ..... -40°C to +85°C

Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = +25°C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_{JS} = -40°C TO +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND CHARGE PUMPS								
V_{DD} Quiescent Current	I_{DD}	All Inputs = 0V	7	9	11	6	12	mA
V_{DD} Operating Current	I_{DDO}	Outputs Switching f = 500kHz	8	9.5	12	7	13	mA
V_{CC} Quiescent Current	I_{CC}	All Inputs = 0V, $I_{ALO} = I_{BLO} = 0$	-	0.1	10	-	20	µA
V_{CC} Operating Current	I_{CCO}	f = 500kHz, No Load	1	1.25	2.0	0.8	3	mA
AHB, BHB Quiescent Current - Qpump Output Current	I_{AHB}, I_{BHB}	All Inputs = 0V, $I_{AHO} = I_{BHO} = 0$ $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V$	-50	-30	-15	-60	-10	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 500kHz, No Load	0.5	0.9	1.3	0.4	1.7	mA
AHS, BHS, AHB, BHB Leakage Current	I_{HLK}	$V_{AHS} = V_{BHS} = V_{AHB} = V_{BHB} = 95V$	-	0.02	1.0	-	10	µA
AHB-AHS, BHB-BHS Qpump Output Voltage	V_{AHB}-V_{AHS} V_{BHB}-V_{BHS}	$I_{AHB} = I_{AHB} = 0$, No Load	11.5	12.6	14.0	10.5	14.5	V
INPUT PINS: ALI, BLI, AHI, BHI, AND DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	µA
TURN-ON DELAY PINS: LDEL AND HDEL								
LDEL, HDEL Voltage	V_{HDEL}, V_{LDEL}	$I_{HDEL} = I_{LDEL}$ = -100µA	4.9	5.1	5.3	4.8	5.4	V
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO								
Low Level Output Voltage	V_{OL}	I_{OUT} = 100mA	0.7	0.85	1.0	0.5	1.1	V
High Level Output Voltage	V_{CC}-V_{OH}	I_{OUT} = -100mA	0.8	.95	1.1	0.5	1.2	V
Peak Pullup Current	I_O+	V_{OUT} = 0V	1.7	2.6	3.8	1.4	4.1	A
Peak Pulldown Current	I_O-	V_{OUT} = 12V	1.7	2.4	3.3	1.3	3.6	A

Switching Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, $C_L = 1000pF$

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_{JS} = -40°C TO +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPHL}		-	30	60	-	80	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPHL}		-	35	70	-	90	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPLH}		-	45	70	-	90	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPLH}		-	60	90	-	110	ns
Rise Time	T_R		-	10	25	-	35	ns
Fall Time	T_F		-	10	25	-	35	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$		50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$		40	-	-	40	-	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	45	75	-	95	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	55	85	-	105	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	T_{DLPLH}		-	35	70	-	90	ns
Refresh Pulse Width (ALO and BLO)	T_{REF-PW}		160	260	380	140	420	ns
Disable to Upper Enable (DIS - AHO and BHO)	T_{HEN}		-	335	500	-	550	ns

TRUTH TABLE

INPUT			OUTPUT	
ALI, BLI	AHI, BHI	DIS	ALO, BLO	AHO, BHO
X	X	1	0	0
1	X	0	1	0
0	1	0	0	1
0	0	0	0	0

NOTE: X signifies that input can be either a "1" or "0".

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 20). BLI (Pin 5) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold BHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold DIS high if this pin is not driven.
4	V_{SS}	Chip negative supply, generally will be ground.
5	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 18). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold BLI high if this pin is not driven.
6	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold ALI high if this pin is not driven.
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 11). ALI (Pin 6) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold AHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (Pin 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (Pin 15). De-couple this pin to V_{SS} (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

X = A OR B, A AND B HALVES OF BRIDGE CONTROLLER ARE INDEPENDENT

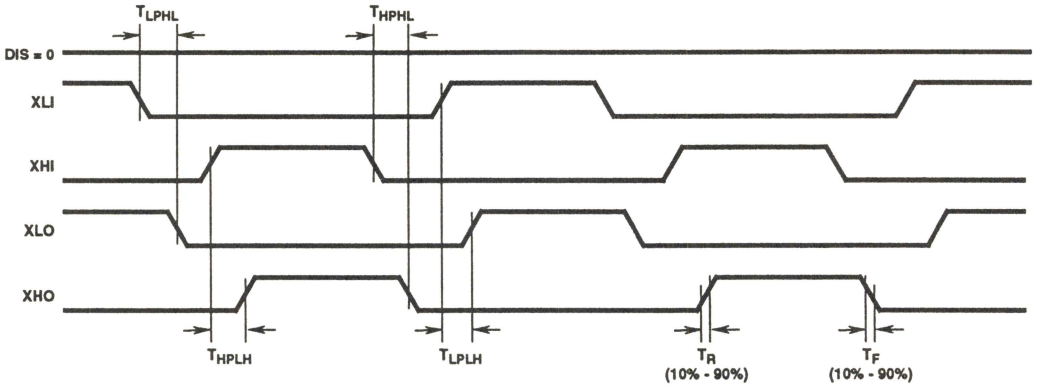


FIGURE 1. INDEPENDENT MODE

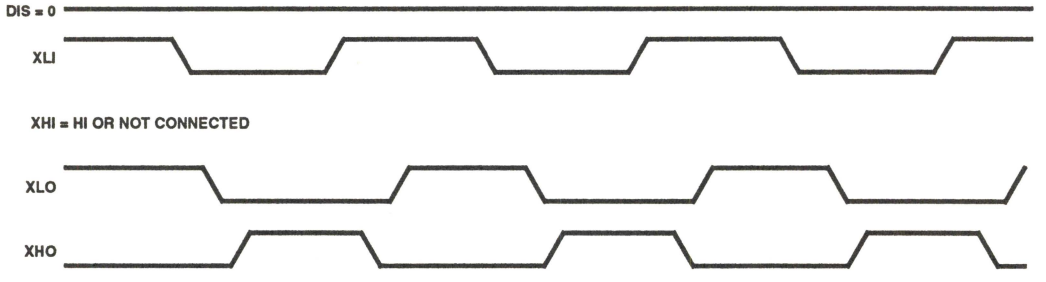


FIGURE 2. BISTATE MODE

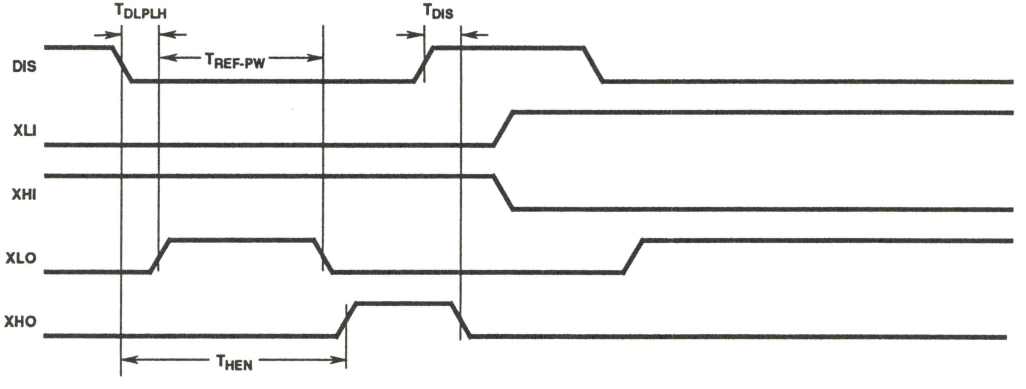


FIGURE 3. DISABLE FUNCTION

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = +25°C$, Unless Otherwise Specified

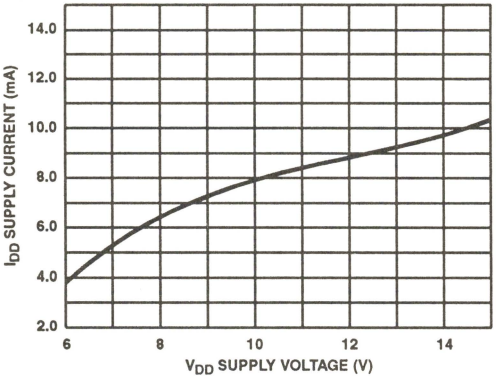


FIGURE 4. QUIESCENT I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

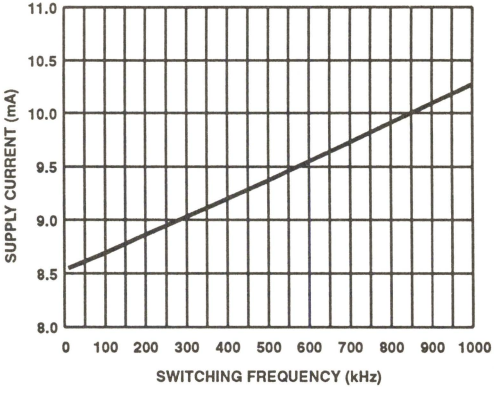


FIGURE 5. I_{DDO}, NO-LOAD I_{DD} SUPPLY CURRENT vs FREQUENCY (kHz)

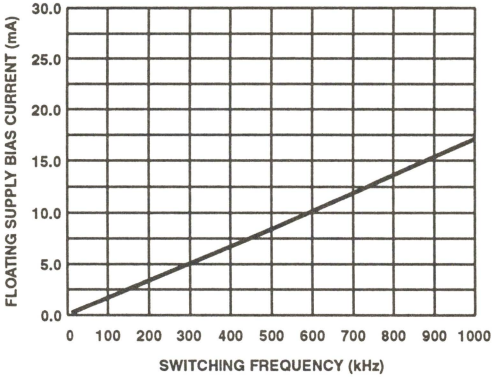


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

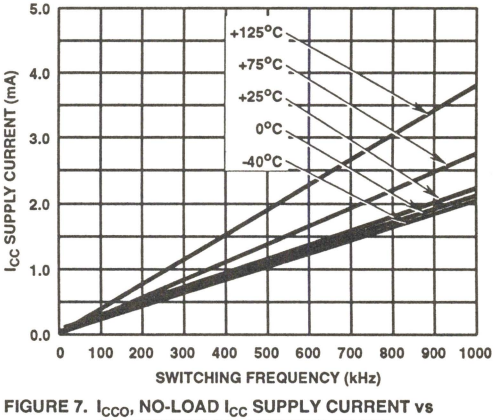


FIGURE 7. I_{CCO}, NO-LOAD I_{CC} SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

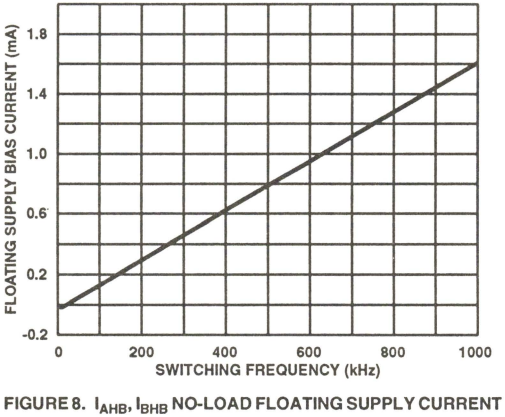


FIGURE 8. I_{AHB}, I_{BHB} NO-LOAD FLOATING SUPPLY CURRENT vs FREQUENCY

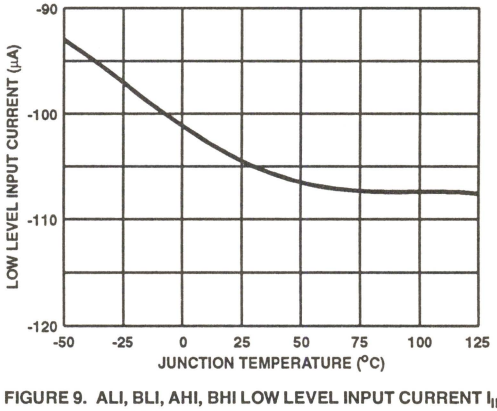


FIGURE 9. ALI, BLI, AHI, BHI LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

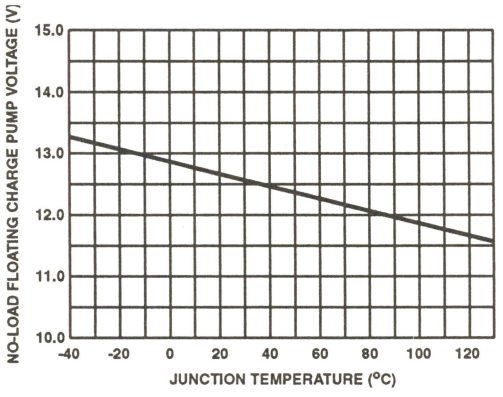


FIGURE 10. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

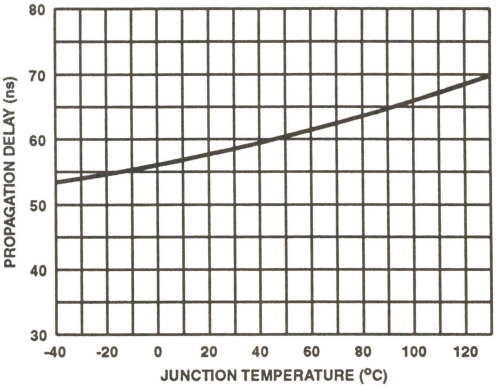


FIGURE 11. UPPER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISHIGH}$ vs TEMPERATURE

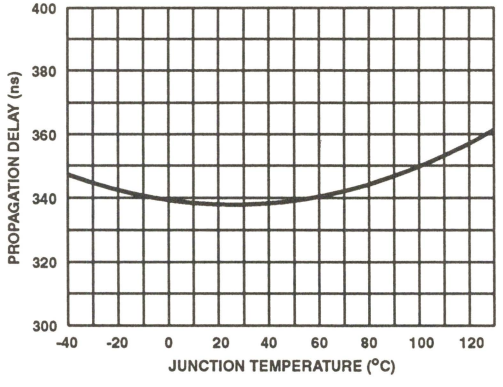


FIGURE 12. DISABLE TO UPPER ENABLE T_{UEN} PROPAGATION DELAY vs TEMPERATURE

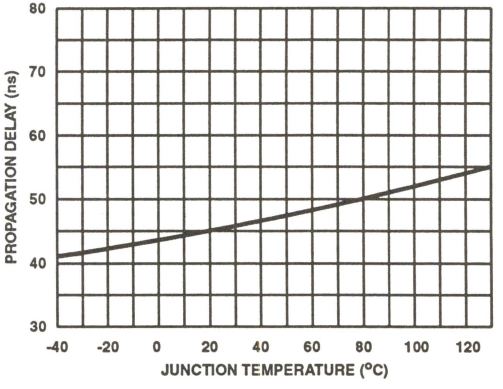


FIGURE 13. LOWER DISABLE TURN-OFF PROPAGATION DELAY T_{DISLO} vs TEMPERATURE

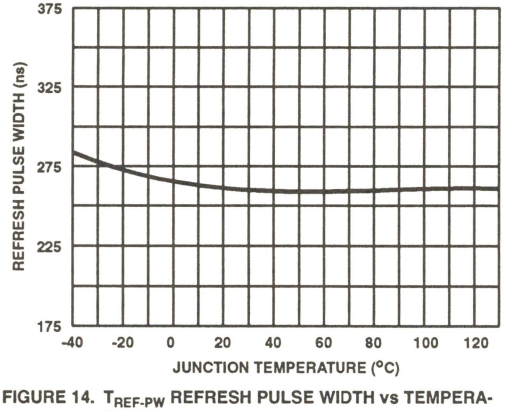


FIGURE 14. T_{REF-PW} REFRESH PULSE WIDTH vs TEMPERATURE

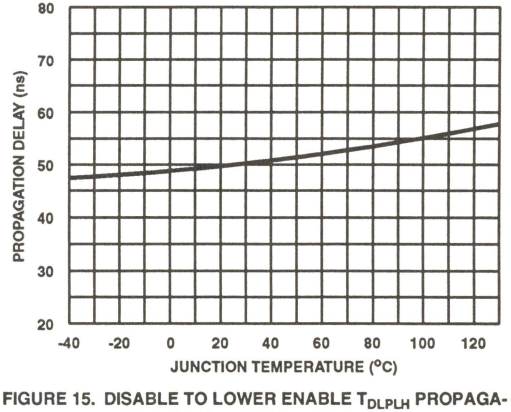


FIGURE 15. DISABLE TO LOWER ENABLE T_{DLPLH} PROPAGATION DELAY vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$ and $T_A = +25^oC$, Unless Otherwise Specified

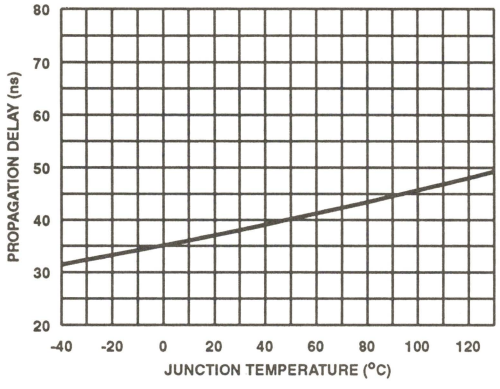


FIGURE 16. UPPER TURN-OFF PROPAGATION DELAY T_{HPHL} vs TEMPERATURE

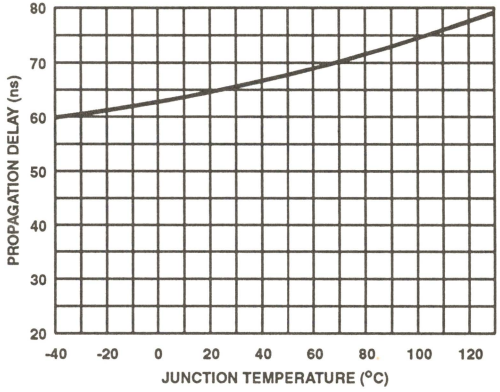


FIGURE 17. UPPER TURN-ON PROPAGATION DELAY T_{HPLH} vs TEMPERATURE

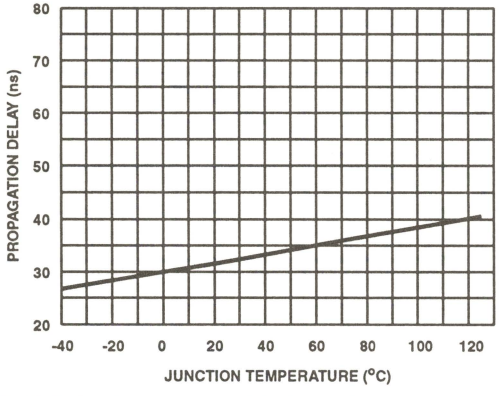


FIGURE 18. LOWER TURN-OFF PROPAGATION DELAY T_{LPHL} vs TEMPERATURE

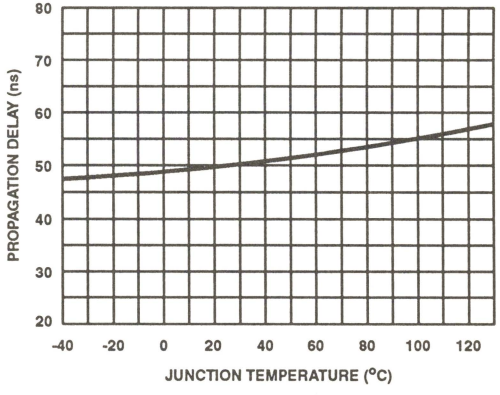


FIGURE 19. LOWER TURN-ON PROPAGATION DELAY T_{LPLH} vs TEMPERATURE

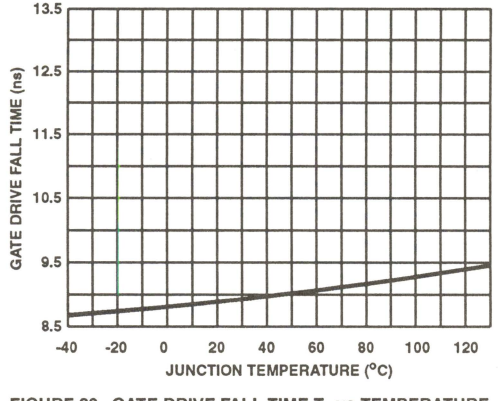


FIGURE 20. GATE DRIVE FALL TIME T_F vs TEMPERATURE

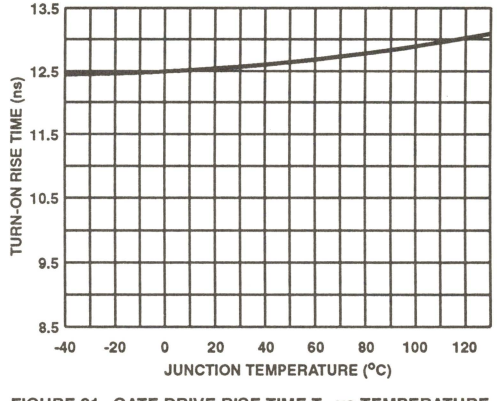


FIGURE 21. GATE DRIVE RISE TIME T_R vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = +25°C$, Unless Otherwise Specified

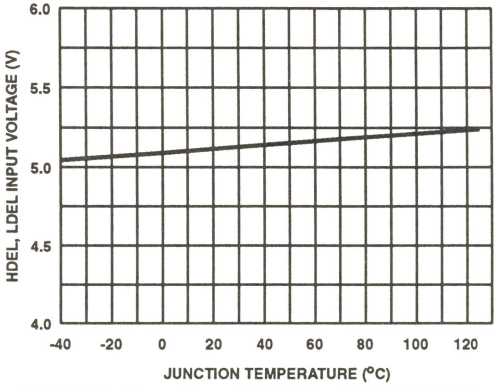


FIGURE 22. V_{LDEL}, V_{HDEL} VOLTAGE vs TEMPERATURE

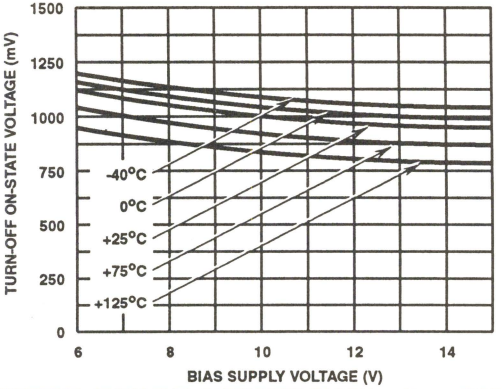


FIGURE 23. HIGH LEVEL OUTPUT VOLTAGE $V_{CC} - V_{OH}$ vs BIAS SUPPLY AND TEMPERATURE AT 100mA

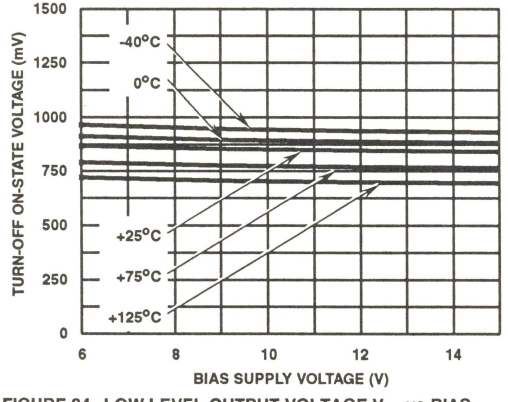


FIGURE 24. LOW LEVEL OUTPUT VOLTAGE V_{OL} vs BIAS SUPPLY AND TEMPERTURE AT 100mA

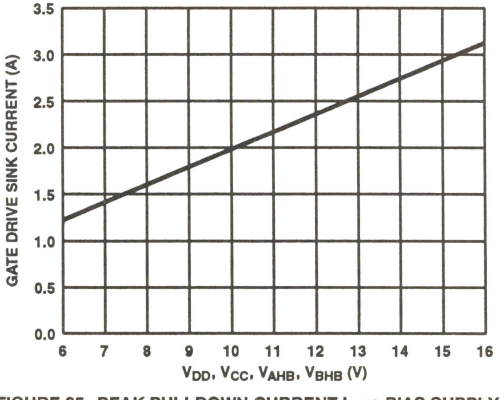


FIGURE 25. PEAK PULLDOWN CURRENT I_O vs BIAS SUPPLY VOLTAGE

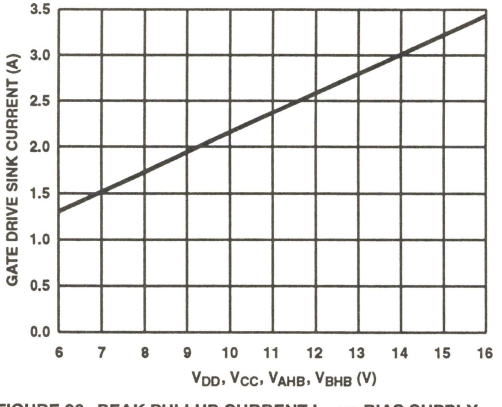


FIGURE 26. PEAK PULLUP CURRENT I_{O+} vs BIAS SUPPLY VOLTAGE

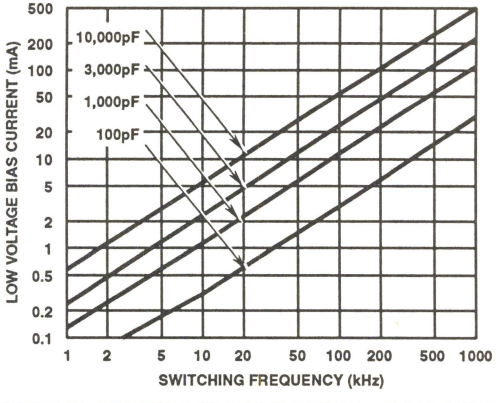


FIGURE 27. LOW VOLTAGE BIAS CURRENT I_{DD} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

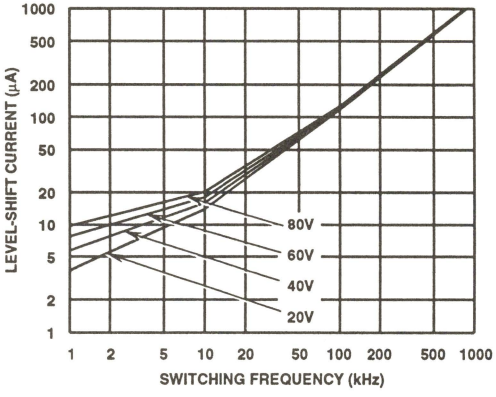


FIGURE 28. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

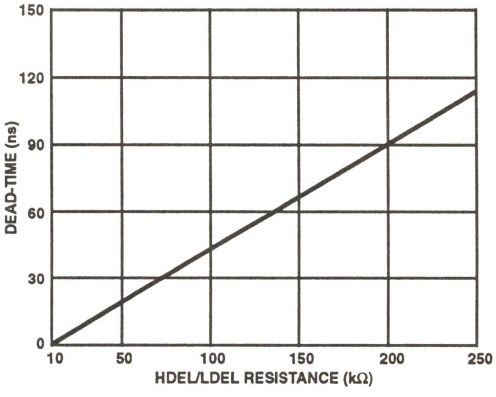


FIGURE 29. MINIMUM DEAD-TIME vs DEL RESISTANCE

HIP4081 Power-up Application Information

The HIP4081 H-Bridge Driver IC requires external circuitry to assure reliable start-up conditions of the upper drivers. If not addressed in the application, the H-bridge power MOSFETs may be exposed to shoot-through current, possibly leading to MOSFET failure. Following the instructions below will result in reliable start-up.

The HIP4081 has four inputs, one for each output. Outputs ALO and BLO are directly controlled by input ALI and BLI. By holding ALI and BLI low during start-up no shoot-through conditions can occur. To set the latches to the upper drivers such that the driver outputs, AHO and BHO, are off, the DIS pin must be toggled from low to high after power is applied. This is accomplished with a simple resistor divider, as shown below in Figure 30. As the V_{DD}/V_{CC} supply ramps from zero up, the DIS voltage is below its input threshold of 1.7V due to the R1/R2 resistor divider. When V_{DD}/V_{CC} exceeds approximately 9V to 10V, DIS becomes greater than the input threshold and the chip disables all outputs. It is critical that ALI and BLI be held low prior to DIS reaching its threshold level of 1.7V while V_{DD}/V_{CC} is ramping up, so that shoot through is avoided. After power is up the chip can be enabled by the ENABLE signal which pulls the DIS pin low.

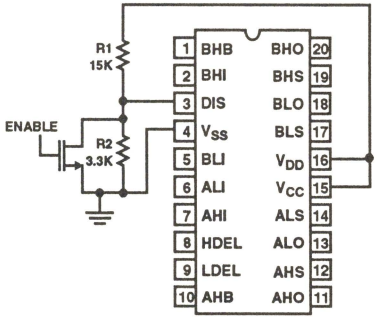
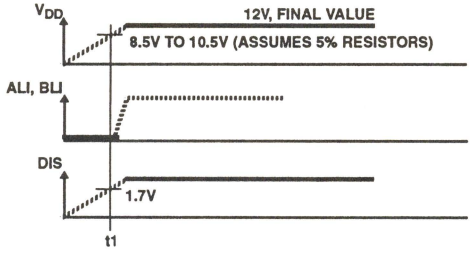


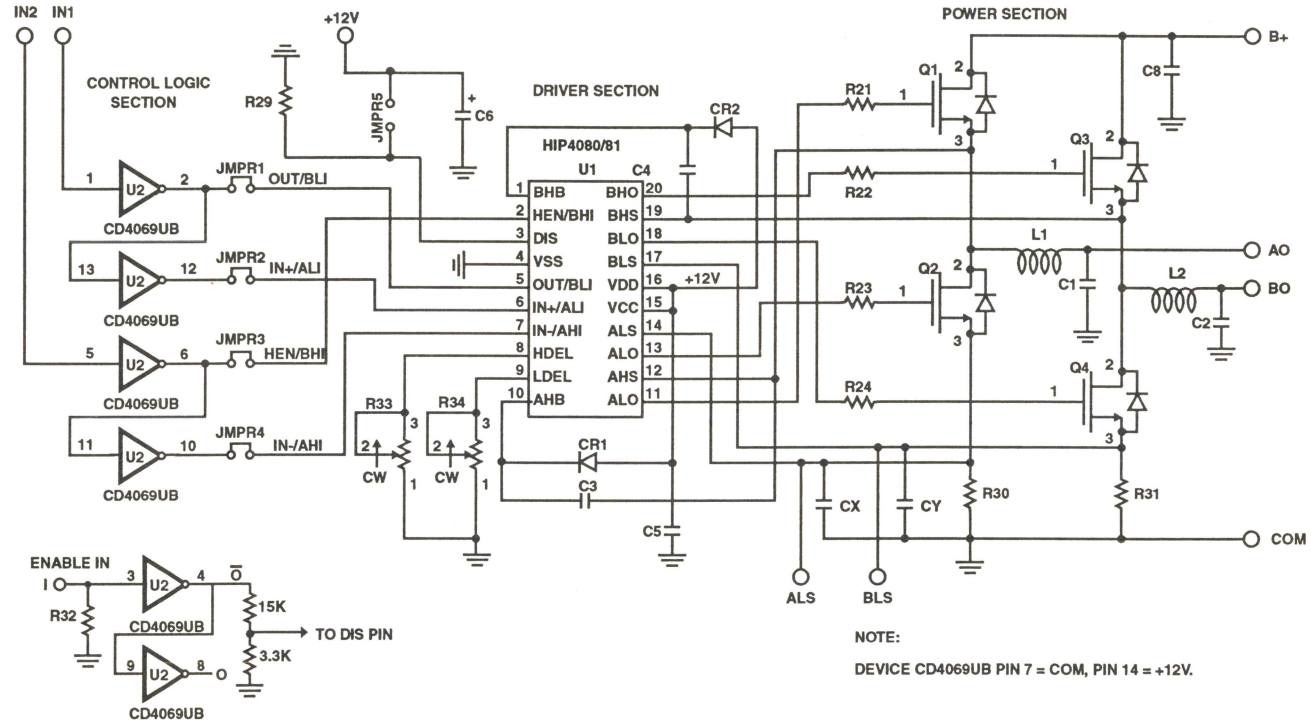
FIGURE 30.



TIMING DIAGRAM FOR FIGURE 30

NOTE:

1. ALI and/or BLI may be high after t1, whereupon the ENABLE pin may also be brought high.
2. Another product, HIP4081A, incorporates undervoltage circuitry which eliminates the need for the above power up circuitry.



NOTE:

DEVICE CD4069UB PIN 7 = COM, PIN 14 = +12V.

FIGURE 31. HIP4081 EVALUATION BOARD SCHEMATIC

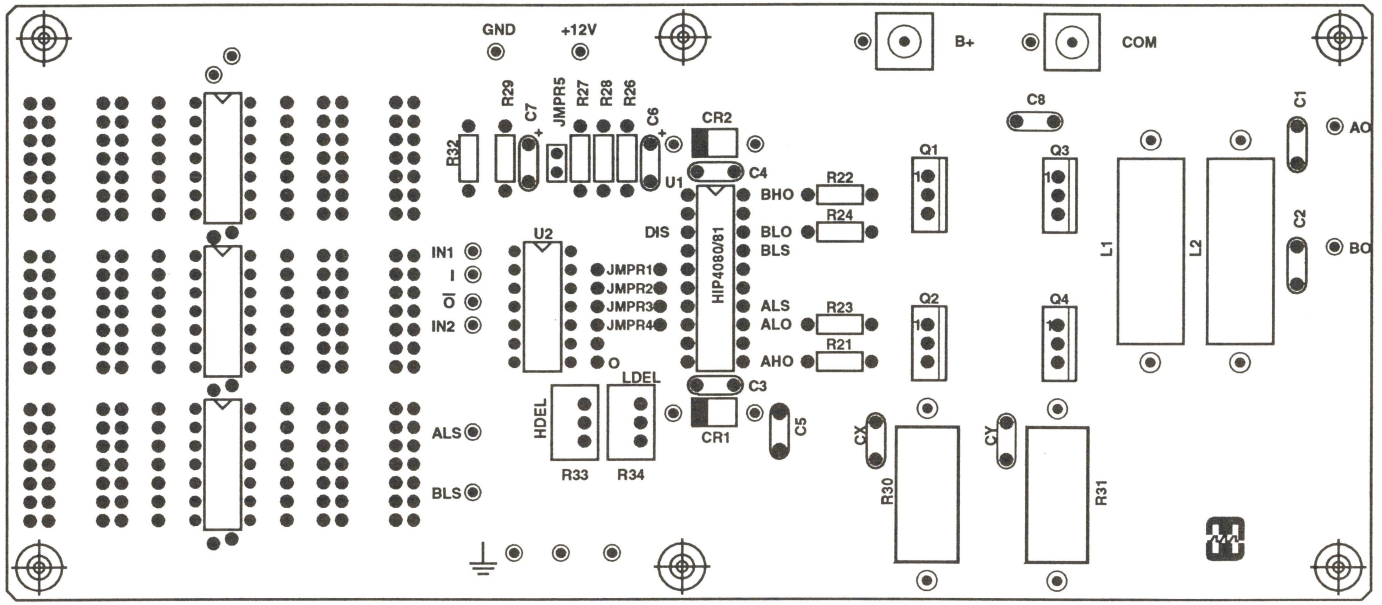


FIGURE 32. HIP4081 EVALUATION BOARD SILKSCREEN

HARRIS SEMICONDUCTOR

HIP4081A

PRELIMINARY

April 1994

80V/2.5A Peak, High Frequency Full Bridge FET Driver

Features

- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load at 1MHz in Free Air at +50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- On-Chip Charge-Pump and Bootstrap Upper Bias Supplies
- DIS (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption
- Undervoltage Protection

Applications

- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Class D Audio Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

Description

The HIP4081A is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4081A can drive every possible switch combination except those which would cause a shoot-through condition. The HIP4081A can switch at frequencies up to 1MHz and is well suited to driving Voice Coil Motors, high-frequency Class D audio amplifiers, and power supplies.

For example, the HIP4081A can drive medium voltage brush motors, and two HIP4081As can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in rapid, precise control of the driven load.

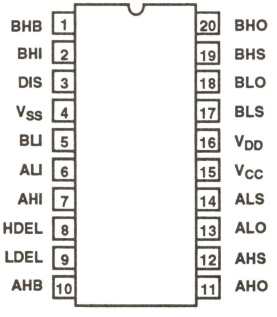
A similar part, the HIP4080A, includes an on-chip input comparator to create a PWM signal from an external triangle wave and to facilitate "hysteresis mode" switching.

Ordering Information

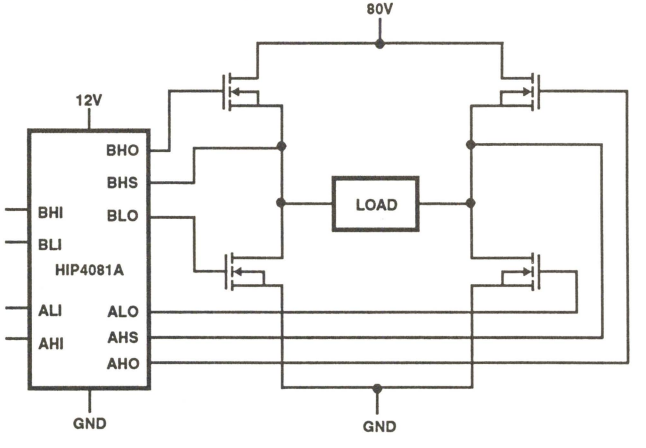
PART NUMBER	TEMP RANGE	PACKAGE
HIP4081AIP	-40°C to +85°C	20 Lead Plastic DIP
HIP4081AIB	-40°C to +85°C	20 Lead Plastic SOIC (W)

Pinout

HIP4081A (PDIP, SOIC)
TOP VIEW



Application Block Diagram

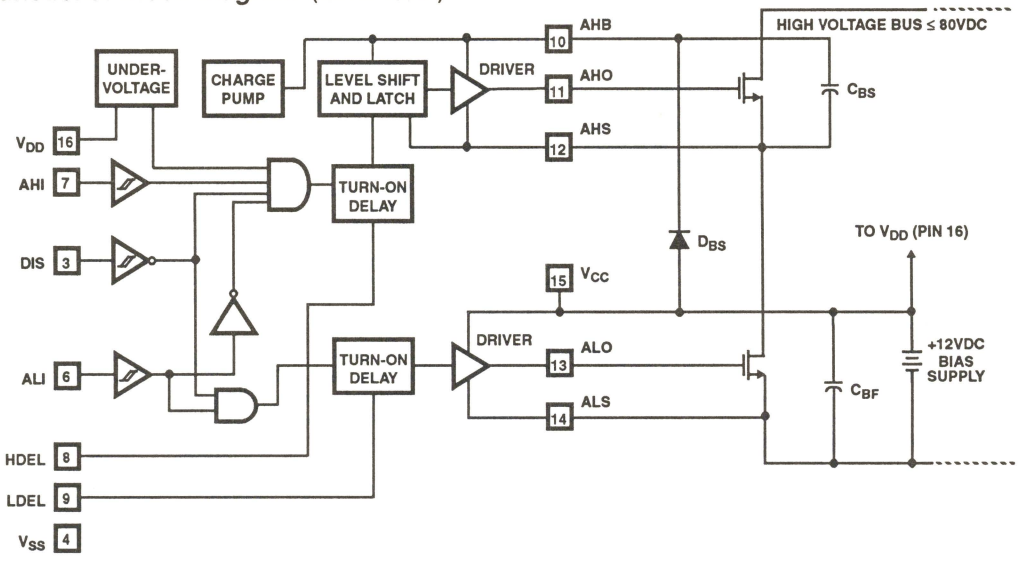


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

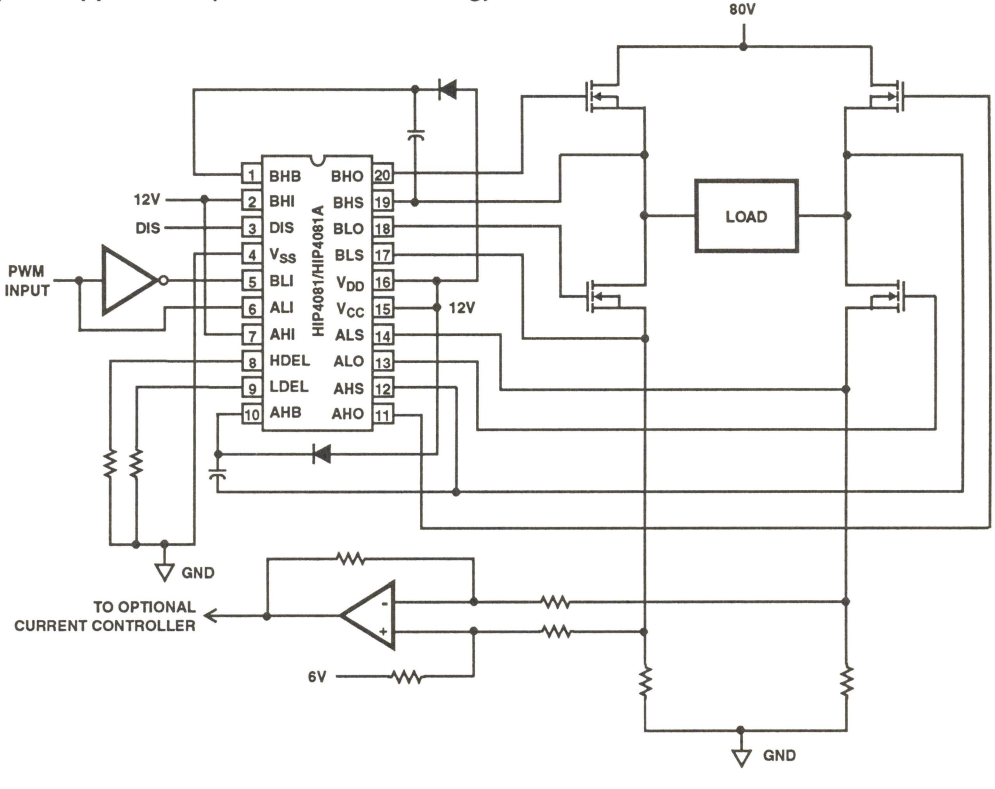
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File Number **3659.1**

Functional Block Diagram (1/2 HIP4081A)



Typical Application (PWM Mode Switching)



Absolute Maximum and Thermal Ratings

Supply Voltage, V_{DD} and V_{CC} ..... -0.3V to 16V
Logic I/O Voltages ..... -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS ..... -6.0V (Transient) to 95V
Voltage on ALS, BLS ..... -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB ..... $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +16V, or 95V, whichever is less
Voltage on ALO, BLO ..... $V_{ALS, BLS}$ -0.3V to V_{CC} +0.3V
Voltage on AHO, BHO ..... $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V
Input Current, HDEL and LDEL ..... -5mA to 0mA
Phase Slew Rate 20V/ns
NOTE: All voltages are relative to pin 4, V_{SS}, unless otherwise specified.

Storage Temperature Range ..... -65°C to +150°C
Operating Max. Junction Temperature ..... +125°C
Lead Temperature (Soldering 10s)
(For SOIC - Lead Tips Only) ..... +300°C
Thermal Resistance, Junction-Ambient
SOIC Package ..... 85°C/W
DIP Package ..... 75°C/W
Maximum Power Dissipation at +85°C
SOIC Package 470mW
DIP Package 530mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} ..... +9.5V to +15V
Voltage on ALS, BLS ..... -1.0V to +1.0V
Voltage on AHS, BHS ..... -1V to 80V

Voltage on AHB, BHB ..... $V_{AHS, BHS}$ +5V to $V_{AHS, BHS}$ +15V
Input Current, HDEL and LDEL ..... -500µA to -50µA
Operating Ambient Temperature Range ..... -40°C to +85°C

Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = +25°C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_{JS} = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND CHARGE PUMPS								
V_{DD} Quiescent Current	I_{DD}	All inputs = 0V	8.5	10.5	14.5	7.5	14.5	mA
V_{DD} Operating Current	I_{DDO}	Outputs switching f = 500kHz	9.5	12.5	15.5	8.5	15.5	mA
V_{CC} Quiescent Current	I_{CC}	All Inputs = 0V, $I_{ALO} = I_{BLO} = 0$	-	0.1	10	-	20	µA
V_{CC} Operating Current	I_{CCO}	f = 500kHz, No Load	1	1.25	2.0	0.8	3	mA
AHB, BHB Quiescent Current - Qpump Output Current	I_{AHB}, I_{BHB}	All Inputs = 0V, $I_{AHO} = I_{BHO} = 0$ $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V$	-50	-30	-11	-60	-10	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 500kHz, No Load	0.6	1.2	1.5	0.5	1.9	mA
AHS, BHS, AHB, BHB Leakage Current	I_{HLK}	$V_{AHS} = V_{BHS} = V_{AHB} = V_{BHB} = 95V$	-	0.02	1.0	-	10	µA
AHB-AHS, BHB-BHS Qpump Output Voltage	V_{AHB}-V_{AHS} V_{BHB}-V_{BHS}	$I_{AHB} = I_{AHB} = 0$, No Load	11.5	12.6	14.0	10.5	14.5	V
INPUT PINS: ALI, BLI, AHI, BHI, AND DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	µA
TURN-ON DELAY PINS: LDEL AND HDEL								
LDEL, HDEL Voltage	V_{HDEL}, V_{LDEL}	$I_{HDEL} = I_{LDEL} = -100µA$	4.9	5.1	5.3	4.8	5.4	V
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO								
Low Level Output Voltage	V_{OL}	I_{OUT} = 100mA	0.7	0.85	1.0	0.5	1.1	V
High Level Output Voltage	V_{CC}-V_{OH}	I_{OUT} = -100mA	0.8	0.95	1.1	0.5	1.2	V
Peak Pullup Current	I_O+	V_{OUT} = 0V	1.7	2.6	3.8	1.4	4.1	A
Peak Pulldown Current	I_O-	V_{OUT} = 12V	1.7	2.4	3.3	1.3	3.6	A

Electrical Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_{JS} = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Undervoltage, Rising Threshold	UV+		8.1	8.8	9.4	8.0	9.5	V
Undervoltage, Falling Threshold	UV-		7.6	8.3	8.9	7.5	9.0	V
Undervoltage, Hysteresis	HYS		0.25	0.4	0.65	0.2	0.7	V

Switching Specifications $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, $C_L = 1000pF$.

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_{JS} = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPHL}		-	30	60	-	80	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPHL}		-	35	70	-	90	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPLH}	$R_{HDEL} = R_{LDEL} = 10K$	-	45	70	-	90	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPLH}	$R_{HDEL} = R_{LDEL} = 10K$	-	60	90	-	110	ns
Rise Time	T_R		-	10	25	-	35	ns
Fall Time	T_F		-	10	25	-	35	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$	$R_{HDEL} = R_{LDEL} = 10K$	50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$	$R_{HDEL} = R_{LDEL} = 10K$	40	-	-	40	-	ns
Turn-on Output Pulse Width	$T_{PWOUT-ON}$	$R_{HDEL} = R_{LDEL} = 10K$	40	-	-	40	-	ns
Turn-off Output Pulse Width	$T_{PWOUT-OFF}$	$R_{HDEL} = R_{LDEL} = 10K$	30	-	-	30	-	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	45	75	-	95	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	55	85	-	105	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	T_{DLPLH}		-	35	70	-	90	ns
Refresh Pulse Width (ALO and BLO)	T_{REF-PW}		240	380	500	200	600	ns
Disable to Upper Enable (DIS - AHO and BHO)	T_{UEN}		-	335	500	-	550	ns

TRUTH TABLE

INPUT				OUTPUT	
ALI, BLI	AHI, BHI	U/V	DIS	ALO, BLO	AHO, BHO
X	X	X	1	0	0
1	X	0	0	1	0
0	1	0	0	0	1
0	0	0	0	0	0
X	X	1	X	0	0

NOTE: X signifies that input can be either a "1" or "0".

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 20). BLI (Pin 5) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold BHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold DIS high if this pin is not driven.
4	V_{SS}	Chip negative supply, generally will be ground.
5	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 18). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold BLI high if this pin is not driven.
6	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold ALI high if this pin is not driven.
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 11). ALI (Pin 6) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold AHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (Pin 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (Pin 15). De-couple this pin to V_{SS} (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

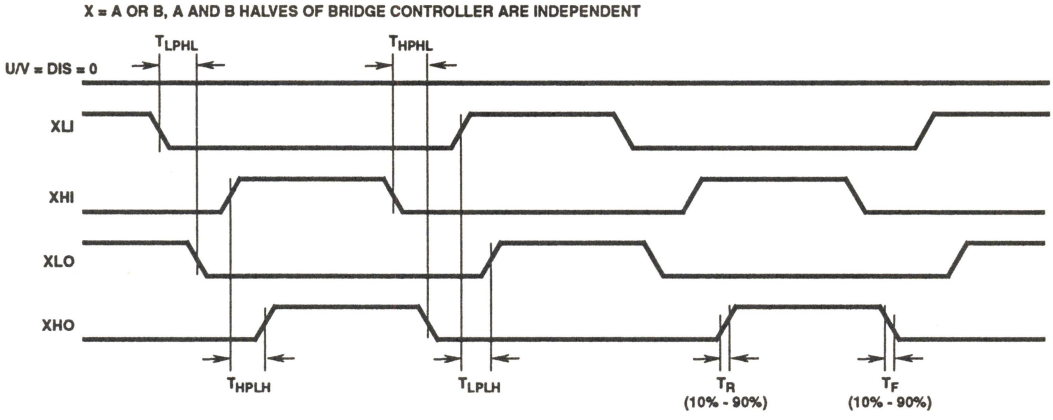


FIGURE 1. INDEPENDENT MODE

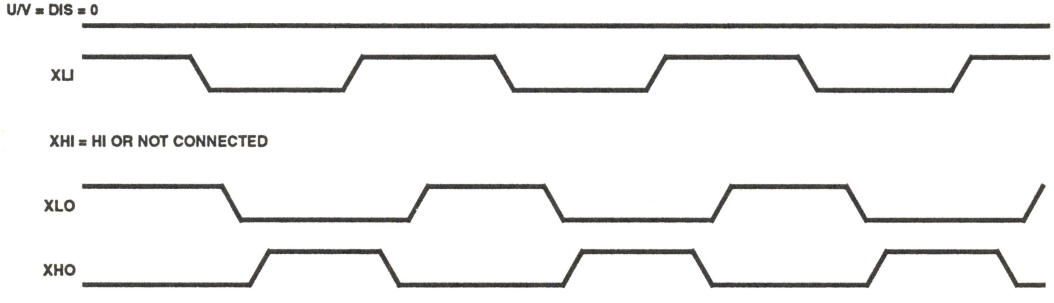


FIGURE 2. BISTATE MODE

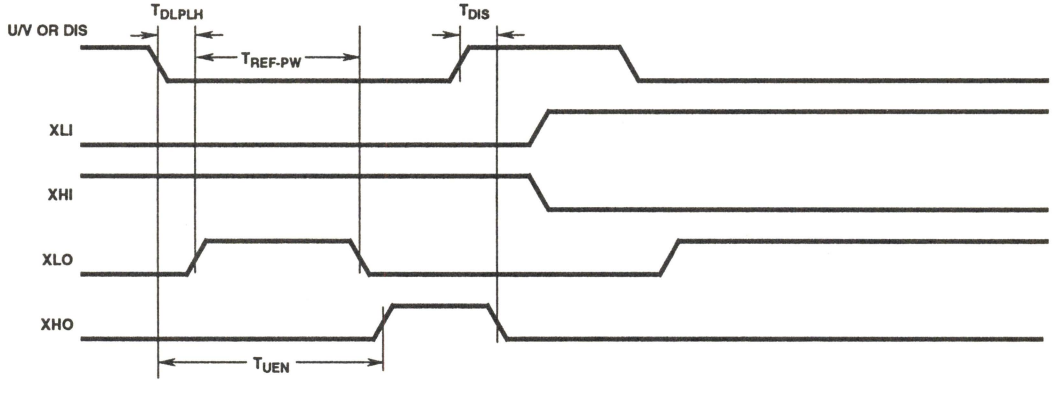


FIGURE 3. DISABLE FUNCTION

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = +25°C$, Unless Otherwise Specified

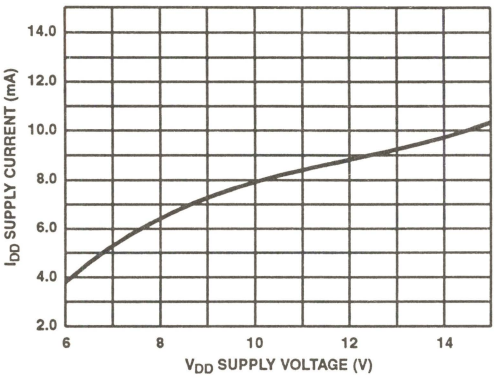


FIGURE 4. QUIESCENT I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

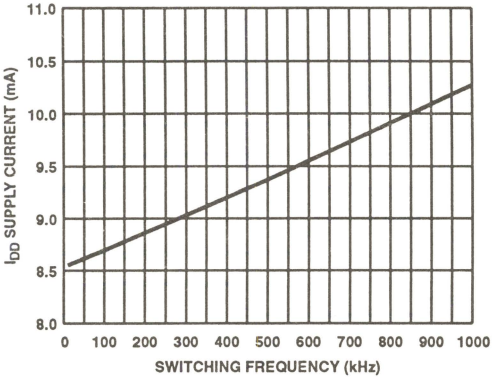


FIGURE 5. I_{DDO}, NO-LOAD I_{DD} SUPPLY CURRENT vs FREQUENCY (kHz)

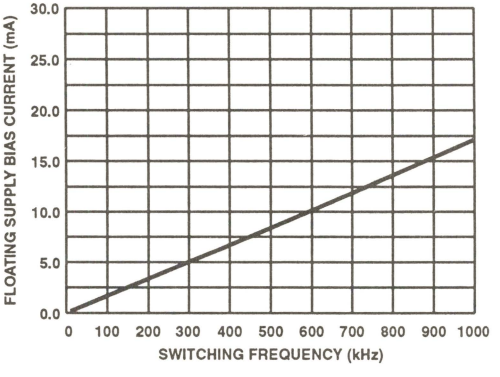


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

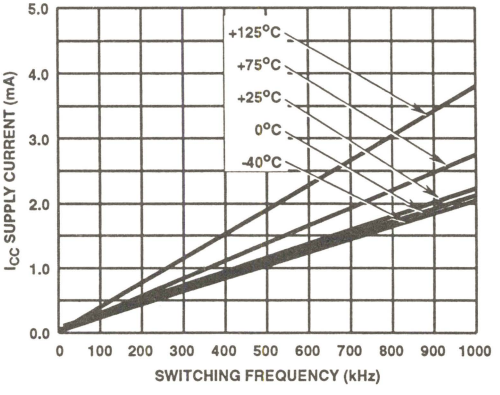


FIGURE 7. I_{CCO}, NO-LOAD I_{CC} SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

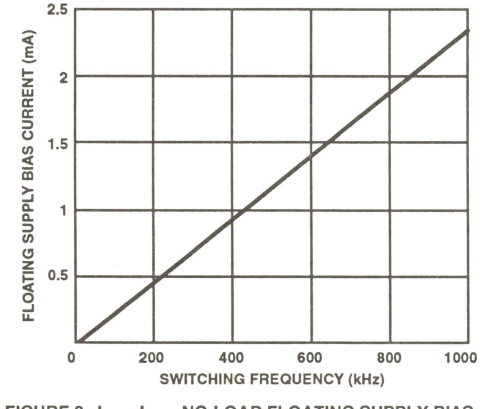


FIGURE 8. I_{AHB}, I_{BHB}, NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

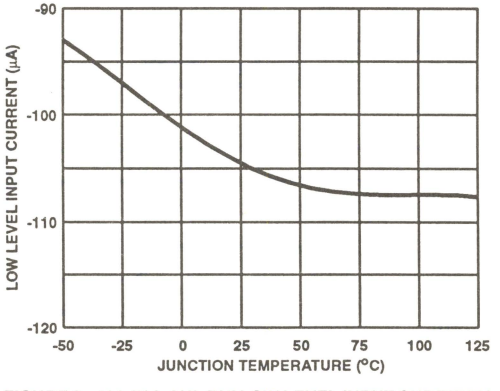


FIGURE 9. ALI, BLI, AHI, BHI LOW LEVEL INPUT CURRENT I_{IL} vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$ and $T_A = +25°C$, Unless Otherwise Specified

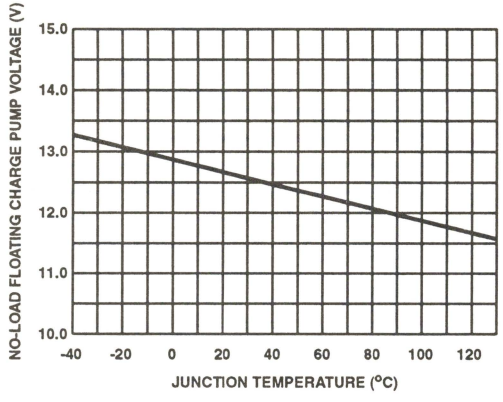


FIGURE 10. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

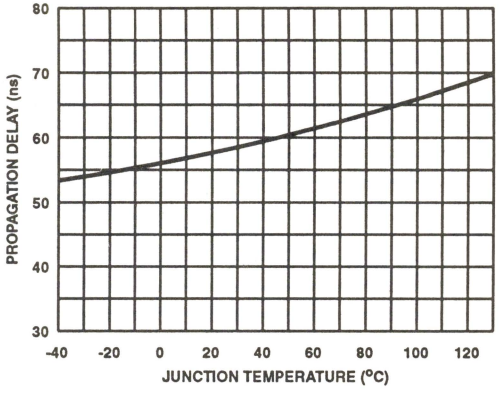


FIGURE 11. UPPER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISHIGH}$ vs TEMPERATURE

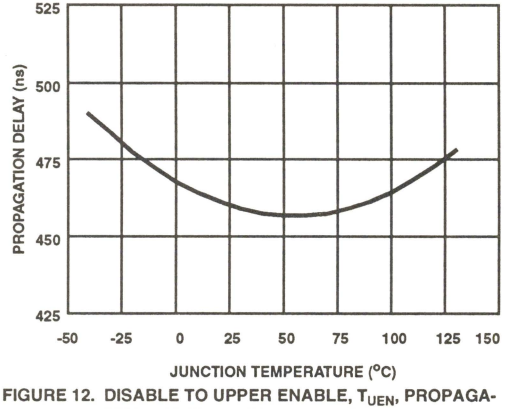


FIGURE 12. DISABLE TO UPPER ENABLE, T_{UEN}, PROPAGATION DELAY vs TEMPERATURE

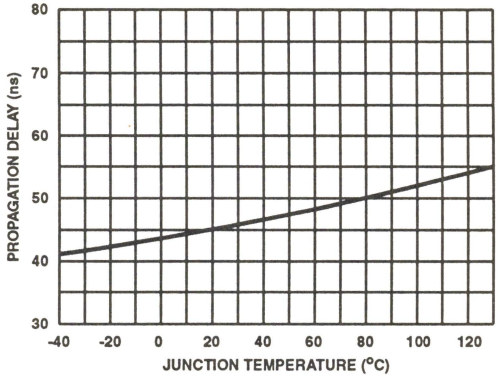


FIGURE 13. LOWER DISABLE TURN-OFF PROPAGATION DELAY T_{DISLOW} vs TEMPERATURE

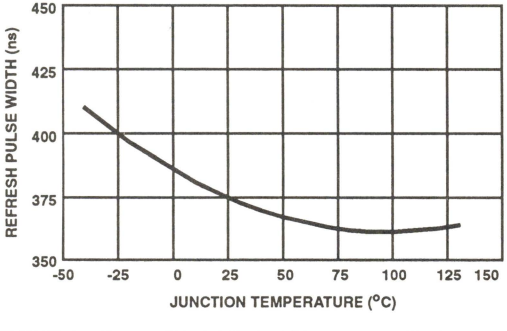


FIGURE 14. T_{REF-PW} REFRESH PULSE WIDTH vs TEMPERATURE

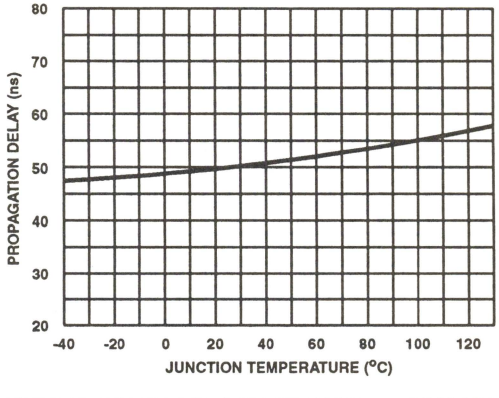


FIGURE 15. DISABLE TO LOWER ENABLE T_{DLPLH} PROPAGATION DELAY vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 10K and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

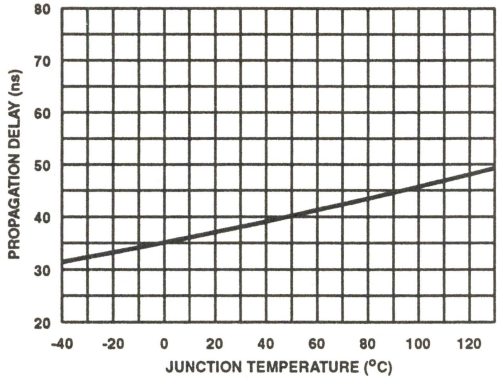


FIGURE 16. UPPER TURN-OFF PROPAGATION DELAY T_{HPHL} vs TEMPERATURE

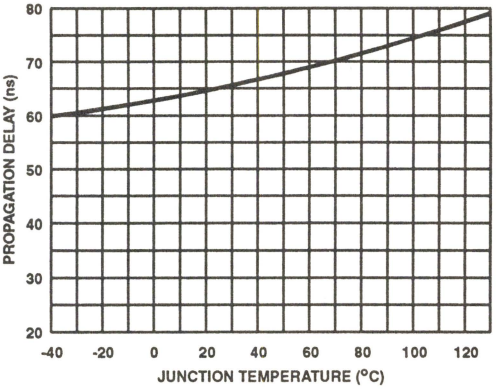


FIGURE 17. UPPER TURN-ON PROPAGATION DELAY T_{HPLH} vs TEMPERATURE

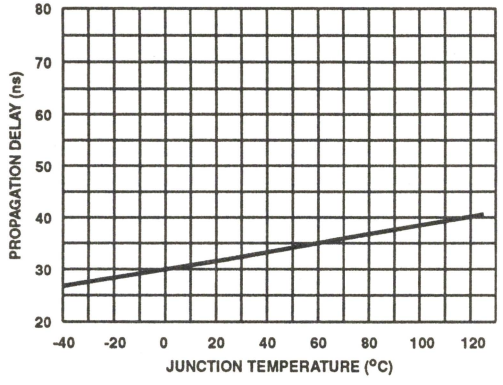


FIGURE 18. LOWER TURN-OFF PROPAGATION DELAY T_{LPHL} vs TEMPERATURE

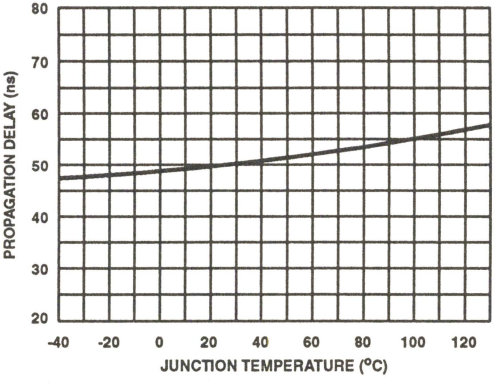


FIGURE 19. LOWER TURN-ON PROPAGATION DELAY T_{LPLH} vs TEMPERATURE

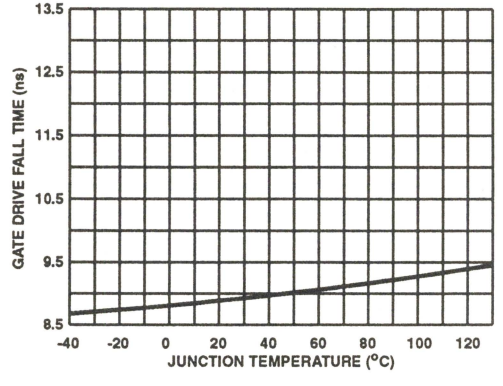


FIGURE 20. GATE DRIVE FALL TIME T_F vs TEMPERATURE

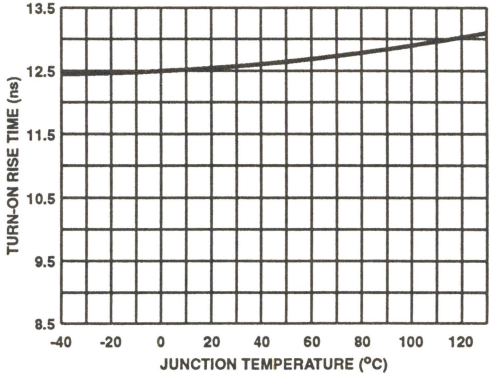


FIGURE 21. GATE DRIVE RISE TIME T_R vs TEMPERATURE

Typical Performance Curves

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$ and $T_A = +25°C$, Unless Otherwise Specified

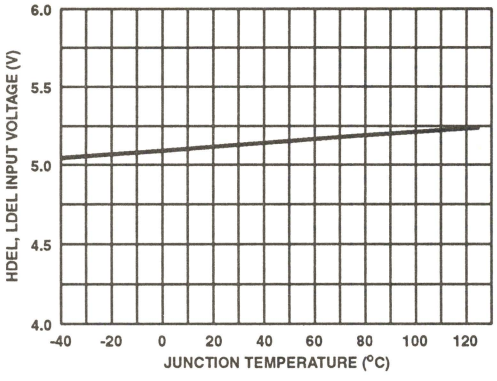


FIGURE 22. V_{LDEL}, V_{HDEL} VOLTAGE vs TEMPERATURE

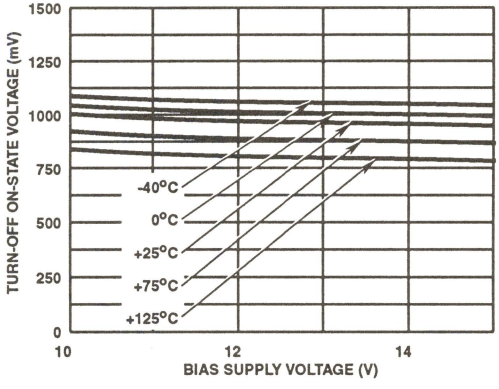


FIGURE 23. HIGH LEVEL OUTPUT VOLTAGE V_{CC} - V_{OH} vs BIAS SUPPLY AND TEMPERATURE AT 100mA

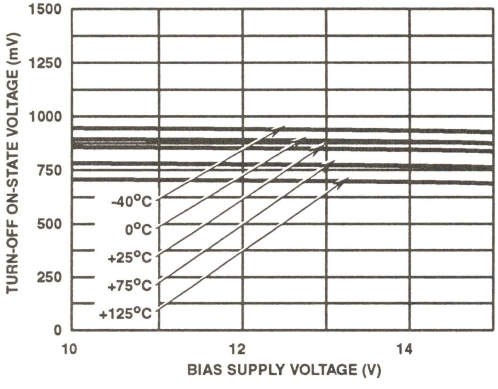


FIGURE 24. LOW LEVEL OUTPUT VOLTAGE V_{OL} vs BIAS SUPPLY AND TEMPERTURE AT 100mA

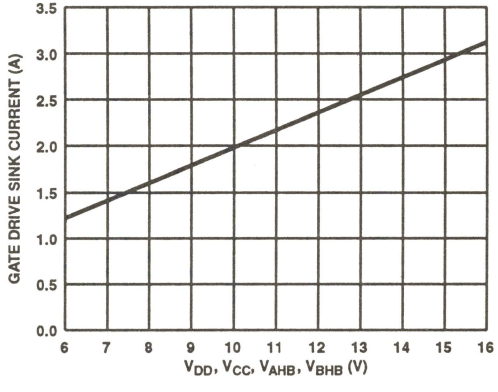


FIGURE 25. PEAK PULLDOWN CURRENT I_O vs BIAS SUPPLY VOLTAGE

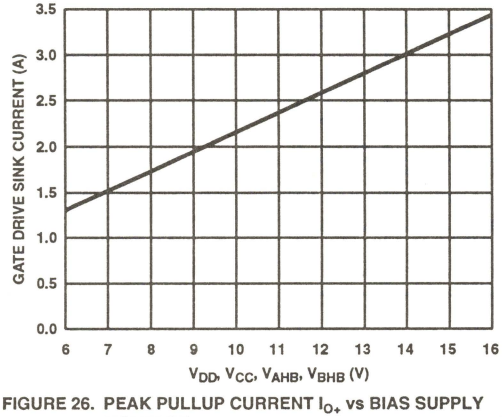


FIGURE 26. PEAK PULLUP CURRENT I_{O+} vs BIAS SUPPLY VOLTAGE

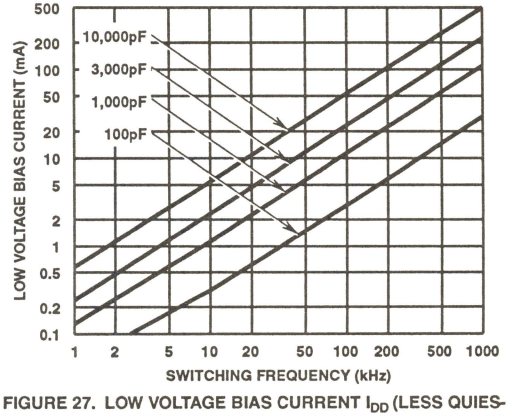


FIGURE 27. LOW VOLTAGE BIAS CURRENT I_{DD} (LESS QUIESCENT COMPOENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

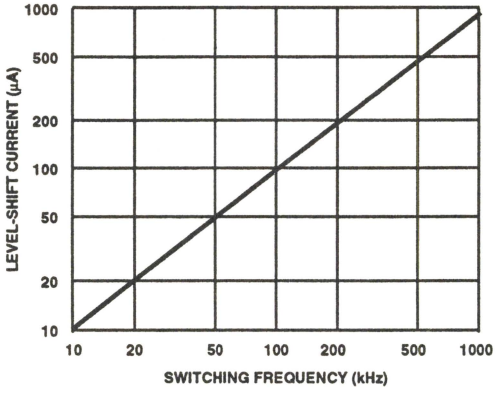


FIGURE 28. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

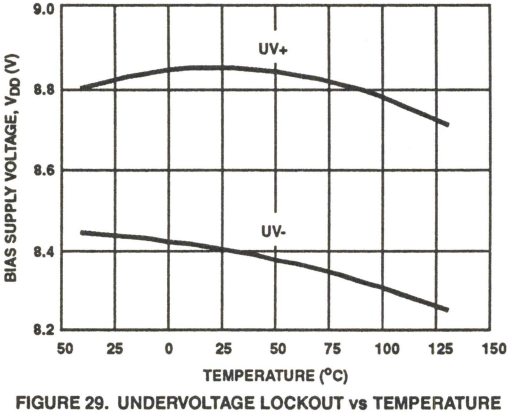


FIGURE 29. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

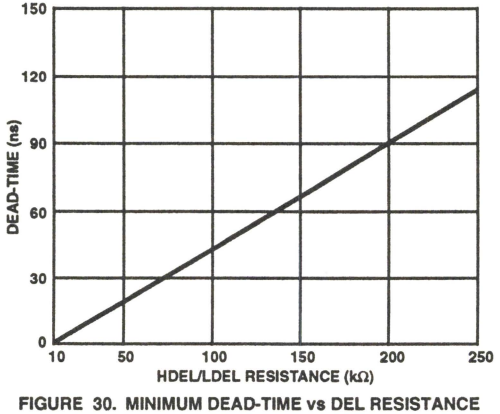


FIGURE 30. MINIMUM DEAD-TIME vs DEL RESISTANCE

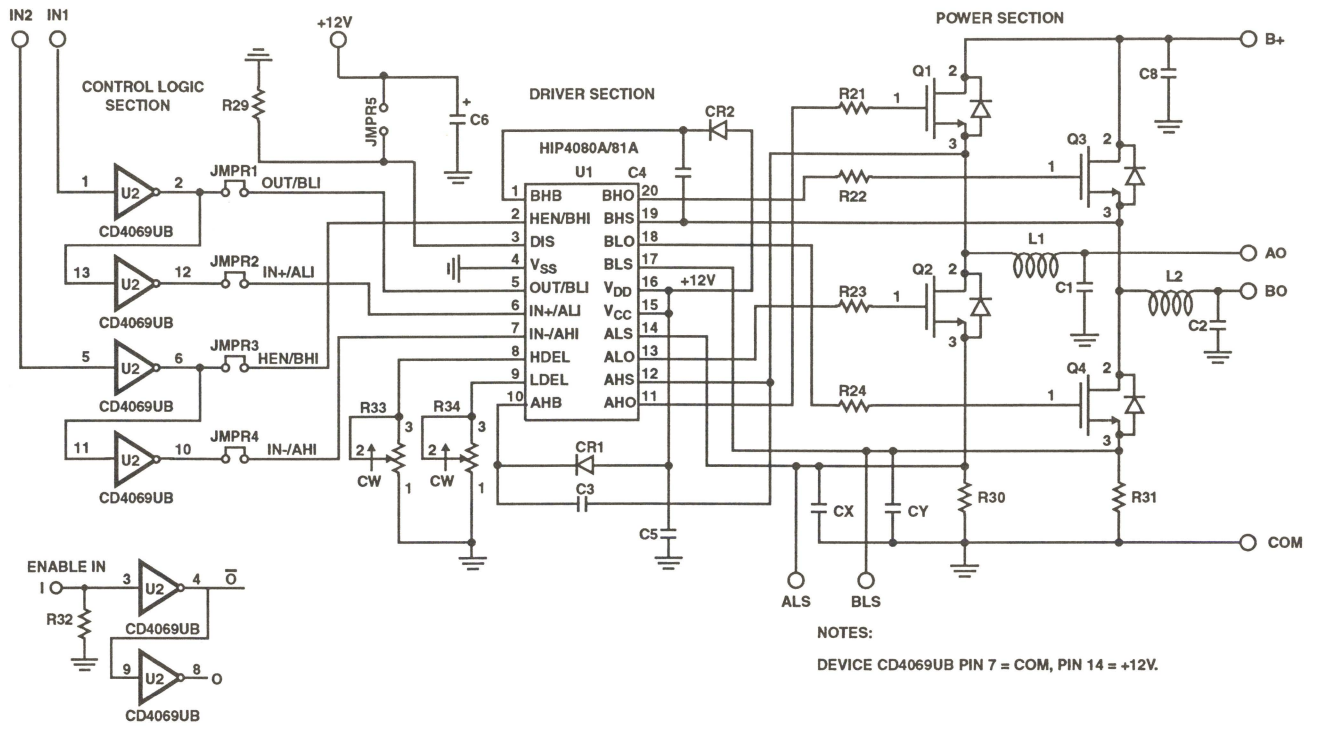


FIGURE 31. HIP4081A EVALUATION PC BOARD SCHEMATIC

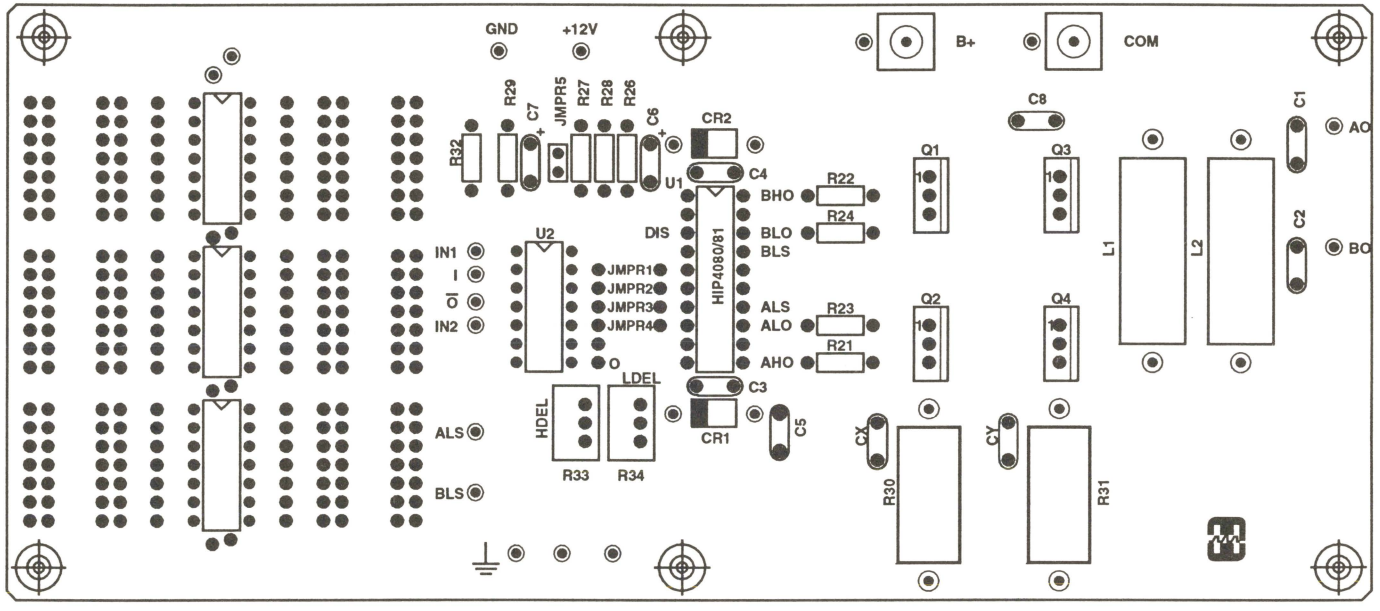


FIGURE 32. HIP4081A EVALUATION BOARD SILKSCREEN

HARRIS SEMICONDUCTOR

HIP4082

ADVANCE INFORMATION

April 1994

80V/1.25A Peak Current Full Bridge FET Driver

Features

- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load in Free Air at 50°C with Rise and Fall Times of Typically 15ns
- User-Programmable Dead Time (0.1 to 4.5us)
- DIS (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Shoot-Through Protection
- Undervoltage Protection

Applications

- UPS Systems
- DC Motor Controls
- Full Bridge Power Supplies
- Class D Audio Power Amplifiers
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- Medium/Large Voice Coil Motors

Description

The HIP4082 is a medium frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 16 lead plastic SOIC and DIP packages.

Specifically targeted for PWM motor control and UPS applications, bridge based designs are made simple and flexible with the HIP4082 Full Bridge Driver. With operation up to 80V, the device is best suited to applications of moderate power levels.

Similar to the HIP4081, it has a flexible input protocol for driving every possible switch combination except those which would cause a shoot-through condition. The HIP4082 has reduced drive current compared to the HIP4081 (1.25 vs 2.5A) and a much wider range of programmable dead times (0.1 to 4.5us) making it ideal for switching frequencies in the 20kHz to 200kHz range. Unlike the HIP4081 the HIP4082 does not contain an internal charge pump.

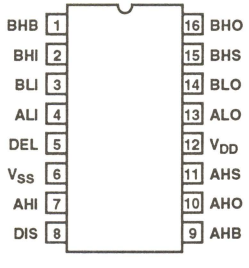
This set of features and specifications is optimized for applications where size and cost are important. For applications needing higher drive capability the HIP4080A and HIP4081A are recommended.

Ordering Information

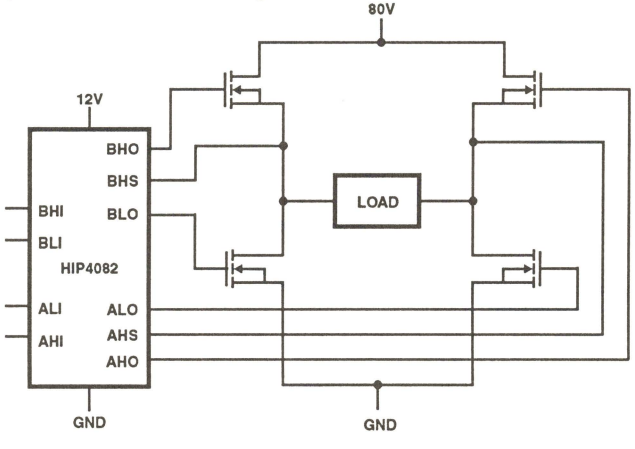
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4082IP	-40°C to +85°C	16 Lead Plastic DIP
HIP4082IB	-40°C to +85°C	16 Lead Plastic SOIC (N)

Pinout

HIP4082 (PDIP, SOIC)
TOP VIEW



Applicationn Block Diagram

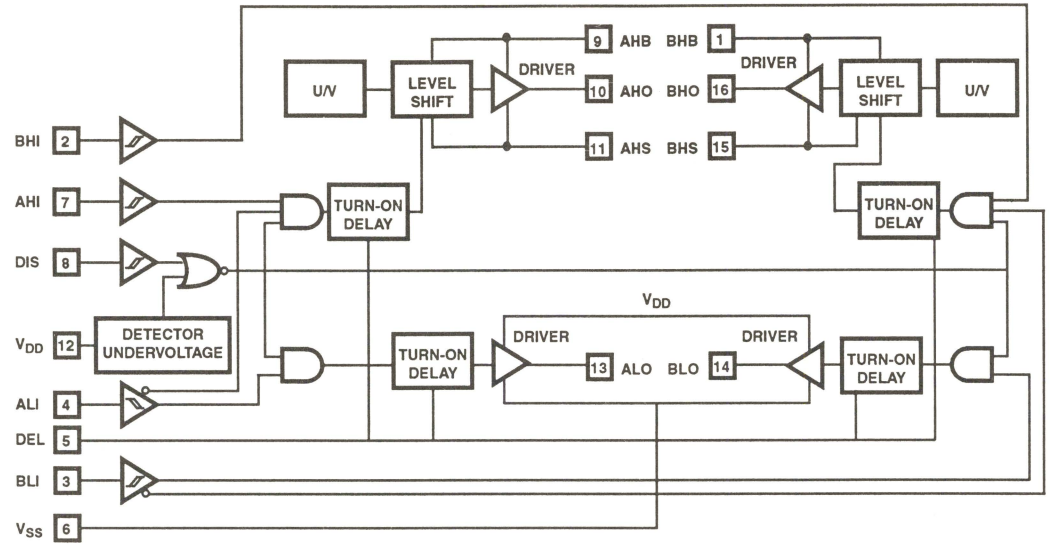


6 FULL BRIDGE

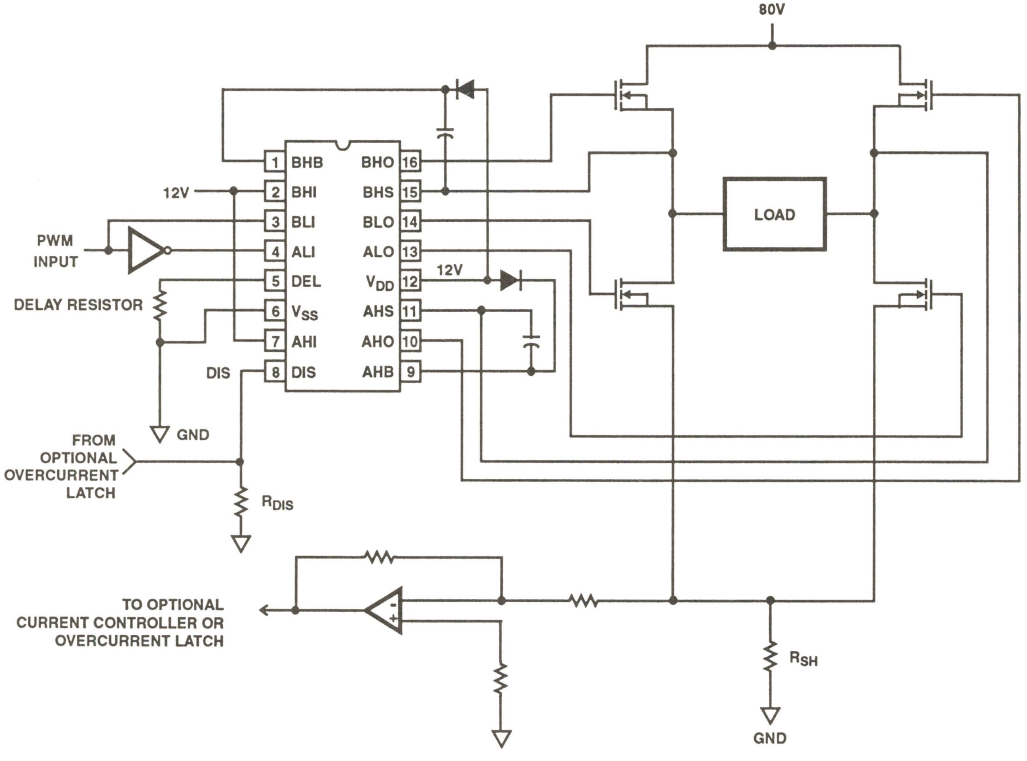
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3676

Functional Block Diagram



Typical Application (PWM Mode Switching)



Absolute Maximum and Thermal Ratings

Supply Voltage, V_{DD} ..... -0.3V to 16V
Logic I/O Voltages ..... -0.3V to V_{DD} +0.3V
Voltage on AHS, BHS ..... -6.0V (Transient) to 88V
Voltage on AHB, BHB ..... V_{AHS}, V_{BHS} -0.3V to $V_{AHS, BHS}$ +16V, or 95V, whichever is less
Voltage on ALO, BLO ..... V_{SS} -0.3V to V_{CC} +0.3V
Voltage on AHO, BHO ..... V_{AHS}, V_{BHS} -0.3V to V_{AHB}, V_{BHB} +0.3V
Input Current, DEL ..... -5mA to 0mA
Phase Slew Rate 20V/ns

Thermal Information

Storage Temperature Range ..... -65°C to +150°C
Operating Max. Junction Temperature ..... +125°C
Lead Temperature (Soldering 10s) ..... +300°C
(For SOIC - Lead Tips Only)
Thermal Resistance, Junction-Ambient
SOIC Package ..... 150°C/W
DIP Package ..... 90°C/W
Maximum Power Dissipation at +85°C
SOIC Package 266mW
DIP Package 445mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage, V_{DD} ..... +8V to +15V
Voltage on V_{SS} ..... -1.0V to +1.0V
Voltage on AHS, BHS ..... -1V to 80V
Voltage on AHB, BHB ..... V_{AHS}, V_{BHS} +7V to V_{AHS}, V_{BHS} +15V
Input Current, DEL ..... -4mA to -100µA
Operating Ambient Temperature Range ..... -40°C to +85°C

Electrical Specifications

$V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_{JS} = -40°C TO +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS & UNDER VOLTAGE PROTECTION								
V_{DD} Quiescent Current	I_{DD}	All inputs = 0V	-	2.25	-	-	-	mA
V_{DD} Operating Current	I_{DDO}	Outputs Switching f = 50kHz,	-	4.25	-	-	-	mA
AHB, BHB Off Quiescent Current	I_{AHBL}, I_{BHBL}	AHI = BHI = 0V	-	145	-	-	-	µA
AHB, BHB On Quiescent Current	I_{AHBH}, I_{BHBH}	AHI = BHI = V_{DD}	-	1.0	-	-	-	mA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 50kHz, CL=1000pF	-	0.8	-	-	-	mA
V_{DD} Rising Undervoltage Threshold	VDDUV+		-	7.5	-	-	-	V
V_{DD} Falling Undervoltage Threshold	UV-		-	7.0	-		-	V
Undervoltage Hysteresis	UVHYS		-	0.5	-	-	-	V
AHB, BHB Undervoltage Threshold	VHBUV		-	5.5	-	-	-	V
INPUT PINS: ALI, BLI, AHI, BHI, & DIS								
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	µA
TURN-ON DELAY PIN DEL								
Dead Time	T_{DEAD}	I_{DEL} = -100µA	-	4.4	-	-	-	uS
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, & BHO								
Low Level Output Voltage	V_{OL}	I_{OUT} = 50mA	0.7	0.85	1.0	0.5	1.1	V
High Level Output Voltage	V_{CC}-V_{OH}	I_{OUT} = -50mA	0.8	.95	1.1	0.5	1.2	V
Peak Pullup Current	I_O+	V_{OUT} = 0V	-	1.3	-	-	-	A
Peak Pulldown Current	I_O-	V_{OUT} = 12V	-	1.2	-	-	-	A

Switching Specifications $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$, $C_L = 1000pF$.

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_{JS} = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPHL}		-	25	-	-	-	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPHL}		-	30	-	-	-	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPLH}	$R_{DEL} = 10K$	-	35	-	-	-	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPLH}	$R_{DEL} = 10K$	-	50	-	-	-	ns
Rise Time	T_R		-	15	-	-	-	ns
Fall Time	T_F		-	15	-	-	-	ns
Turn-on Input Pulse Width	$T_{PWIN-ON}$	$R_{DEL} = 10K$	50	-	-	50	-	ns
Turn-off Input Pulse Width	$T_{PWIN-OFF}$	$R_{DEL} = 10K$	50	-	-	50	-	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	50	-	-	-	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	60	-	-	-	ns
Disable to Lower Turn-on Propagation Delay (DIS - ALO & BLO)	T_{DLPLH}		-	50	-	-	-	ns
Disable to Upper Enable (DIS - AHO & BHO)	T_{DHPLH}		-	620	-	-	-	ns
Refresh Pulse Width (ALO & BLO)	T_{REF-PW}		-	580	-	-	-	ns

NOTE:

1. All voltages are relative to pin 6, V_{SS}, unless otherwise specified.

TRUTH TABLE

INPUT					OUTPUT	
ALI, BLI	AHI, BHI	VDDUV	VHBUV	DIS	ALO, BLO	AHO, BHO
X	X	X	X	1	0	0
X	X	1	X	X	0	0
0	X	0	1	0	0	0
1	X	0	X	0	1	0
0	1	0	0	0	0	1
0	0	0	0	0	0	0

NOTE: X signifies that input can be either a "1" or "0".

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 16). BLI (Pin 3) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold BHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
3	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 14). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold BLI high if this pin is not driven.
4	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold ALI high if this pin is not driven.
5	DEL	Turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the dead time between drivers. All drivers turn-off with no adjustable delay, so the DEL resistor guarantees no shoot-through by delaying the turn-on of all drivers. The voltage across the DEL resistor is approximately V_{DD} -2V.
6	V_{SS}	Chip negative supply, generally will be ground.
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 10). ALI (Pin 4) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold AHI high, so no connection is required if high-side and low-side outputs are to be controlled by the low-side input.
8	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold DIS high if this pin is not driven.
9	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
10	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
11	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
12	V_{DD}	Positive supply to control logic and lower gate drivers. De-couple this pin to V_{SS} (Pin 6).
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
15	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
16	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Timing Diagrams

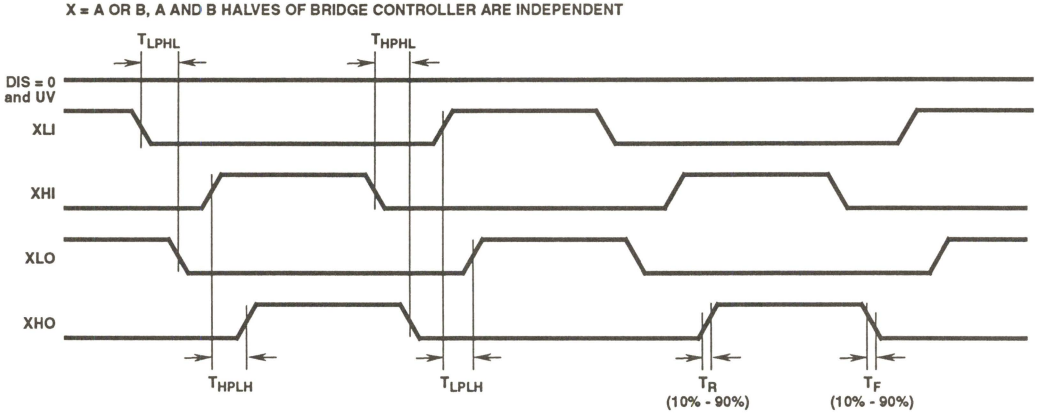


FIGURE 1. INDEPENDENT MODE

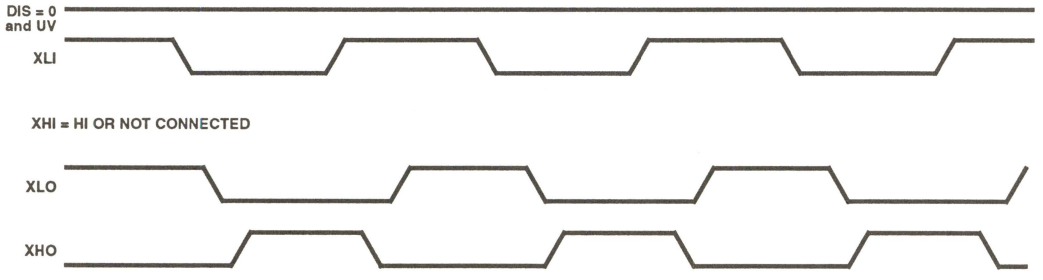


FIGURE 2. BISTATE MODE

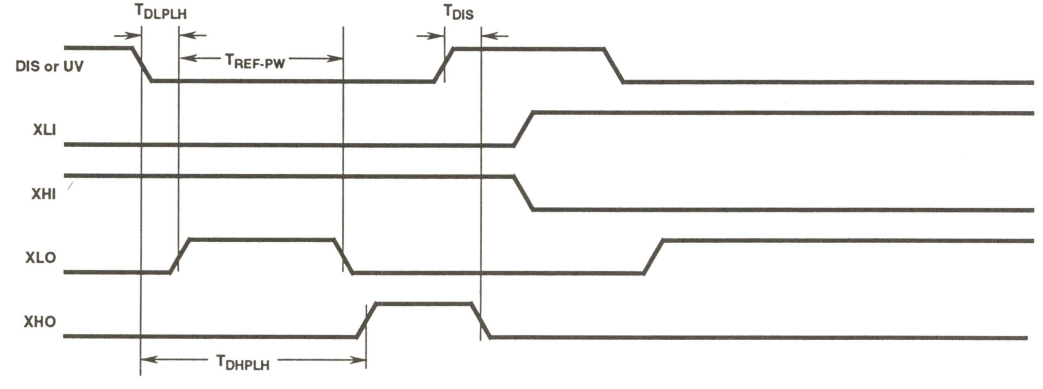


FIGURE 3. DISABLE FUNCTION

INTELLIGENT POWER ICs 7

REGULATORS/POWER SUPPLIES

		PAGE
REGULATORS/POWER SUPPLIES SELECTION GUIDES		7-2
REGULATORS/POWER SUPPLIES DATA SHEETS		
CA723, CA723C	Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors	7-3
CA1523	Voltage Regulator Control Circuit for Variable Switching Regulator	7-11
CA1524, CA2524, CA3524	Regulating Pulse Width Modulator	7-16
CA3085, CA3085A, CA3085B	Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA	7-31
CA3277	Dual 5V Regulator with Serial Data Buffer Interface for Microcontroller Applications	7-39
HIP5060	Power Control IC Single Chip Power Supply	7-47
HIP5061	7A, High Efficiency Current Mode Controlled PWM Regulator	7-53
HIP5062	Power Control IC Single Chip Dual Switching Power Supply	7-73
HIP5063	Power Control IC Single Chip Power Supply	7-80
HIP5500	High Voltage IC Half Bridge Gate Driver	7-84
HIP5600	Thermally Protected High Voltage Linear Regulator	7-94
ICL7660	CMOS Voltage Converter	7-109
ICL7660S	Super Voltage Converter	7-118
ICL7662	CMOS Voltage Converter	7-128
ICL7663S	CMOS Programmable Micropower Positive Voltage Regulator	7-138
ICL7665S	CMOS Micropower Over/Under Voltage Detector	7-145
ICL7673	Automatic Battery Back-Up Switch	7-155
ICL8211, ICL8212	Programmable Voltage Detectors	7-161

Regulators/Power Supplies Selection Guides

POWER SUPPLY CIRCUITS

DEVICE	DESCRIPTION	INPUT VOLTAGE RANGE	OUTPUT VOLTAGE RANGE	MAXIMUM OUTPUT CURRENT	SWITCHING FREQUENCY	QUIESCENT CURRENT	TEMPERATURE RANGE
CA723	Linear Voltage Regulators	9.5V to 40V	2V to 37V	150mA	-	3.5mA	-55°C to +125°C
CA723C						4.0mA	0°C to +70°C
CA1523	Variable Internal Pulse Regulator for Switch Mode Power Supplies	11V to 15V	5.9V to 7.5V (Note 1)	50mA	≈ 200kHz	34mA	0°C to +70°C
CA1524	Pulse Width Modulators	8V to 40V	4.8V to 5.2V (Note 1)	100mA Max Rating for Each Output Driver	1kHz to 300kHz	10mA	-55°C to +125°C
CA2524			4.8V to 5.2V (Note 1)				0°C to +70°C
CA3524			4.6V to 5.4V (Note 1)				0°C to +70°C
CA3085	Linear Voltage Regulators	7.5V to 30V	1.8V to 26V	12mA to 100mA	-	4.5mA at V_{IN} = 30V	-55°C to +125°C
CA3085A		7.5V to 40V	1.7V to 36V	12mA to 100mA		5.0mA at V_{IN} = 40V	
CA3085B		7.5V to 50V	1.7V to 46V	12mA to 100mA		7.0mA at V_{IN} = 50V	
CA3277	Microprocessor Interface Controller Dual-Fixed 5V Regulator, Overvoltage Shutdown, Thermal Shutdown, Current Limited	6.2V to 18V	Output 1 - Full Time 5V ± 0.25V Output 2 - Switched 5V ± 0.25V	Output 1 - 100mA Output 2 - 100mA	-	500µA	-40°C to +85°C
HIP5060	Single Chip, Low Side Switch, Current Controlled PWM	27V to 45V	Determined by External Circuitry	Power DMOS Transistor 60V - 10A	1MHz Internal, External Input	20mA	0°C to +85°C
HIP5061	7A Current Mode PWM Regulator - TO220 Type Package	10.8V Min 14V Zener	Determined by External Circuitry	Power DMOS Transistor 60V-7A	250kHz	25mA	0°C to +85°C Therm. Protect.
HIP5062	Single Chip, Dual Low Side Switch Current Controlled PWM	26V to 42V	Determined by External Circuitry	Two Power DMOS Transistors 60V - 5A	1MHz Latched External Loop	25mA	0°C to +85°C
HIP5063	Basic Single Chip, Low Side Switch Current Controlled PWM	10V to 60V	Determined by External Circuitry	Power DMOS Transistor 60V - 10A	External Clock	14mA	0°C to +85°C
HIP5500	Half Bridge Power Supply Regulator	10V to 15V	500V Peak	2.3A Peak	30kHz to 300kHz	7mA	-40°C to +150°C
HIP5600	High Voltage Linear Regulator	50V to 400V	1.2V to 350V	30mA	-	65µA	-40°C to +100°C Therm. Protect.
ICL7660SM	Super Voltage Converter (Charge Pump Type)	1.5V to 12V	-1.5V to ± 22.8V	45mA	10kHz to 35kHz	200µA	-55°C to +125°C
ICL7660SI						180µA	-40°C to +85°C
ICL7660SC						180µA	0°C to +70°C
ICL7662M	Voltage Converter (Charge Pump Type)	4.5V to 20V	-4.5V to ±38.8V	90mA	10kHz	250µA	-55°C to +125°C
ICL7662C						200µA	0°C to +70°C
ICL7662I						200µA	-40°C to +85°C
ICL7663SA	Linear Voltage Regulators	1.6V to 16V	1.3V to 16V	40mA - V_{OUT2} R_{ON} - 100Ω - V_{OUT2}	-	10µA	-25°C to +85°C
ICL7663S						12µA	0°C to +70°C

Note 1. Reference Voltages - Output Voltage Limited by External Device

VOLTAGE MONITORING CIRCUITS

DEVICE	DESCRIPTION	VOLTAGE RANGE	QUIESCENT CURRENT	OUTPUT CURRENT	INPUT TRIP VOLTAGE	TEMPERATURE RANGE
ICL7665SAI	CMOS Micropower Over/ Under Voltage Detector	1.8V to 16V	10µA	2mA	1.3 ± 2%	-40°C to +85°C
ICL7665SAC					1.3 ± 8%	0°C to +70°C
ICL7665SI					1.3 ± 2%	-40°C to +85°C
ICL7665SC					1.3 ± 8%	0°C to +70°C
ICL7673I	Automatic Battery Back-up Switch	2.5V to 15V	5µA	38mA	50mV (Note 2)	-25°C to +85°C
ICL7673C						0°C to +70°C
ICL8211M	Programmable Voltage Detectors	1.8V to 30V	350µA	3mA	1.15 + 3.5% 1.15 - 6.0%	-55°C to +125°C
ICL8211C						0°C to +70°C
ICL8212M				9mA	1.15 + 3.5% 1.15 - 13%	-55°C to +125°C
ICL8212C						0°C to +70°C

Note 2. Primary to Back-up Source Voltage Differential

HARRIS SEMICONDUCTOR CA723, CA723C

Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors

April 1994

Features

- Up to 150mA Output Current
- Positive and Negative Voltage Regulation
- Regulation in Excess of 10A with Suitable Pass Transistors
- Input and Output Short-Circuit Protection
- Load and Line Regulation 0.03%
- Direct Replacement for 723 and 723C Industry Types
- Adjustable Output Voltage . . . . . 2V to 37V

Applications

- Series and Shunt Voltage Regulator
- Floating Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Temperature Controller

Ordering Information

PART	TEMPERATURE	PACKAGE
CA723E	-55°C to +125°C	14Lead Plastic DIP
CA723T	-55°C to +125°C	10 Pin Metal Can
CA723CE	0°C to +70°C	14 Lead Plastic DIP
CA723CT	0°C to +70°C	10 Pin Metal Can

Description

The CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2V to 37V at currents up to 150mA.

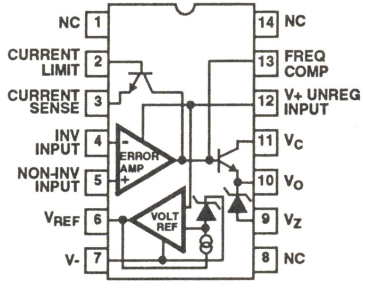
Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150mA and in excess of 10A with the use of suitable n-p-n or p-n-p external pass transistors.

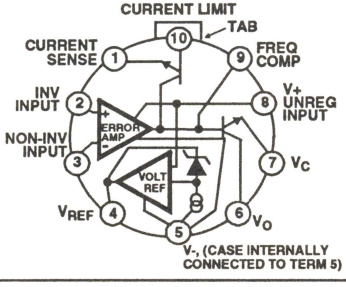
The CA723 and CA723C are supplied in the 10 lead TO-100 metal can(T suffix), and the 14 lead dual-in-line plastic package (E suffix), and are direct replacements for industry types LM723, LM723C in packages with similar terminal arrangements.

Pinouts

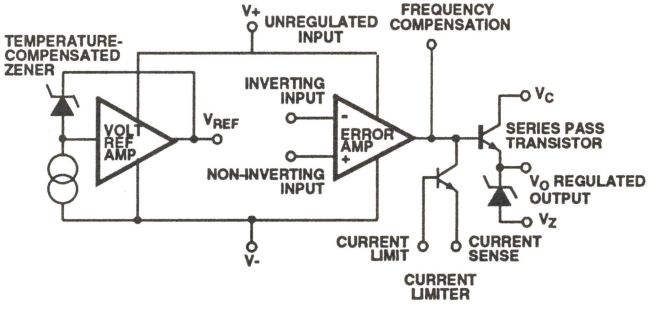
CA723 (PDIP)
TOP VIEW



CA723C (CAN)
TOP VIEW



Functional Block Diagram



7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 788.3

Absolute Maximum Ratings

DC Supply Voltage 40V
(Between V+ and V- Terminals)
Pulse Voltage for 50ms
Pulse Width (Between V+ and V- Terminals) 50V
Differential Input-Output Voltage 40V
Differential Input Voltage
Between Inverting and Noninverting Inputs..... ±5V
Between Noninverting Input and V- 8V
Current From Zener Diode Terminal (V_Z) 25mA

Operating Conditions

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	120°C/W	-
Metal Can	136°C/W	65°C/W

Device Dissipation
CA723T, CA723CT, Up to T_A = +25°C..... 900mW
CA723E, CA723CE, Up to T_A = +25°C 1000mW
CA723T, CA723CT, Above T_A = +25°C .....7.4mW/°C
CA723E, CA723CE, Above T_A = +25°C .....8.3mW/°C
Ambient Temperature Range
Operating Temperature Range .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature, During Soldering .....+265°C
At a distance 1/16" ± 1/32" (1.59mm ± 0.79mm) from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

T_A = +25°C, V+ = V_C = V_I = 12V, V- = 0, V_O = 5V, I_L = 1mA, C_1 = 100pF, C_{REF} = 0, R_{SCP} = 0, Unless Otherwise Specified. Divider impedance R_1 R_2 + R_1 + R_2 at noninverting input, Terminal 5 = 10kΩ. (Figure 20)

PARAMETERS	TEST CONDITION	CA723			CA723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30V	-	2.3	3.5	-	2.3	4	mA
Input Voltage Range, V_I		9.5	-	40	9.5	-	40	V
Output Voltage Range, V_O		2	-	37	2	-	37	V
Differential Input-Output Voltage, V_I - V_O		3	-	38	3	-	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (Note 1)	V_I = 12V to 40V	-	0.02	0.2	-	0.1	0.5	% V_O
	V_I = 12V to 15V	-	0.01	0.1	-	0.01	0.1	% V_O
	V_I = 12V to 15V, T_A = -55°C to +125°C	-	-	0.3	-	-	-	% V_O
	V_I = 12V to 15V, T_A = 0°C to +70°C	-	-	-	-	-	0.3	% V_O
Load Regulation (Note 1)	I_L = 1mA to 50mA	-	0.03	0.15	-	0.03	0.2	% V_O
	I_L = 1mA to 50mA, T_A = -55°C to +125°C	-	-	0.6	-	-	-	% V_O
	I_L = 1mA to 50mA, T_A = 0°C to +70°C	-	-	-	-	-	0.6	% V_O
Output-Voltage Temperature Coefficient, ΔV_O	T_A = -55°C to +125°C	-	0.002	0.015	-	-	-	%/°C
	T_A = 0°C to +70°C	-	-	-	-	0.003	0.015	%/°C
Ripple Rejection (Note 2)	f = 50Hz to 10kHz	-	74	-	-	74	-	dB
	f = 50Hz to 10kHz, C_{REF} = 5μF	-	86	-	-	86	-	dB
Short Circuit Limiting Current, I_{LIM}	R_{SCP} = 10Ω, V_O = 0	-	65	-	-	65	-	mA
Equivalent Noise RMS Output Voltage, V_N (Note 2)	BW = 100Hz to 10kHz, C_{REF} = 0	-	-20	-	-	20	-	μV
	BW = 100Hz to 10kHz, C_{REF} = 5μF	-	2.5	-	-	2.5	-	μV

NOTES:

1. Line and load regulation specifications are given for condition of a constant chip temperature. For high dissipation condition, temperature drifts must be separately taken into account.
2. For C_{REF} (See Figure 20)

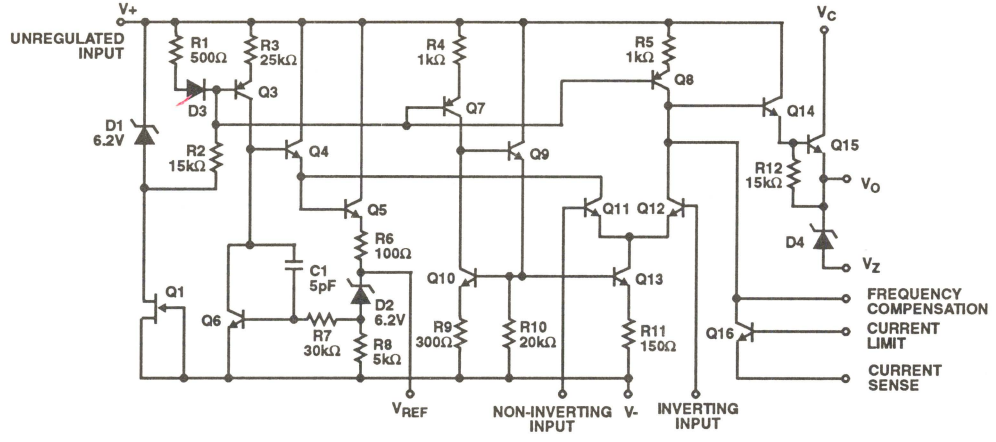


FIGURE 1. EQUIVALENT SCHEMATIC DIAGRAM OF THE CA723 AND CA723C

Typical Performance Curves (CA723)

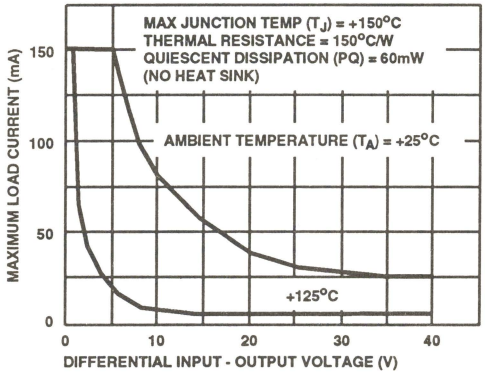


FIGURE 2. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

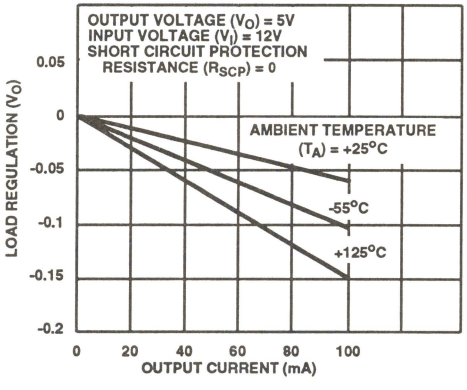


FIGURE 3. LOAD REGULATION WITHOUT CURRENT LIMITING

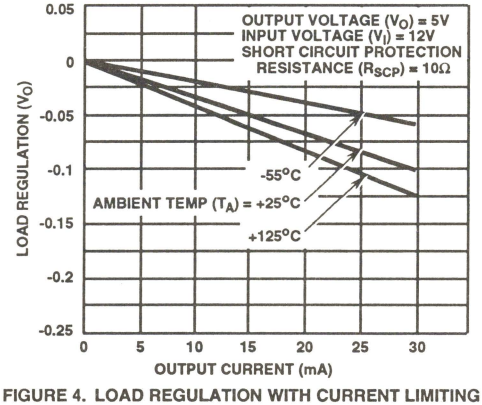


FIGURE 4. LOAD REGULATION WITH CURRENT LIMITING

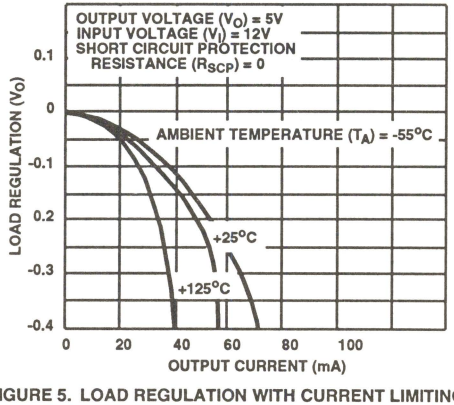


FIGURE 5. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

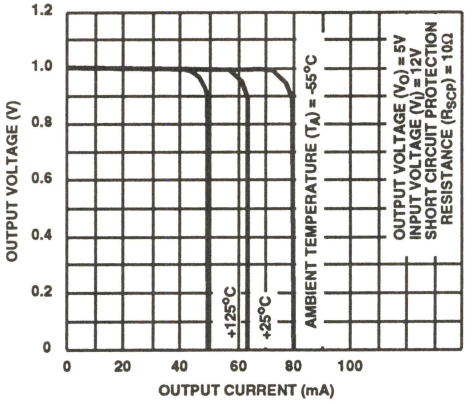


FIGURE 6. CURRENT LIMITING CHARACTERISTICS

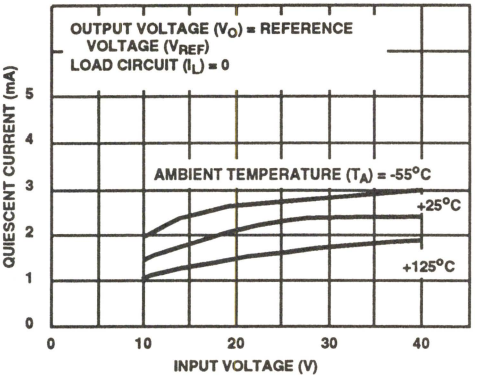


FIGURE 7. QUIESCENT CURRENT vs INPUT VOLTAGE

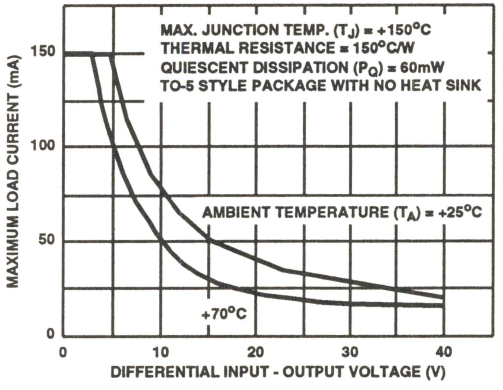


FIGURE 8. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

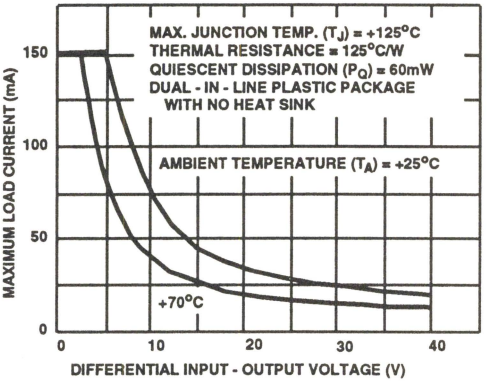


FIGURE 9. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE FOR CA723CE

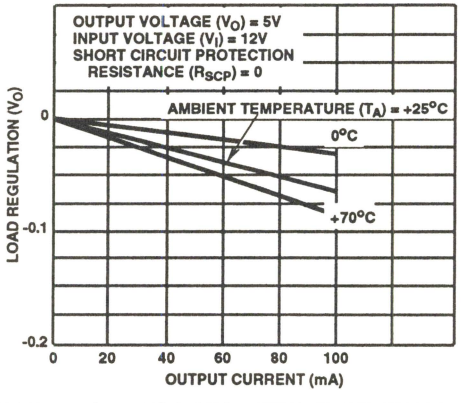


FIGURE 10. LOAD REGULATION WITHOUT CURRENT LIMITING

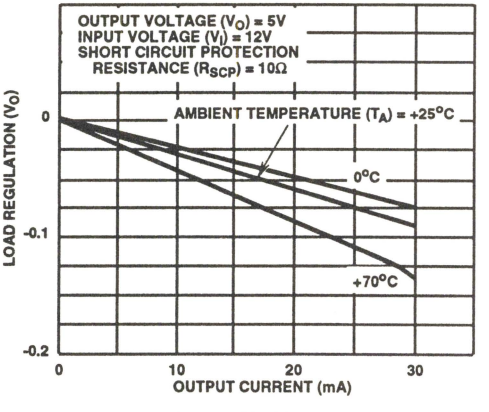


FIGURE 11. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

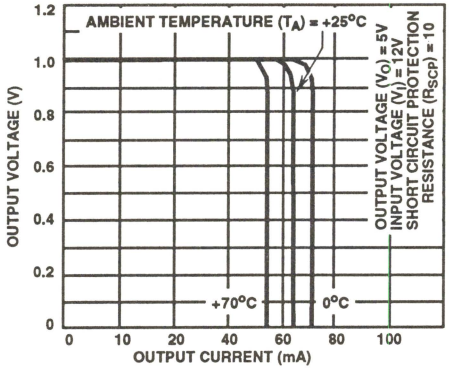


FIGURE 12. CURRENT LIMITING CHARACTERISTICS

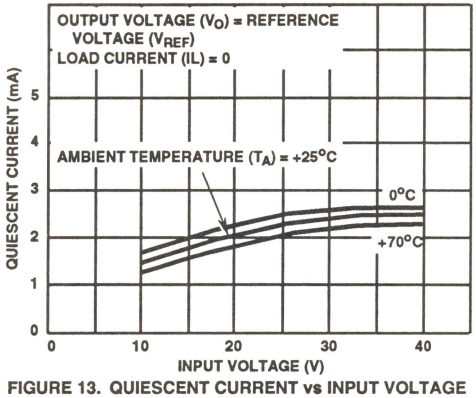


FIGURE 13. QUIESCENT CURRENT vs INPUT VOLTAGE

Typical Performance Curves (CA723 and CA723C)

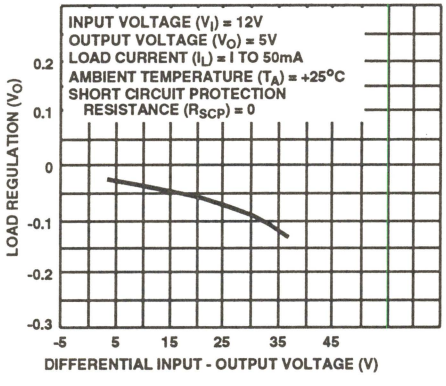


FIGURE 14. LOAD REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

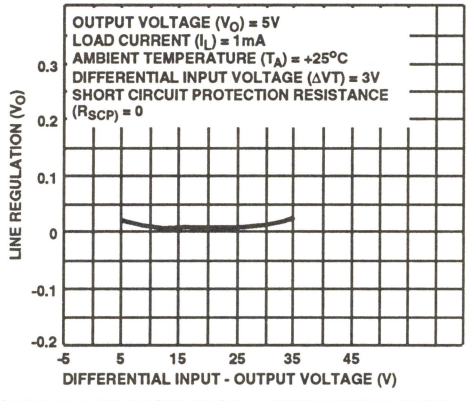


FIGURE 15. LINE REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

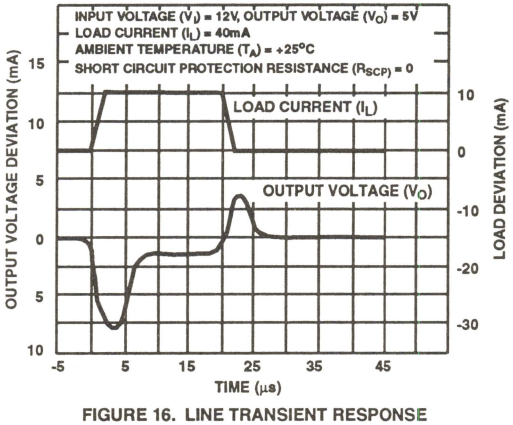


FIGURE 16. LINE TRANSIENT RESPONSE

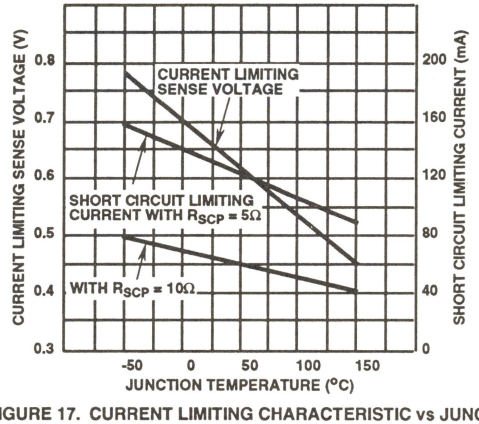


FIGURE 17. CURRENT LIMITING CHARACTERISTIC vs JUNCTION TEMPERATURE

Typical Performance Curves (CA723 and CA723C) (Continued)

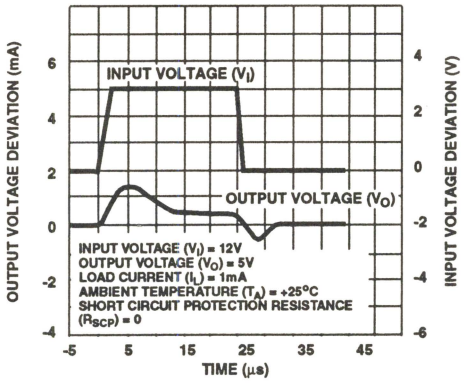


FIGURE 18. LOAD TRANSIENT RESPONSE

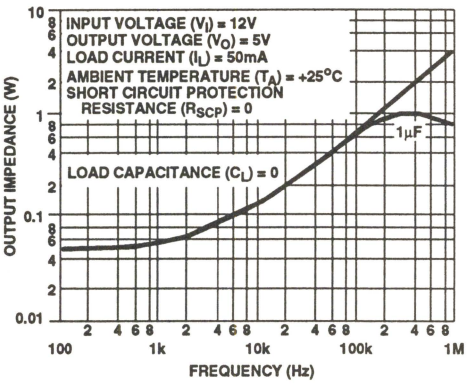
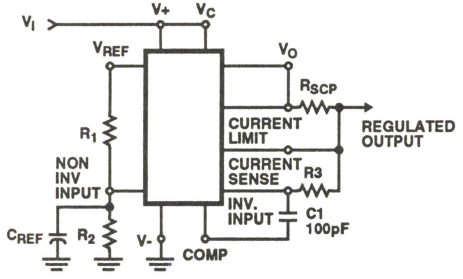


FIGURE 19. OUTPUT IMPEDANCE vs FREQUENCY

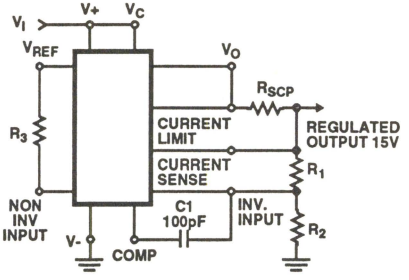
Typical Application Circuits



Circuit Performance Data:
Regulated Output Voltage 5V
Line Regulation (ΔV_I= 3V) 0.5mV
Load Regulation (ΔI_L = 50mA) 1.5mV

Note: R3 = $\frac{R1\,R2}{R1 + R2}$ For Minimum Temperature Drift

FIGURE 20. LOW VOLTAGE REGULATOR CIRCUIT (V_O = 2V TO 7V)

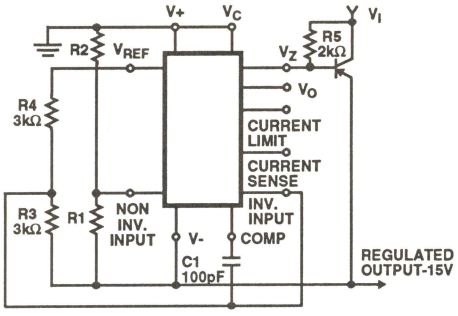


Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 1.5mV
Load Regulation (ΔI_L = 50mA) 4.5mV

Note: R3 = $\frac{R1\,R2}{R1 + R2}$ For Minimum Temperature Drift
R3 May Be Eliminated For Minimum Component Count

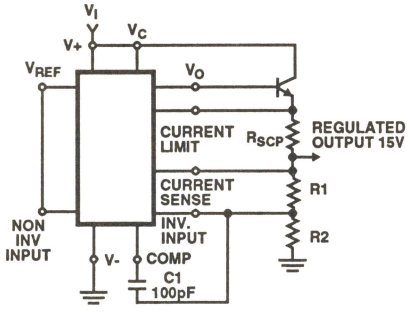
FIGURE 21. HIGH VOLTAGE REGULATOR CIRCUIT (V_O = 7V TO 37V)

Typical Application Circuits (Continued)



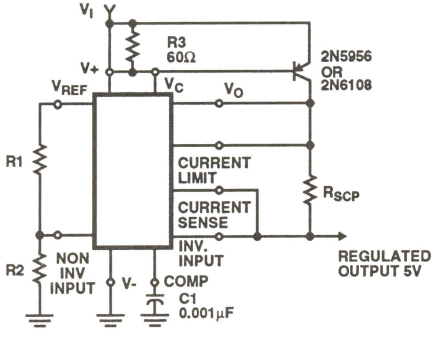
Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 1mV
Load Regulation (ΔI_L = 100mA) 2mV
Note: For Applications Employing the TO-5 Style Package and Where V_Z Is Required, An External; 6.2V Zener Diode Should be Connected in Series with V_O (Terminal 6).

FIGURE 22. NEGATIVE VOLTAGE REGULATOR CIRCUIT



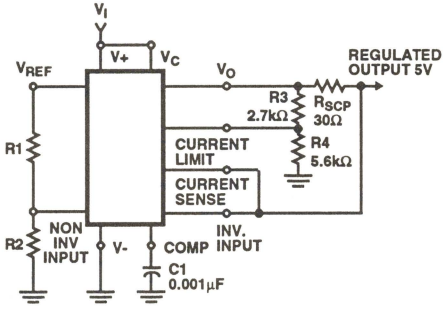
Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 1.5mV
Load Regulation (ΔI_L = 1A) 15mV

FIGURE 23. POSITIVE VOLTAGE REGULATOR CIRCUIT (WITH EXTERNAL n-p-n PASS TRANSISTOR)



Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 0.5mV
Load Regulation (ΔI_L = 1A) 5mV

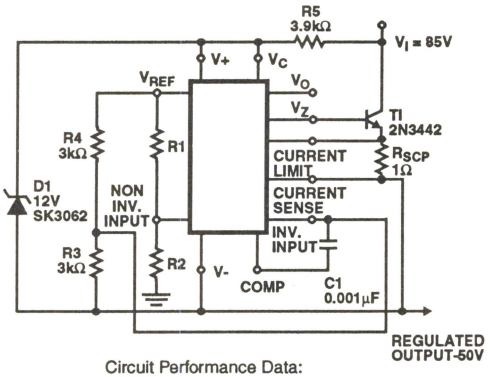
FIGURE 24. POSITIVE VOLTRAGE REGULATOR CIRCUIT (WITH EXTERNAL p-n-p PAS TRANSISTOR)



Circuit Performance Data:
Line Regulation (ΔV = 3V) 0.5mV
Load Regulation (ΔI_L = 10mA) 1mV
Short Circuit Current 20mA

FIGURE 25. FOLDBACK CURRENT LIMITING CIRCUIT

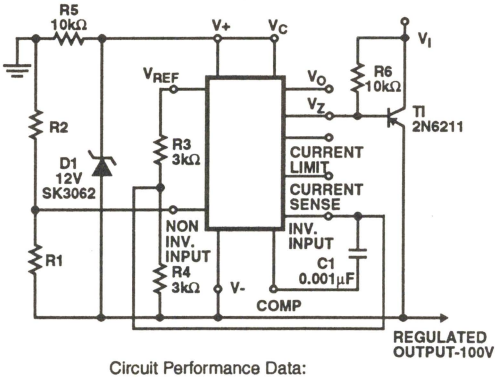
Typical Application Circuits (Continued)



Circuit Performance Data:
Line Regulation (ΔV = 20V) 15mV
Load Regulation (ΔI_L = 50mA) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

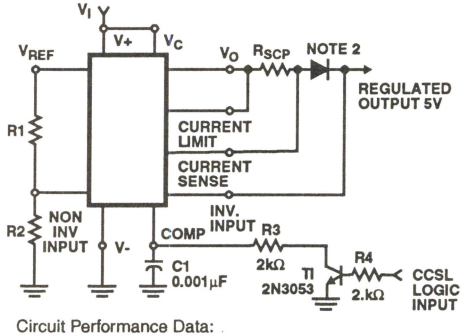
FIGURE 26. POSITIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
Line Regulation (ΔV_I = 20V) 30mV
Load Regulation (ΔI_L =100mA) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

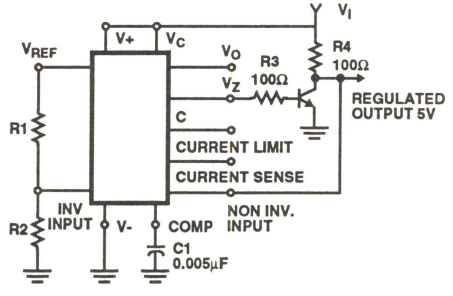
FIGURE 27. NEGATIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 0.5mV
Load Regulation (ΔI_L = 50mA) 1.5mV
Short Circuit Current 20mA

NOTE: 1. A current limiting transistor may be used for shutdown if current limiting is not required.
2. Add a diode if V_O > 10V.

FIGURE 28. REMOTE SHUTDOWN REGULATOR CIRCUIT WITH CURRENT LIMITING



Circuit Performance Data:
Line Regulation (ΔV_I = 10V) 0.5mV
Load Regulation (ΔI_L = 100mA) 1.5mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6).

FIGURE 29. SHUNT REGULATOR CIRCUIT

HARRIS SEMICONDUCTOR

CA1523

Voltage Regulator Control Circuit for Variable Switching Regulator

April 1994

Features

- Operates up to 200kHz
- Pins ESD Protected
- Remote ON/OFF
- Slow Start with Reset
- Overcurrent Sensing
- Lower Peak Currents than PWM Regulator
  - Less Prone to Magnetic Saturation

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA1523E	0°C to +70°C	14 Lead Plastic DIP

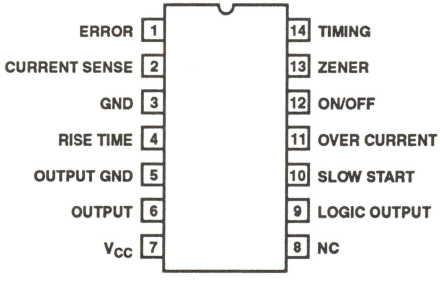
Description

The CA1523 monolithic silicon integrated circuit is a variable interval pulse regulator designed to provide the control circuitry for use in switching regulator circuits. It operates from 11V to 15V.

The regulator provides a single output drive capable of 300mA source/200mA sink. The maximum operating frequency is better than 200kHz. An attractive feature of the CA1523 is that the timing capacitor charge and discharge current is set up externally via a single resistor. The ratio of charge to discharge current is internally set at a maximum of 2 to 1 allowing simultaneous change in output pulse width with increased frequency at higher load. The pulse width variation at higher frequencies effectively compensates for the losses in magnetics and thereby increases the power supply efficiency at higher load end by as much as 20 percent.

Pinout

CA1523 (PDIP)
TOP VIEW



7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 1785.2

Absolute Maximum Ratings

DC Supply Voltage 15V
Supply Current
$I_{6(MAX)}$ . . . . . ±50mA
$I_{6(MAX)}$, 1µs,1800pF Load . . . . . +300, -200mA
Device Dissipation
Up to T_A = 70°C 530mW
Above T_A = 70°C. . . . . .Derate Linearly at 6.7mW/°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package . . . . . 120°C/W
Device Dissipation
Up to T_A = 70°C. 665mW
Ambient Temperature Range
Operating. . . . . 0°C to +70°C
Storage . . . . . -55°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± in. (1.59mm ±0.79mm)
from case for 10s Max. . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, Refer to condition shown in test circuit; V_7 = 13V, V_1 = 5.9V Unless Otherwise Specified

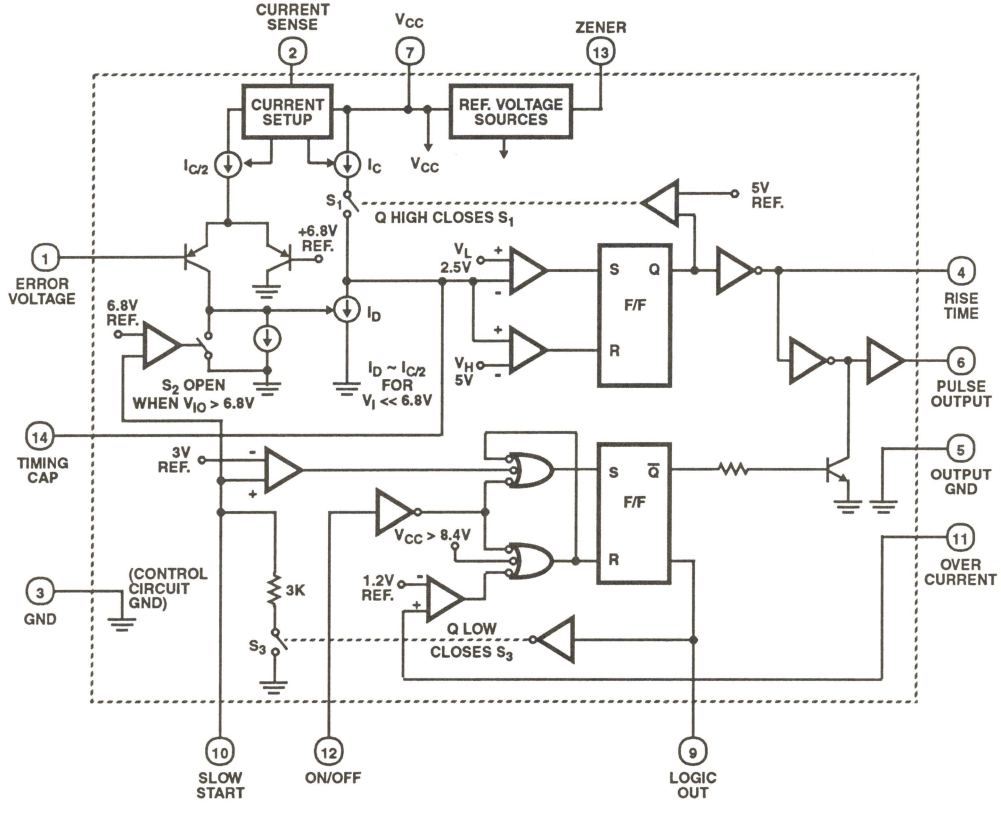
PARAMETERS	PIN	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY, V_{CC} (PIN 7)						
Supply Voltage	7		9.5	13	-	V
Supply Current	7	V_{CC} = +13V	20	27	34	mA
Zener Voltage	13		7.8	8.4	8.9	V
OUTPUT PULSE (PIN 6)						
Maximum Pulse Width	6	Measured at 6V Threshold Level	5.5	6.5	7.5	µs
Minimum Pulse Width	6	Measured at 6V Threshold Level	2	3	4	µs
Output High Voltage	6	I_6 = 0mA, V_4 = 0V	11.1	12	12.6	V
Output Low Voltage	6	I_6 = 50mA, V_{12} = 0V	0.6	1	1.3	V
Rise Time	6	Measured at 1.8V and 10V Threshold Levels	250	600	1250	ns
Fall Time	6	Measured at 1.8V and 10V Threshold Levels	50	200	350	ns
ERROR VOLTAGE RANGE (PIN 1)						
Error Voltage Reference	1	Adjust R_T; Observe Pin 6 Min/Max Frequency Range	5.9	6.8	7.5	V
CHARGE CURRENT (PIN 14)						
Charge Current	14	Adjust R_T, V_1 = 7.5V; Set V_{14} = 0V, Then V_{14} = 2.5V	190	220	250	µA
Discharge Current	14	Adjust R_T = 5.9V; Set V_{14} = 5.5V, Then 5V	95	110	125	µA
Slow Start Discharge Current	14	Maintain V_{14} = 5V, V_{10} = 5.5V Set V_{10} = 5.5V, Measure I_{14} (Hi) Set V_{10} = 4V, Measure I_{14} (Lo) Limits = $\frac{I_{14}\text{ (Hi)} - I_{14}\text{ (Lo)}}{1.5}$	20	30	40	µA/V
LOGIC TESTS						
Discharge Voltage	10	Pin 12 = 1kΩ to GND	1.7	2.4	3.2	V
Output Inhibit Voltage	7	Increase V_7 Until $V_9 \geq 2V$	7.9	8.4	9.1	V
Overcurrent Trip Voltage	11	V_{12} = 5V; V_{10} = 0V; Increase V_{11} Until $V_9 \leq 0.5V$	1.1	1.25	1.4	V

Other Desirable Features

Other desirable features along with various circuit block function explanations are listed below.

- The **Oscillator** is a sawtooth generator whose charge (rise) cycle determines the output pulse width and discharge which is continuously variable from very low to maximum of I_{CHARGE}.
- Charge $I_{CHARGE} = I_O - I_{DISCHARGE}$ giving 2 to 1 pulse-width control
- Discharge $I_{DISCHARGE}$ = approximately 0 to 1/2 I_O to frequency control.
- **Pulse Shaping:** Applied to the oscillator output via RS Flip-Flop with parallel inhibit controlled by slow-start overcurrent sense, supply voltage monitor and ON/OFF functions.
- **Pulse Rise Time:** Modified to meet RFI requirements by external slow-down capacitor.
- **Slow Start with Reset:** Externally programmed against internal 3V reference. Reset is initiated upon Inhibit ensuring soft start at power up and restart.
- **Over Current Sense:** Internal stable thresholds of 1.2V.
- **Supply Voltage Monitors:** Locks out the drive until V_{SUPPLY} has reached 8V-9V.
- **ON/OFF:** Activates regulator independent of raw DC.
- **Error Amplifier:** Compares output against a stable 6.8V internal reference and controls the discharge current sink on the timing capacitor.
- **Band-Gap:** Reference voltage (internal) provides temperature compensated 1.2V and 6.8V references.
- **Separate GND:** The power GND is separated from circuit ground for improved noise.
- **ESD Protection:** Pins are protected against ESD.

Block Diagram



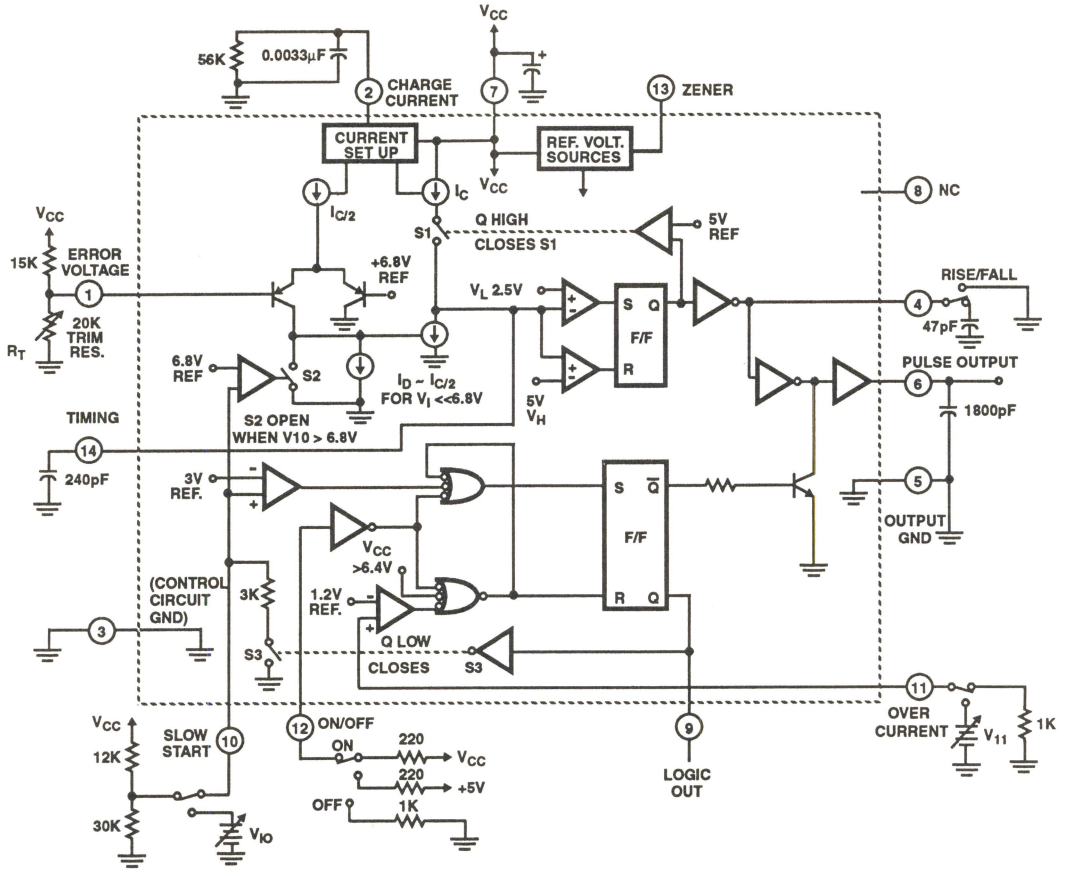


FIGURE 1. TEST CIRCUIT FOR THE CA1523

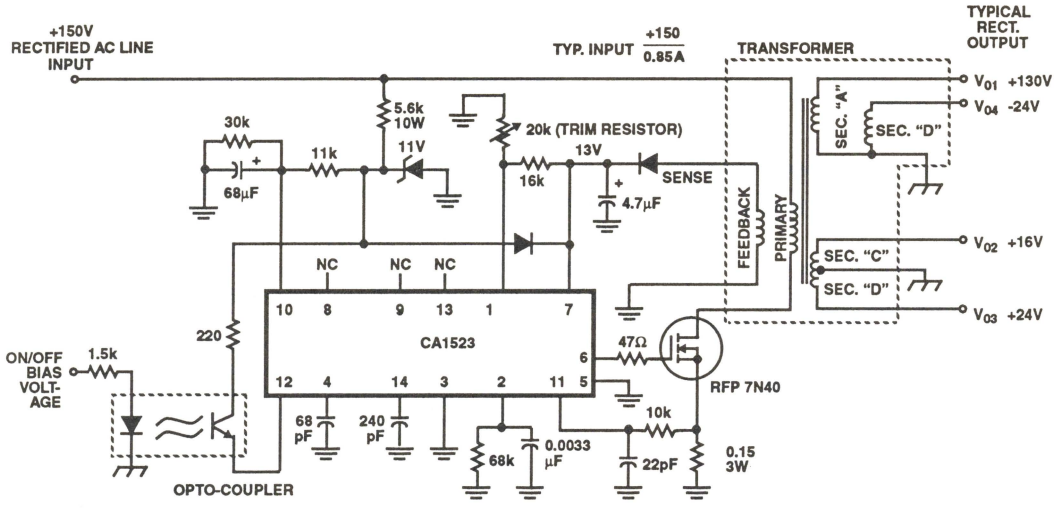


FIGURE 2. TYPICAL APPLICATION CIRCUIT FOR THE CA1523

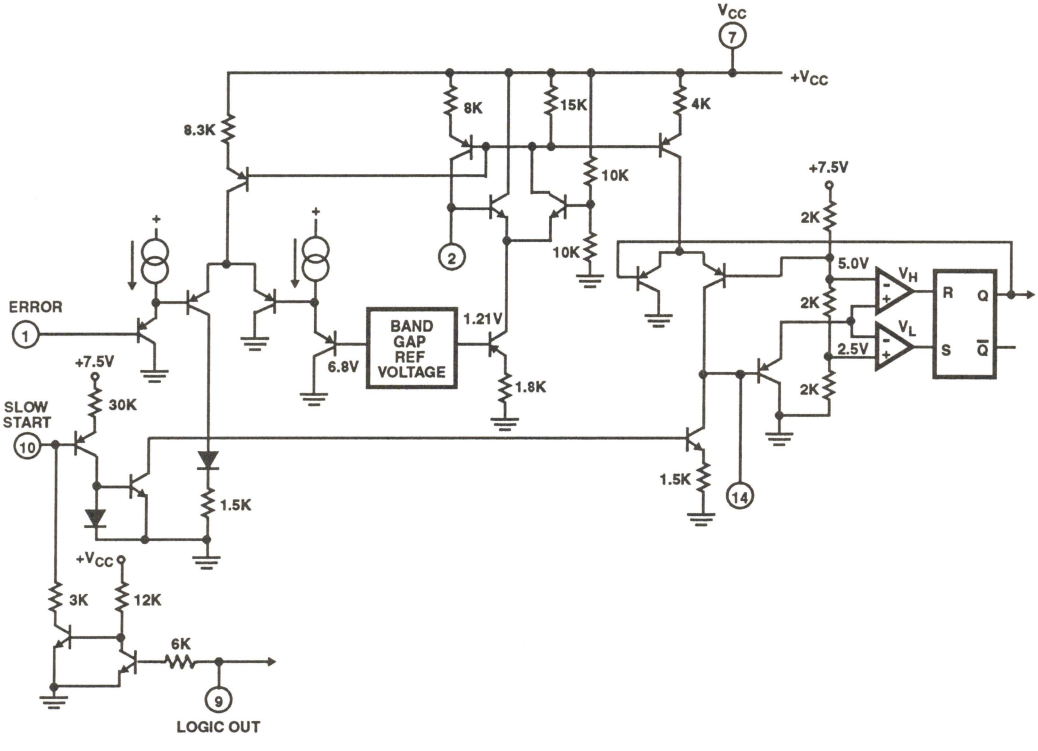


FIGURE 3. TIMING CIRCUIT FOR THE CA1523

HARRIS SEMICONDUCTOR

CA1524, CA2524 CA3524

April 1994

Regulating Pulse Width Modulator

Features

- Complete PWM Power Control Circuitry
- Separate Outputs for Single-Ended or Push-Pull Operation
- Line and Load Regulation . . . . . 0.2% (Typ)
- Internal Reference Supply with 1% (Max) Oscillator and Reference Voltage Variation Over Full Temperature Range
- Standby Current of Less Than 10mA
- Frequency of Operation Beyond 100kHz
- Variable-Output Dead Time of 0.5μs to 5μs
- Low $V_{CE(sat)}$ Over the Temperature Range

Applications

- Positive and Negative Regulated Supplies
- Dual-Output Regulators
- Flyback Converters
- DC-DC Transformer-Coupled Regulating Converters
- Single-Ended DC-DC Converters
- Variable Power Supplies

Description

The CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

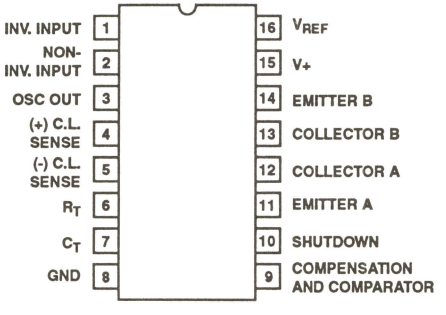
The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524, respectively. A block diagram of the CA1524 series is shown in Figure 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converter, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converter, as well as other power-control applications.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA1524E	-55°C to +125°C	16 Lead Plastic DIP
CA1524F	-55°C to +125°C	16 Lead CerDIP
CA2524E	0°C to +70°C	16 Lead Plastic DIP
CA2524F	0°C to +70°C	16 Lead CerDIP
CA3524E	0°C to +70°C	16 Lead Plastic DIP
CA3524F	0°C to +70°C	16 Lead CerDIP

Pinout

CA1524, CA2524, CA3524
(PDIP, CERDIP)
TOP VIEW

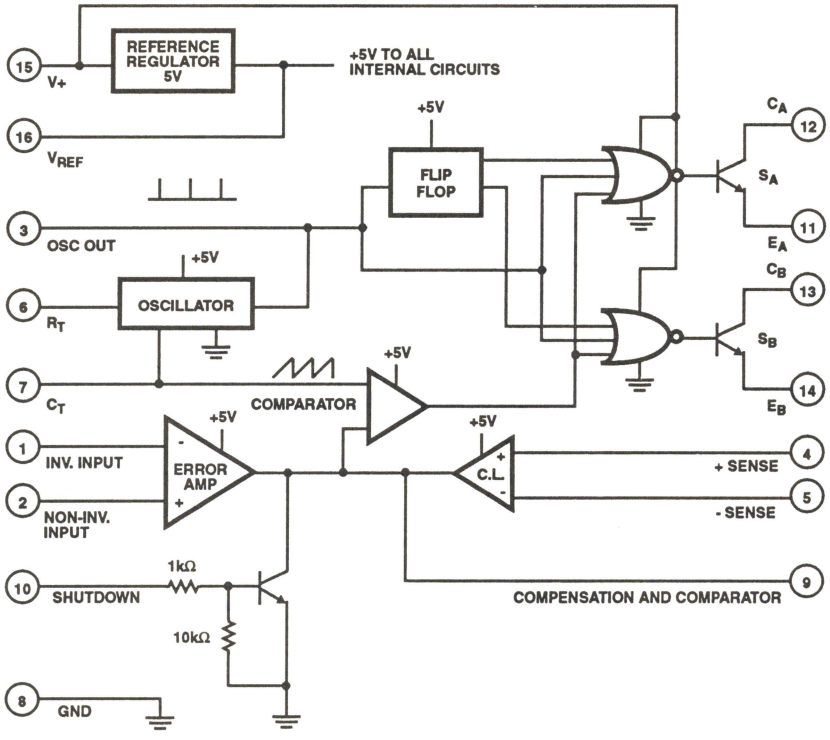


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

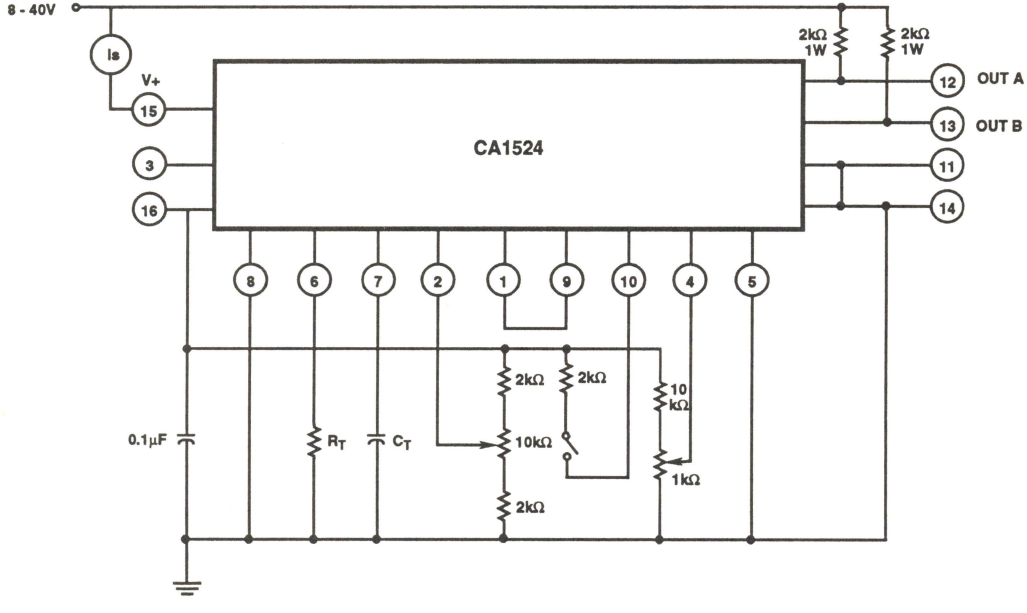
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File Number 1239.3

Functional Block Diagram



Test Circuit



Absolute Maximum Ratings

Input Voltage (Between V_{IN} and GND Terminals) 40V
Operating Voltage Range (V_{IN} to GND) . . . . . 8 to 40V
Output Current Each Output:
(Terminal 11, 12 or 13, 14) 100mA
Output Current (Reference Regulator) 50mA
Oscillator Charging Current 5mA

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package . . . . . 100°C/W
Device Dissipation
Up to T_A = +25°C 1.25W
Above T_A = +25°C . . . . . Derate Linearly at 10mW/°C
Operating Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± in. (1.59mm ±0.79mm)
from case for 10s Max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

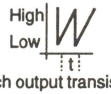
T_A = -55°C to +125°C for CA1524, 0°C to +70°C for the CA2524 and CA3524; V+ = 20V and f = 20kHz, Unless Otherwise Stated.

PARAMETER	TEST CONDITIONS	CA1524, CA2524			CA3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output Voltage		4.8	5	5.2	4.6	5	5.4	V
Line Regulation	V+ = 8 to 40V	-	10	20	-	10	30	mV
Load Regulation	I_L = 0 to 20mA	-	20	50	-	20	50	mV
Ripple Rejection	f = 120Hz, T_A = 25°C	-	66	-	-	66	-	db
Short Circuit Current Limit	V_{REF} = 0, T_A = 25°C	-	100	-	-	100	-	mA
Temperature Stability	Over Operating Temperature Range	-	0.3	1	-	0.3	1	%
Long Term Stability	T_A = 25°C	-	20	-	-	20	-	mV/khr
OSCILLATOR SECTION								
Maximum Frequency	C_T = 0.001µF, R_T = 2KΩ	-	300	-	-	300	-	kHz
Initial Accuracy	R_T and C_T Constant	-	5	-	-	5	-	%
Voltage Stability	V+ = 8 to 40V, T_A = 25°C	-	-	1	-	-	1	%
Temperature Stability	Over Operating Temperature Range	-	-	2	-	-	2	%
Output Amplitude	Terminal 3, T_A = 25°C	-	3.5	-	-	3.5	-	V
Output Pulse Width (Pin 3)	C_T = 0.01µF, T_A = 25°C	-	0.5	-	-	0.5	-	µs
Ramp Voltage Low (Note 1)	Pin 7	-	0.6	-	-	0.6	-	V
Ramp Voltage High (Note 1)	Pin 7	-	3.5	-	-	3.5	-	V
Capacitor Charging Current Range	Pin 7 (5-2 V_{BE})/R_T	0.03	-	2	0.03	-	2	mA
Timing Resistance Range	Pin 6	1.8	-	120	1.8	-	120	kΩ
Charging Capacitor Range	Pin 7	0.001	-	0.1	0.001	-	0.1	µF
Dead Time Expansion Capacitor on Pin 3 (when a small osc. cap is used)	Pin 3	100	-	1000	100	-	1000	pF
ERROR AMPLIFIER SECTION								
Input Offset Voltage	V_{CM} = 2.5V	-	0.5	5	-	2	10	mV
Input Bias Current	V_{CM} = 2.5V	-	1	10	-	1	10	µA
Open Loop Voltage Gain		72	80	-	60	80	-	dB
Common Mode Voltage	T_A = 25°C	1.8	-	3.4	1.8	-	3.4	V
Common Mode Rejection Ratio	T_A = 25°C	-	70	-	-	70	-	dB
Small Signal Bandwidth	A_V = 0dB, T_A = 25°C	-	3	-	-	3	-	MHz

Electrical Specifications T_A = -55°C to +125°C for CA1524, 0°C to +70°C for the CA2524 and CA3524; V+ = 20V and f = 20kHz, Unless Otherwise Stated. (Continued)

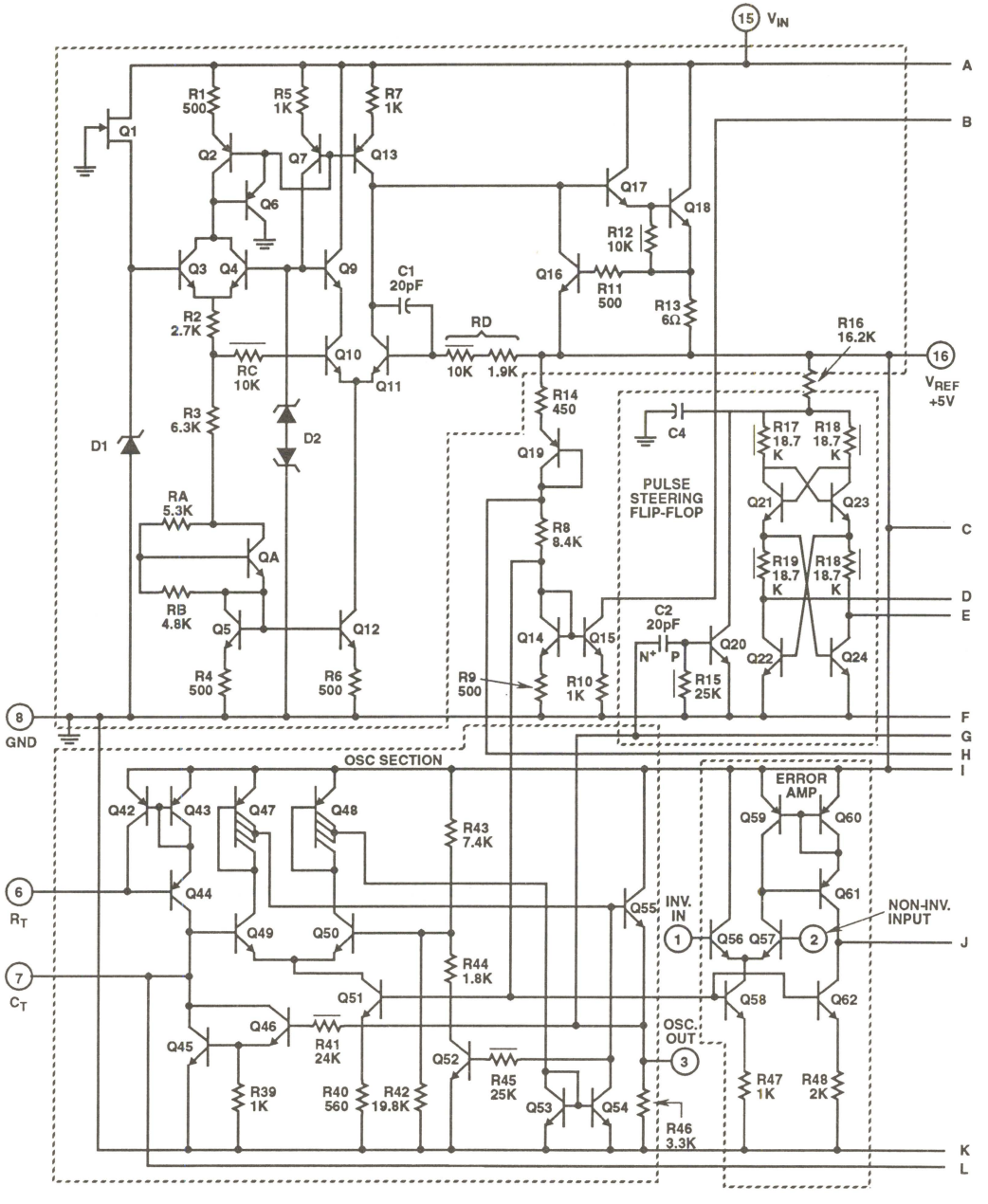
PARAMETER	TEST CONDITIONS	CA1524, CA2524			CA3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	T_A = 25°C	0.5	-	3.8	0.5	-	3.8	V
Amplifier Pole		-	250	-	-	250	-	Hz
Pin 9 Shutdown Current	External Sink	-	200	-	-	200	-	µA
COMPARATOR SECTION								
Duty Cycle	% Each Output On	0	-	45	0	-	45	%
Input Threshold	Zero Duty Cycle	-	1	-	-	1	-	V
Input Threshold	Max. Duty Cycle	-	3.5	-	-	3.5	-	V
Input Bias Current		-	1	-	-	1	-	µA
CURRENT LIMITING SECTION								
Sense Voltage for 25% Output Duty Cycle	Terminal 9 = 2V with Error Amplifier Set for Max Out, T_A = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.		-	0.2	-	-	0.2	-	mV/°C
Common Mode Voltage		-1	-	+1	-1	-	+1	V
Rolloff Pole of R51 C3 + Q64		-	300	-	-	300	-	Hz
OUTPUT SECTION (EACH OUTUT)								
Collector-Emitter Voltage		40	-	-	40	-	-	V
Collector Leakage Current	V_{CE} = 40V	-	0.1	50	-	0.1	50	µA
Saturation Voltage	V+ = 40V, I_C = 50mA	-	0.8	2	-	0.8	2	V
Emitter Output Voltage	V+ = 20V	17	18	-	17	18	-	V
Rise Time	R_C = 2KΩ, T_A = 25°C	-	0.2	-	-	0.2	-	µs
Fall Time	R_C = 2KΩ, T_A = 25°C	-	0.1	-	-	0.1	-	µs
Total Standby Current: (Note 2) I_S	V+ = 40V	-	4	10	-	4	10	mA

NOTES:

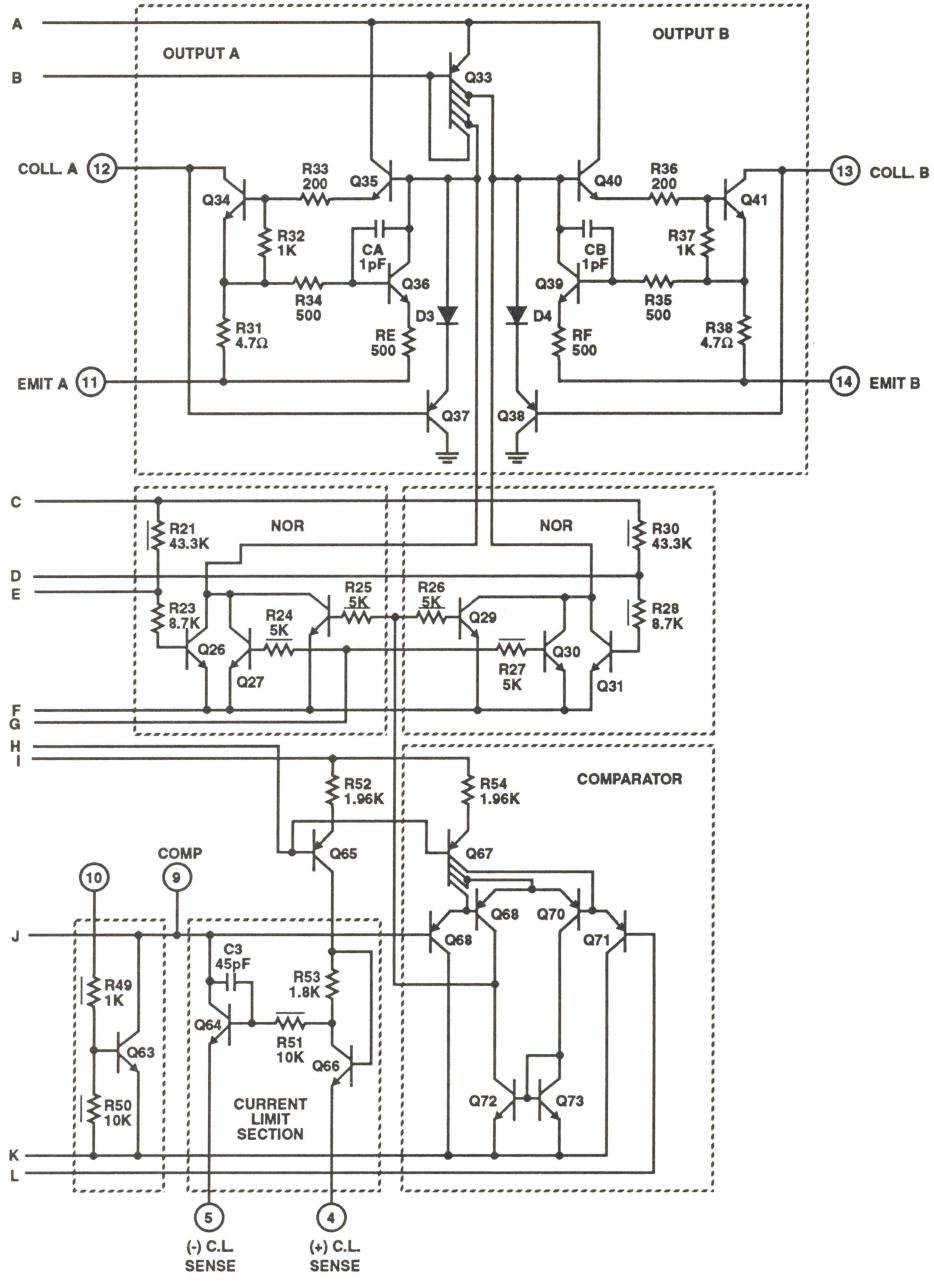
1. Ramp voltage at Pin 7 

where t = OSC period in microseconds
$t \cong R_T C_T$ with C_T in microfarads and R_T in ohms.
Output frequency at each output transistor is half OSC frequency when each output is used separately and is equal to the OSC frequency when each output is connected in parallel.
2. Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Schematic Diagram



Schematic Diagram (Continued)



Circuit Description

Voltage Reference Section

The CAI524 series contains an internal series voltage regulator employing a zener reference to provide a nominal 5-volt output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal l6 and is capable of supplying up to 50mA output current.

Figure 1 shows the temperature variation of the reference voltage with supply voltages of 8V to 40V and load currents up to 20mA. Load regulation and line regulation curves are shown in Figures 2 and 3, respectively.

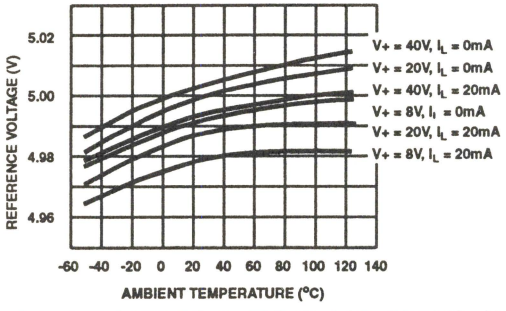


FIGURE 1. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

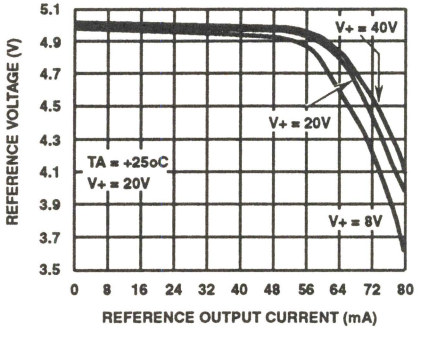


FIGURE 2. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF REFERENCE OUTPUT CURRENT

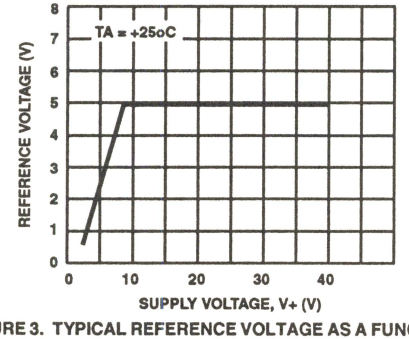


FIGURE 3. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6V to 3.5V and is used as the reference for the comparator in the device. The charging current is equal to $(5\text{-}2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30pA to 2mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5µs to 5µs for a capacitor range of 0.001 to 0.1µF. The pulse has two internal uses: as a dead-time control of blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Figure 4. Pulse widths less than 0.5µs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

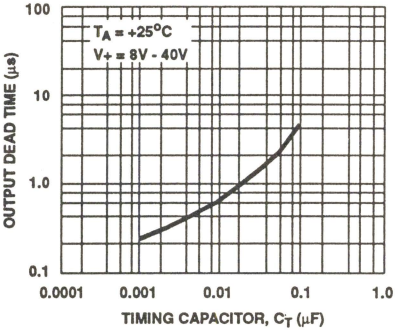


FIGURE 4. TYPICAL OUTPUT STAGE DEAD TIME AS A FUNCTION OF TIMING CAPACITOR VALUE

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100pF but no greater than 1000pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2-KΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_TC_T$, where R_T is in ohms, C_T is in µF, and t is in µs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals. Figure 5 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves

of the output duty cycle as a function of the voltage at terminal 9 are shown in Figure 7. To synchronize two or more CAI524's, one must be designated as master, with R_T C_T set for the correct period. Each of the remaining units (slaves) must have a C_T of 1/2 the value used in the master and approximately a 1010 longer R_TC_T period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

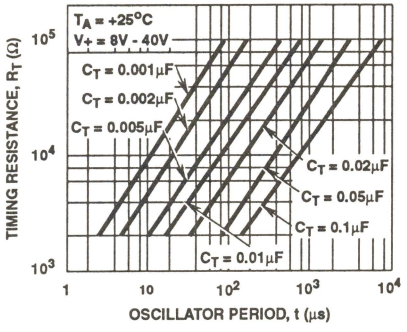


FIGURE 5. TYPICAL OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

Error Amplifier Section

The error amplifier consists of a differential pair (Q56,Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{OUT}, terminal 9, is very high (≅ 5MΩ).

The gain is:

$$A_V = g_m R = 8\, I_C\, R/2KT = 10^4,$$

where $$R = \frac{R_{OUT}\, R_L}{R_{OUT} + R_L}, \; R_L = \infty, \; A_V \propto 10^4$$

Since R_{OUT} is extremely high, the gain can be easily reduced from a nominal 10^4 (80dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Figure 6.

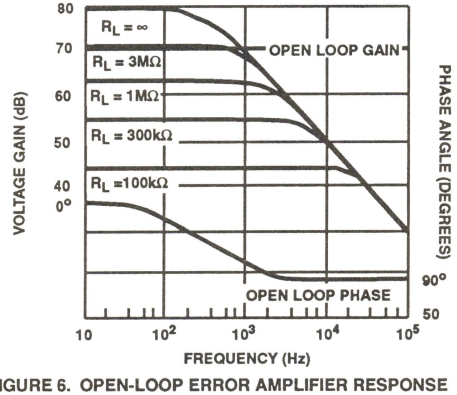


FIGURE 6. OPEN-LOOP ERROR AMPLIFIER RESPONSE CHARACTERISTICS.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Figure 7. The uncompensated amplifier has a single pole at approximately 250Hz and a unity gain cross-over at 3MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000-pF capacitor and a variable series 50-KΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5V reference can be used for conventional regulator applications if divided as shown in Figure 8. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

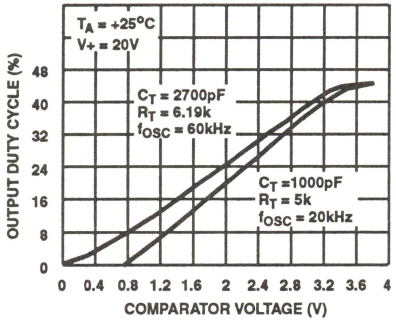


FIGURE 7. TYPICAL DUTY CYCLE AS A FUNCTION OF COMPARATOR VOLTAGE (AT TERMINAL 9).

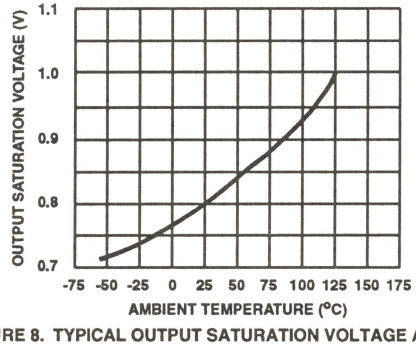


FIGURE 8. TYPICAL OUTPUT SATURATION VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE.

Output Section

The CA1524 series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100mA for each output and 100mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figures 8 and 9, respectively. There are a number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

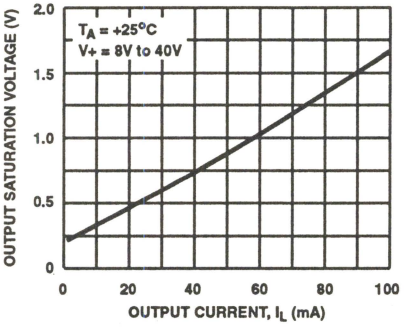


FIGURE 9. TYPICAL OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

Device Application Suggestions

For higher currents, the circuit of Figure 10 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5V supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6V.

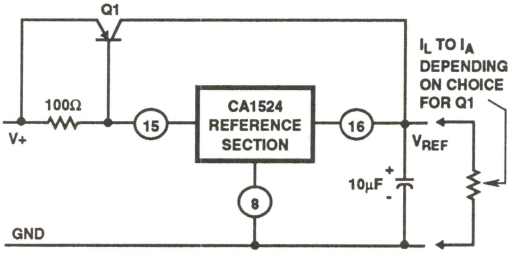


FIGURE 10. CIRCUIT FOR EXPANDING THE REFERENCE CURRENT CAPABILITY

The internal 5V reference can be used for conventional regulator applications if divided as shown in Figure 11. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

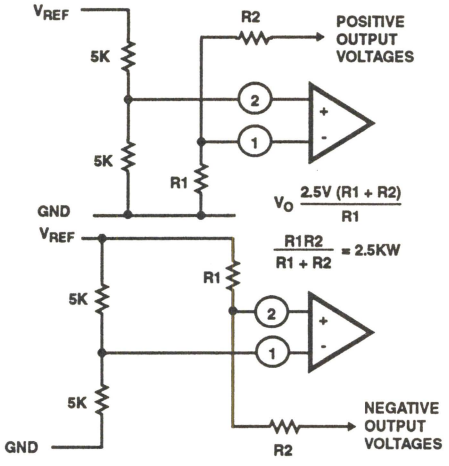
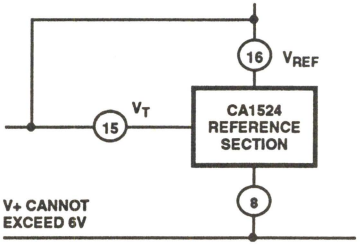


FIGURE 11. ERROR AMPLIFIER BIASING CIRCUITS



NOTE: V+ Should Be in the 5V Range And Must Not Exceed 6V

FIGURE 12. CIRCUIT TO ALLOW EXTERNAL BYPASS OF THE REFERENCE REGULATION

To provide an expansion of the dead time without loading the oscillator, the circuit of Figure 13 may be used.

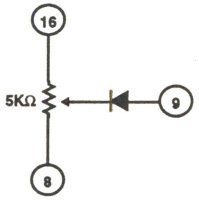


FIGURE 13. CIRCUIT FOR EXPANSION OF DEAD TIME, WITHOUT USING A CAPACITOR ON PIN 3 OR WHEN A LOW VALUE OSCILLATOR CAPACITOR IS USED

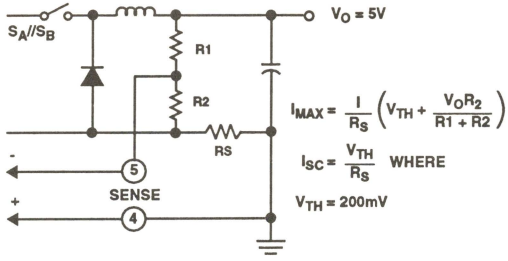
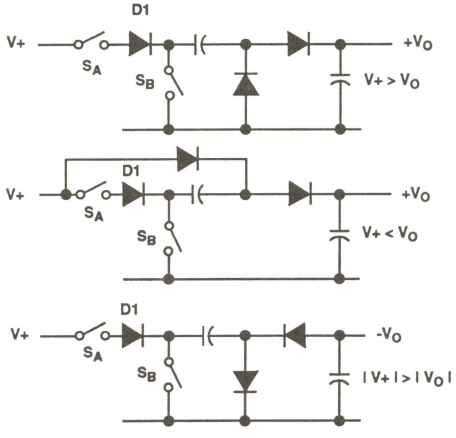


FIGURE 14. FOLDBACK CURRENT-LIMITING CIRCUIT USED TO REDUCE POWER DISSIPATION UNDER SHORTED OUTPUT CONDITIONS



NOTE: Diode D1 Is Necessary To Prevent Reverse Emitter-Base Breakdown of Transistor Switch S_A.

FIGURE 15. CAPACITOR-DIODE COUPLED VOLTAGE MULTIPLIER OUTPUT STAGES

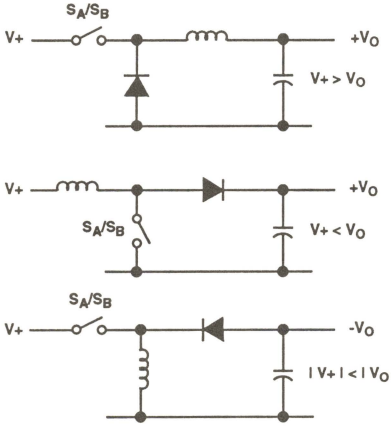


FIGURE 16. SINGLE-ENDED INDUCTOR CIRCUITS WHERE THE TWO OUTPUTS OF THE 1524 ARE CONNECTED IN PARALLEL

TABLE 1. INPUT vs. OUTPUT VOLTAGE, AND FEEDBACK RESISTOR VALUES FOR I_L = 40mA (FOR CAPACITOR-DIODE OUTPUT CIRCUIT IN FIGURE 18)

V_O (V)	R_2 (KΩ)	V+ (Min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

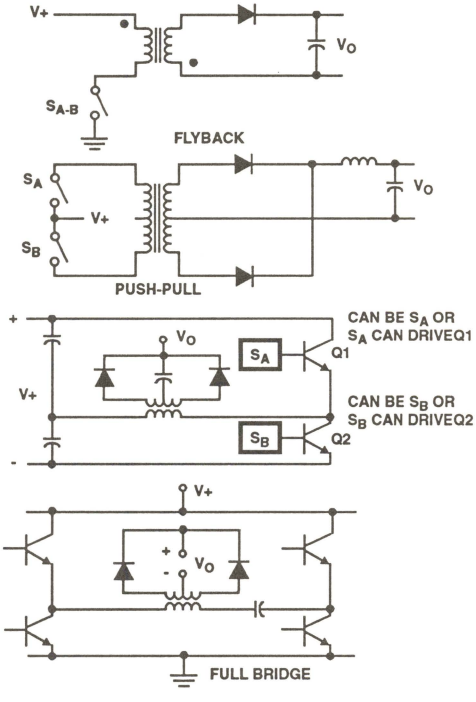


FIGURE 17. TRANSFORMER-COUPLED OUTPUTS

Applications (Note 1)

A capacitor-diode output filter is used in Figure 19 to convert +15V_{DC} to -5V_{DC} at output currents up to 50mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table 1 gives the required minimum input voltage and feedback resistor values, R2, for an output voltage.

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Figure18 to convert +15V_{DC} to -5V_{DC} at output currents up to 50mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table 1 gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5V to -20V with an output current of 40mA.

Single-Ended Switching Regulator

The CA1524 in the circuit of Figure 19 has both output stages connected in parallel to produce an effective 0% - 90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

NOTE:

1. For additional information on the application of this device and a further explanation of the circuits below, see Harris Application Note AN6915 "Application of the CA1524 series PWM IC".

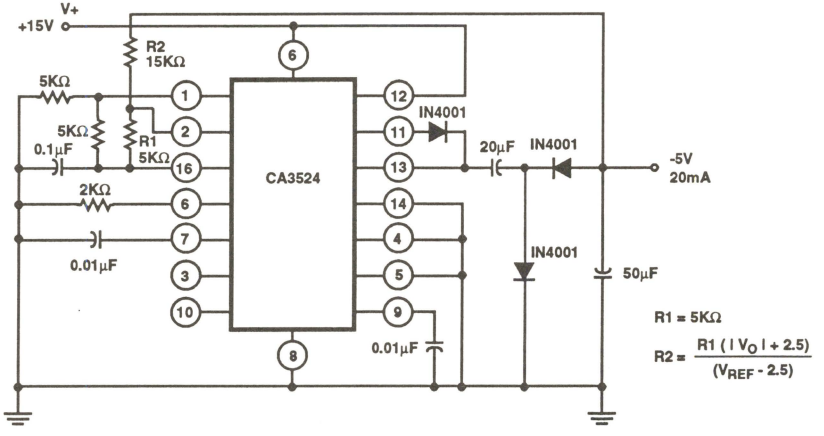
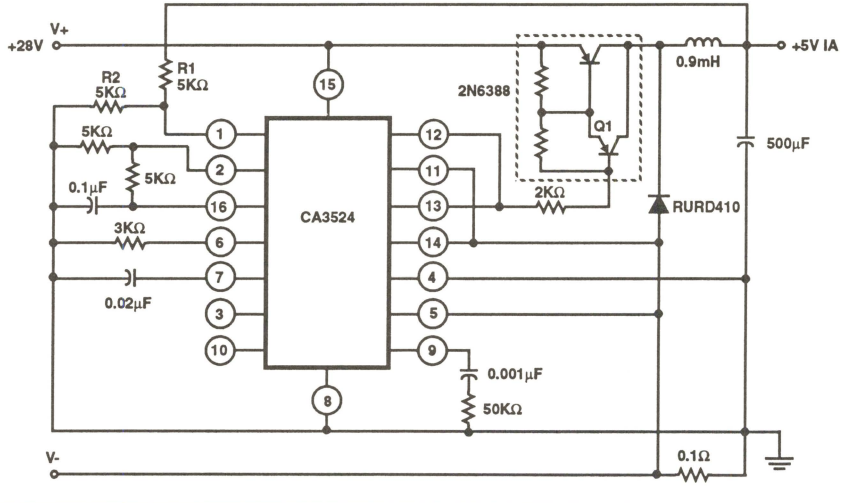


FIGURE 18. CAPACITOR-DIODE OUTPUT CIRCUIT



Flyback Converter

Figure 20 shows a flyback converter circuit for generating a dual 15V output at 20mA from a 5V regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Figure 21. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low-Frequency Pulse Generator

Figure 22 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5-V (or 2.5-V) pulse of 0% - 45% (or 0% - 90%) on time is possible over a frequency range of 150 to 500Hz. Switch S1 is used to go from a 5-V output pulse (S1 closed) to a 2.5-V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75Hz to 250Hz, respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500Hz. The frequency is adjusted by R1; R2 controls duty cycle.

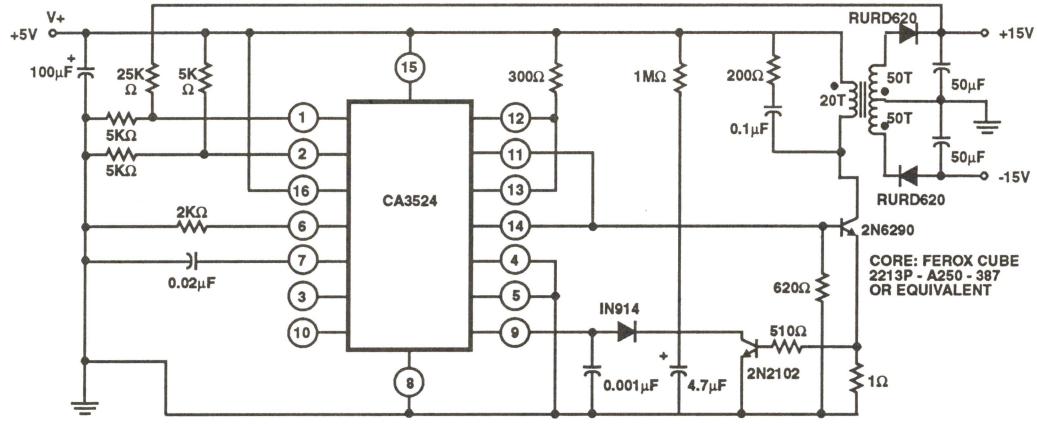


FIGURE 20. FLYBACK CONVERTER CIRCUIT

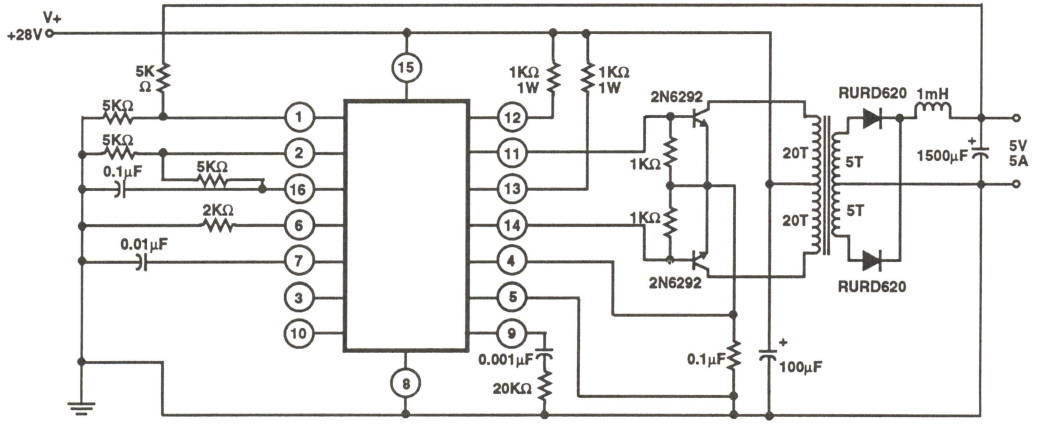
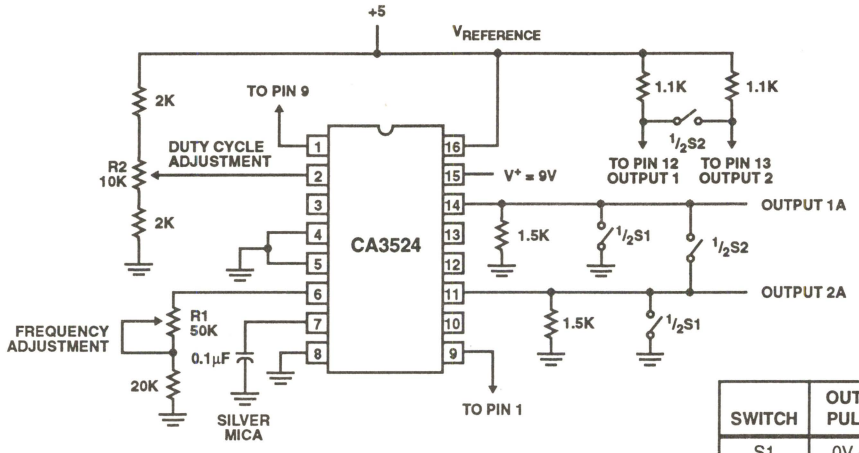


FIGURE 21. PUSH-PULL TRANSFORMER-COUPLED CONVERTER



SWITCH	OUTPUT PULSES	DUTY CYCLE
S1	0V - 5V	0% - 45%
S2	-	0% - 90%

FIGURE 22. LOW-FREQUENCY PULSE GENERATOR

The Variable Switcher

The circuit diagram of the CA1524, used as a variable output voltage power supply is shown in Figure 23. By connecting the two output transistors in parallel, the duty cycle is doubled, i.e., 0% - 90%. As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage.

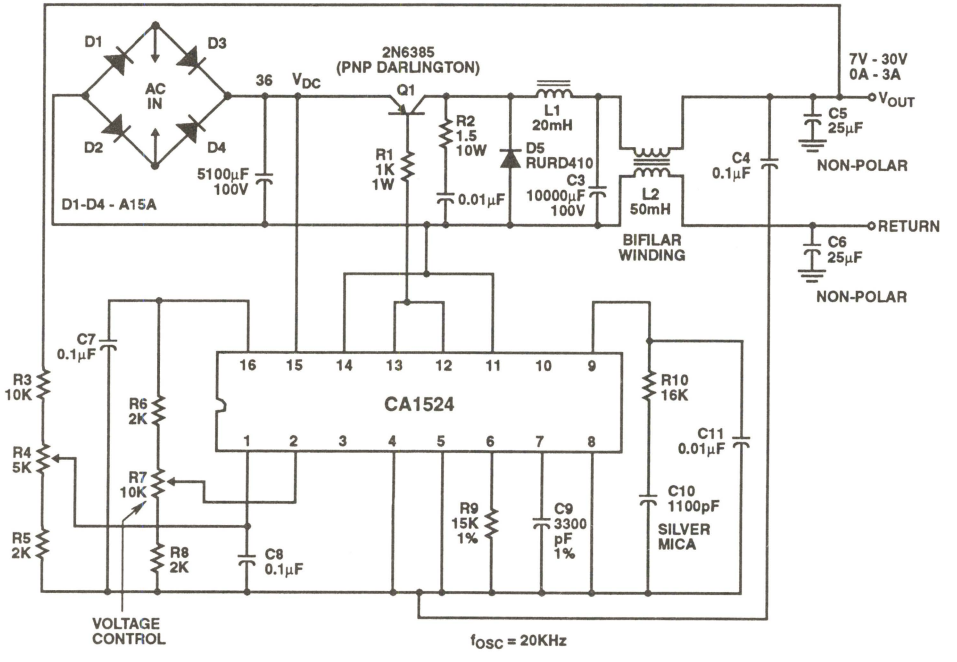


FIGURE 23. THE CA1524 USED AS A 0-5A, 7-30 V LABORATORY SUPPLY

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figures 24 and 25 uses half (Q2) of the CA1524 output in a low-voltage switching regulator (2.2V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5V internal regulator and a wide operating range of 8V to 40V, a single 9V battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

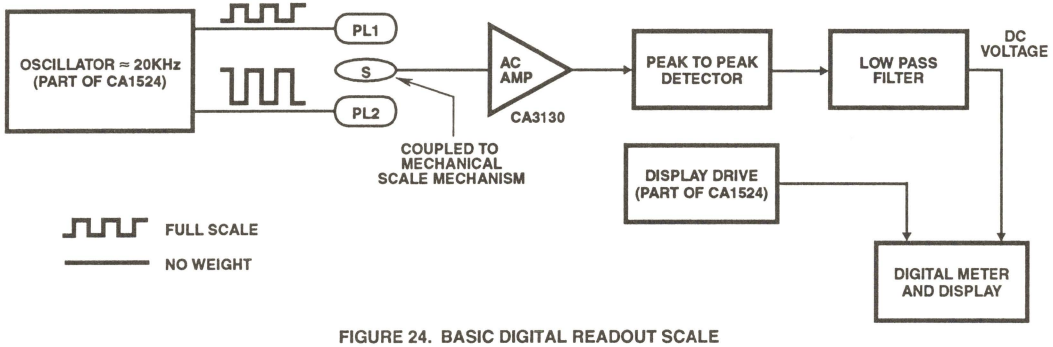


FIGURE 24. BASIC DIGITAL READOUT SCALE

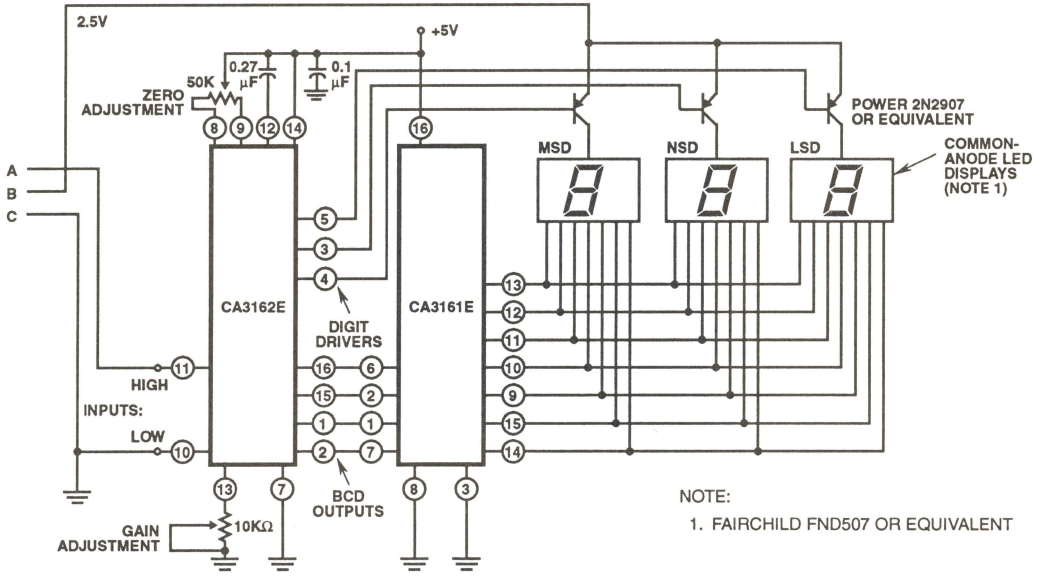


FIGURE 25. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE (CONT'D)

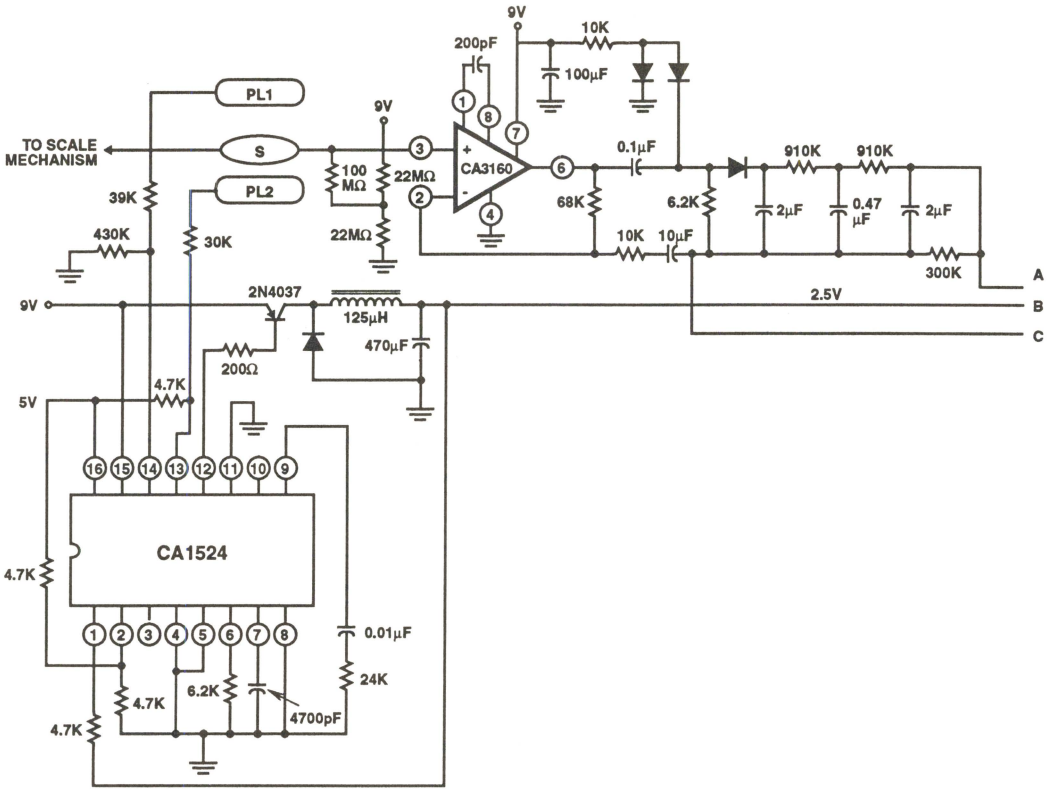
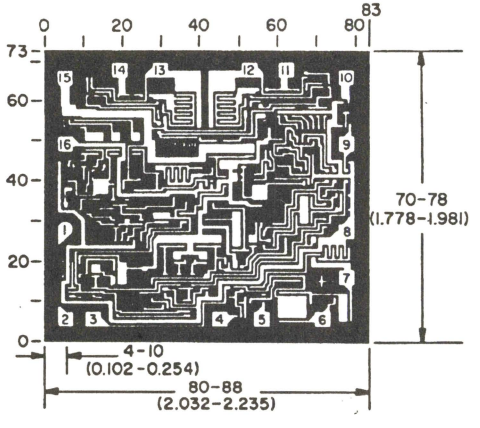


FIGURE 26. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE



DIMENSIONS AND PAD LAYOUT FOR CA3524RH CHIP

NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch). The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

HARRIS SEMICONDUCTOR

CA3085, CA3085A CA3085B

Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA

April 1994

Features

- Up to 100mA Output Current
- Input and Output Short-Circuit Protection
- Load and Line Regulation 0.025%
- Pin Compatible with LM100 Series
- Adjustable Output Voltage

Applications

- Shunt Voltage Regulator
- Current Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Combination Positive and Negative Voltage Regulator
- Dual Tracking Regulator

TYPE	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	MAX I_{OUT} (mA)	MAX LOAD REGULATION (%V_{OUT})
CA3085	7.5 to 30	1.8 to 26	12 (Note 1)	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

NOTE:

1. This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

Description

The CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7V to 46V at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

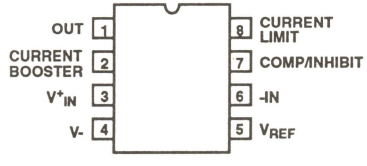
The CA3085A and CA3085B have output current capabilities up to 100mA and the CA3085 up to 12mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5V to 30V (CA3085), 7.5V to 40V (CA3085A), and 7.5V to 50V (CA3085B) and a minimum regulated output voltage of 26V (CA3085), 36V (CA3085A), and 46V (CA3085B).

Ordering Information

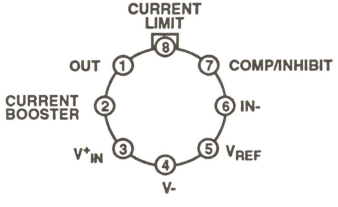
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3085, A, B	-55°C to +125°C	8 Pin Metal Can
CA3085E, AE, BE	-55°C to +125°C	8 Lead Plastic DIP

Pinouts

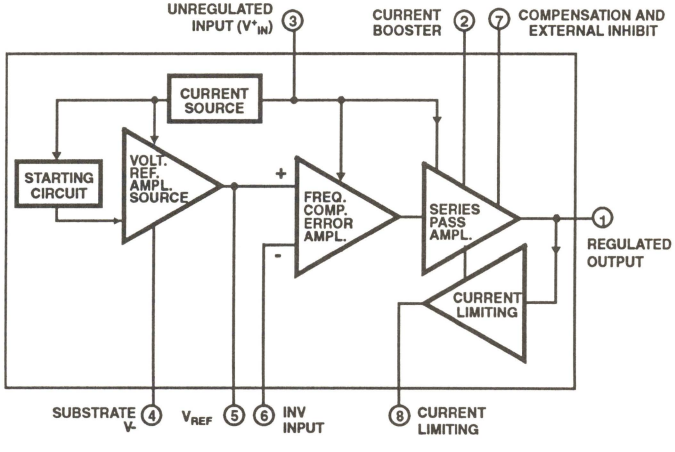
CA3085, A, B, E, AE, BE (PDIP)
TOP VIEW



CA3085S, AS, BS (CAN)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 491.4

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Unregulated Input Voltage
  CA3085 . . . . . 30V
  CA3085A 40V
  CA3085B 50V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
  Plastic DIP Package . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Metal Can (Without Heat Sink)	156°C/W	68°C/W
Plastic DIP Package	155°C/W	-

Maximum Package Power Dissipation
  Plastic DIP (Without Heat Sink)
    Up to T_A = 55°C 630mW
    Above T_A = 55°C . . . . . Derate Linearly at 6.67mW/°C
  Metal Can (With Heat Sink)
    Up to T_C = 55°C 1.6W
    Above T_C = 55°C . . . . . Derate Linearly at 16.7mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +1.7V to +46V Operating Temperature Range . . . . . -55°C to +125°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminal listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal Number 7 and horizontal Terminal Number 1 is +3 to -10V.

TERMINAL NUMBER	5	6	7	8	1	2	3	4
5	-	+5 -5	Note 1	Note 1	Note 1	Note 1	Note 1	+10 0
6	-	-	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
7	-	-	-	+3 -10	-103	Note 1	Note 1	+ (Note 2) 0
8	-	-	-	-	+5 -1	Note 1	Note 1	Note 1
1	-	-	-	-	-	+10 - (Note 2)	0 - (Note 2)	+ (Note 2) 0
2	-	-	-	-	-	-	0 -	+ (Note 2) 0
3	-	-	-	-	-	-	-	+ (Note 2) 0
4	-	-	-	-	-	-	-	Substrate and Case

NOTES:

1. Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.
2. 30V (CA3085); 40V (CA3085A); 50V (CA3085B)

Maximum Current Ratings

TERMINAL NUMBER	I_{IN} (mA)	I_{OUT} (mA)
5	10	1.0
6	1.0	-0.1
7	1.0	-0.1
8	0.1	10
1	20	150
2	150	60
3	150	60
4	-	-

DC Electrical Specifications T_A = +25°C, Unless Otherwise Specified

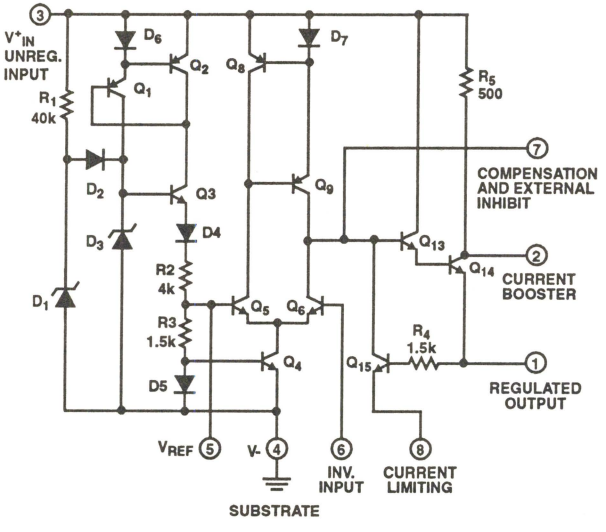
PARAMETERS	SYMBOL	TEST CONDITIONS	CA3085			CA3085A			CA3085B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS												
Reference Voltage	V_{REF}	V^+_{IN} = 15V (Figure 3)	1.4	1.6	1.8	1.5	1.6	1.7	.15	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	V^+_{IN} = 30V (Figure 3)	-	3.3	4.5	-	-	-	-	-	-	mA
		V^+_{IN} = 40V (Figure 3)	-	-	-	-	3.65	5	-	-	-	mA
		V^+_{IN} = 50V (Figure 3)	-	-	-	-	-	-	-	4.05	7	mA
Input Voltage Range	$V_{IN(range)}$		7.5	-	30	7.5	-	40	7.5	-	50	V
Maximum Output Voltage	$V_{O(MAX)}$	V^+_{IN} = 30, 40, 50V (Note 1); R_L = 365Ω; Term. No. 6 to GND (Figure 3)	26	27	-	36	37	-	46	47	-	V
Maximum Output Voltage	$V_{O(MIN)}$	V^+_{IN} = 30V (Figure 3)	-	1.6	1.8	-	1.6	1.7	-	1.6	1.7	V
Input - Output Voltage Differential	V_{IN}-V_{OUT}		4	-	28	4	-	38	3.5	-	48	V
Limiting Current	I_{LIM}	V^+_{IN} = 16V, V^+_{OUT} = 10V, RSCP = 6Ω (Note 2) (Figure 6)	-	96	120	-	96	120	-	96	120	mA
Load Regulation (Note 3)		I_L = 1 to 100mA, R_{SCP} = 0	-	-	-	-	0.025	0.15	-	0.025	0.15	%V_{OUT}
		I_L = 1 to 100mA, R_{SCP} = 0, T_A = 0°C to +70°C	-	-	-	-	0.035	0.6	-	0.035	0.6	%V_{OUT}
		I_L = 1 to 12mA, R_{SCP} = 0	-	0.003	0.1	-	-	-	-	-	-	%V_{OUT}
Line Regulation (Note 4)		I_L = 1mA, R_{SCP} = 0	-	0.025	0.1	-	0.025	0.075	-	0.025	0.04	%/V
		I_L = 1mA, R_{SCP} = 0, T_A = 0°C to +70°C	-	0.04	0.15	-	0.04	0.1	-	0.04	0.08	%/V
Equivalent Noise Output Voltage	V_{NOISE}	V^+_{IN} = 25V (Figure 10), C_{REF} = 0	-	0.5	-	-	0.5	-	-	0.5	-	mVp-p
		V^+_{IN} = 25V (Figure 10), C_{REF} = 0.22µF	-	0.3	-	-	0.3	-	-	0.3	-	mVp-p
Ripple Rejection		V^+_{IN} = 25V, f = 1kHz (Figure 11), C_{REF} = 0	-	50	-	-	50	-	45	50	-	dB
		V^+_{IN} = 25V, f = 1kHz (Figure 11), C_{REF} = 2µF	-	56	-	-	56	-	50	56	-	dB
Output Resistance	r_O	V^+_{IN} = 25V, f = 1kHz (Figure 11)	-	0.075	1.1	-	0.075	0.3	-	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	V_{REF}, V_O (Note 4)	I_L = 0, V_{REF} = 1.6V	-	0.0035	-	-	0.0035	-	-	0.0035	-	%/°C

DC Electrical Specifications T_A = +25°C, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3085			CA3085A			CA3085B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
LOAD TRANSIENT RECOVERY TIME												
Turn On	t_{ON}	V^+_{IN} = 25V, +50mA Step (Figure 16)	-	1	-	-	1	-	-	1	-	µs
Turn Off	t_{OFF}	V^+_{IN} = 25V, -50mA Step (Figure 16)	-	3	-	-	3	-	-	3	-	µs
LOAD TRANSIENT RECOVERY TIME												
Turn On	t_{ON}	V^+_{IN} = 25V, f = 1kHz, 2V Step	-	0.8	-	-	0.8	-	-	0.8	-	µs
Turn Off	t_{OFF}		-	0.4	-	-	0.4	-	-	0.4	-	µs

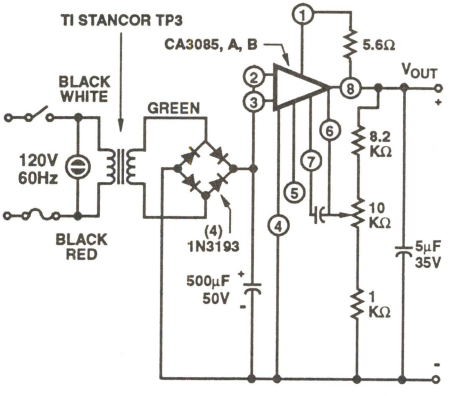
NOTES:

1. 30V (CA3085), 40V (CA3085A), 50V (CA3085B)
2. R_{SCP}: Short Circuit Protection Resistance
3. Load Regulation = $[\Delta V_{OUT} + V_{OUT}(initial)]$ x 100%
4. Line Regulation = $[\Delta V_{OUT} + V_{OUT}(initial)(\Delta V_{IN})]$ x 100%



All Resistance Values are in Ohms

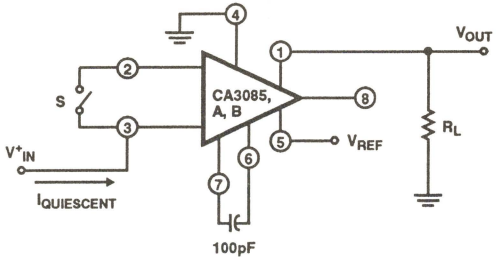
FIGURE 1. SCHEMATIC DIAGRAM OF CA3085 SERIES



V_{OUT} = 3.5V to 20V (0 to 90mA)
Regulation = 0.2% (Line and Load)
Ripple < 0.5mV at Full Load

FIGURE 2. APPLICATION OF THE CA3085 SERIES IN A TYPICAL POWER SUPPLY

Test Circuits and Typical Performance Curves



TEST	R_L	V_{IN}	CONNECT TERM NO. 6	S
V_{REF}	∞	+1.6	Open	Open
$I_{QUIESCENT}$	∞	+40	Open	Open
$V_{OUT(MAX)}$	365Ω	+40	Ground	Closed
$V_{OUT(MIN)}$	10k	+30	Terminal No.1	Open

FIGURE 3. TEST CIRCUIT FOR V_{REF}, $I_{QUIESCENT}$, $V_{OUT(MAX)}$, $V_{OUT(MIN)}$

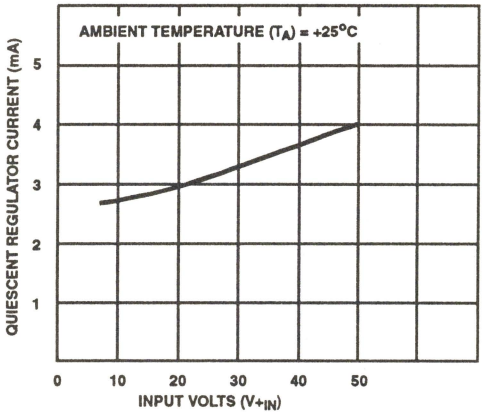


FIGURE 4. $I_{QUIESCENT}$ vs V^+_{IN}

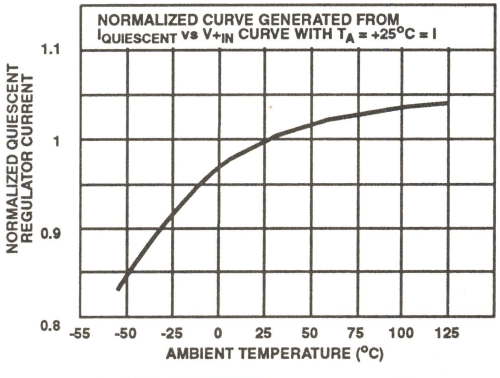
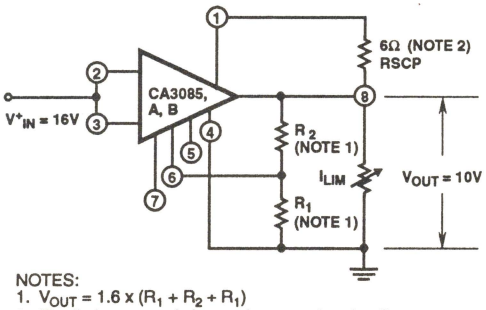


FIGURE 5. NORMALIZED $I_{QUIESCENT}$ vs T_A



NOTES:
1. $V_{OUT} = 1.6 \times (R_1 + R_2 + R_1)$
2. The limits current is inversely proportional to R_{SCP}

FIGURE 6. TEST CIRCUIT FOR LIMITING CURRENT

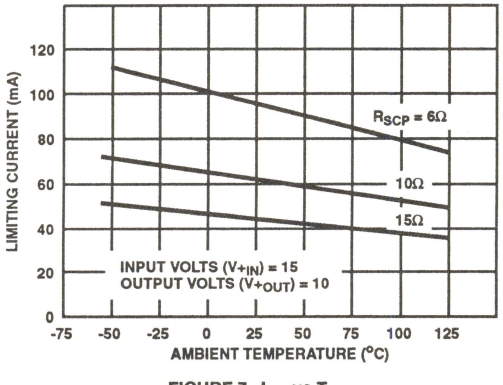


FIGURE 7. I_{LIM} vs T_A

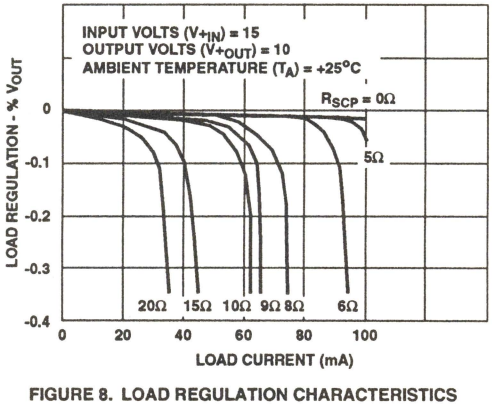


FIGURE 8. LOAD REGULATION CHARACTERISTICS

Test Circuits and Typical Performance Curves (Continued)

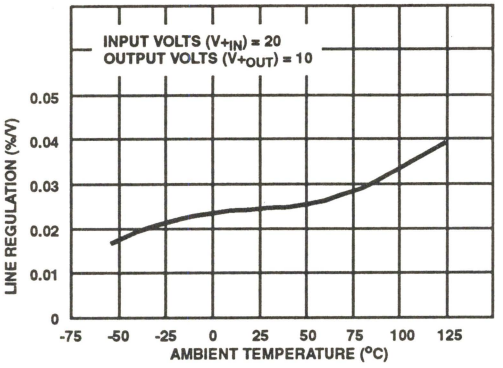


FIGURE 9. LINE REGULATION TEMPERATURE CHARACTERISTICS

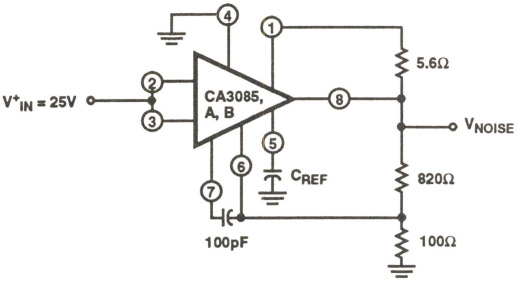


FIGURE 10. TEST CIRCUIT FOR NOISE VOLTAGE

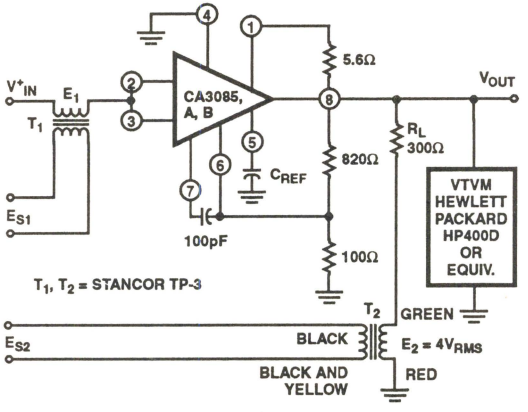


FIGURE 11. TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions

1. V_{IN} = +25V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1kHz so that $E_2 = 4V_{RMS}$
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or Equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT(R_L/E_2)}$

Ripple Rejection - I

Conditions

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1kHz so that $E_1 = 3V_{RMS}$
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or Equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection - II

Conditions

1. Repeat Ripple Rejection I with C_{REF} = 2µF

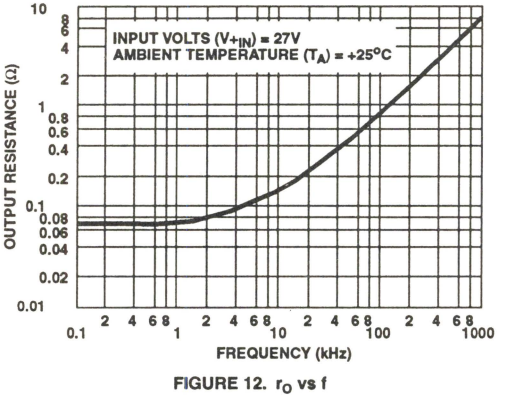


FIGURE 12. r_O vs f

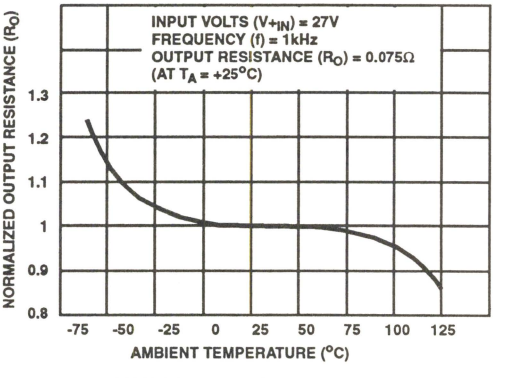


FIGURE 13. NORMALIZED r_O vs T_A

Test Circuits and Typical Performance Curves (Continued)

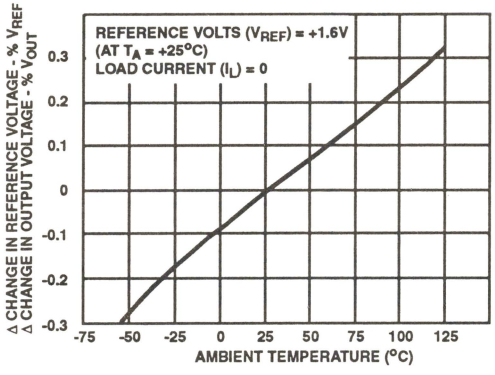


FIGURE 14. TEMPERATURE COEFFICIENT OF V_{REF} AND V_{OUT}

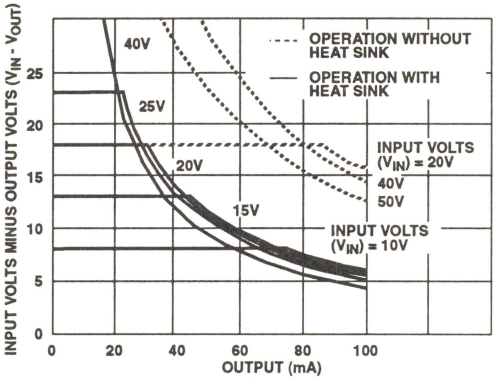
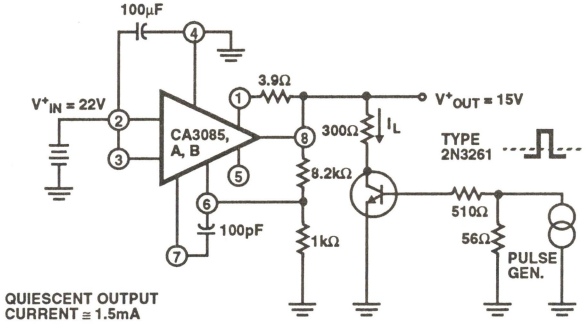


FIGURE 15. DISSIPATION LIMITATION (V_{IN} - V_{OUT} vs I_{OUT})



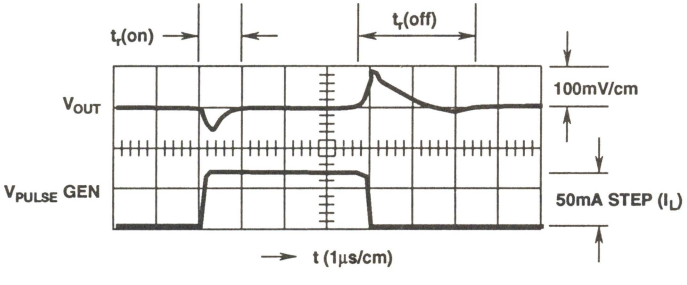


FIGURE 16. TURN-ON AND TURN-OFF RECOVERY TIME TEST CIRCUIT WITH ASSOCIATED WAVEFORMS

See Application Note AN6157 for further information

Typical Regulator Circuits

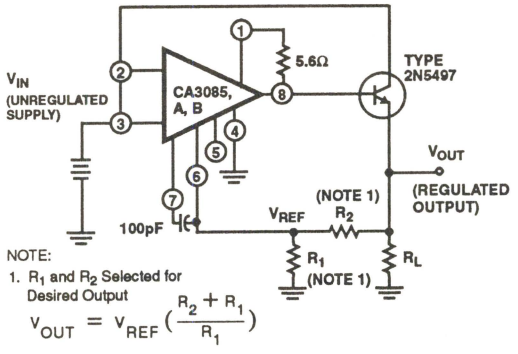
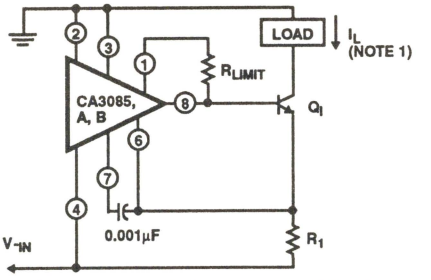


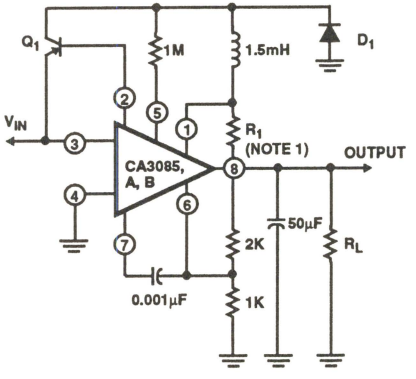
FIGURE 17. TYPICAL HIGH CURRENT VOLTAGE REGULATOR CIRCUIT



Q_1: Any N-P-N Silicon Transistor that can handle a 2A Load Current such as 2N3772 or Equivalent

NOTE
1. $I_L = 1.6 + R_1$, $200\mu A \leq I_L \leq 2A$

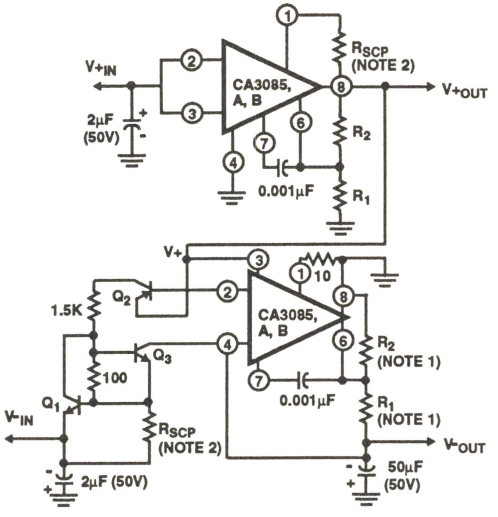
FIGURE 18. TYPICAL CURRENT REGULATOR CIRCUIT



All Resistance Values are in Ohms
D_1: 1N4001 or Equivalent
Q_1: 2N5322 or Equivalent

NOTE:
1. $R_1 = 0.7\ I_L$ (Max)

FIGURE 19. TYPICAL SWITCHING REGULATOR CIRCUIT



All Resistance Values are in Ohms
Q_1: 2N2102 or Equivalent
Q_2: Any P-N-P Silicon Transistor (2N5322 or Equivalent)
Q_3: Any N-P-N Silicon Transistor that can handle the desired Load Current (2N3772 or Equivalent)

NOTE:
1. $V_{OUT} = (R_1 + R_2) + R_1$
2. R_{SCP}: Short Circuit Protection Resistance

FIGURE 20. COMBINATION POSITIVE AND NEGATIVE VOLTAGE REGULATOR CIRCUIT

HARRIS SEMICONDUCTOR

CA3277

Dual 5V Regulator with Serial Data Buffer Interface for Microcontroller Applications

April 1994

Features

- Dual 5V Regulator
  - $V_{OUT}1$ at 5V 100mA - Standby
  - $V_{OUT}2$ at 5V 100mA - Enabled
  - Regulation Range 6V to 18V
  - Bandgap Voltage References
- Low Quiescent Idle Current, 500µA Typ.
- Over-Voltage Shutdown Protection, 20.5V Typ.
- Reverse Battery Protection, -26V Max.
- Thermal Shutdown Protection
- Short Circuit Current Limiting
- Low Input P.S. Flag and Delayed Reset Control
- Low Voltage Shutdown Control, Ouput1
- Ignition Comparator Logic Level Control
- Data Comparator and 100X Current Mult. Used as Input/Output Buffers for Remote Serial Data Communication

Applications

- Automotive 5V Regulators and Data Buffers
- Industrial Controller Remote System
- Microcontroller and Memory Power Supply
- Radio, TV, CATV, Consumer Applications

Description

The CA3277 is a Dual 5V Voltage Regulator IC intended for microprocessor and logic controller applications. It is supplied with features that are commonly specified for sequentially controlled shutdown and startup requirements of microcontrollers. Over-voltage shutdown, short circuit current limiting and thermal shutdown features are provided for protection in the harsh environmental applications of industrial and automotive systems. The CA3277 functions are complementary to the needs of microcontroller and memory circuits, providing for sustained memory with a 5V standby output.

The Ignition Comparator senses the voltage level at the IGN IN input and provides a 5V logic switched output (supply sourced from OUT1). The Ignition Output, IGN OUT can be used to signal a system microcontroller which can respond with a logic switched output to the CA3277 ENABLE input control for OUT2. The OUT1 +5V Standby Supply of the regulator is normally used as a power supply for microcontroller/memory circuits to preserve stored data when in the standby mode.To allow for maximum heat transfer from the chip, the four center leads are directly connected to the die mounting pad.

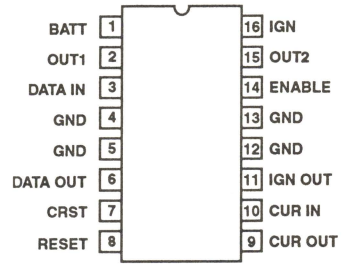
Refer to AN9302 for further information on CA3277 circuit Applications.

Ordering Information

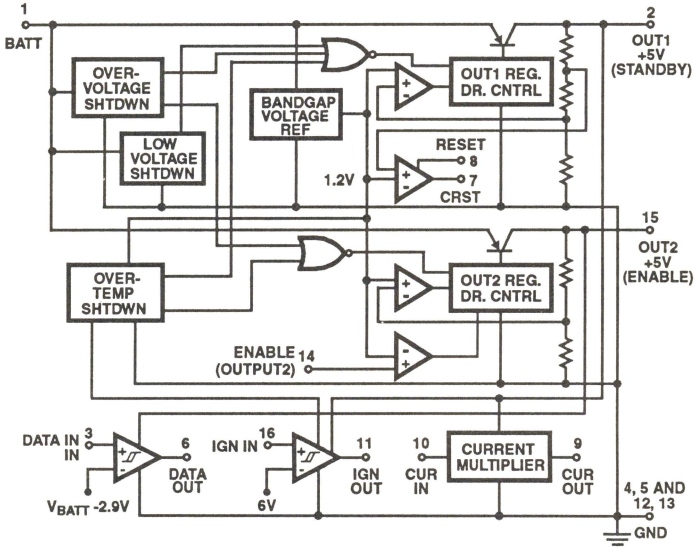
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3277E	-40°C to +85°C	16 Lead Plastic DIP

Pinout

CA3277 (PDIP)
TOP VIEW



Functional Block Diagram



7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
Copyright © Harris Corporation 1994

File Number 2792.4

Absolute Maximum Ratings

Max. BATT, IGN IN Input Voltage (Note1) ..... ±26V
Max. Operating Voltage; BATT, IGN IN ..... $V_{BATT(SD)}$ (~20.5V)
Max. Positive Voltages: (For Negative Voltages, Note 2)
ENABLE Input ..... V_{BATT}
DATA IN Input ..... V_{BATT}
CUR OUT, Output ..... V_{BATT}
RESET, Output ..... V_{BATT}
Max. Operating Load Current, OUT1 ..... 100mA
Max. Operating Load Current, OUT2 ..... 100mA
Max. Current Mult. Load Currents:
Min. Load Resistance, CUR OUT .. 225Ω to BATT (75mA max)
Min. Load Resistance, CUR IN ..... 1KΩ to GND (-5mA max)
Max. Load Current OUT1, OUT2 (Short Duration) ... Self-Limiting
Max. Plus/Minus Load Currents: (Note 3)
IGN OUT Output ..... Self-Limiting
DATA OUT Output ..... Self-Limiting
RESET Output ..... Self-Limiting

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JL}
Plastic DIP Package	60°C/W	12°C/W
(Temp. meas. on center lead next to case)		

Power Dissipation, P_D (Note 4):
Up to +60°C (Free Air) 1.5W
Above +60°C: ..... Derate Linearly at 16.6mW/°C
Up to +85°C w/heat sink (PC Board): ..... 1.6 W
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +150°C
Max. Junction Temperature ..... +150°C
Lead Temperature (During Solder) ..... +265°C
1/16 ± 1/32" from case, 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +85°C, V_{BATT} = 13.5V, ENABLE ON (V_{EN} = 3.5V), IGN IN connected to BATT, OUT1 and OUT2 bypassed with 20µF to GND, DATA IN connected through 250Ω to BATT, LOADS: OUT1 = 50mA, OUT2 = 80mA; Unless Otherwise Specified (Refer to Figure 4 Test Circuit)

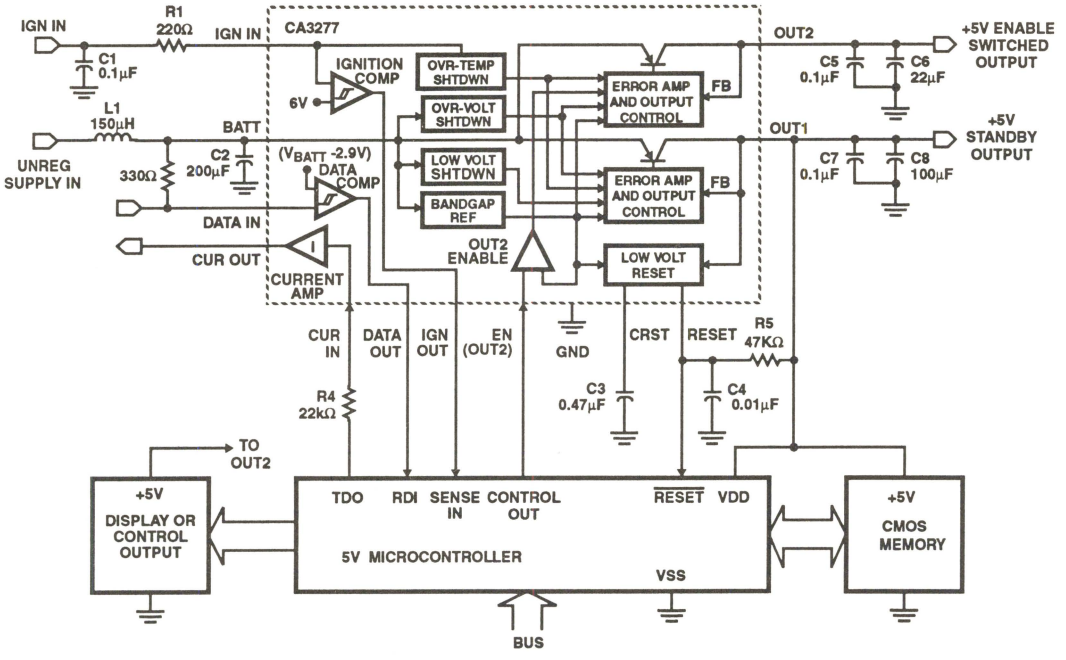
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REGULATOR OUTPUT1						
Output Voltage	V_{OUT1}	V_{BATT} = 9V to 16V	4.75	5	5.25	V
Dropout Voltage (Note 5)	V_{DO1}	V_{BATT} = 4.75V	4.15	4.6	-	V
Line Reg		V_{BATT} = 6.2V to 16V	-	9	40	mV
Load Reg		I_{LOAD} = 0.5mA to 50mA	-	30	60	mV
Current Limiting			-	170	250	mA
Low Voltage Shutdown		Ramp V_{BATT} Down Until OUT1 drops (PNP Driver Cutoff)	-	3.5	-	V
REGULATOR OUTPUT2						
Output Voltage	V_{OUT2}	V_{BATT} = 9V to 16V	4.75	5	5.25	V
Dropout Voltage (Note 5)	V_{DO2}	V_{BATT} = 5.6V	4.6	5	-	V
Line Reg		V_{BATT} = 6.2V to 16V	-	7.5	40	mV
Load Reg		I_{LOAD} = 0.5mA to 80mA	-	35	60	mV
Current Limiting			-	190	250	mA
ENABLE Input Current	I_{EN}	V_{EN} = 5V	-	50	150	µA
ENABLE Input Sw. Thd.	$V_{EN(THD)}$	Ramp ENABLE Input Up Until OUT2 is Switched ON	-	1.2	-	V
CURRENT MULTIPLIER						
Current Mult. Gain, (I_{COUT}/I_{CIN})		I_{CIN} = -200µA	80	100	-	Gain Ratio
Current Mult. Output Sat.	$V_{COUT(SAT)}$	I_{CIN} = -200µA, CUR OUT Load = 1KΩ to V_{BATT}	-	0.3	1	V
Current Mult., Max. Drive Cur.	$I_{COUT(MAX)}$	I_{CIN} = -700µA	35	50	-	mA
RESET						
Reset, (RST) Threshold		Ramp V_{BATT} Down, Measure V_{BATT} when RESET (V_{RST}) goes low	3.8	4.2	4.5	V
Reset Delay Time (Note 6)	t_{RST}	CRST Cap. = 0.47µF, V_{BATT} = 6.8V RESET Load = 5KΩ to OUT1	50	150	250	ms
RESET Out High	$V_{OH(RST)}$	47KΩ to OUT1	4	-	-	V
RESET Low	$V_{OL(RST)}$	V_{BATT} = 3.75V, RST 47KΩ to OUT1	-	-	0.2	V
RESET Output Sink Current	I_{OL}	CRST to GND, V_{BATT} = 6.8V	-	8	-	mA

Electrical Specifications T_A = -40°C to +85°C, V_{BATT} = 13.5V, ENABLE ON (V_{EN} = 3.5V), IGN IN connected to BATT, OUT1 and OUT2 bypassed with 20µF to GND, DATA IN connected through 250Ω to BATT, LOADS: OUT1 = 50mA, OUT2 = 80mA; Unless Otherwise Specified (Refer to Figure 4 Test Circuit) **(Continued)**

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DATA COMPARATOR						
Data Comp Thd			V_{BATT} - 3.6	V_{BATT} -2.9	V_{BATT} -2.2	V
Data Comp Hysteresis			-	200	-	mV
DATA OUT Low	V_{OL}	V_{BATT} = 16V, $V_{DATA\ IN}$ = (V_{BATT} -5V)	-	-	0.15	V
DATA OUT High	V_{OH}	V_{BATT} = 16V, $V_{DATA\ IN}$ = 16V	V_{OUT1} -0.15	-	5.25	V
DATA OUT Low Sink Current	I_{OL}	$V_{DATA\ IN}$ Low	-	1	-	mA
DATA OUT High Source Current	I_{OH}	$V_{DATA\ IN}$ High	-	-50	-	µA
IGNITION COMPARATOR						
Ign Comp Thd			5.5	6	6.5	V
Ign Comp Hysteresis			-	200	-	mV
IGN OUT Low	V_{OL}		-	-	0.15	V
IGN OUT High	V_{OH}		4.6		5.25	V
IGN OUT Low Sink Current	I_{OL}	$V_{IGN\ IN}$ Low	-	1	-	mA
IGN OUT High Source Current	I_{OH}	$V_{IGN\ IN}$ High	-	-70	-	µA
OTHER PARAMETERS						
Idle Current	I_Q	V_{BATT} = 12.6V, No Loads, V_{EN} = $V_{IGN\ IN}$ = 0V	-	500	800	µA
Over-Voltage Shutdown	$V_{BATT(OVSD)}$	Ramp V_{BATT} Up Until OUT1 and OUT2 Shut-down	19	20.5	23	V
Thermal Shutdown	T_J		-	150	-	°C
Ripple Rejection		1V_{PP} at 3kHz on BATT INPUT, Measure AC Ripple on OUT1, OUT2	45	55	-	dB

NOTES:

1. For negative voltages on the BATT and IGN IN inputs, current drain is primarily reverse junction leakage, except when DATA IN, CUR OUT, ENABLE and RESET are directly connected to BATT. (Note 2)
2. For negative voltage DATA IN, CUR OUT, ENABLE and RESET interface to NPN or equivalent on-chip structures; providing a forward junction for current conduction into the IC. Negative current must be limited by the impedance of the external connection. This is also the case where these terminals are interconnected to BATT, Normal application does not require the BATT connection, except for DATA IN where a series diode for reverse current blocking may be used. (see Description text information)
3. Refer to the Electrical Characteristic TABLE for all Self-Limiting values.
4. Dissipation, approximately equals: $P_D \approx [(V_{IN}I_{IN}) + (V_{CUR\ OUT}I_{CUR\ OUT}) - 5(I_{OUT1}+I_{OUT2})]$, where $I_{IN}V_{IN}$ is IGN IN and BATT input dissipation and V_{OUT1}~V_{OUT2}~5V. This assumes neglibible dissipation for the Ignition Comp., Reset and Data Comp. Outputs.
5. Dropout Voltage is V_{DO1} = (V_{BATT} - V_{OUT1}) for REG. OUT1 and V_{DO2} = (V_{BATT} - V_{OUT2}) for REG. OUT2
6. Reset Delay Time, t_{RST} is the time period that the RESET (Pin 8) is low following the discharge of the CRST capacitor to ground. For test evaluation, the CRST pin may be discharged repetitively with a transistor switch. The RESET pin switches from low to high when the CRST pin is charged to approximately 3V. Normal ATE testing measures the source charging current. which is typically 10µA. For any other value of Capacitor the charge time, t for reset is determined as follows: t ~308C, where C is in µF and t is in milliseconds. (i.e. C = 0.47µF, t = 141ms)



NOTE: DATA IN and CUR OUT are remote/host Serial Data Communication Buffers. Typical Remote Source Impedance for DATA IN is 1kΩ. Typical Remote Load for CUR OUT is 250Ω.

FIGURE 1. TYPICAL APPLICATION CIRCUIT OF THE CA3277 DUAL 5V REGULATOR WITH MICROCONTROLLER AND SERIAL DATA BUFFER INTERFACE TO A REMOTE HOST

Applications

Other functions of the CA3277 include a Data Comparator and Current Multiplier for use as interface buffers to transfer serial data at higher level logic to and from a remote host microcontroller. The OUT1 5V Standby Supply provides power to the local microcontroller which interfaces to the CA3277 interface buffers at a 5V logic level. As shown in Figure 1, the DATA IN input of the Data Comparator receives serial data referenced to the BATT voltage level. The output of the Data Comparator is 5V CMOS compatible logic and is connected to the RDI (remote data input) terminal of the microcontroller. The TDO (data out) output of the microcontroller is connected to the Current Multiplier input of the CA3277.

Current Multiplier - The Current Multiplier, with internal circuitry shown in Figure 2, receives data from the microcontroller in the form of an open drain or gate switched output driving a 22KΩ resistor load in series to the Current Input at pin 10 (CUR IN). The input stage of the Current Multiplier is a current mirror amplifier which is internally connected to the 5V regulated OUT1 voltage source. The output stage of the Current Multiplier is a current mirror amplifier referenced to GND and has an open collector Current Output at pin 9 (CUR OUT), with a minimum drive capability of 35mA. The Current Multiplier output load is normally connected via resistive loading to the BATT voltage supply level. As such, the microcontroller transmits data out (TDO output) to the input of the CA3277 Current Multiplier which amplifies and translates the signal back to the voltage reference level of the BATT power supply input. When driving a similar remote CA3277, the voltage drop from the BATT input line switches the Data Comparator which provides serial data to the RDI input of the remote microcontroller. The nominal current gain of the Current Multiplier is 100X.

The application use of the Current Multiplier is not limited to digital serial data transfer. The Current Multiplier is an independent function and is open to use for other purposes, including linear signal amplification, sensor output amplification and current controlled threshold switching. The current output terminal, CUR OUT may be externally load-connected to OUT1, OUT2, BATT or any other power supply level up to the maximum ratings given for the BATT input terminal. It is important to note that some applied uses of the Current Multiplier may contribute significant on-chip power dissipation. A nominal current mirror input drive of 200µA will provide sufficient drive to switch a 250Ω resistor load at the input of the data comparator. As such, the quiescent OFF condition of the Data comparator should be in the High state.

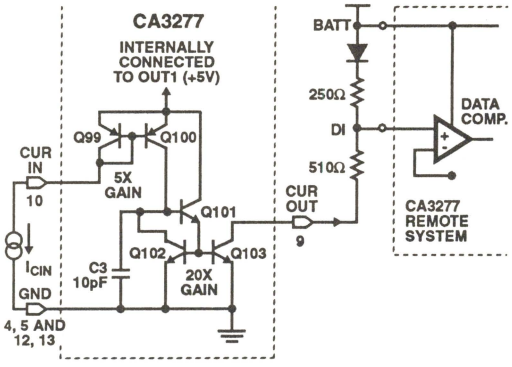


FIGURE 2. CURRENT MULTIPLIER DRIVING A REMOTE CA3277 DATA COMPARATOR

Data Comparator - The Data Comparator provides a means of translating serial data from a high to low voltage. The DATA IN terminal of the Data Comparator is biased to receive signal input that is source referenced to the BATT supply voltage level. In normal use the signal input would be supplied from a remote Current Multiplier having a resistor load tied to the BATT voltage supply. The DATA OUT output from the Data Comparator is CMOS compatible 5V non-inverting logic data referenced to GND. The switching threshold at the DATA IN input is bias stabilized by the bandgap voltage and is typically at (V_{BATT} - 2.9V). The Data Comparator is in a high state when DATA IN input is at the BATT voltage level and is in a low state when DATA IN is at (V_{BATT} - 5V). The output stage of the Data Comparator is internally supply biased from the Switched 5V Regulator output to provide a high state of 5V and a low state of 0V (GND). The DATA OUT terminal can typically sink 1.2mA in a low state or source 50µA in a high state.

In system applications the Data Comparator is used to translate remote data at high voltage down to 5V logic levels. The Current Multiplier is used to reverse the process by translating 5V logic data back to the BATT voltage level when sending data back to the remote system. The Data Comparator and Current Multiplier are level matched for remote communication between microcontroller systems using the common BATT power supply voltage of the CA3277. The current driven serial data from the Current Multiplier is sent to a remote system by translating the signal up to the BATT voltage level, or an external power supply level that is compatible with the remote device. The Data Comparator of the remote system receives the data, interfaces to its microcontroller and responds with signal drive from its Current Multiplier to translate the signal back to the host. For best noise immunity the transmission in each direction should be over a twisted pair or shielded line. As such, two microcontrollers, each with the interface protection of a CA3277, can provide intelligent master/slave system communications under adverse environmental conditions.

Ignition Comparator - While the Ignition Comparator is provided as an essential part of the start-up control in automotive systems, this circuit function may be used as an independent switching comparator. **It is important to note that the thermal shutdown feature on the chip is disabled when the IGN IN input is low.** Disabling of the on-chip thermal protection is done to satisfy the requirement of low idle current when the system is in a standby condition. The non-inverting IGN IN input has a switching threshold of typically 6V with 200mV of hysteresis and is switched with logic levels reference to GND as the low state and BATT as the high state. The IGN OUT output is 5V CMOS compatible logic, equivalent to the Data Comparator output stage, but is internally supply biased from the Standby 5V Regulator. As such, the high state is level referenced to OUT1. The IGN OUT output terminal can typically sink 1.2mA in a low state or source 70µA in a high state.

Enable - A CMOS or TTL high at the ENABLE input switches the regulated 5V/Switched Output ON at OUT2. The ENABLE input has an internal pull-down of typically 50µA to ensure that OUT2 is OFF when the ENABLE input is not connected. The input threshold level for switching is the bandgap voltage reference of 1.2V. When the ENABLE input is low, all drive current to the output pass transistor is cutoff and OUT2 voltage drops to ground level. The ENABLE input is normally switched from the interfacing microcontroller but may be activated from a remote source.

Reset - The purpose of the Low Voltage Reset function is to flag a low voltage condition at OUT1. When the RESET output, pin 8 switches low, the voltage level at OUT1 has dropped below the regulation level. The CRST and RESET are high when OUT1 is at 5V. When OUT1 drops to less than 4.2V (typical), the CRST Capacitor at pin 7 is internally discharged, causing the RESET pin to change from a high to a low state, outputting a negative going pulse. The RESET output is an NPN open collector driver requiring an external load resistor, normally connected to OUT1. The RESET output flag may be sent to a microcontroller to initiate a power-down sequence. For any condition that causes OUT1 to drop below the reset threshold, such as undesired transients, the RESET output is switched low for a delay period, t_{RST} determined by the value of the external capacitor, C_{RST} at CRST terminal. For a value of 0.47µF the delay period is typically 141ms. This correlates to approximately 10µA of charging current sourced from the CRST terminal to charge C_{RST}.

Regulation - The regulated output stages of the CA3277 have similar circuits, each having an error amplifier to compare the output voltage to the bandgap reference voltage. The circuit of the 5V/Switched regulator is shown in Figure 3. By feedback, the output voltage is differentially compared to the bandgap reference voltage. The error signal is then amplified to drive a PNP pass transistor and maintain a stable 5V output with both line and load regulation over the full operating temperature range. Except for the ENABLE control of OUT2, the OUT1 drive circuit is similar to the OUT2 circuit.

Protection - Both OUT1 and OUT2 PNP output pass transistors are protected with Over-Voltage Shutdown and Over-Temperature Shutdown. Current Limiting for each output is independent and is accomplished by limited drive current from the pre-drivers (Q135 for OUT2) to the PNP output pass transistor (Q136). Over-Voltage is sensed as a threshold voltage level at the BATT input. Both output stages are shutdown when the V_{BATT} voltage level is typically greater than 20.5V. When the Ignition voltage is high, the Over-Temperature level is sensed as V_{BE} changes and compared to the bandgap reference voltage. When the chip temperature exceeds 150°C, both output stages are shutdown. When Over-Voltage or Over-Temperature thresholds are exceeded, the sensed states are ORd to switch OFF drive to the output stages. The ENABLE control for OUT2 is added to the OR control of the OUT2 drive circuit. The Low Voltage Shutdown control is added to the OR control of the OUT1 drive circuit. Low Voltage Shutdown occurs at approximately 3.5V as the BATT supply input is ramped down, forcing cutoff of the PNP output pass transistor. The external capacitor on OUT1 holds charge, with a long RC time constant delay to sustain shutdown control in the microcontroller. The internal shunt resistance at the OUT1 terminal is typically 148KΩ.

Under conditions of reverse battery or negative supply voltages on the BATT input, current in the IC is primarily reverse junction leakage. The design of the CA3277 is configured to prevent high current if the power supply is reversed. Exceptions to this are preventable. One example is current through the DATA IN input line terminating resistor, normally connected directly to the BATT supply line. This provides a path for current conduction into the IC through an internal diode junction. The current is limited by the external resistor and may be as high as 100mA at -26V. Where negative supply voltages are potentially a problem, the resistive load from DATA IN to BATT can be in series with a reverse voltage blocking diode, such as a 1N914. This input diode-resistor circuit is shown in Figure 2 as the remote interface and load to the Current Multiplier output.

Dissipation - The CA3277 device dissipation is the combined watts of input voltage times current less the external watts of power supplied by the chip. For normal use, the major contribution to on-chip dissipation is primarily the BATT input dissipation. The Current Multiplier output has a potential to add significant dissipation. The open collector driver of the Current Multiplier Output, pin 9 may or may not be in saturation when sinking current. Because it is a current mirror output with a constant current drive, the voltage may be increased on pin 9, with a significant increase in the resulting dissipation. The chip dissipation is approximately equal to:

$$P_D \approx [(V_{IN}I_{IN}) + (V_{COUT}I_{COUT}) - 5(I_{OUT1}+I_{OUT2})]$$

where $I_{IN}V_{IN}$ is IGN IN and BATT input dissipation, assuming $V_{BATT} = V_{IGN\ IN}$, and $V_{OUT1} \sim V_{OUT2} \sim 5V$. This assumes negligible dissipation for the Ignition Comparator, Data Comparator and Reset outputs.

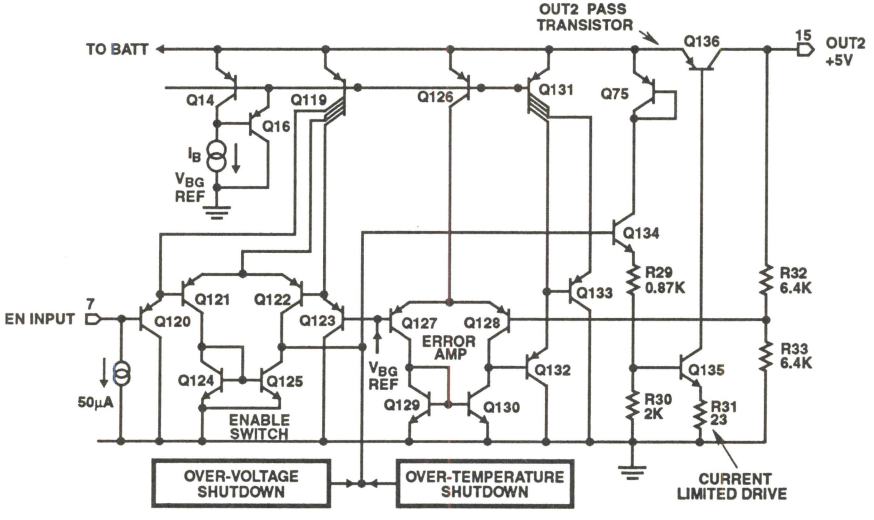


FIGURE 3. OUTPUT2 DRIVER AND ERROR AMPLIFIER WITH THE ENABLE CONTROL

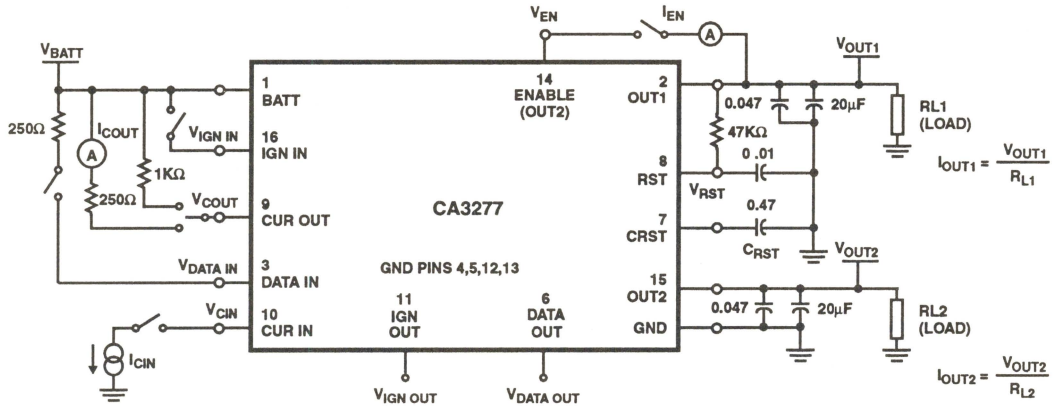


FIGURE 4. CHARACTERISTIC EVALUATION AND TEST CIRCUIT

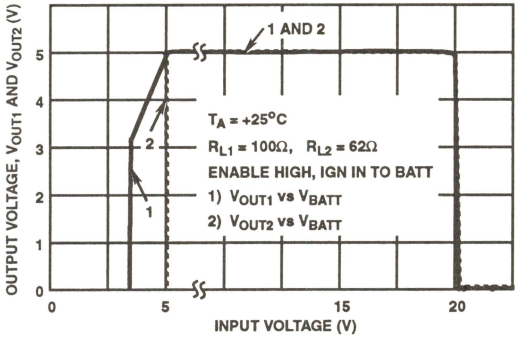


FIGURE 4A. TYPICAL CHARACTERISTIC CURVES FOR OUT1 AND OUT2 OUTPUT VOLTAGE vs BATT VOLTAGE INPUT

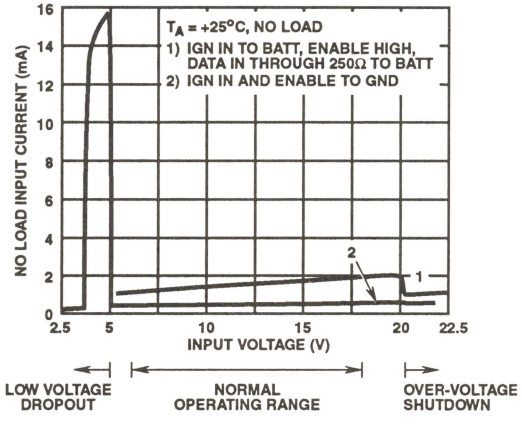


FIGURE 4B. TYPICAL CHARACTERISTICS CURVES FOR NO-LOAD BATT INPUT CURRENT vs BATT INPUT VOLTAGE FOR OFF STATE IDLE CURRENTS

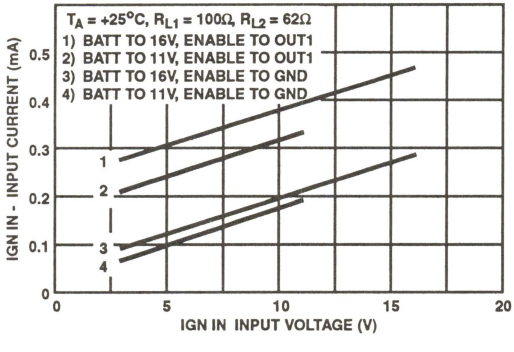


FIGURE 4C. TYPICAL IGN IN CURRENT vs IGN IN INPUT VOLTAGE

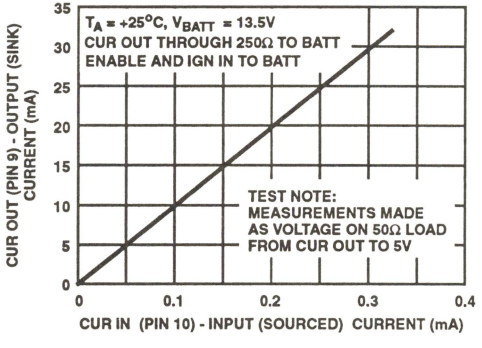


FIGURE 4D. TYPICAL CURRENT MULTIPLIER CURRENT GAIN CHARACTERISTIC

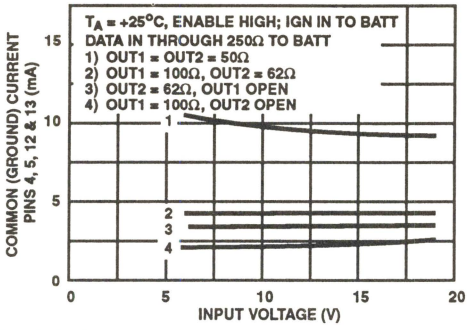


FIGURE 4E. TYPICAL CHARACTERISTIC CURVES FOR COMMON (GROUND) CURRENT vs BATT VOLTAGE INPUT WITH OUTPUT LOAD

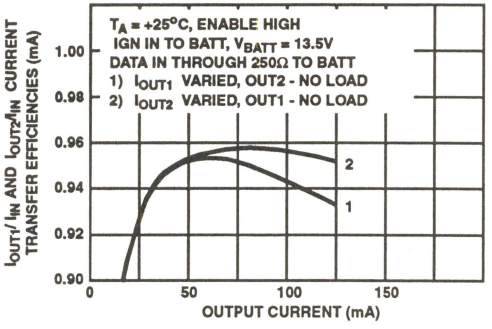


FIGURE 4F. TYPICAL CHARACTERISTIC CURVES FOR CURRENT TRANSFER EFFICIENCY OF I_{OUT1}/I_{IN} AND I_{OUT2}/I_{IN} WHERE I_{IN} INCLUDES ($I_{IGN\ IN}$ + $I_{DATA\ IN}$) BIAS CURRENTS

HARRIS SEMICONDUCTOR

HIP5060

Power Control IC
Single Chip Power Supply

April 1994

Features

- Single Chip Current Mode Control IC
- 60V, 10A On-Chip DMOS Transistor
- Thermal Protection
- Over-Voltage Protection
- Over-Current Protection
- 1MHz Operation or External Clock
- Synchronization Output
- On-Chip Reference Voltage - 5.1V
- Output Rise and Fall Times ~ 3ns
- Designed for 27V to 45V Operation

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters

Description

The HIP5060 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC. Both the standard "Boost" and the "SEPIC" (Single-Ended Primary Inductance Converter) power supply topologies are easily implemented with this single control IC.

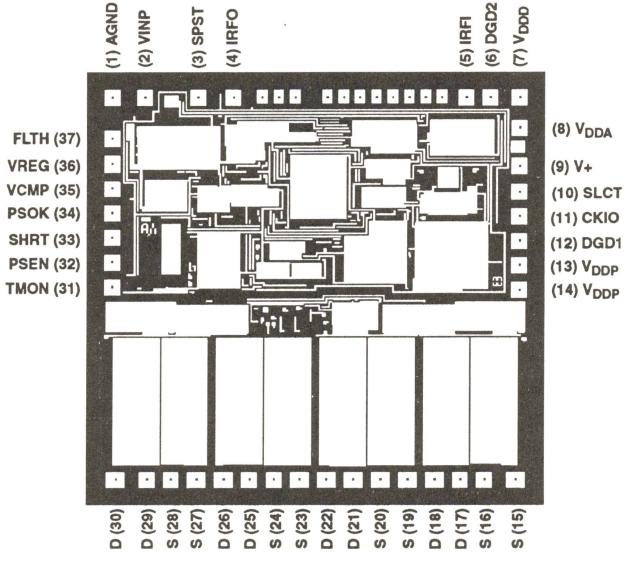
Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Moreover, over-temperature and over-voltage detection circuitry is incorporated within the IC to monitor the chip temperature and the actual power supply output voltage. These circuits can disable the drive to the power transistor to protect both the transistor and, most importantly, the load from over-voltage.

As a result of the power DMOS transistor's current and voltage capability (10A and 60V), power supplies with output power capability up to 100 watts are possible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5060DY	0°C to +85°C	37 Pad Chip
HIP5060DW	0°C to +85°C	Wafer

Chip



NOTE: Unused pads are for trim and test.
153 mils x 165 mils (3.88mm x 4.19mm)

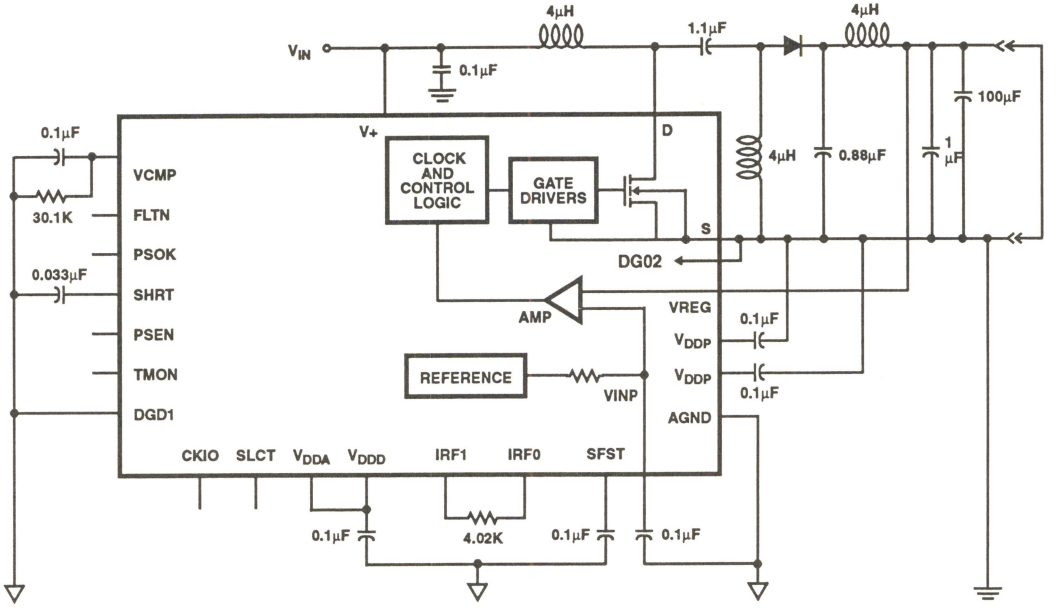
7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3207.1

Simplified Block Diagram



TYPICAL SEPIC CONFIGURATION

Absolute Maximum Ratings

DC Supply Voltage, V+ ..... -0.3V to 45V
DMOS Drain Voltage ..... -0.3V to 60V
DMOS Drain Current 20A
DC Logic Supply ..... -0.3V to 16V
Output Voltage, Logic Outputs ..... -0.3V to 16V
Input Voltage, Analog and Logic ..... -0.3V to 16V
Operating Junction Temperature Range ..... 0°C to +110°C
Storage Temperature Range ..... -55°C to +150°C

Thermal Information

Thermal Resistance (θ_{JC})
(Solder Mounted to 0.050" Thick Copper Heat Sink) ..... 3°C/W Max
Maximum Junction Temperature ..... +110°C
(Controlled By Thermal Shutdown Circuit)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = 36V, T_J = 0°C to +110°C; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I+	Supply Current	PSEN = 12V	-	19.5	32	mA
V_{DDA}	Internal Regulator Output Voltage	V+ = 15V to 45V, I_{OUT} = 10mA	11.0	-	13.2	V
VINP	Reference Voltage	I_{VINP} = 0mA	5.01	5.1	5.19	V
R_{VINP}	VINP Resistance	VINP = 0	-	900	-	Ω
ERROR AMPLIFIERS						
$\lvert V_{IO}\rvert$	Input Offset Voltage (VREG - VINP)	I_{VCMP} = 0mA	-	-	10	mV
R_{IN} VREG	Input Resistance to GND	VREG = 5.1V	-	56	-	kΩ
g_m (VREG)	VREG Transconductance I_{VCMP}/(VREG - VINP)	VCMP = 1V to 8V, SFST = 11V	15	30	50	mS
g_m (SFST)	SFST Transconductance I_{VCMP}/(VREG - SFST)	V_{SFST} < 4.9V	0.8	-	6	mS
I_{VCMP}	Maximum Source Current	VREG = 4.95V, VCMP = 8V	-2.5	-	-0.75	mA
I_{VCMP}	Maximum Sink Current	VREG = 5.25V, VCMP = 0.4V	0.75	-	2.5	mA
OVTH	Over-Voltage Threshold	Voltage at VREG for FLTN to be latched	6.2	-	6.7	V
CLOCK						
fq	Internal Clock Frequency	SLCT = 0V, V_{DDD} = 12V	0.9	1.0	1.1	MHz
V_{TH} CKIN	External Clock Input Threshold Voltages	SLCT = 12V	33	-	66	$\%V_{DDD}$
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 5A, T_J = +25°C	-	-	0.13	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	µA
CURRENT CONTROLLED PWM						
$\lvert V_{IO}\rvert$ VCMP	Buffer Offset Voltage (VCMP - V_{IRFO})	IRFO = 0mA to -5mA, VCMP = 0.2V to 7.6V	-	-	125	mV
V_{TH} IRFO	Voltage at IRFO that disables PWM. This is due to low load current		100	-	270	mV

Electrical Specifications V+ = 36V, T_J = 0°C to +110°C; Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT CONTROLLED PWM (Continued)						
I_{TH} IRFO	Voltage at IRFO to enable SHRT output current. This is due to Regulator Over Current Condition		7.4	-	8.0	V
I_{SHRT}	SHRT Output Current, During Over-Current	V_{IRFO} = 8.1V	-37	-	-17	µA
V_{TH} SHRT	Threshold voltage on SHRT to set FLTN latch		4	6	8	V
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	3.8	-	4.9	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{IRFI} = 2mA	150	-	360	Ω
t_{RS} (Note 1)	Current Comparator Response Time	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/µs	-	30	-	ns
MCPW (Note 1)	Minimum Controllable Pulse Width		25	50	100	ns
MCPI (Note 1)	Minimum Controllable DMOS Peak Current		200	400	800	mA
START-UP						
V+	Rising V+ Power-On Reset Voltage		22	-	27	V
V+	Falling V+ Power-Off Set Voltage		-	15	-	V
V+	V+ Power-On Hysteresis		9	-	12	V
V_{TH} PSEN	Voltage at PSEN to Enable Supply		0.8	-	2.0	V
r_{PSEN}	Internal Pull-Up Resistance, to 5.1V		-	20	-	KΩ
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 0V to 10V	-1.0	-0.7	-0.4	µA
I_{PSOK}	PSOK High-State Leakage Current	SFST = 0V, PSOK = 12V	-1	-	1	µA
V_{PSOK}	PSOK Low-State Voltage	SFST = 11V, I_{PSOK} = 1mA	-	-	0.4	V
V_{TH} SFST	PSOK Threshold, Rising V_{SFST}		9.4	-	11	V
THERMAL MONITOR						
TEMP (Note 1)	Substrate Temperature for Thermal Monitor to Trip	TMON pin open	105	-	135	°C

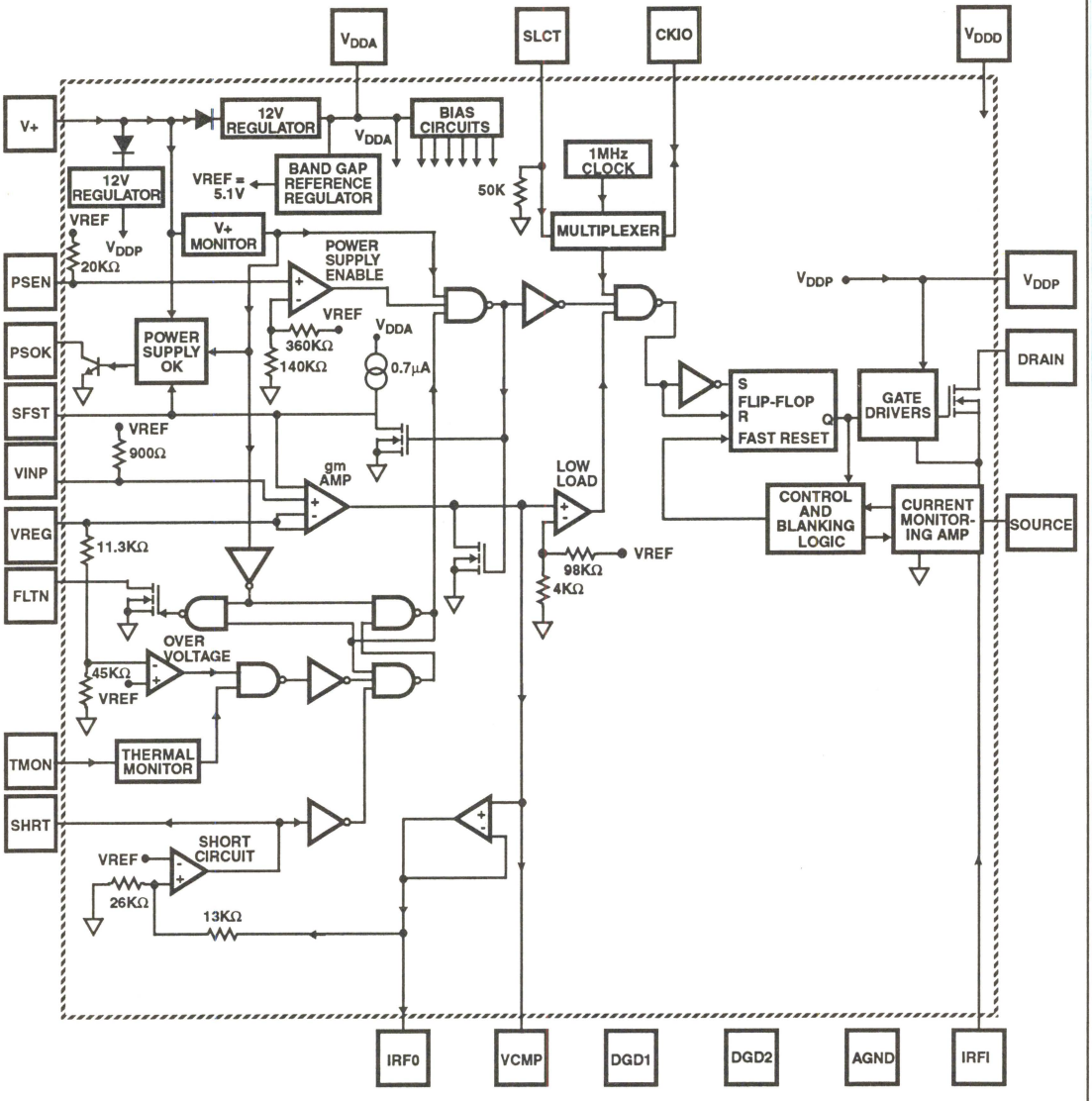
NOTE:

1. Determined by design, not a measured parameter.

Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1	AGND	Analog ground.
2	VINP	Internal 5.1V reference.
3	SFST	Controls the rate of rise of the output voltage. Time is determined by an internal 0.7µA current source and an external capacitor.
4	IRFO	A resistor placed between this pad and IRFI converts the VCMP signal to a current for the current sense comparator. The maximum current is set by the value of the resistor, according to the equation: $I_{PEAK} = 32/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 17.8A. This assumes VCMP is 7.3V. Maximum output current should be kept below 20A.
5	IRFI	See IRFO
6	DGD2	Ground of the DMOS gate driver. This pad is used for bypassing.
7	V_{DDD}	Voltage input for the chip's digital circuits. This pad also allows decoupling of this supply.
8	V_{DDA}	This is the analog supply and internal 12V regulator output.
9	V+	This is the main supply voltage input pad to the regulator IC. Because of the high peak currents this pad must be well bypassed with at least a 0.7µF capacitor and may be composed of seven, single 0.1µF chip capacitors.
10	SLCT	This pad provides for the option of using either internal 1MHz operation of for an external clock. Floating or grounding this pad will place the internal clock at the CKIO pad. Returning this terminal to V_{DDD} or 12V will allow application of an external clock to the IC via the CKIO pad. There is an internal 50K pull down
11	CKIO	Clock output when SLCT is floated or grounded. External clock input when SLCT is returned to 12V.
12	DGD1	This pad is the return for the digital supply.
13 & 14	V_{DDP}	These pads are used to decouple the high current pulses to the output driver transistors. The capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
15, 16, 19, 20, 23, 24, 27, 28	S	Source pads of the DMOS power transistor.
17, 18, 21, 22, 25, 26, 29, 30	D	Drain pads of the DMOS power transistor.
31	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to 12V the function is disabled. Returning this pad to ground will put the IC into the thermal shutdown state. Normally, this pad is left floating. Thermal shutdown occurs at a nominal junction temperature of +125°C.
32	PSEN	This terminal is provided to activate the converter. This terminal may be left open or returned to 5V for normal operation. When the input is low, the DMOS driver is disabled.
33	SHRT	25µA is internally applied to this node when there is an over-current condition.
34	PSOK	This pad provides a delayed positive indication when the supply is enabled.
35	VCMP	Output of the transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
36	VREG	Input to the transconductance error amplifier is available on this pad. The other input is internally connected to the 5.1V reference, VINP, Pad 2.
37	FLTN	This is an open drain output that remains low when V+ is too low for proper operation. This node and PSEN are useful in multiple converter configurations. This pad will be latched low when over-temperature, over-voltage or over-current is experienced.

Functional Block Diagram



HARRIS SEMICONDUCTOR

HIP5061

7A, High Efficiency Current Mode Controlled PWM Regulator

April 1994

Features

- Single Chip Current Mode Control IC
- 60V, On-Chip DMOS Power Transistor
- Thermal Protection
- Over-Current Protection
- 250kHz Operation
- Output Rise and Fall Times - 10ns
- On-Chip Reference Voltage - 5.1V
- Slope Compensation
- V_{DD} Clamp Allows 10.8V to 60V Supply
- Supply Current Does Not Increase When Power Device is On

Applications

- Distributed / Board Mounted Power Supplies
- DC - DC Converter Modules
- Voltage Inverters
- Small Uninterruptable Power Supplies
- Cascode Switching for Off Line SMPS

Description

The HIP5061 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC. The standard "Boost", "Buck-Boost", "Cuk", "Forward", "Flyback" and the "SEPIC" (Single-Ended Primary Inductance Converter) power supply topologies may be implemented with this single control IC.

Over-temperature and rapid short-circuit recovery circuitry is incorporated within the IC. These protection circuits disable the drive to the power transistor to protect the transistor and insure rapid restarting of the supply after the short circuit is removed.

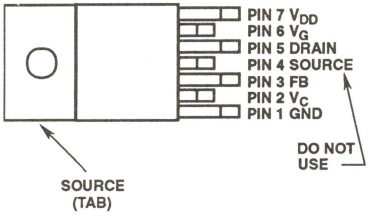
As a result of the power DMOS transistors current (7A at 30% duty cycle, 5A DC) and 60V capability, supplies with output power over 50W are possible.

Ordering Information

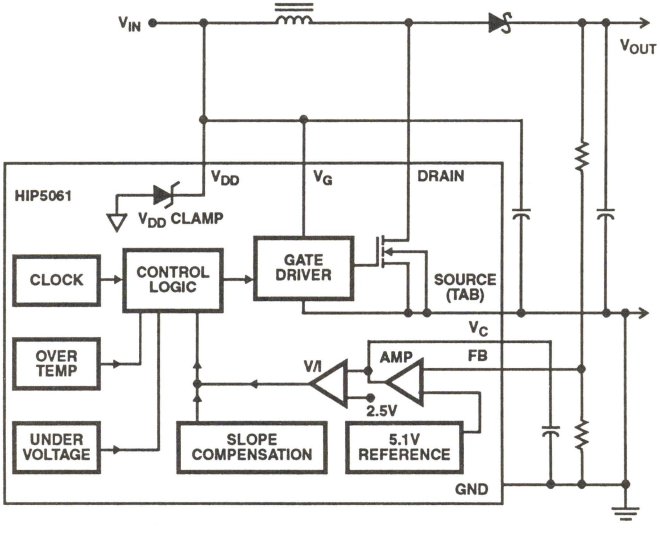
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5061DS	0°C to +85°C	7 Lead Staggered "Gullwing" SIP

Pinout

HIP5061 (SIP)
TOP VIEW



Simplified Functional Diagram



7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3390.2

Absolute Maximum Ratings (Note 1)

DC Supply Voltage, V_{DD} ..... -0.3V to 16V
DC Supply Current, I_{DD} 105mA
DMOS Drain Voltage ..... -0.3V to 60V
Average DMOS Drain Current 5A
DMOS Source Voltage, V_{SOURCE}, TAB ..... -0.1V to 0.1V
DC Supply Voltage, V_G ..... -0.3V to V_{DD} + 0.3V
Compensation Pin Current, I_{VC} ..... -5mA to 35mA
Voltage at All Other Pins ..... -0.3V to V_{DD} + 0.3V
Operating Junction Temperature Range ..... 0°C to +105°C
Storage Temperature Range ..... -55°C to +150°C
ESD Classification ..... Class 2 - 2KV
Single Pulse Avalanche Energy Rating, µs (Note 2) ... EAS 100mJ

Thermal Information

Thermal Resistance θ_{JC}
Plastic SIP Package ..... 2°C/W
Maximum Package Power Dissipation at +85°C
(Depends Upon Mounting, Heat Sink and Application) 10W
Max. Junction Temperature ..... +105°C
(Controlled By Thermal Shutdown Circuit)
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{DD} = V_G$ =12V, V_C = 5V, V_{FB} = 5.1V, SOURCE = GND = DRAIN = 0V, T_J = 0°C to +105°C, Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I_{DD}	Quiescent Supply Current	$V_{DD} = V_G$ = 13.2V, V_C = 0V, V_{FB} = 4V	6	12	18	mA
I_{DD}	Operating Supply Current	$V_{DD} = V_G$ = 13.2V, V_C = 8.5V, V_{FB} = 4V	-	24	31	mA
IV_G	Quiescent Current to Gate Driver	$V_{DD} = V_G$ = 13.2V, V_C = 0V	-	0	10	µA
IV_G	Operating Current to Gate Driver	V_C = 3V	-	1	2	mA
V_{DDC}	Clamp Voltage	I_{DD} = 100mA	13.3	14	15	V
V_{REF}	Reference Voltage	I_{VC} = 0µA, $V_C = V_{FB}$	5.0	5.1	5.2	V
AMPLIFIERS						
$I I_{FB} I$	Input Current	$V_{FB} = V_{REF}$	-	-0.85	0.5	µA
$g_m (V_{FB})$	V_{FB} Transconductance $I_{VC}/(V_{FB} - V_{REF})$	$/I_{VC}/$ = 500µA, Note 3	20	30	43	mS
IV_{CMAX}	Maximum Source Current	V_{FB} = 4.6V	-4	-1.8	-1	mA
IV_{CMAX}	Maximum Sink Current	V_{FB} = 5.6V	1	1.8	4	mA
A_{OL}	Voltage Gain	$/I_{VC}/$ = 500µA, Note 3	44	50	-	dB
V_{CMAX}	Short Circuit Recovery Comparator Rising Threshold Voltage		5.4	6.6	8.9	V
V_{CHYS}	Short Circuit Recovery Comparator Hysteresis Voltage		0.7	1.1	1.8	V
IVC_{OVER}	V_C Over-Voltage Current	$V_{DD} = V_G$ = 10.8V, $V_C = V_{CMAX}$	0	10	25	mA
CLOCK						
fq	Internal Clock Frequency		210	250	290	kHz
DMOS TRANSISTOR						
$r_{DS(ON)}$	Drain-Source On-State Resistance	I_{DRAIN} = 5A, $V_{DD} = V_G$ = 10.8V T_J = +25°C	-	0.15	0.22	Ω
$r_{DS(ON)}$	Drain-Source On-State Resistance	I_{DRAIN} = 5A, $V_{DD} = V_G$ = 10.8V T_J = +105°C	-	-	0.33	Ω
I_{DSS}	Drain-Source Leakage Current	V_{DRAIN} = 60V	-	0.5	10	µA
I_{DSH}	Average Drain Short Circuit Current	V_{DRAIN} = 5V, Note 4	-	-	5	A
C_{DRAIN}	DRAIN Capacitance	Note 4	-	200	-	pF

Electrical Specifications $V_{DD} = V_G = 12V$, $V_C = 5V$, $V_{FB} = 5.1V$, SOURCE = GND = DRAIN = 0V, $T_J = 0°C$ to $+105°C$, Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT CONTROLLED PWM						
$g_m(V_C)$	$\Delta I_{DRAIN, PEAK} / \Delta V_C$	Note 3	1.4	2.2	3.0	A/V
V/I_{REF}	Voltage to Current Converter Reference Voltage	$I_{DRAIN} = 0.25A$, Note 3	2.4	2.8	3.1	V
t_{BT}	Current Comparator Blanking Time	Note 3	40	100	175	ns
t_{ONMIN}	Minimum DMOS "ON" Time	Note 3	60	150	250	ns
t_{OFFMIN}	Minimum DMOS "OFF" Time	Note 3	40	125	200	ns
MinCI	Minimum Controllable DMOS Peak Current	Note 3	-	100	250	mA
MaxCI	Maximum Controllable DMOS Peak Current	Duty Cycle = 6% to 30%, Note 3	7	9.5	12	A
MaxCI	Maximum Controllable DMOS Peak Current	Duty Cycle = 30% to 96%, Note 3	5	8	12	A
CURRENT COMPENSATION RAMP						
$\Delta I/\Delta t$	Compensation Ramp Rate	$\Delta I_{DRAIN, PEAK} / \Delta$Time, Note 3	-1.4	-0.85	-0.45	A/µs
t_{RD}	Compensation Ramp Delay	Note 3	1.3	1.5	1.8	µs
START-UP						
V_{DDMIN}	Rising V_{DD} Threshold Voltage	$V_{FB} = 4V$	9.3	10.3	10.8	V
V_{DDHYS}	Power-On Hysteresis	$V_{FB} = 4V$	0.3	0.45	0.6	V
V_{CEN}	Enable Comparator Threshold Voltage		1.0	1.5	2.0	V
R_{VC}	Power-Up Resistance	$4V < V_{DD} < 10.8V$, $V_C = 0.8V$	50	500	3000	Ω
THERMAL MONITOR						
T_J	Substrate Temperature for Thermal Monitor to Trip	Note 4	105	-	145	°C
T_{JHY}	Temperature Hysteresis	Note 4	-	5	-	°C

NOTES:

1. All Voltages relative to pin 1, GND.
2. $V_D = 10V$, Starting $T_J = +25°C$, $L = 4mH$, $I_{PEAK} = 7A$.
3. Test is performed at wafer level only.
4. Determined by design, not a measured parameter.

TABLE 1. CONDITIONS FOR UNCLAMPED ENERGY CIRCUIT

V_D (V)	I_L (PEAK AMPS)	L (mH)	EAS (mJ)
10	5	40	550
10	7	4TZ	120
6	10	0.33	18
6	12.5	0.14	12

NOTE: Device Selected to Obtain Peak Current without Clocking

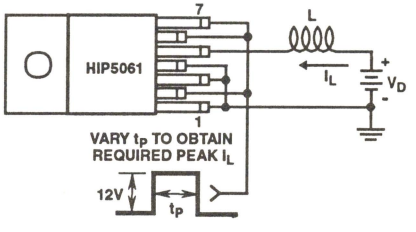


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

Definitions of Electrical Specifications

Refer to the Functional Block Diagram of Figure 1 for locations of functional blocks and devices.

Device Parameters

I_{DD}, Quiescent Supply Current - Supply current with the chip disabled. The Clock, Error Amplifier, Voltage-to-Current Converter, and Current Ramp circuits draw only quiescent current. The supply voltage must be kept lower than the turn-on voltage of the V_{DD} clamp or else the supply current increases dramatically.

I_{DD}, Operating Supply Current - Supply current with the chip enabled. The Error Amplifier is drawing its maximum current because V_{FB} is less than its reference voltage. The voltage-to-current amplifier is drawing its maximum because V_C is at its maximum. The ramp circuit is drawing its maximum because it is not being disabled by the DMOS transistor turning off.

IV_G, Quiescent Gate Driver Current - Gate Drivers supply current with the IC disabled. The Gate Driver is not toggling and so it draws only leakage current.

IV_G, Operating Gate Driver Current - Gate Drivers supply current with the IC enabled. The DMOS transistor drain is loaded with a large resistor tied to 60V so that it is swinging from 0V to 60V during each cycle.

V_{DDC}, V_{DD} Clamp - V_{DD} voltage at the maximum allowed current through the V_{DD} Clamp.

V_{REF}, Reference Voltage - The voltage on FB that sets the current on V_C to zero. This is the reference voltage for the DC/DC converter.

Amplifiers

I_{FB}, Input Current - Current through FB pin when it is at its normal operating voltage. This current must be considered when connecting the output of a DC/DC convertor to the FB pin via a resistor divider.

$g_m(V_{FB})$, Transconductance - The change in current through the V_C pin divided by the change in voltage on FB. The g_m times the resistance between V_C and ground gives the voltage gain of the Error Amplifier.

IV_{CMAX}, Maximum Source Current - The current on V_C when FB is more than a few hundred millivolts less than V_{REF}.

IV_{CMAX}, Maximum Sink Current - The current on V_C when FB is more than a few hundred millivolts more than V_{REF}.

A_{OL}, Voltage Gain - Change in the voltage on V_C divided by the change in voltage on FB. There is no resistive load on V_C. This is the voltage gain of the error amplifier when g_m times load resistance is larger than this gain.

V_{CMAX}, V_C Rising Threshold - The voltage on V_C that causes the Voltage-to-Current Amplifier to reach full-scale. When V_C reaches this voltage, the V_C NMOS transistor (transistor with its drain connected to the V_C pin in the Functional Block Diagram of Figure 2) turns on and tries to lower the voltage on V_C.

V_{CHYS}, V_{CMAX} Hysteresis - The voltage on V_C that causes the NMOS transistor to turnoff if it had been turned on by V_C exceeding V_{CMAX}. At this voltage the current out of the Voltage-to-Current Converter is at roughly three quarters of full-scale.

IVC_{OVER}, V_C Over-Voltage Current - The current drawn through the V_C pin after the NMOS transistor is turned on due to excessive voltage on V_C. The NMOS transistor connected to the V_C pin draws more than enough current to overcome the full scale source current of the Error Amplifier.

Clock

fq, Frequency - The frequency of the DC/DC converter. The Clock actually runs faster than this value so that various control signals can be internally generated.

DMOS Transistor

$r_{DS(ON)}$, "On" Resistance - Resistance from DMOS transistor Drain to Source at maximum drain current and minimum Gate Driver voltage, V_G.

I_{DSS}, Leakage Current - Current through DMOS transistor at the Maximum Rated Voltage.

Current Controlled PWM

$g_m(V_C)$, Transconductance - The change in the DMOS transistor peak drain current divided by the change in voltage on V_C. When analyzing DC/DC converters the DMOS transistor and the inductor tied to the drain are sometimes modelled as a voltage-controlled current source and this parameter is the gain of the voltage-controlled current source.

V/I_{REF}, Current Control Threshold - The voltage on V_C that causes the DMOS transistor to shut off at the minimum controllable current. This voltage is greater than the Enable Comparator Threshold (V_{CEN}) so that as V_C rises the IC does not jump from the disabled state to the DMOS transistor conducting a large current.

t_{BT}, Blanking Time - At the beginning of each cycle there is a blanking time that the DMOS transistor turns-on and stays-on no matter how high drain the current. This blanking time permits ringing in the external parasitic capacitances and inductances to dampen and for the charging of the reverse bias on the rectifier diode.

t_{ONMIN}, Minimum DMOS Transistor "On" Time - The minimum on-time for the DMOS transistor where small changes in the V_C voltage make predictable changes in the DMOS transistor peak current. Converters should be designed to avoid requiring pulse widths less than the minimum on time.

t_{OFFMIN}, Minimum DMOS Transistor "Off" Time - The minimum off-time for the DMOS transistor that allows enough time for the IC to get ready for the next cycle. Converters should be designed to avoid requiring pulse widths so large that the minimum off time is violated. (However, zero off time is allowed, that is, the DMOS transistor can stay on from one cycle to the next.)

MinCI, Minimum Controllable Current - When the voltage on V_C is below V/I_{REF}, the peak current for the DMOS transistor is too small for the Current Comparator to operate reliably. Converters should be designed to avoid operating the DMOS transistor at this low current.

MaxCl, Maximum Controllable Current - The peak current for the DMOS transistor when the Voltage-to-Current Converter is at its full scale output. The DMOS transistor current may exceed this value during the blanking time so proper precautions should be taken. This parameter is unchanged for the first 3/8 of the cycle and then decreases linearly with time because of the Current Ramp becoming active.

Current Compensation Ramp

$\Delta I/\Delta t$, Compensation Ramp Rate - At a given voltage on V_C the DMOS transistor will turn off at some current that stays constant for about the first 1.5µs of the cycle. After 1.5µs, the turnoff current starts to linearly decrease. This parameter specifies the change in the DMOS transistor turnoff current.

t_{RD}, Compensation Ramp Delay - The time into each cycle that the compensation ramp turns on. The Current Compensation Ramp, used for Slope Compensation, is developed by the Current Ramp block shown in the FUNCTIONAL BLOCK DIAGRAM of Figure 2.

Start-Up

V_{DDMIN}, Rising V_{DD} Threshold Voltage - The minimum voltage on V_{DD} needed to enable the IC.

V_{DDHYS}, Power - On Hysteresis Voltage - The difference between the voltage on V_{DD} that enables the IC and the voltage that disables the IC.

V_{CEN}, Enable Comparator Threshold Voltage - The minimum voltage on V_C needed to enable the IC. The IC can be shutdown from an open-collector logic gate by pulling down the V_C pin to GND.

R_{VC}, Power - Up Resistance - When V_{DD} is below V_{DDMIN}, the NMOS transistor connected to the V_C pin is turned on to make sure the V_C node is low. Thus the voltage on V_C can gradually build up as will the trip current on the DMOS transistor. This is the only form of "soft start" included on the IC. The resistance is measured between the V_C and GND pins.

Thermal Monitor

T_J, Rising Temperature Threshold - The IC temperature that causes the IC to disable itself so as to prevent damage. Proper heat-sinking is required to avoid over-temperature conditions, especially during start-up when the DMOS transistor may stay on for a long time if an external soft-start circuit is not added.

T_{JHY}, Temperature Hysteresis - The IC must cool down this much after it is disabled by being too hot before it can resume normal operation.

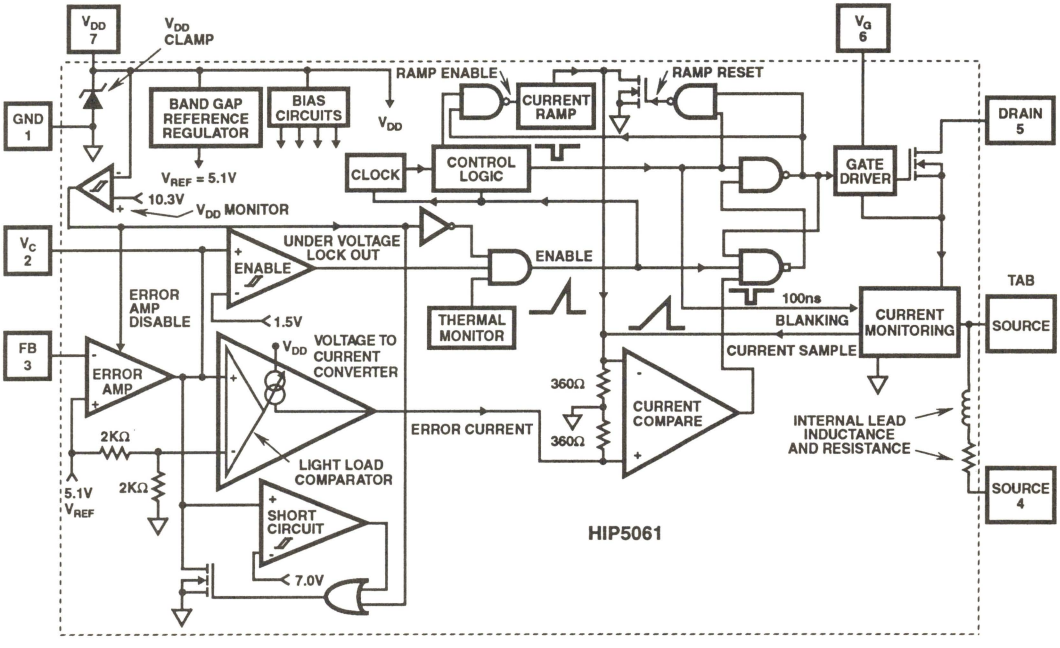


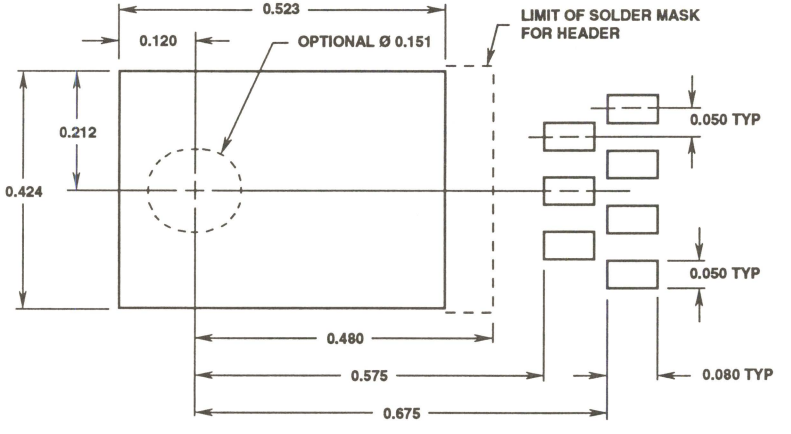
FIGURE 2. FUNCTIONAL BLOCK DIAGRAM OF THE HIP5061

Pin Description

TERMINAL NUMBER	DESIGNATION	DESCRIPTION
1	GND	This is the analog ground terminal of the IC.
2	V_C	The output of the transconductance amplifier appears at this terminal. Input to the internal voltage to current converter also appears at this node. Transconductance amplifier gain and loop response are set at this terminal. When the V_{DD} terminal voltage is below the starting voltage, V_{DDMIN}, this terminal is held low. When the voltage at this terminal exceeds V_{CMAX}, 7V typical, implying an over-current condition, a typical 10mA current, I_{VCOVER} pulls this terminal towards ground. This current remains "ON" until the voltage on the V_C terminal falls by V_{CHYS}, typically 1.1V, below the upper threshold, V_{CMAX}. When the voltage on this terminal falls below V_{CEN}, typically 1.5V, the IC is disabled.
3	FB	Feedback from the regulator output is applied to this terminal. This terminal is the input to the transconductance amplifier. The amplifier compares the internal 5.1V reference and the feedback signal from the regulator output.
4	SOURCE	The terminal, labeled TAB, has a connection to this terminal, but because of the long lead length and resulting high inductance of this terminal, it should not be used as a means of bypassing. Therefore, this terminal is labeled "Do Not Use."
5	DRAIN	Connection to the Drain of the internal power DMOS transistor is made at this terminal.
6	V_G	Gate drive supply voltage is provided at this terminal. A 10Ω to 150Ω resistor connected between this terminal and the V_{DD} terminal provides decoupling and the supply voltage for the gate drivers.
7	V_{DD}	External supply input to the IC. A nominal 14V shunt regulator is connected between this terminal and the TAB. A series resistor should be connected to this terminal from the external voltage source to supply a minimum current of 33mA and a maximum current of 105mA under the worst cast supply voltage. The series resistor is not required if the supply voltage is 12V, ±10%.
TAB	SOURCE	This is the internal power DMOS transistor Source terminal. It should be used as the ground return for the V_{DD} bypass capacitor. In addition high frequency bypassing for both the regulator output load voltage and supply input voltage should be returned to this terminal.

For more information refer to Application Notes AN9208, AN9212, AN9323.

Foot Print For Soldering



TO-220 STAGGERED GULL WING SIP

Typical Performance Curves

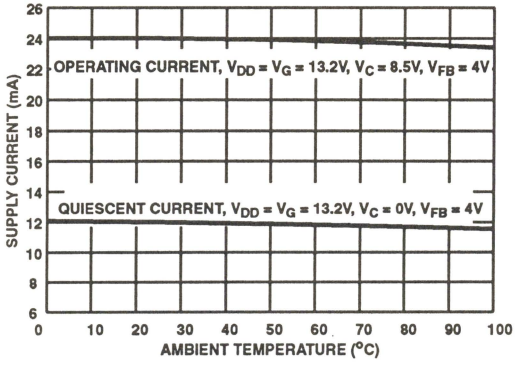


FIGURE 3. TYPICAL SUPPLY CURRENT vs TEMPERATURE

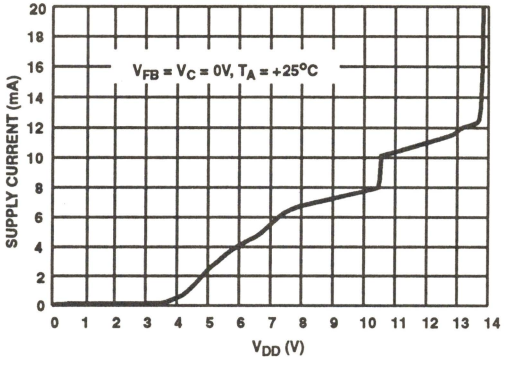


FIGURE 4. TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE

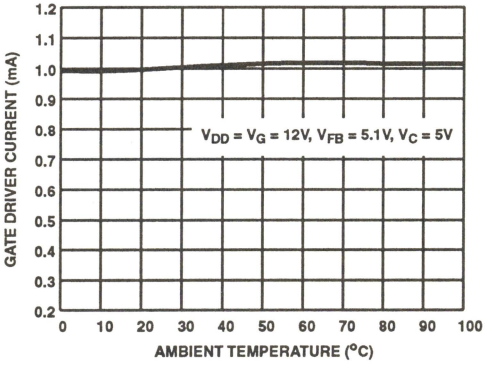


FIGURE 5. TYPICAL GATE DRIVER OPERATING CURRENT vs TEMPERATURE

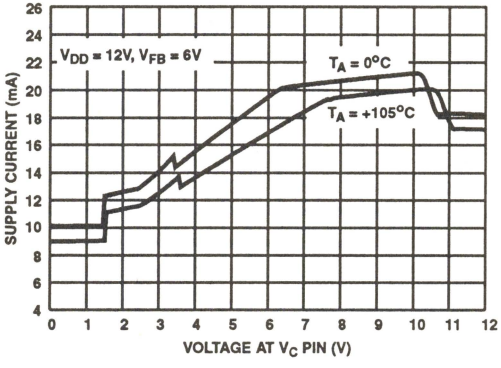


FIGURE 6. TYPICAL SUPPLY CURRENT vs VOLTAGE AT PIN V_C FOR 0°C AND +105°C

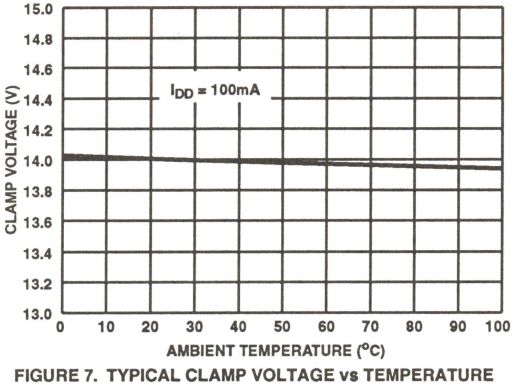


FIGURE 7. TYPICAL CLAMP VOLTAGE vs TEMPERATURE

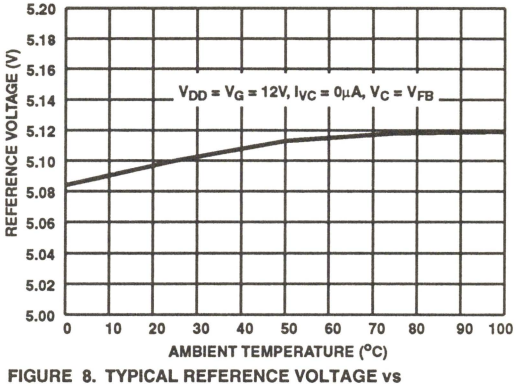


FIGURE 8. TYPICAL REFERENCE VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

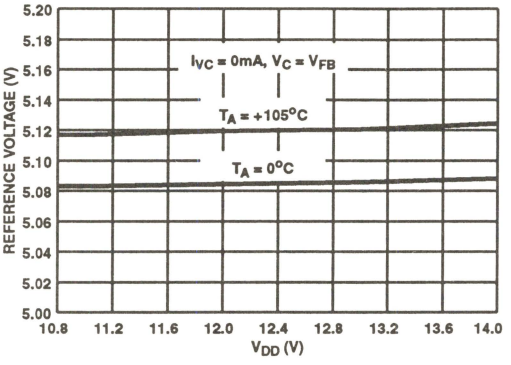


FIGURE 9. TYPICAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE FOR 0°C AND +105°C

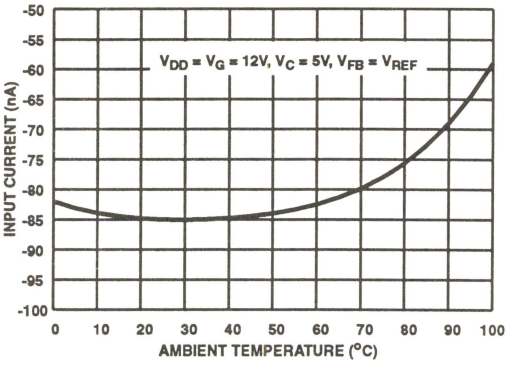


FIGURE 10. TYPICAL INPUT CURRENT TO FB PIN vs TEMPERATURE

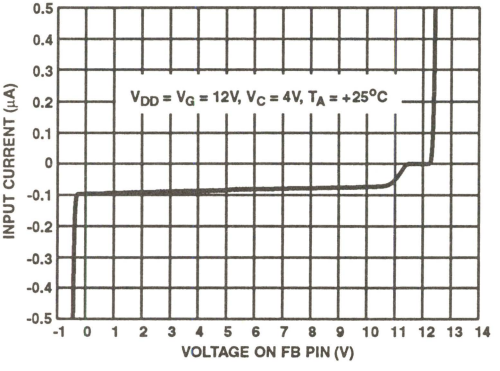


FIGURE 11. TYPICAL INPUT CURRENT TO FB PIN vs V_{FB}

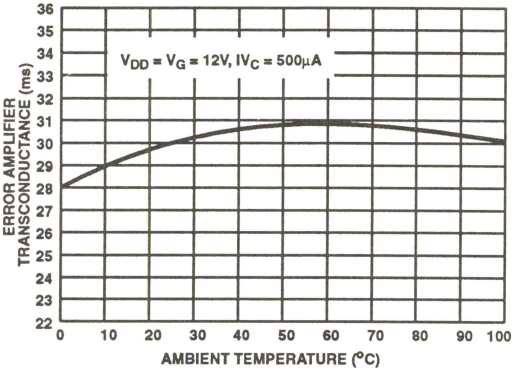


FIGURE 12. TYPICAL ERROR AMPLIFIER TRANSCONDUCTANCE vs TEMPERATURE

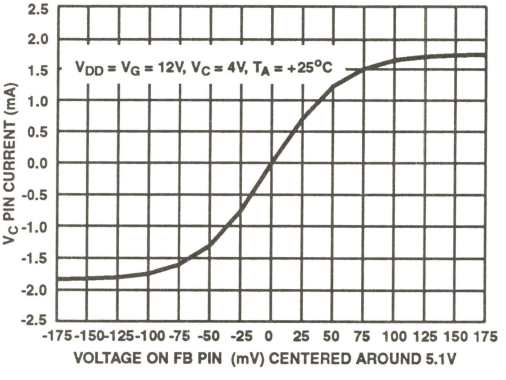


FIGURE 13. TYPICAL V_C PIN CURRENT IV_C PIN vs VOLTAGE ON FB PIN (SHOWS ERROR AMPLIFIER TRANSCONDUCTANCE)

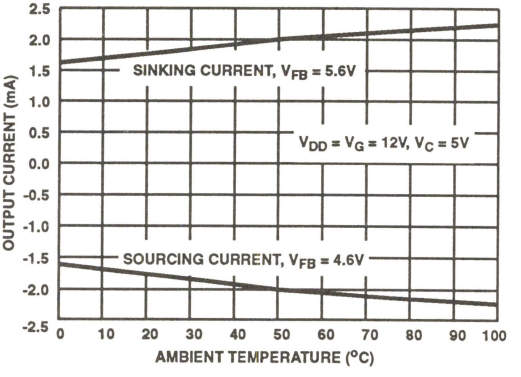


FIGURE 14. TYPICAL ERROR AMPLIFIER SINKING AND SOURCING CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

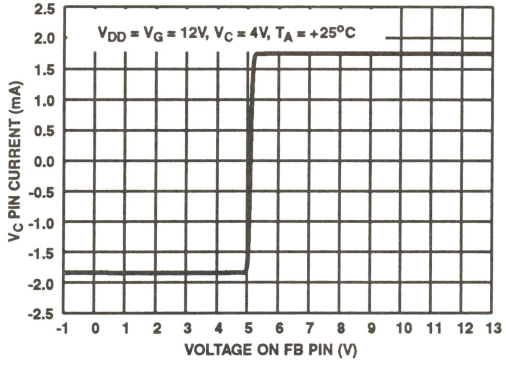


FIGURE 15. TYPICAL V_C PIN CURRENT vs VOLTAGE ON FB PIN

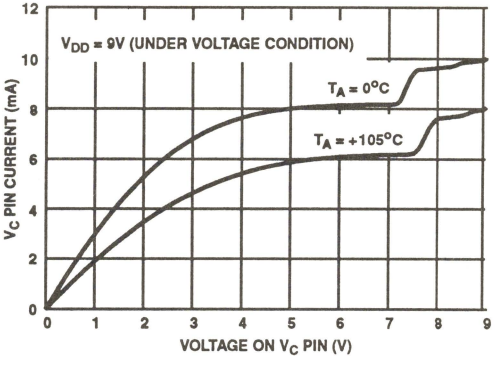


FIGURE 16. TYPICAL V_C PIN CURRENT vs VOLTAGE ON V_C PIN FOR 0°C AND +105°C

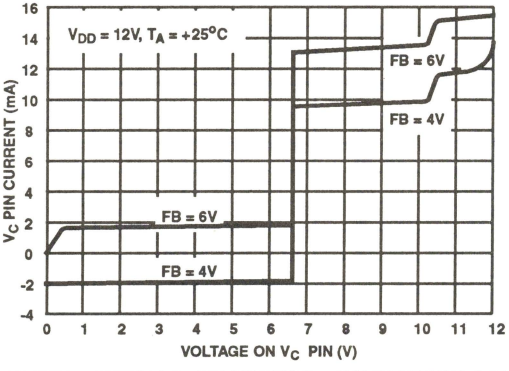


FIGURE 17. TYPICAL V_C PIN CURRENT vs VOLTAGE ON V_C PIN FOR VOLTAGES ABOVE AND BELOW V_{REF}

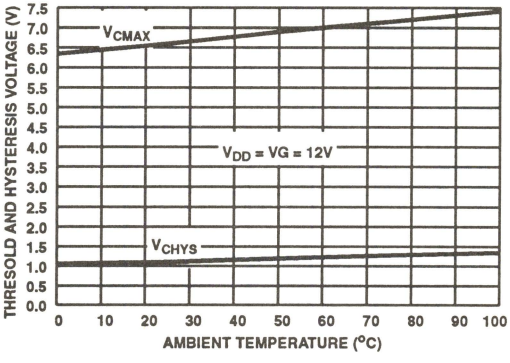


FIGURE 18. TYPICAL SHORT CIRCUIT COMPARATOR THRESHOLD VOLTAGE vs TEMPERATURE

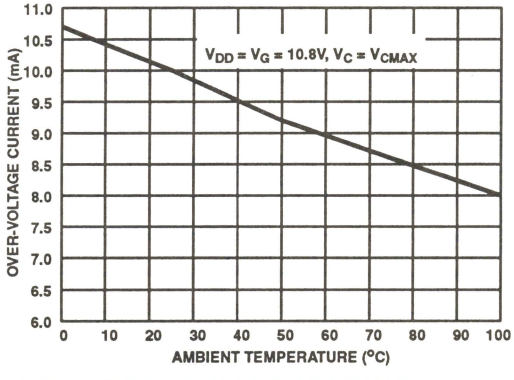


FIGURE 19. TYPICAL OVER-VOLTAGE CURRENT vs TEMPERATURE

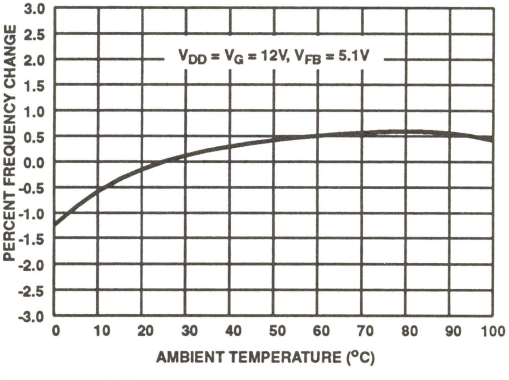


FIGURE 20. TYPICAL CLOCK FREQUENCY PERCENT CHANGE vs TEMPERATURE

Typical Performance Curves (Continued)

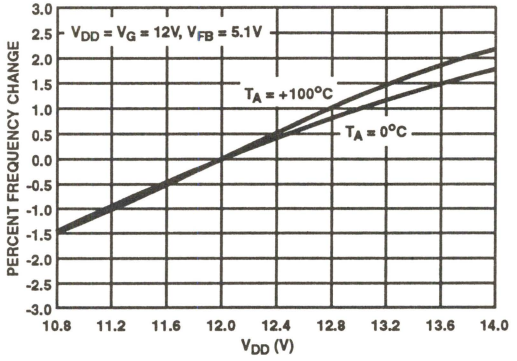


FIGURE 21. TYPICAL CLOCK FREQUENCY PERCENT CHANGE vs SUPPLY VOLTAGE V_{DD} AT 0°C AND +100°C

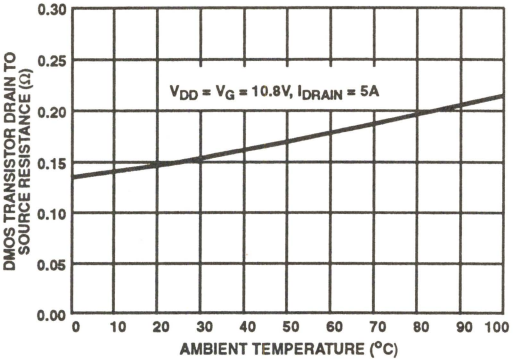


FIGURE 22. TYPICAL DMOS TRANSISTOR DRAIN TO SOURCE RESISTANCE vs TEMPERATURE

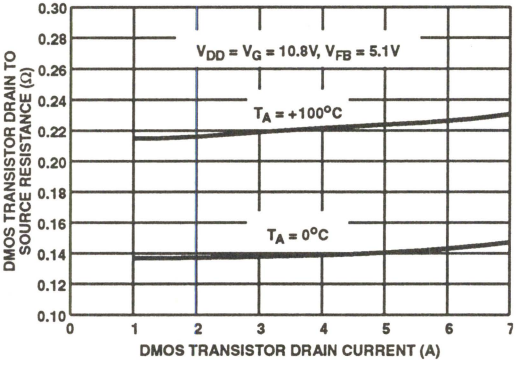


FIGURE 23. TYPICAL DMOS TRANSISTOR DRAIN TO SOURCE RESISTANCE vs DRAIN CURRENT I_{DRAIN} AT 0°C AND +100°C

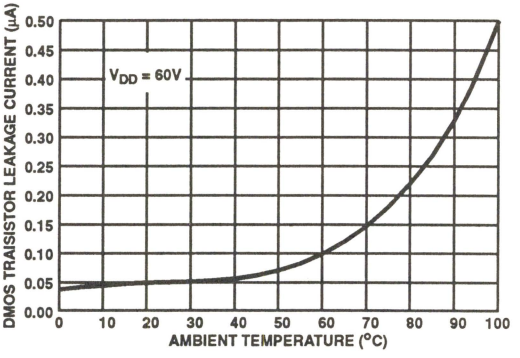


FIGURE 24. TYPICAL DMOS TRANSISTOR DRAIN TO SOURCE LEAKAGE CURRENT vs TEMPERATURE

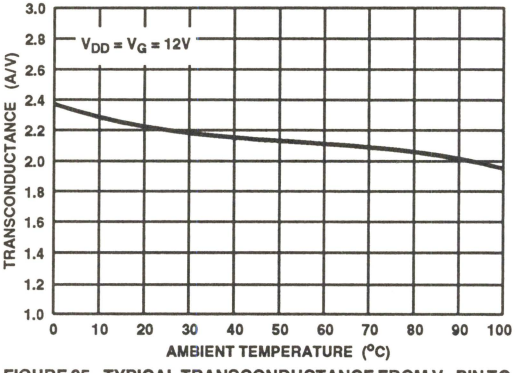


FIGURE 25. TYPICAL TRANSCONDUCTANCE FROM V_C PIN TO DMOS TRANSISTOR DRAIN (PEAK CURRENT) vs TEMPERATURE

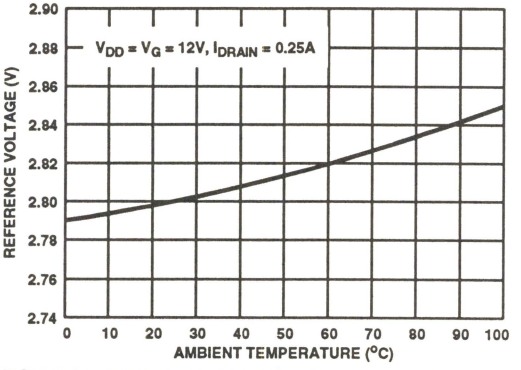


FIGURE 26. TYPICAL VOLTAGE TO CURRENT CONVERTER REFERENCE VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

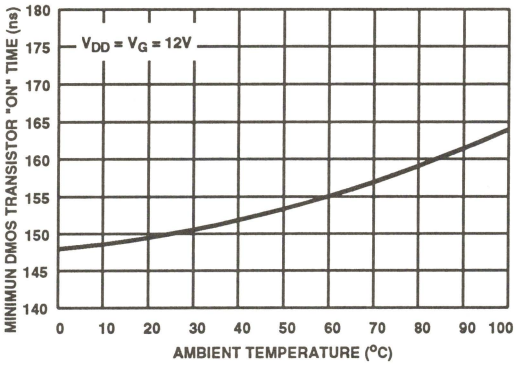


FIGURE 27. TYPICAL MINIMUM DMOS TRANSISTOR "ON" TIME vs TEMPERATURE

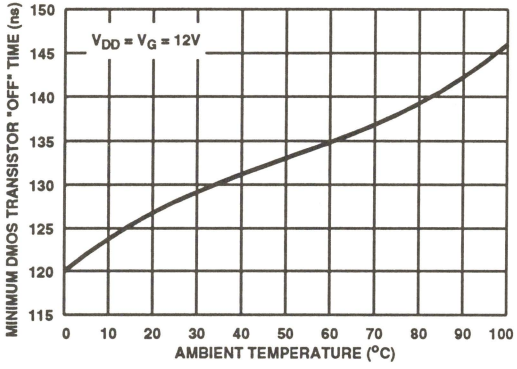


FIGURE 28. TYPICAL MINIMUM DMOS TRANSISTOR "OFF" TIME vs TEMPERATURE

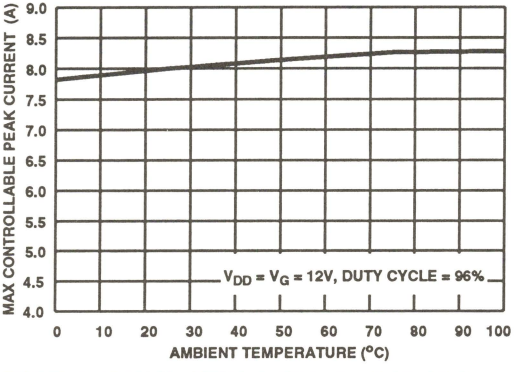


FIGURE 29. TYPICAL MAXIMUM CONTROLLABLE PEAK DMOS DRAIN CURRENT vs TEMPERATURE

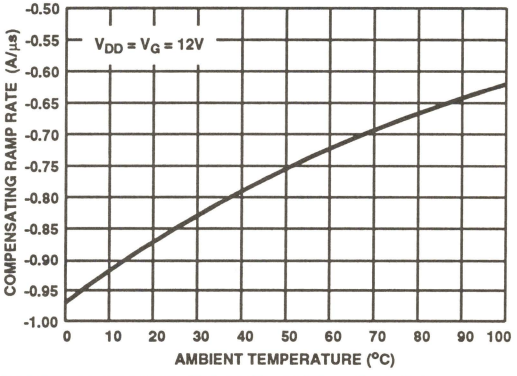


FIGURE 30. TYPICAL COMPENSATING RAMP RATE vs TEMPERATURE

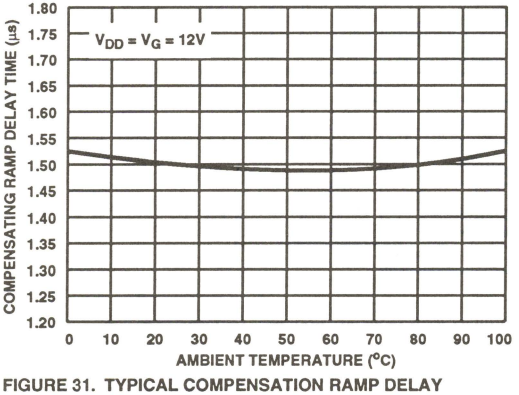


FIGURE 31. TYPICAL COMPENSATION RAMP DELAY TIME vs TEMPERATURE

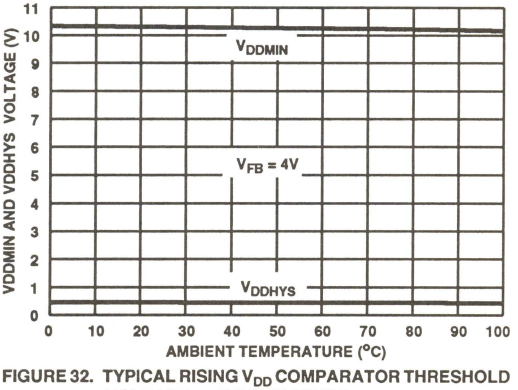


FIGURE 32. TYPICAL RISING V_{DD} COMPARATOR THRESHOLD VOLTAGE vs TEMPERATURE

Typical Application Circuit

Figure 33 shows a Simplified Block Diagram of the HIP5061 in a typical Boost converter. A resistor connected from the V_{IN} supply to the V_{DD} terminal of the IC powers the internal 14V shunt regulator. The Gate Driver supply is decoupled from the main supply by a small external resistor connected between V_{DD} and the V_G terminal. A bypass capacitor is connected between the V_{DD} terminal and ground to reduce coupling between analog and digital circuitry. A Schottky diode insures efficient energy transfer from the DMOS drain circuit inductor to the load. To set the output voltage, two resistors are used to scale the output supply voltage down to the 5.1V internal reference.

The heart of the IC is the high current DMOS power transistor with its associated gate driver and high-speed peak current control loop. A portion of the converters DC output is applied to a transconductance error amplifier that compares the fed back signal with the internal 5.1V reference. The output of this amplifier is brought out at the V_C terminal to provide for soft start and frequency compensation of the control loop. This same signal is also applied internally to program the peak DMOS transistor drain current. To assure precise current control, the response time of this peak current control loop is less than 50ns.

A 2MHz internal clock provides all the timing signals for the converter operating at 250kHz. A slope compensation circuit is also incorporated within the converter IC to eliminate sub-harmonic oscillation that occurs in continuous-current mode converters operating with duty cycles greater than 50%.

HIP5061 Description of Operation

Figure 2 shows a more detailed Functional Block Diagram of the HIP5061. An internal 14V shunt regulator in conjunction with an external series resistor provides internal operating voltage to the IC in applications where no 12V auxiliary supply is available. Note that In applications where the input voltage at V_{DD} is 12V, +/-10%, the regulator is not used. This regulator is shown as a zener diode on the diagrams of Figure 2 and Figure 33.

The 2MHz clock is processed in the Control Logic block to provide various timing signals. A cycle of operation begins when a 100ns pulse (which occurs at a 4µs interval) triggers the latch that initiates the DMOS transistor on-time. This pulse also provides a blanking interval in the Current Monitoring block to eliminate false turn-offs caused by high transient pulse currents that occur during turn-on. The output of

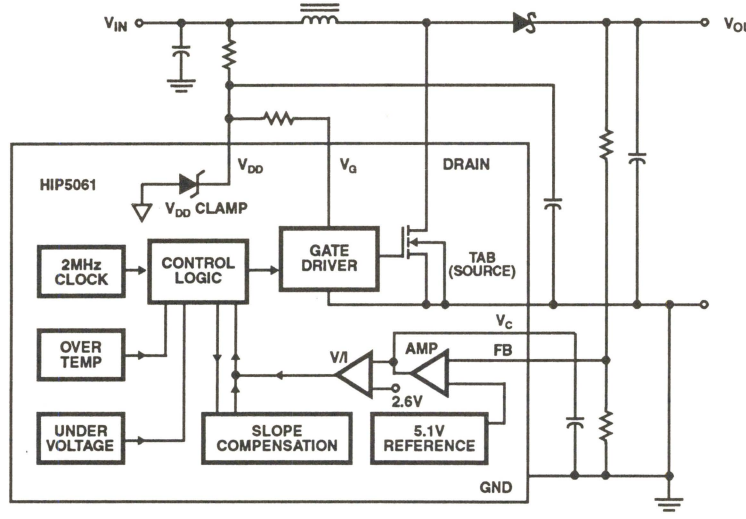


FIGURE 33. SIMPLIFIED BLOCK DIAGRAM OF THE HIP5061 IN A TYPICAL "BOOST" CONFIGURATION

the Current Ramp block is summed with the sensed DMOS transistor current (to provide slope compensation) before being compared with the Error Current signal. The current ramp, -0.45A/µs, is inhibited for the first 1.5µs (37.5%) of the duty cycle by the Ramp Enable signal, since ramp is not needed for slope compensation during this interval. Inhibiting of the compensating ramp has the effect of reducing the peak short-circuit current.

The output of the power supply is divided down and monitored at the FB terminal. A transconductance error amplifier compares the DC level of the fed back voltage with an internal bandgap reference, while providing voltage loop compensation by means of external resistors and capacitors. The Error Amplifier output (the error voltage) is then converted into a current (the Error Current) that is used to program the required peak DMOS transistor current that produces the desired output voltage. When the sum of the sensed DMOS transistor current and the compensating ramp exceed the Error Current signal, the latch is reset and the DMOS transistor is turned off. Current comparison around this loop takes place in less than 50ns, allowing for excellent 250kHz converter operation. The latch can also be reset by an under-voltage (V_{DD} < 10.3V typical), over temperature (T_J > +125°C typical) or a shutdown signal externally applied at the V_C terminal. See Figure 36.

Note that if the error voltage (at the V_C pin) is less that 2.55V, then the output of the Voltage-to-Current Converter will be held at zero. This condition will produce the minimum possible pulse width, typically 150ns (100ns blanking pulse plus 50ns delay). Error voltages lower than this 2.55V level will not produce shorter pulse widths. Under very light loads (when V_C goes below 1.5V), the Enable Comparator will temporarily hold-off the PWM latch (and the DMOS transistor) until the V_C voltages rises above 1.5V. This low V_C inhibit circuit results in a burst-mode of operation that maintains regulation under light or no loads.

During an over-current condition, the output of the Error Amplifier will attempt to exceed the 7.0V threshold. At this point, the Short-Circuit Comparator will pull down on this signal and induce a low-level oscillation about the threshold, serving to clamp the peak error voltage. This clamping action, in turn, will limit the peak current in the DMOS transistor, reducing the duty ratio of the switch as the demand for current continues to increase. This action, in conjunction with the Thermal Monitor, serves to protect the IC from over-current (short-circuit) conditions.

Using the Transconductance Error Amplifier

A transconductance amplifier with a typical g_m of 30mS is used as the input gain stage where the power supply output voltage is compared with the internally generated 5.1V reference voltage. A PNP transistor input structure allows this amplifier to accommodate large negative going transient voltages without causing amplifier phase reversal, often associated with PNP input structures. Negative transients up to 5V applied to the input though at least 5.1k will not result in phase reversal. The amplifier output stage has the customary drain to drain output to help improve the output impedance, ideally infinity. The amplifier gain is typically 50dB and is not significantly altered when operating into the stages that follow within the IC. To minimize the output stage idling current, while providing high peak currents to insure rapid response to load and input transients, a class B type of output stage was used in the amplifier. Placing a 100k resistor from the amplifier output terminal, V_C, to ground will bias the output stage to an active state and still minimize power consumption. In all cases, the resistor shunting the transconductance amplifier output must be greater than 10kΩ to insure that the output will rise sufficiently high to obtain the maximum DMOS transistor drain current.

Start-Up Sequence

Upon initial power up of the HIP5061 in a typical application circuit, the voltage at V_C will be zero, and the DMOS transistor will be off. When the voltage at V_{DD} rises above the 10.3V typical threshold, the error amplifier output is enabled and the V_C voltage begins to rise in response to the low voltage at the FB terminal. When the V_C voltage rises above 1.5V the DMOS transistor begins to switch at the minimum duty cycle, and when it rises above 2.55V the duty cycle begins to increase. The V_C voltage (and peak DMOS transistor current) will then continue to rise until the voltage loop gains control and establishes regulation. Note that the rate of rise in the V_C voltage can be controlled by an external soft start circuit (See **Soft Start Implementation**).

If the V_C voltage is unrestricted in its rate of rise, then it will typically rise quickly to its maximum (peak current) value, causing the DMOS transistor to turn-on and stay on until it reaches the peak current value. At this point, the DMOS transistor begins switching, and the V_C voltage (and peak DMOS transistor current) will drop down to the level commanded by the voltage loop.

Using the Shunt Regulator

The internal 14V shunt regulator in conjunction with an external series resistor allows the IC to operate from quite high input voltages, limited only by power dissipation in the external resistor. When only higher voltages are available, a bootstrap or other 12V auxiliary supply can be used to eliminate this dissipation. The series resistor should be chosen to be as large as possible to reduce power dissipation at high line, while ensuring adequate V_{DD} voltage at low line. The maximum value for this resistor, ***R***, is given by:

$$R_{MAX}(\Omega) = \frac{V_{I,MIN} - 10.5}{0.033}$$

Where $\mathbf{V_I}$ is the input voltage to the power supply. The value chosen for this resistor must also result in a current, ***I***, into the V_{DD} clamp that is less than 105mA when the input voltage is at its maximum:

$$I_{MAX}(A) = \frac{(V_{I,MAX} - 13.3)}{R_{MAX}}$$

Inductor Selection

The selection of the energy storage inductor(s) L_{STOR} for a DC to DC converter has tremendous influence on the behavior of the converter. It is particularly important in light of the high level of integration (and necessarily few degrees of freedom) achieved in the HIP5061. There are several factors influencing the selection of this inductor. First, the inductance of L_{STOR} will determine the basic mode of operation for the converter: continuous or discontinuous current. In order to maximize the output power for the given maximum controllable DMOS transistor current, a converter may be designed to operate in continuous current mode (CCM). However, this tends to require a larger inductor, and for many converter topologies results in a feedback loop tha is difficult to stabilize. For these and other reasons, the inductor L_{STOR} may be chosen so as to operate the converter in discontinuous current mode (DCM). The relative merits of CCM and DCM operation for various topologies and the corresponding selection of L_{STOR} is well documented and will not be covered here.

A second factor influencing the selection of L_{STOR} is the stability requirement for current-mode control. This constraint is only applicable for converters operating in CCM, since open-loop instabilities of this type are not observed in converters operating in DCM. For marginal stability, the compensating ramp (internal to the HIP5061) must have a slope that is greater than one-half the difference between the inductor current's down slope and up slope. (To ensure stability for duty ratios D > 0.8, the slope of the compensating ramp should be equal to the inductor current downslope.) A generally accepted goal is to set the slope of the compensating ramp to be at least one-half of the inductor current down slope. Since there is no external control over the internal compensating ramp, one must be sure that the inductor is large enough so that the down slope of the inductor current is not too large. Table 2 summarizes this requirement for minimum inductance for several common topologies.

A third constraint on the size of the inductor is one that is common among current-mode controlled PWM converters, and applies to both DCM and CCM operation. The stable generation of the desired DMOS transistor pulse width depends on the accurate comparison of the error signal and the peak L_{STOR} (DMOS) transistor drain current. Thus, as the peak L_{STOR} ripple current becomes smaller, immunity from noise on the error signal is eventually reduced until the pulse width can no longer be adequately controlled. For the HIP5061, the inductor current ripple must be at least 200mA peak to peak to ensure proper control of the DMOS transistor current. This effectively establishes a maximum value for the inductor L_{STOR}, so as to maintain at least 200mA of ripple. Note that under extremely light or no load conditions, all converters will eventually operate in DCM, and the 200mA requirement will eventually be violated. Under these conditions, the HIP5061 will continue to regulate, although the switching of the DMOS transistor will be in a burst-mode, controlled by the Light Load Comparator. (See Figure 2.)

TABLE 2. MINIMUM INDUCTANCE FOR STABLE CCM OPERATION ABOVE 50% DUTY CYCLE

CONVERTER TYPE	MINIMUM INDUCTANCE
Boost	$L = \frac{V_O + V_D - V_{I,MIN}}{2M_{R,MIN}}$
SEPIC (Note 1)	$\frac{L_1 L_2}{L_1 + L_2} > \frac{V_O + V_D}{2M_{R,MIN}}$
Cuk (Note 2)	$\frac{L_1 L_2}{L_1 + L_2} > \frac{V_O - V_D}{2M_{R,MIN}}$
Flyback	$L_P > \left(\frac{N_P}{N_S}\right)\frac{(V_O + V_D)}{2M_{R,MIN}}$
Forward	$L > \left(\frac{N_S}{N_P}\right)\frac{(V_O + V_D)}{2M_{R,MIN}}$

NOTES:

1. Assumes that L_1 and L_2 are both CCM.
2. L = Inductance in Henrys, V_O = Output Voltage, V_D = Diode Voltage Drop, V_I = Input Voltage, $M_{R,MIN} = (\Delta I/\Delta t)_{MIN} = 0.45A/\mu s$, L_1 = Drain Inductor, L_2 = Secondary Inductor, N_P = Primary Turns, N_S = Secondary Turns

DMOS Transistor Turn-Off Snubber

In order to reduce dissipation in the DMOS transistor due to turn-off losses, the turn-off time has been minimized. However, the rapid reduction of current that occurs in the drain of the DMOS transistor can result in large transient voltages being induced across any parasitic inductance in the drain path. For this reason, it is important that such parasitic inductance be reduced by good, high frequency layout practices. Nevertheless, there are many instances (e.g., transformer isolated topologies) in which voltages in excess of 60V may be developed at the DMOS transistor drain. In some cases, a simple R-C snubber may be added to reduce the overshoot of the drain voltage to a safe level.

It is also possible that the large amount of ringing that can occur at the DMOS transistor drain at turn-off will induce noise in the IC. This noise may result in false triggering of the PWM latch, particularly at high peak DMOS transistor drain currents. Noise related instability can also be eliminated by the addition of a snubber, which will rapidly damp out such turn-off ringing. Good layout practices will reduce the need for such protective measures, and ensure that the DMOS transistor is not overstressed.

Under-Voltage Lockout

The V_{DD} input voltage is monitored by a comparator that holds off the DMOS transistor gate drive signal when the V_{DD} voltage is less that about 10.3V. The typical 0.5V hyster-

esis of this comparator is intended to reduce oscillation when the voltage at V_{DD} is in the vicinity of 10V. Note, however, that when an external series resistor is used to feed the shunt regulator, the voltage drop across this resistor (which sharply decreases when the IC shuts down), effectively reduces the hysteresis. To reduce the tendency for oscillation in the vicinity of the 10V threshold, the impedance of the source that feeds the DC to DC converter input should be minimized. The addition of a capacitor (1µF-47µF) at the V_{DD} terminal can also help to provide smooth turn-on or turn-off of the converter if the input supply rises or falls gradually through the V_{DD} Comparator threshold.

Peak Controllable DMOS Transistor Current

Figure 34 shows the guaranteed minimum, peak controllable DMOS transistor current versus duty cycle. This peak current value is established by the current limit circuitry, which effectively clamps the voltage at V_C (the error voltage) to perform current limiting. Since the sensed DMOS transistor current is summed with a compensating current ramp that begins its rise 1.5µs after the initiation of a cycle, current limiting will *begin* to occur at a peak DMOS transistor current that varies with the operating duty cycle. The highest current limit threshold occurs for D<0.375, where no ramp is added to the sensed DMOS transistor current. At higher operating duty ratios, the onset of current limit will occur at increasingly lower currents, due to the effect of adding the compensating ramp to the sensed current. Note that this curve represents guaranteed minimum values. The guaranteed maximum values are considerable higher, although they are still limited to levels that protect the IC.

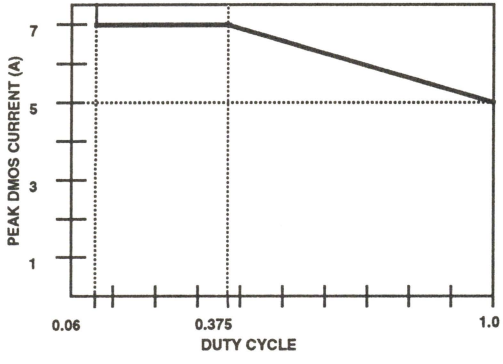


FIGURE 34. PEAK DMOS TRANSISTOR DRAIN CURRENT vs DUTY CYCLE

When the DMOS transistor first turns ON there may be substantial current spikes exceeding the normal maximum peak current established by the current control stages within the IC. To prevent these spurious spikes from conveying erroneous information to the Current Comparator, a 100ns blanking signal is applied to the current monitoring circuitry. Thus, there is no peak current protection during the first 6% of the duty cycle (see Figure 36).

DMOS Transistor Turn-On Noise

Although the large DMOS transistor turn-on current spikes are "blanked over" by the control circuit, it is important to minimize these current spikes, since they often result in voltage spikes considerably below the device substrate that can activate parasitic devices within the IC. Such activation of parasitic devices will often result in improper operation of the IC. An external terminal labeled V_G brings out the power supply to the gate drive circuitry. This allows for the control of the peak current delivered to the gate of the DMOS transistor, which in turn establishes the turn-on speed. The V_G pin may be externally bypassed for the fastest possible turn-on, or series resistance may be added with no bypassing capacitor to slow down the turn-on of the DMOS transistor. Depending upon the actual layout of the supply, it is generally recommended that a series resistor be added (10Ω-150Ω) so that the DMOS transistor turn-on speed is reduced. By properly adjusting the turn-on speed, undershoot can be avoided while turn-on switching losses are kept to a minimum.

Soft Start Implementation

It is often desirable to allow the regulator to start up slowly, Figure 35 shows one means of implementing this action. The normally high output current from the HIP5061 transconductance amplifier (when V_{FB} = 0 and V_{REF} = 5.1V) is directed to an external capacitor through a diode. This slows down the rate of rise of the voltage at the V_C terminal. After the regulator starts, the external capacitor is charged to V_{DD} and is effectively removed from the frequency compensation network by a reverse biased diode. To ensure rapid recycling of the capacitor voltage with removal of power, a diode is placed across the 100kΩ resistor. Logic Shutdown Input (V_C Pin).

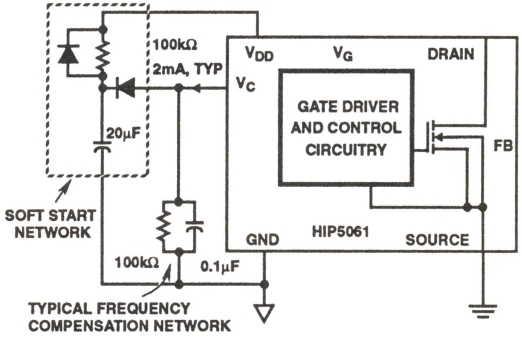


FIGURE 35. SOFT START CIRCUIT FOR THE HIP5061

The DC to DC converter may be shut down by returning the V_C output terminal to ground. A sinking current greater than 4mA will insure that this output is pulled to ground. It must be remembered that once switching operation ceases, the drain of the DMOS transistor is open. When the supply is in the Boost configuration, the output voltage is not zero but the input voltage less diode and inductor voltage drops. If the SEPIC

topology is used, this is not the case. Shutting down the regulator via the V_C terminal will cut off the output. Figure 36 shows two methods of shutting down the IC. In each case the current sinking circuit must be able to sink at least 4mA, the maximum current from the HIP5061 V_C terminal.

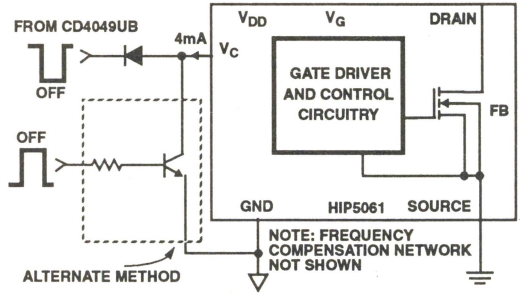


FIGURE 36. TWO METHODS OF SHUTTING DOWN THE HIP5061

Mounting, Layout and Component Selection

The TO-220 package with its gullwing leads was designed to be surface mounted. To aid in the external reduction of lead length and hence inductance and resistance, the IC leads were staggered. To keep the inductance and resistance of the critical drain terminal as low as possible, it is suggested that the PC trace to the DMOS transistor drain terminal be made as wide as possible. The adjacent source terminal is not recommended to be used and therefore allows the metal to the drain terminal to be widened beyond the normal widths for these terminals. Figure 37 illustrates these points.

One of the most important aspects to the proper application of this device is high frequency bypassing. In a Boost converter, for example, there should be a low-inductance interconnect from the DMOS transistor drain, through the output diode and capacitors, and returning to the TAB (source) of the HIP5061. Inductance in this line results in large transient voltages on the DMOS transistor drain terminal which can result in voltages above the maximum DMOS transistor drain voltage rating.

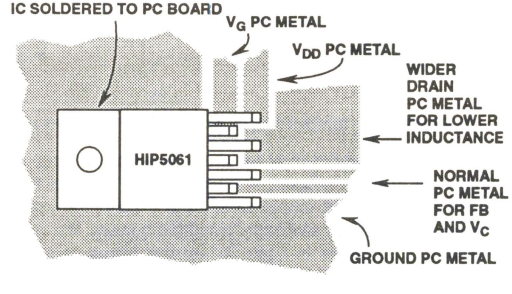


FIGURE 37. SHOWING WIDER PC BOARD METAL FOR CRITICAL

All the capacitors shown with values of 1µF or less are of the multilayer ceramic type with the X7R dielectric material. This material has a fairly flat voltage and temperature coefficient that assures that the capacitance remains comparatively constant at extreme operating temperatures and voltages. The multilayer construction allows for comparatively large values with good volumetric efficiency and low inductance. Capacitors around the power input and output circuits should be returned to the device TAB via a low inductance ground plane. This TAB is internally connected to the DMOS transistor source. The schematic diagram of Figure 38 was drawn with the diagonal leads to show the critical paths for the various high frequency elements. These short interconnects assure the lowest inductance around the output power circuit.

Design of a 28V, 1.8A Boost Converter

Figure 38 shows the schematic diagram and a parts list of a 50W supply designed with the HIP5061. Table 3 tabulates the performance of the power supply.

TABLE 3. TYPICAL LABORATORY PERFORMANCE OF 50W, 28V/1.8A REGULATOR

Input Voltage	11V to 16V
Line Regulation	12mV/V
Output Voltage	28.0V
Load Regulation	64mV/A
Output Ripple, FL (20MHz BW)	600mV P-P
Output Ripple, after Filter, FL (20MHz BW)	80mV P-P
Efficiency: V_I = 11V, I_L = 0.18A	90%
V_I = 11V, I_L = 1.8A	89%
V_I = 16V, I_L = 0.18A	73%
V_I = 16V, I_L = 1.8A	93%

Inductor Selection

In order to maximize the output power for the given maximum controllable DMOS transistor current, this converter has been designed to operate in continuous current mode (CCM). In this mode, the inductor value will generally be large, resulting in a lower inductor ripple current and a lower peak DMOS current. To ensure that the converter operates in CCM over the usable range of input voltage and output current, the value of L2 must be greater than the "critical inductance," given by

$$L_{CRIT} = \frac{V_O V_{I,MAX}^2 (V_O + V_D - V_{I,MAX}) T_S}{2 P_{O,MIN} (V_O + V_D)^2}$$

$$= \frac{(28)(16)^2 (28 + 0.5 - 16) 4\times10^{-6}}{2(5.6)(28 + 0.5)^2}$$

$$= 39\mu H$$

where $P_{O,MIN}$ has been arbitrarily chosen as 5.6W, corresponding to an output current of 0.2A, and V_D is the forward voltage of CR1. Thus, for L2 > 39µH, the converter will be in CCM for V_I = 11V to 16V and I_L = 0.2A to 1.8A.

A second factor influencing the selection of L2 is the stability requirement for current-mode control. Using the above equation for L_{MIN} for the Boost converter:

$$L > \frac{V_O + V_D - V_{I,MIN}}{2 \times M_{RAMP,MIN}} = \frac{28 + 0.5 - 11}{2 \times (0.45 \times 10^6 A/S)} = 19\mu H$$

Thus, L2 must be at least 19µH to ensure good stability of the current loop, and a choice of L2 = 40µH satisfies this requirement, while maintaining CCM operation over an extremely wide load range.

The chosen core material for L2 is Kool Mu ferrous alloy powder from Magnetics, Inc. This material was chosen because of its relatively low cost, while its losses due to AC flux are five to ten times less than conventional powdered iron.

Loop Compensation

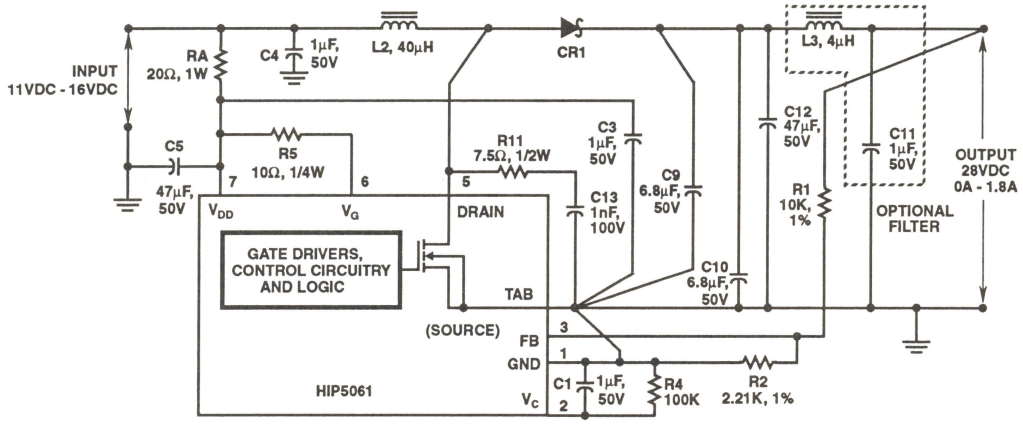
The control to output transfer function for this current-mode boost converter has the following characteristics over the specified load and line conditions:

D.C. Gain: 20dB-40dB
Pole at 88Hz-880Hz
LHP Zero at 1MHz
RHP Zero at 11.0kHz-110kHz
Double Pole at 80kHz (from filter)

To stabilize the voltage loop, it is necessary to establish the unity gain crossover frequency well below the RHP zero, since this zero introduces positive gain and negative phase. A crossover of 4kHz is fairly conservative, and is achieved by adding a 1µF capacitor at the VC pin, which provides near infinite DC gain, and about -5dB of gain at 4kHz. This results in a phase margin of about 15° at full load. Note that R4 is required for proper operation of the transconductance amplifier, since it is providing bias current for the output stage as discussed under Using the Transconductance Error Amplifier section.

Output Filter Design

Inductor L3 was chosen with C11 to provide at least 15dB of ripple attenuation at the switching frequency. The corner frequency (80kHz) of this filter is well above the crossover frequency of the voltage loop (4kHz), and has no effect on stability. This secondary LC filter was used to reduce output ripple instead of a lower-cost, high-value, low ESR aluminum electrolytic capacitor to demonstrate the reduction in volume possible at this switching frequency. A lower cost solution could achieve the same output ripple by replacing C9,10,12 and L3 with one or two large capacitors (e.g.,



PARTS LIST

RA 20Ω, 1W, Wirebound - Dale RWR81S20R0FR or Equivalent
R1 10K, 1%
R2 2.2K, 1%
R4 100K, 1/4W
R5 10Ω, 1/4W
R11 7.5Ω, 1/2W, Carbon - Allen Bradley EB75G5
C1, C3, C4 and C11 1µF, 50V, Ceramic - Murata Erie RPE113X7R105050V
C5 and C12 47µF, 50V, Alum - United Chemicon 515D476M050
C9 and C10 6.8µF, 50V, Ceramin - Mallory M60u6r8M50
C13 1nF, 100V, Ceramin - Kemet C322C102K1G5CA
CR1 Schottky Diode - Motorola MBRD360
L2 40µH at 5A, Pulse Engineering PE - 53571
L3 4µH at 5.5A, Pulse Engineering PE - 53570

FIGURE 38. HIP5061 50W, 28V BOOST REGULATOR SCHEMATIC AND PARTS LIST

390µF, 50V, type 673D from United Chemicon). This change would also greatly improve load transient response, provided that the loop compensation is appropriately adjusted. Note that in the circuit of Figure 38, capacitor C12 does not significantly affect output ripple, but is necessary to absorb the energy stored in L2 during severe load transients. In the event of a step change in load from 1.8A to 0A, C12 will limit the output voltage overshoot to about 10V and protect the drain of the DMOS transistor from overvoltage breakdown.

Input and V_{DD} Filters

Since the boost converter is current fed, input filtering is easily achieved by the addition of a small capacitor C4. This capacitor provides nearly 40dB of ripple current attenuation for the input, reducing the AC ripple current flowing into the converter to less than 200mA.

R5 and C3 have been chosen to provide good filtering of high frequency pulse currents. R5 provides isolation between the analog V_{DD} pin and the high pulse current V_G pin, and also provides a means to control the turn-on speed of the DMOS transistor by limiting the peak current available to the internal gate drive circuitry. Thus the output transition time may be increased to prevent drain voltage undershoot. Undershoot may result in activation of device parasitics and improper circuit operation. For the two-layer board used for this design, C3 could be reduced to 0.22µF without affecting circuit operation. C5 was added to provide low-frequency filtering at the V_{DD} pin. This reduces the tendency of the circuit to oscillate off and on when the voltage at the V_{DD} pin s in the vicinity of the under voltage lockout threshold, typically 10V, and the output power is high (30W - 50W).

Shunt Regulator Resistor

Resistor RA has been chosen to be as large as possible to reduce power dissipation at high line, while ensuring adequate V_{DD} voltage at low line. Note that the guaranteed range of input voltage for proper operation of this circuit is 11.2V to 15.3VDC, based upon data sheet limits. However, the circuit was found to perform well at room temperature for V_I = 10.7VDC to 17VDC. The maximum value for RA is

$$R_{MAX} = \frac{V_{I,MIN} - 10.5}{0.033} = 21\Omega$$

RA has been chosen as 20Ω, which results in a current into the V_{DD} clamp that is less than 105mA when the input voltage is at its maximum:

$$I_{MAX} = \frac{(V_{I,MAX} - 13.3)}{20.0} = 100mA < 105mA$$

Snubber Network

A snubber network has been added to reduce the ringing at the drain due to parasitic layout inductances. In particular, under severe load transient conditions, this snubber is necessary to protect the drain from voltage breakdown. A second benefit of reducing the noise and ringing at the drain is that it reduces the tendency of the HIP5061 to exhibit noise-related instabilities at high peak DMOS transistor currents (4A-6A). A value of 1000pF was chosen for C13, since this is adequate to dampen the ringing associated with the 200pF drain capacitance of the DMOS transistor. R11 was chosen as 7.5Ω to provide the best possible dampening given the parasitic inductances that exist in the layout. Note that this snubber may not be necessary if the layout of the circuit were improved, or if the application did not push the envelope of DMOS transistor current.

Other Power Supply Topologies

Figure 39 shows three other topologies besides the Boost that may be implemented with the grounded source DMOS power transistor used in the HIP5061. Other, more complex power supply topologies such as the Quadratic are also possible to implement with the HIP5061. One noteworthy feature of the Quadratic topology as shown in Figure 41 is the wide input to output voltage transfer ratio possible with reasonable duty cycles. Duty cycles that are not near the Minimum DMOS transistor "ON" Time specification shown in the Data Sheet. This permits easier control at the extremes of the transfer ratios. Compensating the control loop can pose challenges because of the wider changes in the transfer ratio and hence loop gain.

The SEPIC topology[11,13] does not have quite as wide input-output voltage range with reasonably controlled duty cycles as the Quadratic converter mentioned above, but it does allow both voltage increase and decrease with the same circuit. This is particularly advantageous when a power supply is being used in the stabilizing mode and isolation is not required. For example, in an application where a regulated 24V output is required and the input voltage varies ±20% from a nominal 24V. The SEPIC supply can provide both the Boost and Buck functions.

Another outstanding advantage of the SEPIC topology is its fault isolation of the input and output voltage. All energy is transferred via the coupling capacitor. Moreover if the clock stops, voltage transfer stops. If the switching transistor shorts there is no output. The Buck circuit will apply full input voltage to the load with a shorted transistor. This is reason that the SEPIC topology is referred to as the fail-safe Buck.

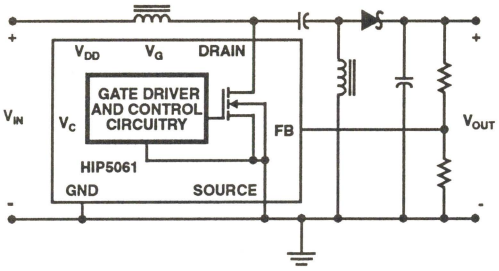


FIGURE 39A. SEPIC (FAIL-SAFE BUCK) CONVERTER

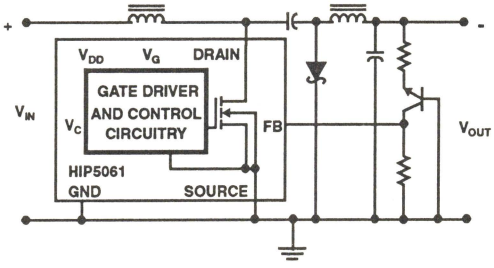


FIGURE 39B. CUK CONVERTER

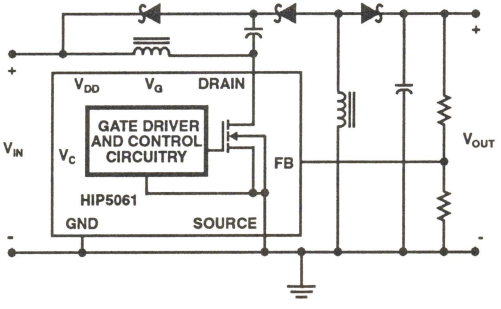


FIGURE 39C. QUADRATIC CONVERTER

FIGURE 39. THREE OTHER TOPOLOGIES

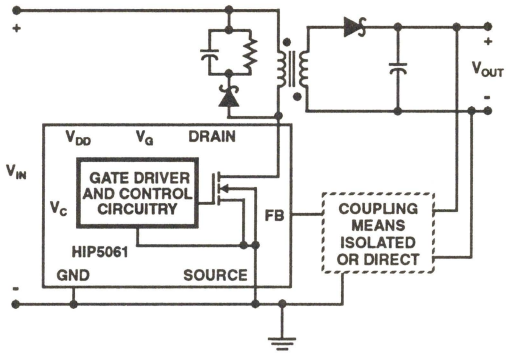


FIGURE 40. FLYBACK CONVERTER

It should be noted that when the Cuk topology is implemented, a transistor current source is used to convert the negative output voltage of the Cuk converter to a current that is level shifted to the FB terminal on the HIP5061.

Two other useful topologies that may be used are the Forward and the Flyback as shown in Figure 40 and Figure 41. As shown, they may either be operated as an isolated or non-isolated converter.

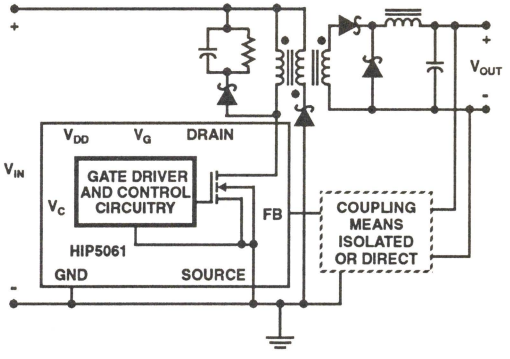


FIGURE 41. FORWARD CONVERTER

Both the SEPIC and the Boost topologies may be operated at high voltages with the addition of a high voltage cascode . Figure 42 shows the Cascode SEPIC converter that is essentially limited by the selection of the external power transistor. The burden of voltage, and power is placed upon the external transistor. The HIP5061 still performs the drain current sampling and the control function is the same as the non cascode configuration.

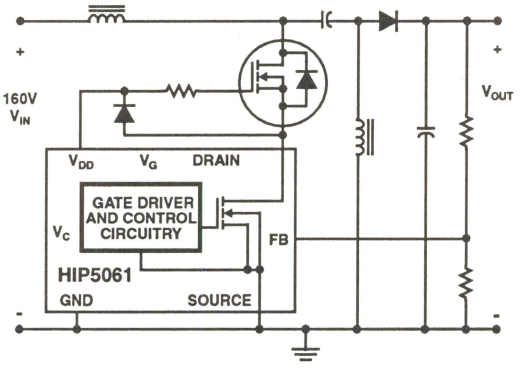


FIGURE 42. OFF LINE CASCODE SEPIC

Figure 43 shows the voltage transfer as a function of duty cycle for the power supply topologies discussed.

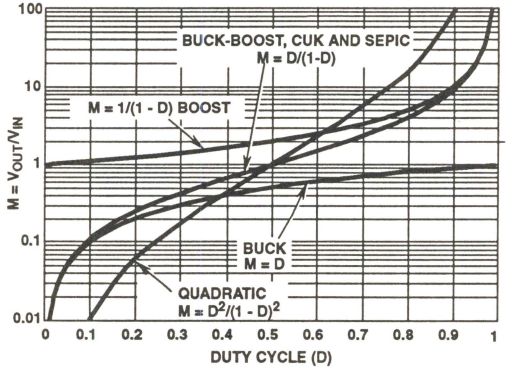


FIGURE 43. VOLTAGE TRANSFER AS A FUNCTION OF DUTY CYCLE FOR VARIOUS TOPOLOGIES

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HARRIS SEMICONDUCTOR

HIP5062

Power Control IC
Single Chip Dual Switching Power Supply

April 1994

Features

- Two Current Mode Control Regulators
- Two 60V, 5A On-chip DMOS Transistors
- Thermal Protection
- Over-Voltage Protection
- Over-Current Protection
- 1MHz Operation or External Clock
- Synchronization Output
- On-Chip Reference Voltage - 5.1V
- Output Rise and Fall Times ~ 3ns
- Designed for 26V to 42V Operation

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters

Description

The HIP5062 is a complete power control IC, incorporating two high power DMOS transistors, CMOS logic and two low level analog control circuits on the same Intelligent Power IC. Both the standard "Boost" and the "SEPIC" (Single-Ended Primary Inductance Converter) power supply topologies are easily implemented with this single control IC.

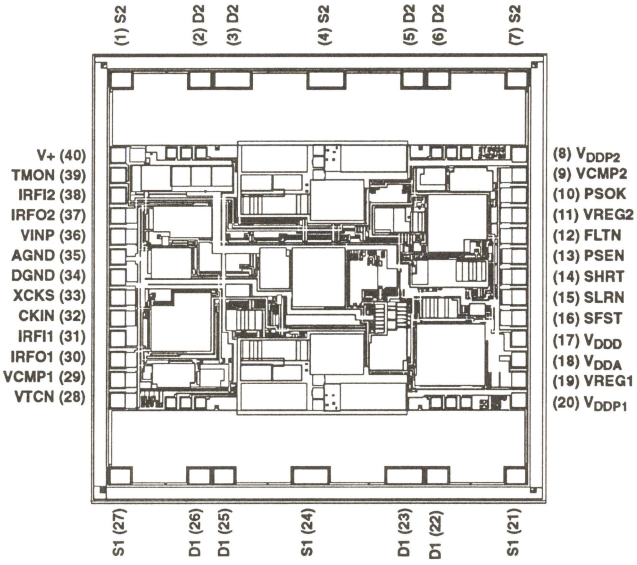
Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Moreover, over-temperature and over-voltage detection circuitry is incorporated within the IC to monitor the chip temperature and the actual power supply output voltage. These circuits can disable the drive to the power transistor to protect both the transistor and, most importantly, the load from over-voltage.

As a result of the power DMOS transistor's current and voltage capability (5A and 60V), multiple output power supplies with total output power capability up to 100W are possible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5062DY	0°C to +85°C	40 Pad Chip
HIP5062DW	0°C to +85°C	Wafer

Chip



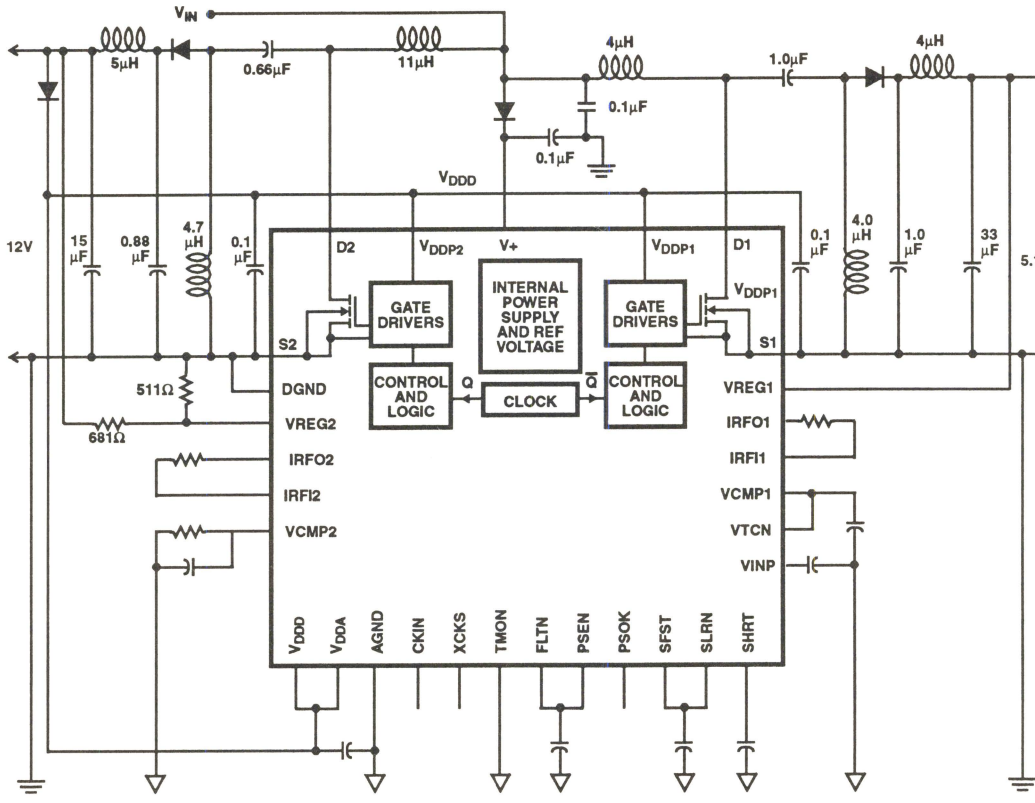
175 mils x 175 mils (4.44mm x 4.44mm)

7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3208.1

Simplified Block Diagram



TYPICAL SEPIC CONFIGURATION

Absolute Maximum Ratings

DC Supply Voltage, V+ ..... -0.3V to 42V
DMOS Drain Voltage ..... -0.3V to 60V
DMOS Drain Current 10A
DC Logic Supply ..... -0.3V to 16V
Output Voltage, Logic Outputs ..... -0.3V to 16V
Input Voltage, Analog and Logic ..... -0.3V to 16V
Operating Junction Temperature Range ..... 0°C to +110°C
Storage Temperature Range ..... -55°C to +150°C

Thermal Information

Thermal Resistance (θ_{JC})
(Solder Mounted to 0.050" Thick Copper Heat Sink) ..... 3°C/W Max
Maximum Junction Temperature ..... +110°C
(Controlled By Thermal Shutdown Circuit)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 36V, Channels 1 and 2, T_J = 0°C to +110°C; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I+	Supply Current	V+ = 42V, PSEN = 12V	-	24.7	30	mA
V_{DDA}	Internal Regulator Output Voltage	V+ = 30V to 42V, I_{OUT} = 0mA	11.7	-	13.3	V
		V+ = 30V to 42V, I_{OUT} = 30mA	11.5	-	13.3	V
		SLRN = 12V, I_{OUT} = 0mA	11.5	-	13.3	V
VINP	Reference Voltage	VDDA = SLRN = 12V, I_{VINP} = 0mA	5.01	5.1	5.19	V
R_{VINP}	VINP Resistance	VINP = 0	-	900	-	Ω
ERROR AMPLIFIERS						
$\lvert V_{IO} \rvert$	Input Offset Voltage (REG - VINP)	I_{VCMP} = 0mA	-	-	10	mV
R_{IN} VREG	Input Resistance to GND	VREG = 5.1V	39	-	85	kΩ
g_m (VREG)	VREG Transconductance (I_{VCMP}/(VREG - VINP)	VCMP = 1V to 8V, SFST = 11V	15	30	50	mS
g_m (SFST)	SFST Transconductance I_{VCMP}/(VREG - SFST)	V_{SFST} < 4.9V	0.8	-	6	mS
I_{VCMP}	Maximum Source Current	VREG = 4.95V, VCMP = 8V	-2.5	-	-0.75	mA
	Maximum Sink Current	VREG = 5.25V, VCMP = 0.4V	0.75	-	2.5	mA
OVTH	Over-Voltage Threshold	Voltage at VREG for FLTN to be latched	6.05	-	6.5	V
CLOCK						
fq	Internal Clock Frequency	XCKS = 12V, V_{DDD} = 12V	0.9	1.0	1.1	MHz
V_{TH} CKIN	External Clock Input Threshold Voltages		33	-	66	%V_{DDD}
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 2.5A, V_{DDD} = 11V, T_J = +25°C	-	-	0.22	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	µA
CURRENT CONTROLED PWM						

Electrical Specifications V+ = 36V, Channels 1 and 2, T_J = 0°C to +110°C; Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\|V_{IO}\|$ VCMP	Buffer Offset Voltage (VCOMP - V_{IFRO})	IFRO = 0mA to -5mA, VTCN = 0.2V to 7.6V, VCMP2 = 0.2V to 7.6V	-	-	125	mV
V_{TH} IFRO	Voltage at IRFO that disables PWM. This is due to low load current		116	-	250	mV
I_{TH} IFRO	Voltage at IRFO to enable SHRT output current. This is due to Regulator Over Current Conditions		6.85	-	7.65	V
I_{SHRT}	SHRT Output Current, During Over-Current	V_{IRFO} = 7.7V	-75	-	-33	µA
V_{TH} SHRT	Threshold voltage on SHRT to set FLTN latch	V_{DDD} = 11V	-	5	-	V
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	2.0	-	3.2	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{IRFI} = 2mA	150	-	360	Ω
t_{RS}	Current Comparator Response Time (Note 1)	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/µs	-	30	-	ns
MCPW	Minimum Controllable Pulse Width (Note 1)		25	50	100	ns
MCPI	Minimum Controllable DMOS Peak Current (Note 1)		125	250	500	mA
START-UP						
V+	Rising V+ Power-On Reset Voltage		23	-	26.3	V
	Falling V+ Power-Off Set Voltage		-	15	-	V
	V+ Power-On Hysteresis		9.5	-	11.8	V
V_{TH} PSEN	Voltage at PSEN to Enable Supply	V_{DDD} = 11V	3.6	-	6.5	V
r_{PSEN}	Internal Pull-Up Resistance, to V_{DDD}		-	12	-	KΩ
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 0V to 11V	-1.5	-1.0	-0.65	µA
I_{PSOK}	PSOK High-State Leakage Current	SFST = 11V, PSOK = 12V	-1	-	1	µA
V_{PSOK}	PSOK Low-State Voltage	SFST = 0V, I_{PSOK} = 1mA	-	-	0.4	V
V_{TH} SFST	PSOK Threshold, Rising V_{SFST}	V_{DDD} = 11V	8.1	-	9.9	V
THERMAL MONITOR						
TEMP	Substrate Temperature for Thermal Monitor to Trip (Note 1)	TMON = 0V	105	-	135	°C

NOTE:

1. Determined by design, not a measured parameter.

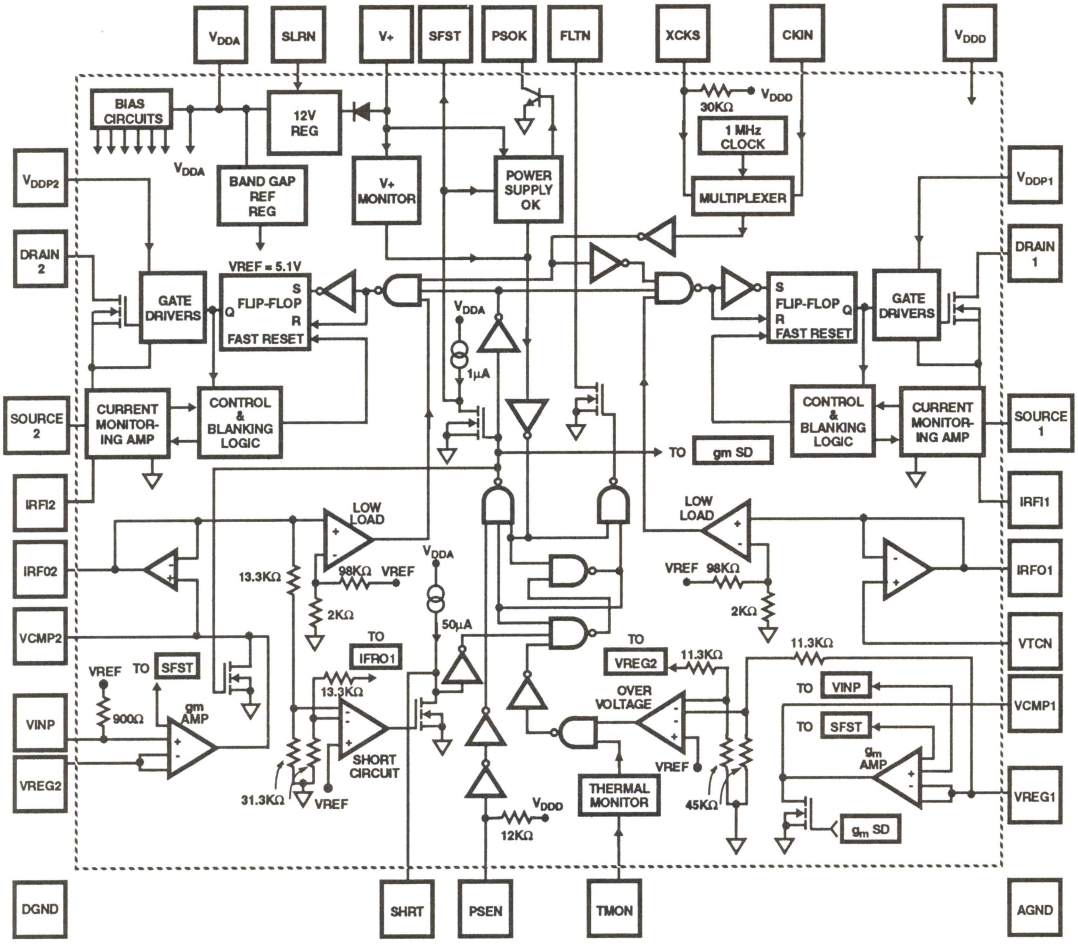
Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1, 4, 7	S2	Source pads for the channel 2 regulator.
2, 3, 5, 6	D2	Drain pads for the channel 2 regulator.
8	V_{DDP2}	This pad is the power input for the channel 2 DMOS gate driver and also is used to decouple the high current pulses to the output driver transistors. The decoupling capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
9	VCMP2	Output of the second channel transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
10	PSOK	This pad provides delayed positive indication when both supplies are enabled.
11	VREG2	Input to the transconductance error amplifier. The other common input for both amplifiers is VINP, Pad 36.
12	FLTN	This is an open drain output that remains low when V+ is too low for proper operation. This node and PSEN are useful in multiple converter configurations. This pad will be latched low when over-temperature, over-voltage or over-current is experienced. V+ must be powered down to reset.
13	PSEN	This terminal is provided to activate the converter. When the input is low, the DMOS drivers are disabled. There is an internal 12K pull-up resistor on this terminal.
14	SHRT	50µA is internally applied to this node when there is an over-current condition.
15	SLRN	Control input to internal regulator that is used during the "start-up" of the supply. In normal operation this terminal starts at 0V and shuts down the internal regulator at approximately 9V. This pad is usually connected to SFST, pad 16.
16	SFST	Controls the rate of rise of both output voltages. Time is determined by an internal 1µA current source and an external capacitor.
17	V_{DDD}	Voltage input for the chip's digital circuits. This pad also allows decoupling of this supply.
18	V_{DDA}	This is the analog supply and internal 12V regulator output usually used only during the start-up sequence. The internal regulator reduced to a nominal 9.2V when SLRN is returned to 12V. Output current capability is 30mA at both voltages.
19	VREG1	Input to channel one transconductance error amplifier. The other, common input for both amplifiers is VINP, pad 36.
20	V_{DDP1}	This pad is the power input for the channel 1 DMOS gate driver and also is used to decouple the high current pulses to the output driver transistors. The decoupling capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
22, 23, 25, 26	D1	Drain pads for the channel 1 regulator.
21, 24, 27	S1	Source pads for the channel 1 regulator.
28	VTCN	Input to transconductance amplifier buffer for channel 1 only. Normally connected to VCMP1, pad 29.
29	VCMP1	Output of the first channel transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
30	IRFO1	A resistor placed between this pad and IRFI1 converts the VCMP1 signal to a current for the current sense comparator. The maximum current is set by the value of the resistor, according to the equation: $I_{PEAK} = 16/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 8.8A. This assumes VCMP1 is 7.3V. Maximum output current should be kept below 10A.

Pin Descriptions (Continued)

PAD NUMBER	DESIGNATION	DESCRIPTION
31	IRFI1	See IRFO1.
32	CKIN	Clock input when XCKS is grounded.
33	XCKS	Grounding this terminal provides for the application of an external clock to CKIN input terminal. For normal internal clock operation, this terminal may be left floating or returned to 12V. There is an internal 30K pull-up resistor on this terminal.
34	DGND	Ground of the DMOS gate drivers. This pad is used for bypassing.
35	AGND	Analog ground.
36	VINP	Internal 5.1V reference. This point is usually bypassed.
37	IRFO2	A resistor placed between this pad and IRFI2 converts the VCMP2 signal to a current for the current sense comparator. The maximum current set by the value of the resistor, according to the equation: $I_{PEAK} = 16/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 8.8A. This assumes VCMP2 is 7.3V. Maximum output current should be kept below 10A.
38	IRFI2	See IRFO2.
39	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to V_{DDA} or 12V the function is disabled. Returning this pad to ground will put the IC into the thermal shutdown state. Thermal shutdown occurs at a nominal junction temperature or +120°C. This terminal is normally returned to ground.
40	V+	This is the main supply voltage input pad to the regulator IC. Because of the high peak currents this pad must be well bypassed with at least a 0.1µF capacitor.

Functional Block Diagram



HARRIS SEMICONDUCTOR

HIP5063

Power Control IC
Single Chip Power Supply

April 1994

Features

- Single Chip Current Mode Control IC
- 60V, 10A On-chip DMOS Transistor
- Thermal Protection
- 1MHz Operation - External Clock
- Output Rise and Fall Times ~ 3ns
- Simple Implementation of High-Speed Current Mode Controlled Regulators and Power Amplifiers
- Designed for 10V to 45V Operation

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters
- Wideband Power Amplifiers for Motor Control

Description

The HIP5063 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC.

This IC allows the user maximum flexibility in implementing high frequency current controlled power supplies and other power sources.

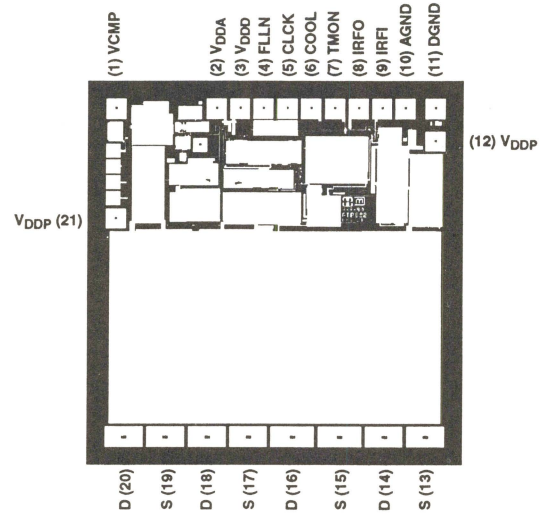
Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Over-temperature detection circuitry is incorporated within the IC to monitor the chip temperature.

As a result of the power DMOS transistor's current and voltage capability (10A and 60V), power supplies with output power capability up to 100 watts are possible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5063DY	0°C to +85°C	21 Pad Chip
HIP5063DW	0°C to +85°C	Wafer

Chip

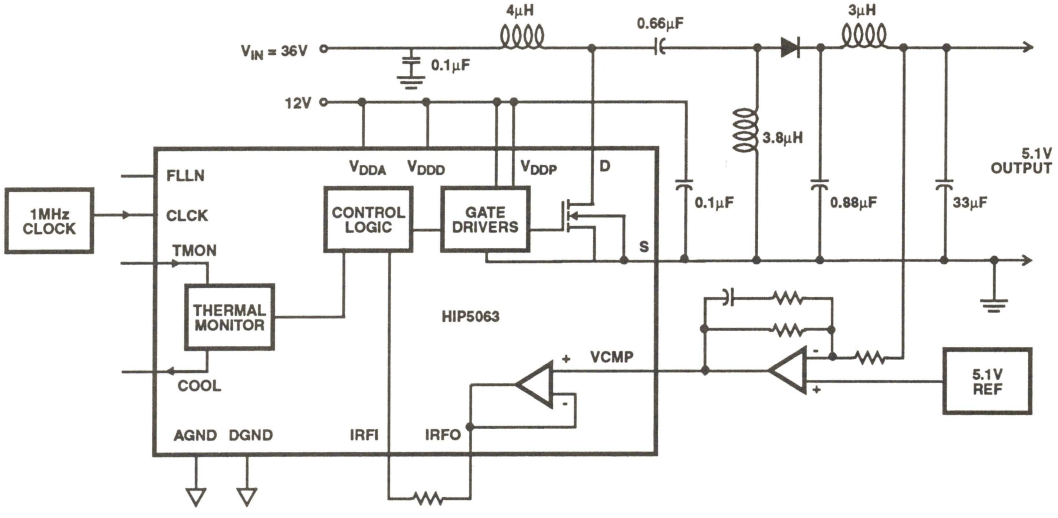


NOTE: Unused pads are for trim and test.
122 mils x 126 mils (3.1mm x 3.2mm)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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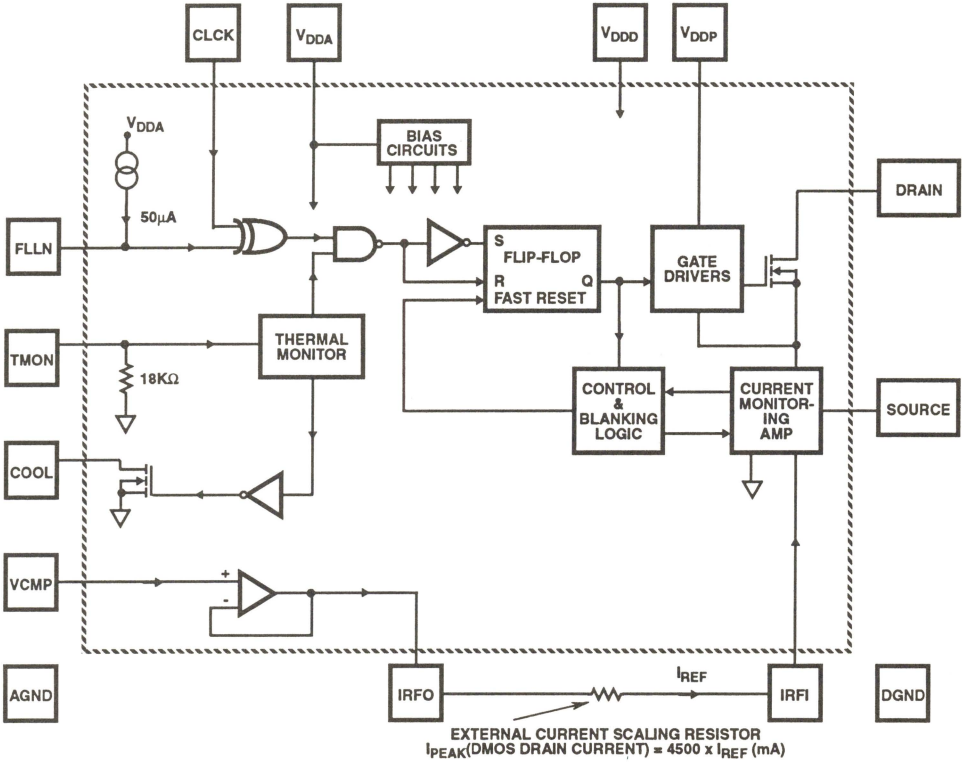
File Number 3209.1

Simplified Block Diagram



TYPICAL SEPIC APPLICATION CONFIGURATION

Functional Block Diagram



Absolute Maximum Ratings

DMOS Drain Voltage ..... -0.3V to 60V
DMOS Drain Current 20A
DC Logic Supply..... -0.3V to 16V
Output Voltage, Logic Outputs ..... -0.3V to 16V
Input Voltage, Analog and Logic..... -0.3V to 16V
Operating Junction Temperature Range..... 0°C to +110°C
Storage Temperature Range ..... -55°C to +150°C

Thermal Information

Thermal Resistance (θ_{JC})
(Solder Mounted to ..... 3°C/W Max
0.050" Thick Copper Heat Sink)
Maximum Junction Temperature..... +110°C
(Controlled By Thermal Shutdown Circuit)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{DDA} = V_{DDD} = V_{DDP} = 12V$, $T_J = 0°C$ to $+110°C$; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I+	Supply Current	External Clock Input = 1MHz	-	14	-	mA
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 5A, $T_J = +25°C$	-	-	0.13	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	µA
CURRENT CONTROLLED PWM						
$\lvert V_{IO} \rvert$ VCMP	Buffer Offset Voltage (VCMP - V_{IRFO})	IRFO = 0mA to -5mA, VCMP = 0.2V to 7.6V	-	-	125	mV
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	3.8	-	4.9	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{RFI} = 2mA	150	-	360	Ω
t_{RS}	Current Comparator Response Time (Note 1)	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/ms	-	30	-	ns
MCPW	Minimum Controllable Pulse Width (Note 1)		25	50	100	ns
MCPI	Minimum Controllable DMOS Peak Current (Note 1)		200	400	800	mA
CLOCK						
V_{TH} CLCK	CLCK Input Threshold Voltage		4	-	8	V
V_{TH} FLLN	FLLN Input Threshold Voltage		4	-	8	V
I_{FLLN}	FLLN Pull-Up Current	VFLLN = 0V	-70	-50	-30	µA
THERMAL MONITOR						
TEMP	Substrate Temperature for Thermal Monitor to Trip (Note 1)	TMON pin open	105	-	135	°C
I_{LEAK} COOL	COOL Leakage Current	V_{COOL} = 12V	-	-	1	µA
V_{COOL}	COOL Low-State Voltage	I_{COOL} = 2mA, $T_J > +125°C$	-	-	0.4	V

NOTE:

1. Determined by design, not a measured parameter.

Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1	VCMP	This is the input terminal from an external error amplifier. A MOS input voltage follower buffers this terminal. The buffer output is the IRFO terminal. The external error amplifier may be either an operational amplifier or a transconductance amplifier like the CA3080. This node may be used for both gain and frequency compensation of the control loop.
2	V_{DDA}	This is the analog supply input. An external 12V supply is required.
3	V_{DDD}	Voltage input for the chip's digital circuits.
4	FLLN	One pad of two clocking terminals. This terminal has an external 50µA pull-up current that allows the terminal to be floated or be left open. With FLLN high, (open or tied to V_{DDD}), the ON cycle will start with the falling edge of the CLCK input. With FLLN low or grounded, the DMOS ON cycle will start on the rising edge of the CLCK input.
5	CLCK	The other clock input pad. An external clock is applied to this terminal. This terminal has no pull-up current or resistance. See FLLN above for phasing information.
6	COOL	Over-temperature indication is provided at this pad. When the chip temperature is below the thermal threshold, the open drain DMOS transistor is in the high impedance state. When the thermal threshold is exceeded, COOL is held low.
7	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to V_{DDA} or 12V the function is disabled. Returning this pad to ground will enable the thermal monitor function. Thermal threshold occurs at a nominal junction temperature of +125°C.
8	IRFO	A resistor placed between this pad and IRFI converts the VCMP signal to a reference current for the current sense comparator. The cycle by cycle peak current is set by the value to this resistor according the the equation: I_{PEAK} = 4500 x VCMP/R. Where I_{PEAK} is in amperes and R is the value of the external resistor in ohms. A maximum VCMP of 8V and a resistor of 1800Ω will keep the drain current below the absolute maximum specification of 20A.
9	IRFI	See IRFO.
10	AGND	Analog ground.
11	DGND	Digital ground.
12 & 21	V_{DDP}	These pads are used to decouple the high current pulses to the output driver transistors. The capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
13, 15, 17, 19	S	Source pads of the DMOS power transistor.
14, 16, 18, 20	D	Drain pads of the DMOS power transistor.

HARRIS SEMICONDUCTOR

HIP5500

High Voltage IC Half Bridge Gate Driver

April 1994

Features

- 500V Maximum Rating
- 2A Peak Gate Drive
- Ability to Interface and Drive N-Channel Power Devices With Complimentary Outputs For Buffered FETs
- Fault Output, Overcurrent Detection and Undervoltage Holdoff
- Over 600kHz Sawtooth Oscillator Frequency
- Adjustable Deadtime Control
- Soft-Start Capability
- Low Current Standby State
- Sleep Mode Reduces Bias Current When Not Enabled

Applications

- Switching and Distributed Power Supplies
- Electronic Lighting Supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5500IP	-40°C to +85°C	20 Lead Plastic DIP
HIP5500IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

Description

The HIP5500, a high voltage integrated circuit (HVIC) half-bridge gate driver for standard power MOSFETs, IGBTs, and the new Harris Buffered MOSFET (RFV10N50BE), can be employed in a wide variety of switching regulator circuits.

The HIP5500 combines the functionality and flexibility of a PWM IC with the convenience of a high voltage half-bridge driver optimized for power supply inverters. It can be used either open-loop or in closed-loop fashion using the SS input for controlling the output waveform duty-cycle.

The HIP5500 incorporates a precision oscillator, adjustable using an external resistor and capacitor. The resistor sets the capacitor charging current and the capacitor sets the integration time of a triangle wave. Another resistor connected to the DIS pin adjusts the dead-time and can be tailored to the application. The oscillator switches at twice the output waveform fundamental frequency. The result is an output waveform whose positive and negative half-cycles are near perfect balance (volt-second equalization).

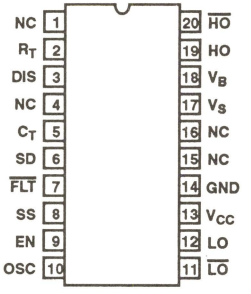
Short-Detect (SD) and Soft-Start (SS) inputs provide alternative means for limiting and regulating respectively the half-bridge output voltage. A capacitor on the SS input will begin charging up once the EN input is made high and causes the duty cycle of each half-cycle to "ramp" the duty cycle of the output waveform.

The SD input can sense a signal proportional to current, providing a means of shortening the conduction periods below that imposed by the SS input.

Other circuits within the HIP5500 "match" upper and lower turn-on and turn-off propagation times in order to minimize flux imbalances when driving output transformer loads.

Pinout

HIP5500 (PDIP, SOIC)
TOP VIEW

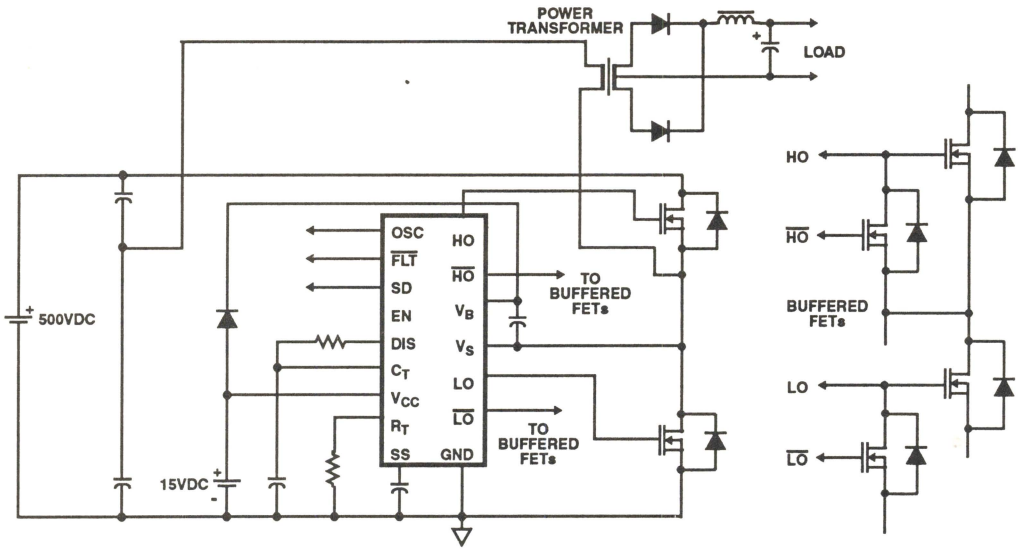


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

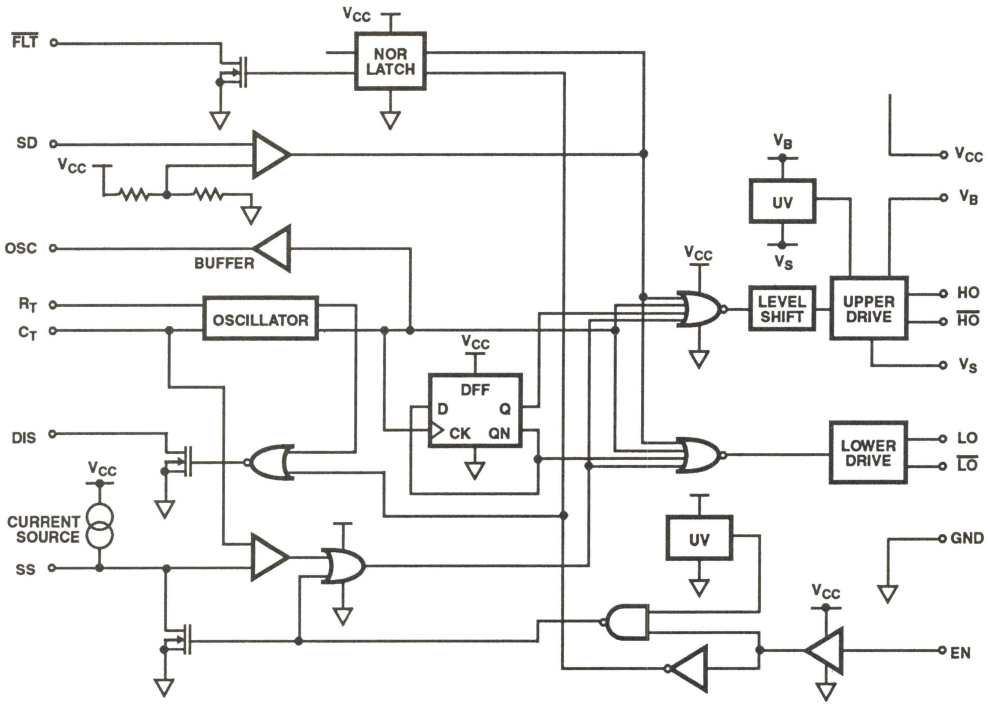
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File Number 3210.2

Typical Application Block Diagram



Functional Block Diagram



Absolute Maximum Ratings

Offset Supply Voltage, V_S ..... $-V_{BS}$ to +500V
Floating Supply Voltage (V_B to V_S) ..... -0.3V to +18V
High Side Channel Output Voltage, V_{HO}, V_{NHO} ... V_S-0.5 to V_B+0.5
Fixed Supply Voltage, V_{CC} ..... -0.5V to +18V
Low Side Channel Output Voltage ..... -0.5V to V_{CC} +0.5V
All Other Pin Voltages
(SD, R_T, C_T, DIS, SS, EN and FLT) ..... -0.5V to V_{CC} +0.5V
Storage Temperature Range ..... -40°C to +150°C
Junction Temperature ..... +125°C
Lead Temperature (Soldering 10s) ..... +300°C
(SOIC - Lead Tips Only)
Offset Supply Maximum dv/dt, dV_S/dt 50V/ns
ESD Classification ..... Class 1

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	75°C/W
Plastic SOIC Package	80°C/W

See Maximum Power Dissipation vs Temperature Curve Figure 21

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions (T_J = -40°C to +125°C Unless Otherwise Noted, All Voltages Referenced to V_{SS})

Offset Supply Voltage, V_S ..... -2.0V to +500V
Floating Supply Voltage, V_{BS} (V_B to V_S) ..... +10V to +15V
High Side Channel Output Voltage, V_{HO},V_{NHO} ..... 0V to V_{BS}
Fixed Supply Voltage, V_{CC} ..... +10V to +15V
Low Side Channel Output Voltage, V_{LO},V_{NLO} ..... 0V to V_{CC}
All Other Pin Voltages (SD, R_T, C_T, DIS, SS, FLT and EN) ... 0V to V_{CC}

Discharge Time Constant ..... 100ns Min
Discharge Resistor Range, R_{DIS} ..... 100kΩ to 50kΩ
Charging Resistor Range, R_T ..... 6.8kΩ to 400kΩ
Oscillator Capacitor Range, C_T ..... 100pF to 0.1μF
Oscillator Frequency Range ..... 300kHz Max
Oscillator Capacitor Charge Current Range, I_{R_T} ..... 21μA to 5mA

Electrical Specifications V_{CC} = V_{BS} = +15V, V_S = GND = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C TO +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Quiescent V_{CC} Current	I_{QCC}		-	5.5	7.0	-	8.0	mA
Quiescent V_{BS} Current	I_{QBS}		-	300	400	-	435	μA
Quiescent Leakage Current	I_{LK}	(V_S - GND) = 5.0V	-	0.4	3.0	-	-	μA
Standby V_{CC} Current	I_{STBY}	R_T = 0	-	2.0	3.5	-	5.0	mA
SS Current Source	$I_{SFT/PWM}$	$^1/_3V_{CC} < V_{SFT} < {}^2/_3V_{CC}$	70	110	145	60	160	μA
Input Threshold	V_{EN}	Low to High Transition	7.5	7.8	8.5	7.4	8.6	V
Input Hysteresis	V_{EN-HYS}		-	2	-	-	-	V
Undervoltage Threshold	V_{UVHL}	High to Low Transition	7.7	8.6	9.5	7.4	9.6	V
Undervoltage Threshold	V_{UVLH}	Low to High Transition	7.9	8.8	9.7	7.6	9.8	V
Undervoltage Hysteresis	V_{UVHYS}		0.08	0.3	0.7	0.05	0.75	V
Short Detect Threshold	V_{THSD}		3.5	4.0	4.5	3.4	4.6	V
C_T/R_T Current Ratio	I_{CTRAT}	I_{R_T} = 100μA, $V_{CC}/3 < V_{CT} < {}^2/_3V_{CC}$	0.9	1	1.1	0.85	1.15	μA
HO, LO Peak Output Current	I_{OUT}+	Sourcing, LO, HO = GND	1.5	1.95	-	1.0	-	A
HO, LO Peak Output Current	I_{OUT}-	Sinking, LO, HO = V_{CC} = V_{BS}	1.5	2.0	-	1.0	-	A
$\overline{LO}$, $\overline{HO}$ Peak Output Current	I_{BUF}+	Sourcing, $\overline{LO}$, $\overline{HO}$ = Vss	170	250	-	110	-	mA
$\overline{LO}$, $\overline{HO}$ Peak Output Current	I_{BUF}-	Sinking, $\overline{LO}$, $\overline{HO}$ = V_{CC} = V_{BS}	170	230	-	110	-	mA
Soft-Start V_{THRESH}, Low to High	V_TSSHL	C_T = 7.5V	7.5	7.8	8.1	7.4	8.2	V

Electrical Specifications $V_{CC} = V_{BS} = +15V$, V_S = GND = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Soft-Start V_{THRESH}, High to Low	V_TSSLH		7.2	7.5	7.8	7.1	7.9	V
OSC Input Upper Threshold	V_TCTLH		9.8	10.4	11.0	9.7	11.1	V
OSC Input Upper Threshold	V_TCTHL	C_T to DIS	5.0	5.6	6.2	4.9	6.3	V
Oscillator Upper to Lower Threshold Difference	VCTDIF	V_TCTLH - V_TCTHL	4.5	4.8	5.1	4.4	5.2	V
OSC_OUT R_{DS}ON, Sinking	OSCR_{DS}L	I_{OSC_OUT} = -50mA	5	8.5	12	2	17	Ω
OSC_OUT R_{DS}ON, Sourcing	OSCR_DH	I_{OSC_OUT} = 50mA	14	19	30	9	40	Ω
DIS Output On Resistance	R_{DS}DIS	I_{DIS} = 10mA	75	115	150	-	200	Ω
$\overline{FLT}$ Output On Resistance	R_{DS}FLT	I_{FLT} = 5mA	100	165	230	40	320	Ω

Dynamic Electrical Specifications $V_{CC} = V_{BS} = +15V$, GND = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO $+125°C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Turn-On Rise Time, HO, LO	t_{DR}	C_L = 2000pF	-	-	50	-	-	ns
Turn-Off Fall Time, HO, LO	t_{DF}	C_L = 2000pF	-	-	50	-	-	ns
Turn-On Rise Time, $\overline{HO}$, $\overline{LO}$	t_{DNR}	C_{BUF} = 200pF	-	25	35	-	-	ns
Turn-Off Fall Time, $\overline{HO}$, $\overline{LO}$	t_{DNF}	C_{BUF} = 200pF	-	25	35	-	-	ns
C_T Fall to LO/HO Rise	T_PCTLH	$C_T = V_T$CTHL LO/HO LOAD = 200pF	-	475	700	-	925	ns
C_T Rise to LO/HO Fall	T_PCTHL	$C_T = V_T$CTLH LO/HO LOAD = 200pF	-	475	700	-	925	ns
LO-HO Prop Delay Mismatch	Delmatch	T_PCTLH and T_PCTHL	-	60	-	-	-	ns
C_T Rise to DIS Fall	T_PCTDISHL	$C_T = V_T$CTHL	-	300	450	-	475	ns
C_T Fall to DIS Rise	T_PCTDISLH	$C_T = V_T$CTLH	-	600	800	-	825	ns
Minimum Dead Time	t_{DTMIN}		-	200	-	-	-	ns
Short Detect Propagation Delay	$t_{SDLO/HO}$	SD = V_{THSD}, LO/HO = 200pF	-	425	850	-	1100	ns
Soft-Start Propagation Delay Time	t_{SSDLY}	SS = V_TSSLH, LO/HO = 200pF	-	500	750	-	775	ns

Typical Performance Curves

All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified

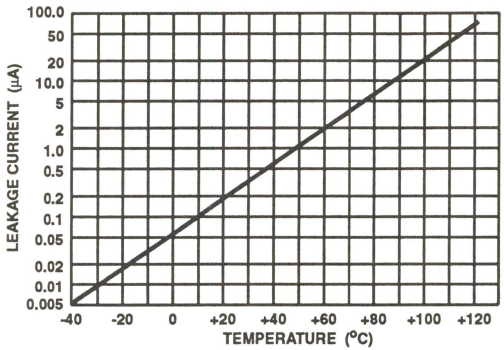


FIGURE 1. OFFSET SUPPLY LEAKAGE CURRENT vs TEMPERATURE AT 300VDC

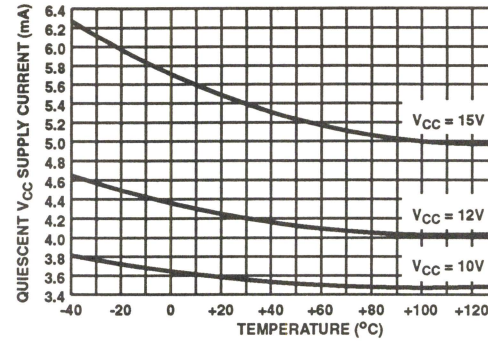


FIGURE 2. QUIESCENT V_{CC} CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

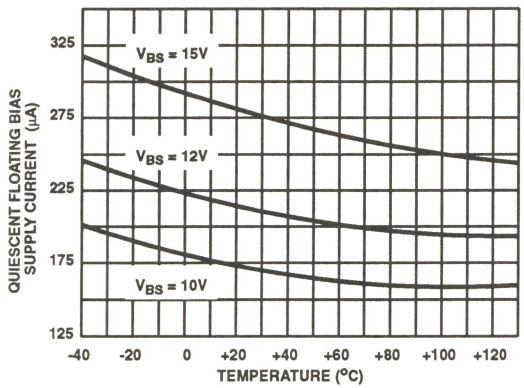


FIGURE 3. QUIESCENT FLOATING BIAS SUPPLY CURRENT vs TEMPERATURE AND V_{BS} SUPPLY VOLTAGE

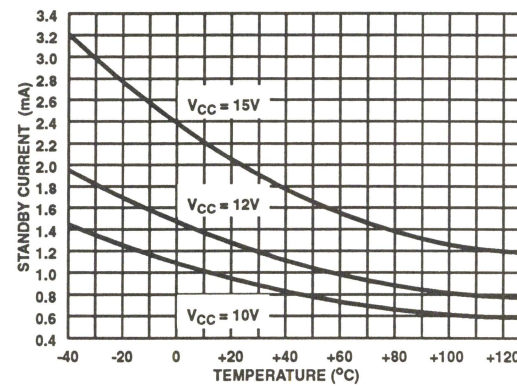


FIGURE 4. QUIESCENT STANDBY CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

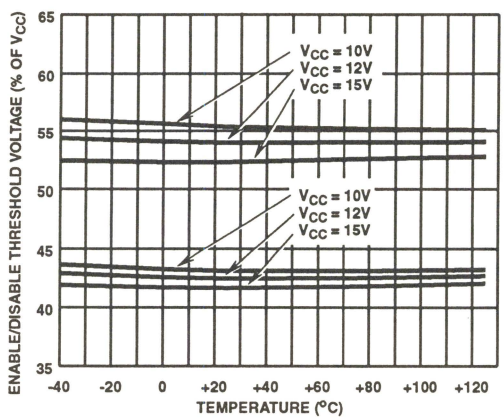


FIGURE 5. ENABLE/DISABLE THRESHOLD (PERCENT V_{CC}) vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

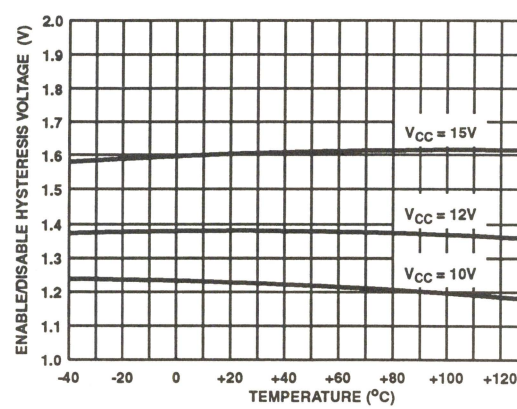


FIGURE 6. ENABLE/DISABLE HYSTERESIS VOLTAGE TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

Typical Performance Curves All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified (Continued)

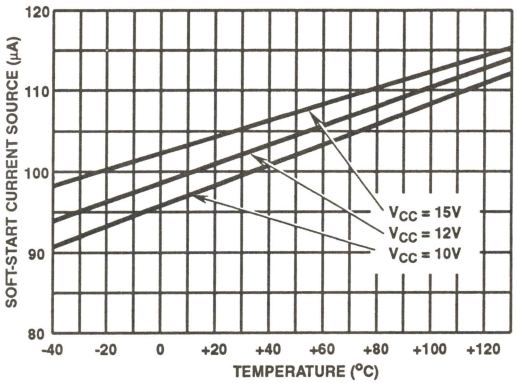


FIGURE 7. SOFT-START CURRENT SOURCE CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

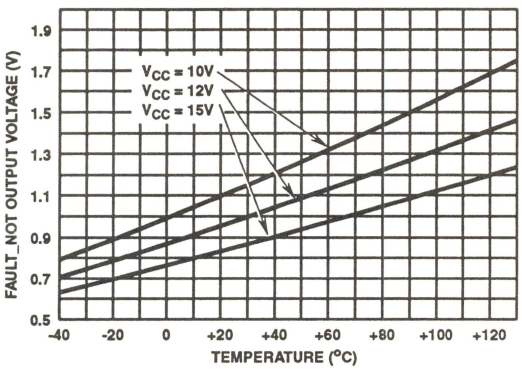


FIGURE 8. FAULT_NOT LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE, SINKING 5mA

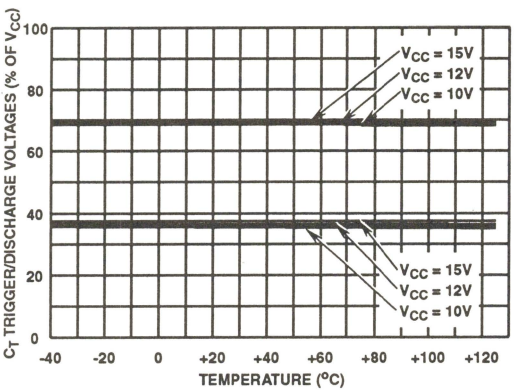


FIGURE 9. C_T RAMP TRIGGER AND DISCHARGE VOLTAGE TRIP POINT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

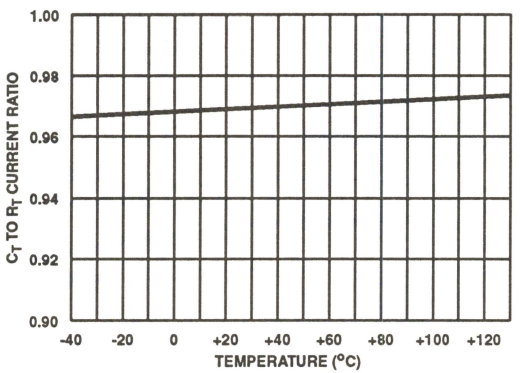


FIGURE 10. C_T TO R_T CURRENT SOURCE RATIO vs TEMPERATURE

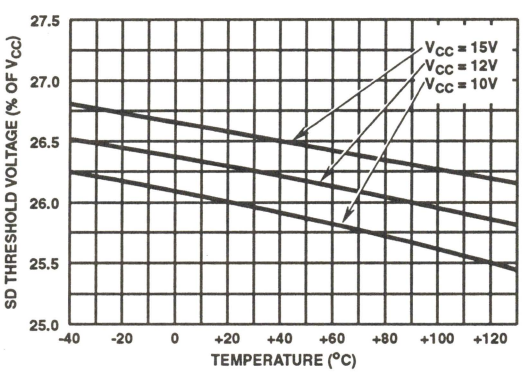


FIGURE 11. SHUTDOWN THRESHOLD VOLTAGE (% OF V_{CC}) vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

Typical Performance Curves All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified (Continued)

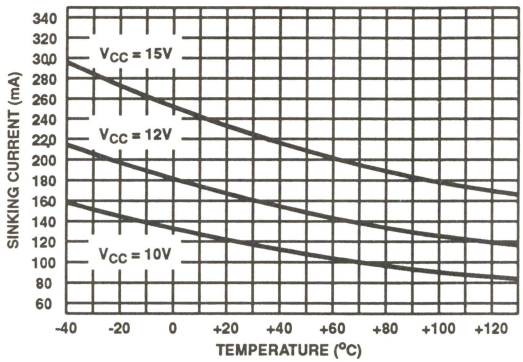


FIGURE 12. BUFFER GATE OUTPUT SHORT CIRCUIT SINKING CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

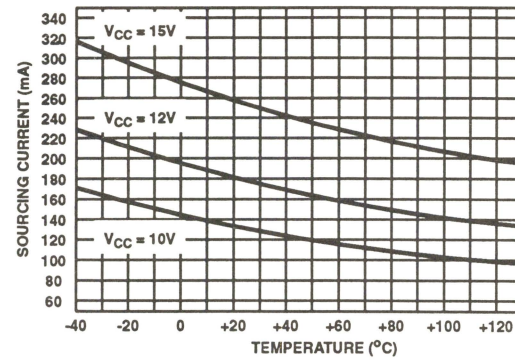


FIGURE 13. BUFFER GATE OUTPUT SHORT CIRCUIT SOURCING CURRENT vs TEMPERATURE AND V_{CC} SUPPLY VOLTAGE

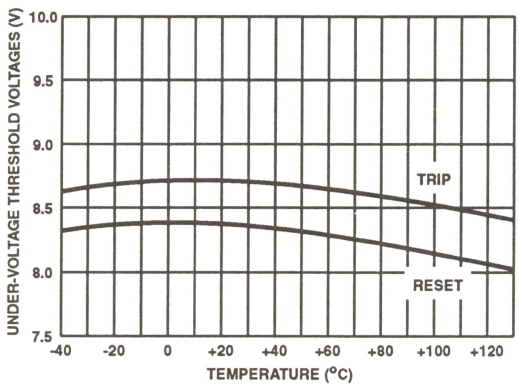


FIGURE 14. LOW-SIDE UNDERVOLTAGE THRESHOLD VOLTAGE (TRIP/RESET) vs TEMPERATURE

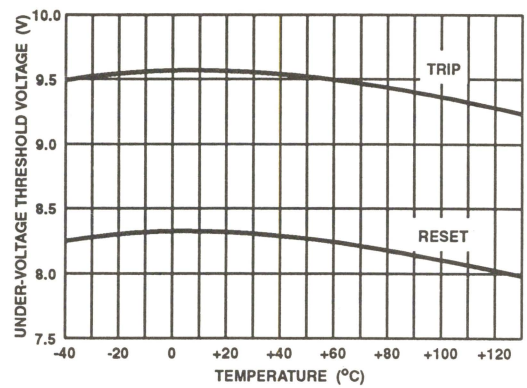


FIGURE 15. HIGH-SIDE UNDERVOLTAGE THRESHOLD VOLTAGE(TRIP/RESET) vs TEMPERATURE

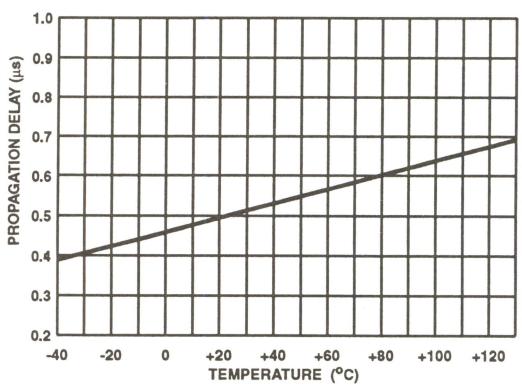


FIGURE 16. PROPAGATION DELAY, C_T TO GATE OUTPUTS vs TEMPERATURE AT V_{CC} = +15V

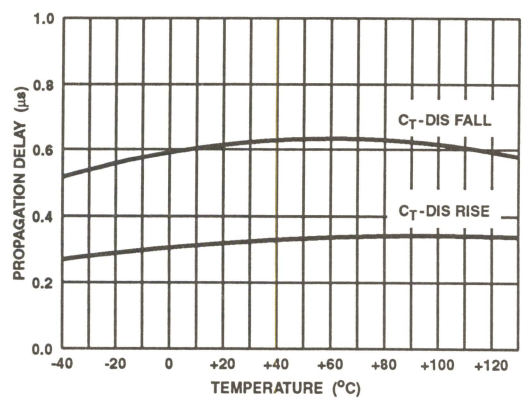


FIGURE 17. PROPAGATION DELAY, C_T TO DIS vs TEMPERATURE AT V_{CC} = +15V

Typical Performance Curves All Curves are V_{CC} = +15V, T_A = +25°C, Unless Otherwise Specified (Continued)

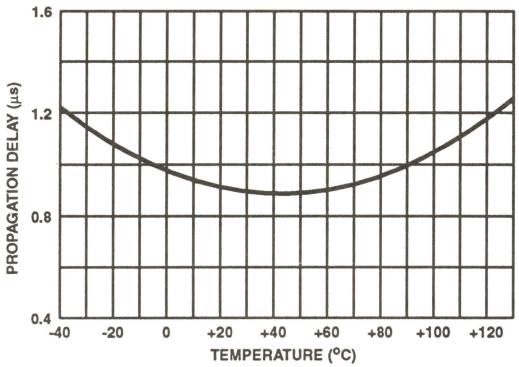


FIGURE 18. PROPAGATION DELAY, SS TO LO GATE RISING vs TEMPERATURE AT V_{CC} = +15V

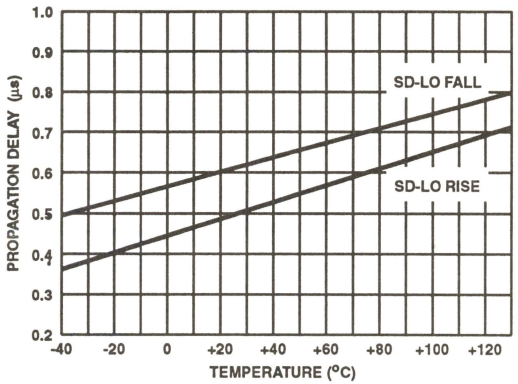


FIGURE 19. PROPAGATION DELAYS, SD TO LO GATE RISE/FALL vs TEMPERATURE AT V_{CC} = +15V

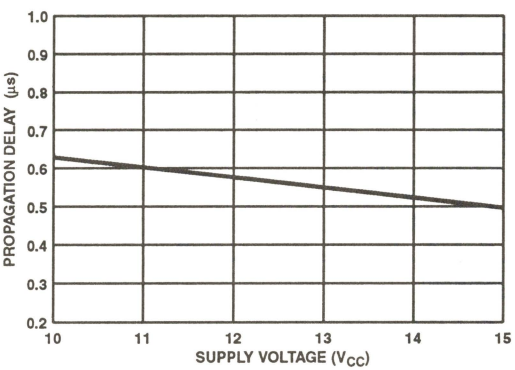


FIGURE 20. PROPAGATION DELAY, C_T TO GATE OUT vs SUPPLY VOLTAGE, V_{CC} AT +25°C FOR RISING AND FALLING GATE OUTPUTS

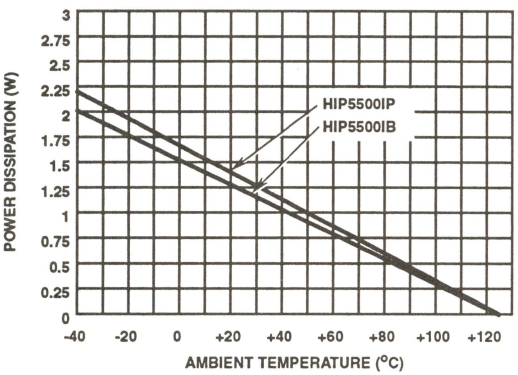


FIGURE 21. MAXIMUM POWER DISSIPATION vs TEMPERATURE

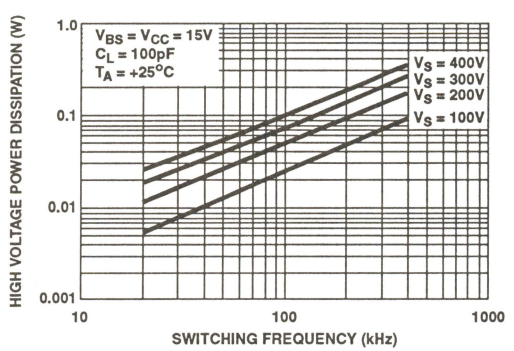
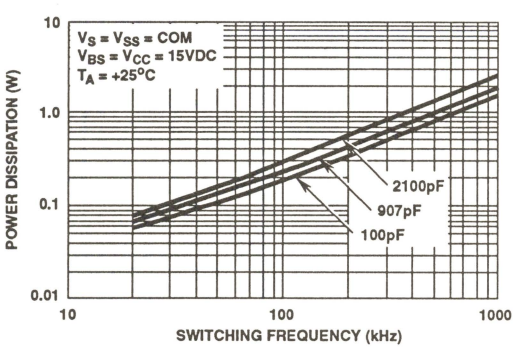


FIGURE 22. HIGH VOLTAGE POWER DISSIPATION vs SWITCHING FREQUENCY



NOTE: All switching losses assumed to be in IC.

FIGURE 23. LOW VOLTAGE POWER DISSIPATION vs FREQUENCY

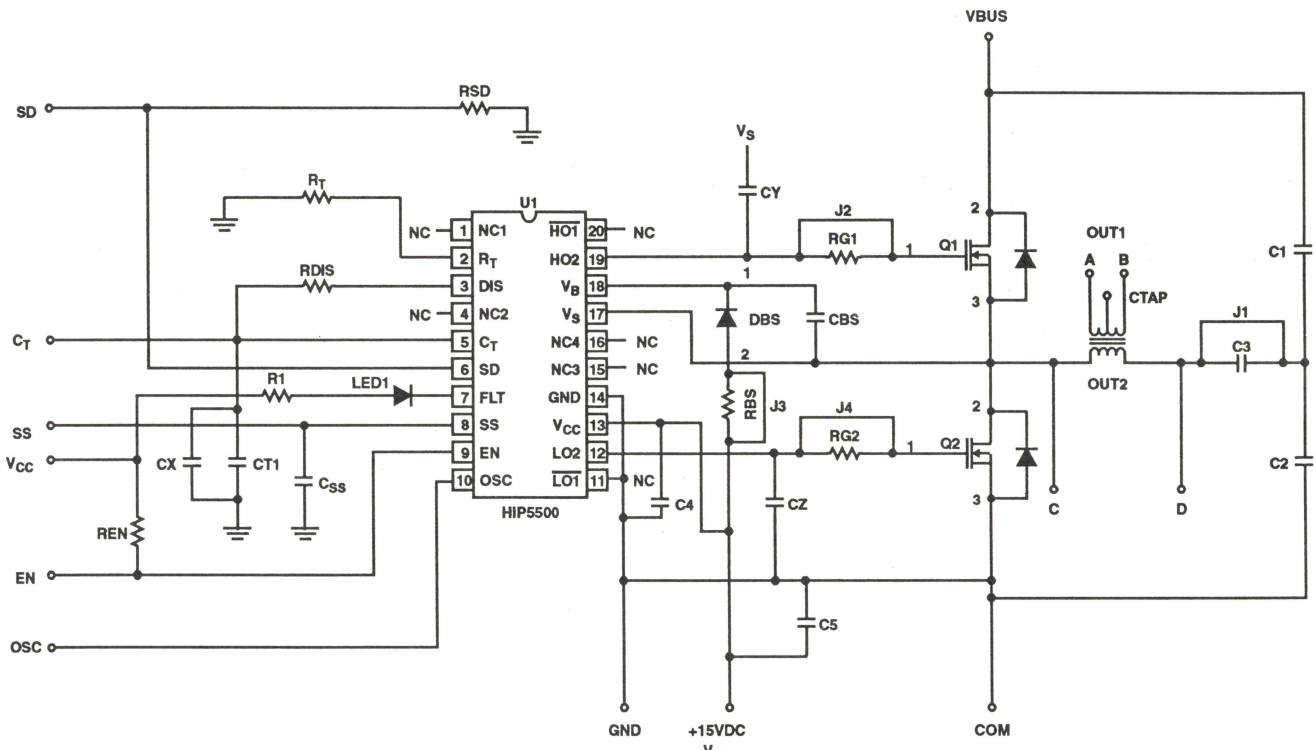


FIGURE 24. EVALUATION BOARD SCHEMATIC

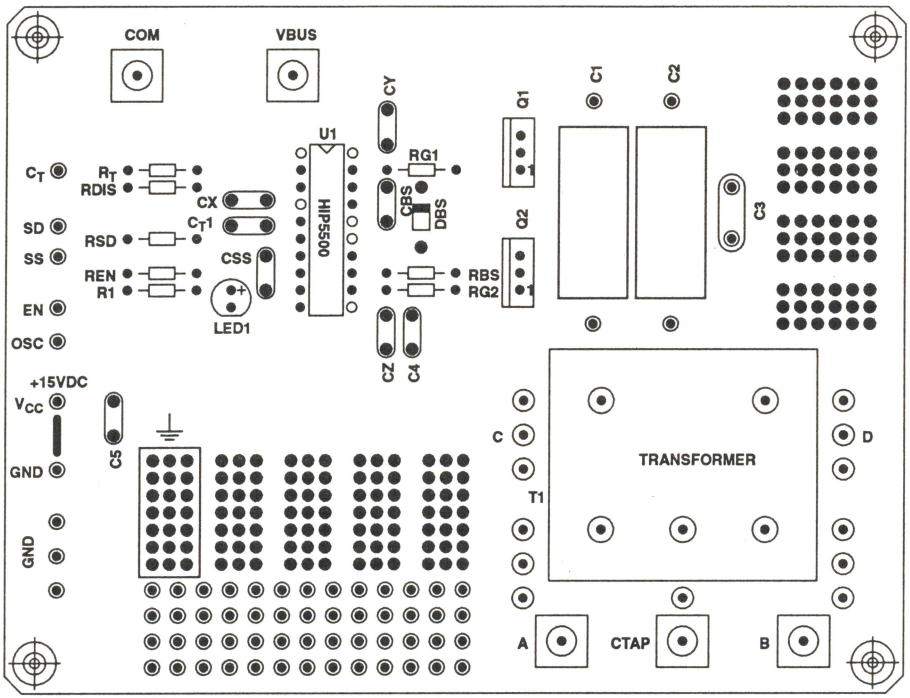


FIGURE 25. HIP5500 EVALUATION BOARD SILKSCREEN

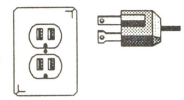
HARRIS SEMICONDUCTOR

HIP5600

Thermally Protected High Voltage Linear Regulator

April 1994

Features



- Operates from 50VDC to 400VDC
- Operates from 50VRMS to 280VRMS Line
- UL Recognized
- Variable DC Output Voltage 1.2VDC to V_{IN} - 50V
- Internal Thermal Shutdown Protection
- Internal Over Current Protection
- Up to 40mA Peak Output Current
- Surge Rated to ±650V; Meets IEEE/ANSI C62.41.1980 with Additional MOV

Applications

- Switch Mode Power Supply Start-Up
- Electronically Commutated Motor Housekeeping Supply
- Power Supply for Simple Industrial/Commercial/Consumer Equipment Controls
- Off-Line (Buck) Switch Mode Power Supply

CAUTION: This product does not provide isolation from AC line.

Ordering Information

PART NUMBER	CASE TEMP. RANGE	PACKAGE
HIP5600IS	-40°C to +100°C	3 Lead Plastic SIP
HIP5600IB	-40°C to +100°C	8 Lead Plastic SOIC

Description

The HIP5600 is an adjustable 3-terminal positive linear voltage regulator capable of operating up to either 400VDC or 280VRMS. The output voltage is adjustable from 1.2VDC to within 50V of the peak input voltage with two external resistors. This high voltage linear regulator is capable of sourcing 1mA to 30mA with proper heat sinking. The HIP5600 can also provide 40mA peak (typical) for short periods of time.

Protection is provided by the on chip thermal shutdown and output current limiting circuitry. The HIP5600 has a unique advantage over other high voltage linear regulators due to its ability to withstand input to output voltages as high as 400V(peak), a condition that could exist under output short circuit conditions.

Common linear regulator configurations can be implemented as well as AC/DC conversion and start-up circuits for switch mode power supplies.

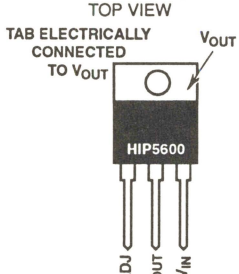
The HIP5600 requires a minimum output capacitor of 10µF for stability of the output and may require a 0.02µF input decoupling capacitor depending on the source impedance. It also requires a minimum load current of 1mA to maintain output voltage regulation.

All protection circuitry remains fully functional even if the adjustment terminal is disconnected. However, if this happens the output voltage will approach the input voltage.

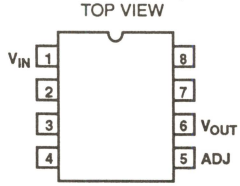
NOTE: Unless otherwise noted, information pertains to the TO-220 package.

Pinouts

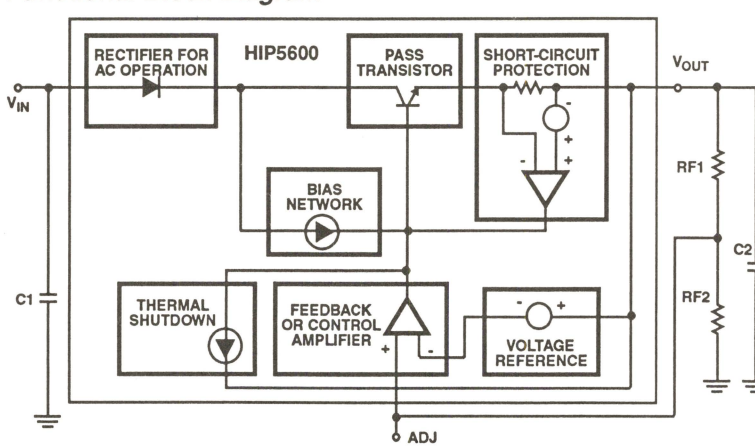
HIP5600 (SIP)
TOP VIEW



HIP5600 (SOIC)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3270.4**

Absolute Maximum Ratings

Input to Output Voltage, Continuous . . . . . +480V to -550V
Input to Output Voltage, Peak (Non Repetitive, 2ms) . . . . . ±650V
Junction Temperature . . . . . +150°C
ADJ to Output, Voltage to ADJ . . . . . ±5V
Storage Temperature Range . . . . . -65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic SIP Package	60°C/W	4°C/W
Plastic SOIC Package	170°C/W	-

Lead Temperature (Soldering 10s) . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . 80VRMS to 280VRMS or 50VDC to 400VDC

Operating Temperature Range . . . . . -40°C to +100°C (Case)

Electrical Specifications

Conditions V_{IN} = 400VDC, I_L = 1mA, C_L = 10µF, V_{ADJ} = 3.79V, V_{OUT} = 5V (Unless Otherwise Specified) Temperature = Case Temperature.

PARAMETER	CONDITION	TEMP	MIN	TYP	MAX	UNITS
INPUT						
Input Voltage	DC	Full	50	-	400	V
Max Peak Input Voltage	Non-Repetitive (2ms)	Full	-	-	±650	V
Input Frequency (Note 1)		Full	DC	-	1000	Hz
Bias Current (I_{BIAS} Note 2)		Full	0.4	0.5	0.6	mA
REFERENCE						
I_{ADJ}		+25°C	50	65	80	µA
$I_{ADJ}T_C$ (Note 1)	I_L = 1mA	Full	-	+0.15	-	µA/°C
$I_{ADJ\ LOAD\ REG}$ (Note 1)	I_L = 1mA to 10mA	+25°C	-	-215	-	nA/mA
V_{REF} (Note 3)		+25°C	1.07	1.18	1.30	V
V_{REF} T_C (Note 1)	I_L = 1mA	Full	-	-460	-	µV/°C
Line Regulation $V_{REF\ LINE\ REG}$	50VDC to 400VDC	+25°C	-	9	14.5	µV/V
		Full	-	9	29	µV/V
Load Regulation $V_{REF\ LOAD\ REG}$	I_{OUT} = 1mA to 10mA	+25°C	-	3	5	mV/mA
		Full	-	3	6	mV/mA
PROTECTION CIRCUITS						
Output Short Circuit Current Limit	V_{IN} = 50V	+25°C	35	-	45	mA
Thermal Shutdown T_{TS} (IC surface, not case temperature. Note 1)	V_{IN} = 400V	-	127	134	142	°C
Thermal Shutdown Hysteresis (Note 1)	V_{IN} = 400V	-	-	34	-	°C

NOTES:

1. Characterized not tested
2. Bias current ≡ input current with output pin floating.
3. $V_{REF} = V_{OUT} - V_{ADJ}$

Schematic Diagram

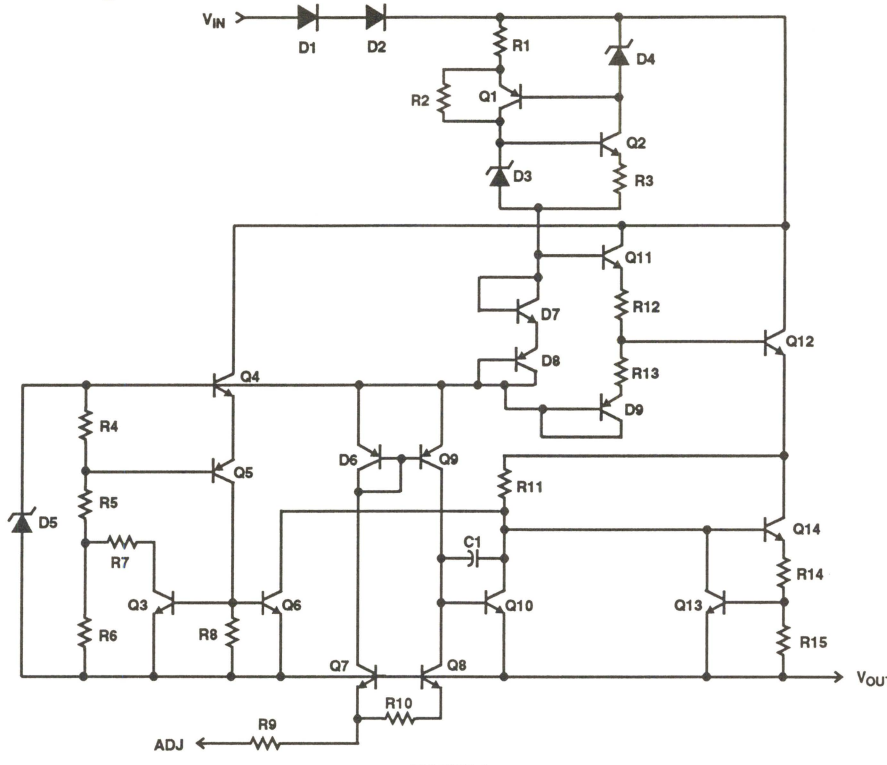


FIGURE 1.

Application Information

Introduction

In many electronic systems the components operate at 3V to 15V but the system obtains power from a high voltage source (AC or DC). When the current requirements are small, less than 10mA, a linear regulator may be the best supply provided that it is easy to design in, reliable, low cost and compact. The HIP5600 is similar to other 3 terminal regulators but operates from much higher voltages. It protects its load from surges +250V above its 400V operating input voltage and has short circuit current limiting and thermal shutdown self protection features.

Output Voltage

The HIP5600 provides a temperature independent 1.18V reference, V_{REF}, between the output and the adjustment terminal ($V_{REF} = V_{OUT} - V_{ADJ}$). This constant reference voltage is impressed across RF1 (see Figure 2) and results in a constant current (I_1) that flows through RF2 to ground. The voltage across RF2 is the product of its resistance and the sum of I_1 and I_{ADJ}. The output voltage is given in equations 1(A, B).

$$V_{OUT} = (V_{REF})\frac{RF1 + RF2}{RF1} + I_{ADJ}(RF2) \qquad \text{EQ 1(A)}$$

$$V_{OUT} = (1.18) \times \frac{RF1 + RF2}{RF1} + 65\mu A\,(RF2) \qquad \text{EQ 1(B)}$$

Error Budget

$$\Delta V_{OUT} = \Delta V^{T}_{REF}\left(\frac{RF1 + RF2}{RF1}\right) + \Delta I^{T}_{ADJ}RF2 + I_{ADJ}RF2\frac{\Delta RF2}{RF2} + V_{REF}\left(\frac{RF2}{RF1}\right)\left(\frac{\Delta RF2}{RF2} - \frac{\Delta RF1}{RF1}\right) \qquad \text{EQ 2(A)}$$

Where;

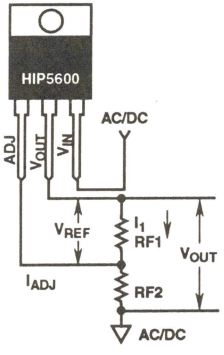
$$\Delta V^{T}_{REF} \equiv \Delta V_{REF} + V_{REF_{LOADREG}}(\Delta I_{OUT}) + V_{REF}{}^{TC}(\Delta Temp) + V_{REF}{}^{TC}(\theta_{SA})\Delta (I_{OUT} \cdot V_{IN}) + V_{REF_{LINEREG}} \qquad \text{EQ 2(B)}$$

$$\Delta I^{T}_{ADJ} \equiv \Delta I_{ADJ} + I_{ADJ_{LOADREG}}(\Delta I_{OUT}) + I_{ADJ}{}^{TC}(\Delta Temp) + I_{ADJ}{}^{TC}(\theta_{SA})\Delta (I_{OUT} \cdot V_{IN}) \qquad \text{EQ 2(C)}$$

Note:

$\frac{\Delta RFx}{RFx}$ = % tolerance of resistor x

Equations 2(A,B,C) are provided to determine the worst case output voltage in relation to; manufacturing tolerances (ΔV_{REF} and ΔI_{REF}),% tolerance in external resistors (ΔRF1/RF1, ΔRF2/RF2), load regulation ($V_{REF\ LOAD\ REG}$, $I_{ADJ\ LOAD\ REG}$), line regulation ($V_{REF\ LINE\ REG}$) and the effects of temperature ($V_{REF}TC$, $I_{REF}TC$), which includes self heating (θ_{SA}).

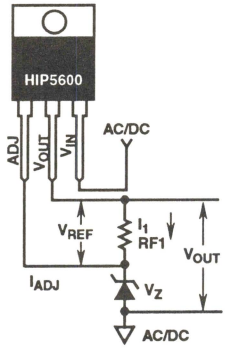


$V_{OUT(NOMINAL)}$	RF1	RF2
3.3V	3.6k	5.6k
4.9V	2.7k	7.5k
12.0V	1.8k	15k
14.8V	1.1k	12k

FIGURE 2.

Example: Given: V_{IN} = 200VDC, V_{OUT} = 15V, I_{OUT} = 2mA to 12mA, θ_{SA} = 10°C/W, RF1 = 1.1kΩ 5% low, RF2 = 12kΩ 5% high, ΔI_{OUT} equals 10mA and ΔTemp equals +60°C (ambient temperature +25°C to +85°C). The worst case ΔV_{OUT} for the given conditions is -1.13V. The shift in V_{OUT} is attributed to the following: -1.55V manufacturing tolerances, +1.33V external resistors, -0.62V load regulation and -0.29V temperature effects.

Regulator With Zener



$V_{OUT} = 1.18 + V_Z$

V_{OUT}	V_Z
3.7V	2.5V
5.1V	3.9V
10.3V	9.1V
12.2V	11V
16.2V	15V

RF1 = 10k

FIGURE 3.

The output voltage can be set by using a zener diode (Figure 3) instead of the resistor divider shown in Figure 2. The zener diode improves the ripple rejection ratio and reduces the value of the worst case output voltage, as illustrated in the example to follow. The bias current of the zener diode is set by the value of RF1 and I_{ADJ}.

The regulator / zener diode becomes an attractive solution if ripple rejection or the worst case tolerance of the output voltage is critical (i.e. one zener diode cost less than one 10µF capacitor (C3) and one 1/4W resistor RF2). Minimum power dissipation is possible by reducing I_1 current, with little effect on the output voltage regulation. The output voltage is given in Equation 3.

$$V_{OUT} = V_{REF} + V_Z \qquad \text{EQ (3)}$$

Error Budget

$$\Delta V_{OUT} = \Delta V^T_{REF} + \Delta V^T_Z \qquad \text{EQ 4(A)}$$

$$\Delta V^T_{REF} \equiv \Delta V_{REF} + V_{REF_{LOADREG}}(\Delta I_{OUT}) + V_{REF}TC(\Delta\ Temp)$$

$$+V_{REF}TC(\theta_{SA})\Delta(I_{OUT} \cdot V_{IN}) + V_{REF_{LINEREG}} \qquad \text{EQ 4(B)}$$

$$\Delta V^T_Z \equiv V_{Z\,tolerance}(V_Z) + V_Z TC(\Delta\ Temp) \qquad \text{EQ 4(C)}$$

Equations 4(A,B,C) are provided to determine the worst case output voltage in relation to; manufacturing tolerances of HIP5600 and the zener diode (ΔV_{REF} and ΔV_Z), load regulation of the HIP5600 ($V_{REF\ LOAD\ REG}$), and the effects of temperature on the HIP5600 and the zener diode ($V_{REF}TC$, $V_Z TC$).

Example: Given: V_{IN} = 200V, V_{OUT} = 14.18V (V_{REF} = 1.18V, V_Z = 13V), ΔV_Z = 5%, $V_Z TC$ = +0.079%/°C (assumes 1N5243BPH), ΔI_{OUT} equal 10mA and ΔTemp equal +60°C. The worst case ΔV_{OUT} is 0.4956V. The shift in V_{OUT} is attributed to the following: -0.2 (HIP5600) and 0.69 (zener diode).

The regulator/zener diode configuration gives a 3.5% (0.49/14.18) worst case output voltage error where, for the same conditions, the regulator/resistor configuration results in an 7.5% (1.129/15) worst case output voltage error.

External Capacitors

A minimum10µF output capacitor (C2) is required for stability of the output stage. Any increase of the load capacitance greater than 10µF will merely improve the loop stability and output impedance.

A 0.02µF input decoupling capacitor (C1) between V_{IN} and ground may be required if the power source impedance is not sufficiently low for the 1MHz - 10MHz band. Without this capacitor, the HIP5600 can oscillate at 2.5MHz when driven by a power source with a high impedance for the 1MHz - 10MHz band.

An optional bypass capacitor (C3) from V_{ADJ} to ground improves the ripple rejection by preventing the ripple at the Adjust pin from being amplified. Bypass capacitors larger than 10µF do not appreciably improve the ripple rejection of the part (see Figure 21 through Figure 26).

Load Regulation

For improved load regulation, resistor RF1 (connected between the adjustment terminal and V_{OUT}) should be tied directly to the output of the regulator (Figure 4A) rather than near the load Figure 4B. This eliminates line drops (R_S) from appearing effectively in series with RF1 and degrading regulation. For example, a 15V regulator with a 0.05Ω resistance

between the regulator and the load will have a load regulation due to line resistance of $0.05\Omega \times \Delta I_L$. If RF1 is connected near the load the effective load regulation will be 11.9 times worse (1+R2/R1, where R2 = 12k, R1 = 1.1k).

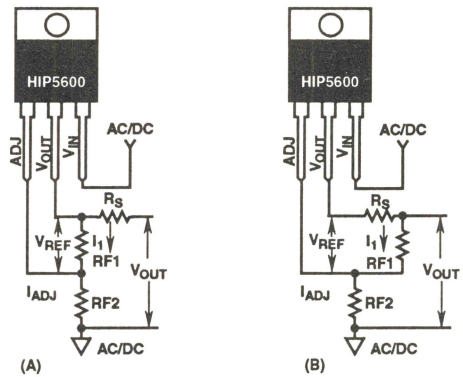


FIGURE 4.

Protection Diodes

The HIP5600, unlike other voltage regulators, is internally protected by input diodes in the event the input becomes shorted to ground. Therefore, **no** external protection diode is required between the input pin and the output pin to protect against the output capacitor (C2) discharging through the input to ground.

If the output is shorted in the absence of D1 (Figure 5), the bypass capacitor voltage (C3) could exceed the absolute maximum voltage rating of ±5V between V_{OUT} and V_{IN}. Note; No protection diode (D1) is needed for output voltages less than 6V or if C3 is not used.

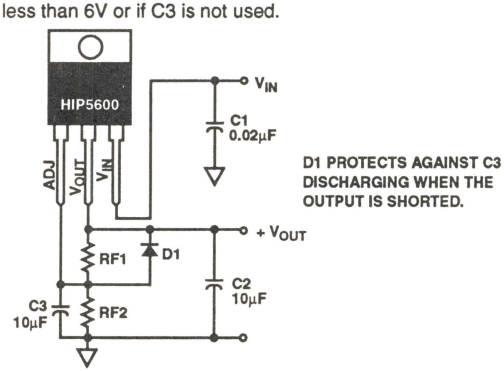


FIGURE 5. REGULATOR WITH PROTECTION DIODE

Selecting the Right Heat Sink

Linear power supplies can dissipate a lot of power. This power or heat must be safely dissipated to permit continuous operation. This section will discuss thermal resistance and show how to calculate heat sink requirements.

Electronic heat sinks are generally rated by their thermal resistance. Thermal resistance is defined as the temperature rise per unit of heat transfer or power dissipated, and is expressed in units of degrees centigrade per watt. For a particular application determine the thermal resistance (θ_{SA}) which the heat sink must have in order to maintain a junction temperature below the thermal shut down limit (T_{TS}).

A thermal network that describes the heat flow from the integrated circuit to the ambient air is shown in Figure 6. The basic relation for thermal resistance from the IC surface, historically called "junction", to ambient (θ_{JA}) is given in Equation 5. The thermal resistance of the heat sink (θ_{SA}) to maintain a desired junction temperature is calculated using Equation 6.

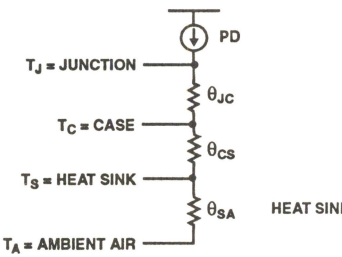


FIGURE 6.

$$\theta_{JA} = \frac{T_J - T_A}{P}\left(\frac{°C}{W}\right) \qquad \text{EQ (5)}$$

Where:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad \text{and} \quad T_J = T_{TS}$$

$$\therefore$$

$$\theta_{SA} + \theta_{CS} \approx \theta_{SA} = \frac{T_{TS} - T_A}{P} - \theta_{JC} \qquad \text{EQ (6)}$$

Where:

θ_{JA} = (Junction to Ambient Thermal Resistance) The sum of the thermal resistances of the heat flow path.
$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$

T_J = (Junction Temperature) The desired maximum junction temperature of the part. $T_J = T_{TS}$

T_{TS} = (Thermal Shutdown Temperature) The maximum junction temperature that is set by the thermal protection circuitry of the HIP5600
(min = +127°C, typ = +134°C and max = +142°C).

θ_{JC} = (Junction to Case Thermal Resistance) Describes the thermal resistance from the IC surface to its case.
$\theta_{JC} = 4.8°C/W$

θ_{CS} = (Case to Mounting Surface Thermal Resistance) The resistance of the mounting interface between the transistor case and the heat sink.
For example, mica washer.

θ_{SA} = (Mounting Surface to Ambient Thermal Resistance) The resistance of the heat sink to the ambient air. Varies with air flow.

T_A = Ambient Temperature

P = The power dissipated by the HIP5600 in watts.
$P = (V_{IN} - V_{OUT})(I_{OUT})$

Worst case θ_{SA} is calculated using the minimum T_{TS} of +127°C in Equation 6.

Example,

Given: V_{IN} = 400VDC V_{OUT} = 15V I_{LOAD} = 15mA

θ_{JC} = 4.8°C/W T_{TS} = +127°C I_{ADJ} = 80µA

T_A = +50°C RF1 = 1.1k

V_{REF} = 1.18V P = 6.2W = $(V_{IN} - V_{OUT})(I_{IN})$

$$I_{IN} \equiv I_{ADJ} + \frac{V_{REF}}{RF1} + I_{LOAD}$$

Find: Proper heat sink to keep the junction temperature of the HIP5600 from exceeding T_{TS} (+127°C).

Solution: Use Equation 6,

$$\theta_{SA} = \frac{T_{TS} - T_A}{P} - \theta_{JC} \qquad \text{EQ (7)}$$

$$\theta_{SA} = \frac{127°C - 50°C}{6.2} - 4.8°C = 7.62\frac{°C}{W} \qquad \text{EQ (8)}$$

The selection of a heat sink with θ_{SA} less than +7.62°C/W would ensure that the junction temperature would not exceed the thermal shut down temperature (T_{TS}) of +127°C. A Thermalloy P/N7023 at 6.2W power dissipation would meet this requirement with a θ_{SA} of +5.7°C/W.

Operation Without A Heatsink

The TO-220 package has a θ_{JA} of +60°C/W. This allows 0.7W power dissipation at +85°C in still air. Mounting the HIP5600 to a printed circuit board (see Figure 40 through Figure 42) decreases the thermal impedance sufficiently to allow about 1.6W of power dissipation at +85°C in still air.

Thermal Transient Operation (TO-220 Package)

For applications such as start-up, the HIP5600 in the TO-220 package can operate at several watts **-without a heat sink-** for a period of time before going into thermal shutdown.

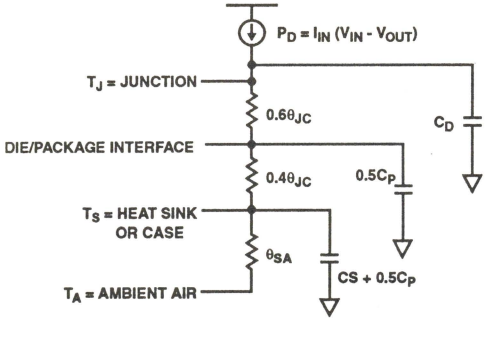


FIGURE 7. THERMAL CAPACITANCE MODEL OF HIP5600

Figure 7 shows the thermal capacitances of the TO-220 package, the integrated circuit and the heat sink, if used.

When power is initially applied, the mass of the package absorbs heat which limits the rate of temperature rise of the junction. With no heat sink C_S equals zero and θ_{SA} equals the difference between θ_{JA} and θ_{JC}. The following equations predict the transient junction temperature and the time to thermal shutdown for ambient temperatures up to +85°C and power levels up to 8W. The output current limit temperature coefficient (Figure 39) precludes continuous operation above 8W.

$$T_J(t) = T_A + P\theta_{JC} + P\theta_{SA}\left(1 - e^{\frac{-t}{\tau}}\right) \qquad \text{EQ (9)}$$

Where:

$$\tau \equiv \theta_{SA}(C_P + C_S)$$

$$t = -\tau \ln\left(\frac{P(\theta_{JC} + \theta_{SA}) + T_A - T_{TS}}{P\theta_{SA}}\right) \qquad \text{EQ (10)}$$

For the TO-220, C_P is 0.9Ws to 1.1Ws per degree compared to about 2.6mWs per degree for the integrated circuit and C_S is 0.9Ws per degree per gram for aluminum heat sinks.

Figure 8 shows the time to thermal shutdown versus power dissipation for a part in +22°C still air and at various elevated ambient temperatures with a θ_{SA} of +27°C/W from forced air flow.

For the shorter shutdown times, the θ_{SA} value is not important but the thermal capacitances are. A more accurate equation for the transient silicon surface temperature can be derived from the model shown in Figure 7. Due to the distributed nature of the package thermal capacitance, the second time constant is 1.7 times larger than expected.

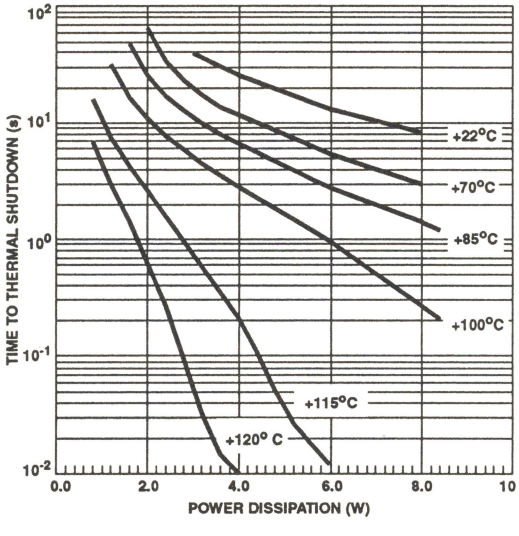


FIGURE 8. TIME TO THERMAL SHUTDOWN vs POWER DISSIPATION (TO-220 PACKAGE ONLY)

$$T_J(t) = T_A + T_1 + T_2 + T_3 \quad \text{(EQ. 11A)}$$

$$T_1 \equiv P\theta_{SA}\left(1 - e^{\frac{-t}{\tau 1}}\right)$$

Where: (EQ. 11B)

$$\tau 1 \equiv \theta_{SA}(C_P + C_S)$$

$$T_2 \equiv 0.4P\theta_{JC}\left(1 - e^{\frac{-t}{\tau 2}}\right) \quad \text{(EQ. 11C)}$$

Where:

$$\tau 2 \equiv 0.7\theta_{JC}\left(\frac{(0.5C_P + C_S)\,0.5C_P}{C_P + C_S}\right)$$

$$T_3 \equiv 0.6P\theta_{JC}\left(1 - e^{\frac{-t}{\tau 3}}\right) \quad \text{(EQ. 11D)}$$

Where:

$$\tau 3 \equiv 0.6\theta_{JC}C_D$$

Thermal Transient Operation (SOIC Package)

Equation (11A) can also be used for the SOIC package provided the following substitutions are made.

$$T_1 \equiv P\theta_1\left(1 - e^{\frac{-t}{\tau 1}}\right) \quad \text{(EQ. 11E)}$$

$$T_2 \equiv P\theta_2\left(1 - e^{\frac{-t}{\tau 2}}\right) \quad \text{(EQ. 11F)}$$

$$T_3 \equiv P\theta_3\left(1 - e^{\frac{-t}{\tau 3}}\right) \quad \text{(EQ. 11G)}$$

where

$\theta_1 = 160^oC/W$ $\tau 1 = 5.8s$

$\theta_1 = 10^oC/W$ $\tau 2 = 86ms$

$\theta_1 = 2.9^oC/W$ $\tau 3 = 7.5ms$

For example, with the SOIC package mounted on a PC board at +85°C in still air, the HIP5600 could dissipate 4W for ~70ms before going into thermal shutdown.

For start-up applications a more useful parameter is the total charge delivered before thermal shutdown.

$$Q_L \approx \frac{(T_{TS} - T_A)}{V_{IN}} C_P \quad \text{(EQ. 12)}$$

C_P is about 35mJ/°C for the SOIC package and about 1000mJ/°C for TO-220.

For example:

with $T_{TS} = +127^oC$, $T_A = +85^oC$

$V_{IN} = 400V$ and $C_P = 35mJ/^oC$

$Q_L \equiv 3670\mu C$

which is enough to charge a 240µF capacitor to 15V.

Thermal Shutdown Hysteresis

Figure 9 shows the HIP5600 thermal hysteresis curve with V_{IN} = 100VDC, V_{OUT} = 5V and I_{OUT} = 10mA. Hysteresis is added to the thermal shutdown circuit to prevent oscillations as the junction temperature approaches the thermal shutdown limit. The thermal shutdown is reset when the input voltage is removed, goes negative (i.e. AC operation) or when the part cools down.

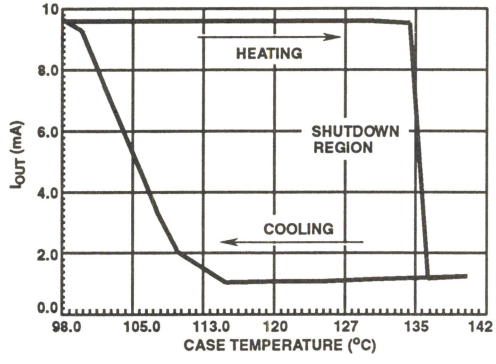


FIGURE 9. THERMAL HYSTERESIS CURVE

AC to DC Operation

Since the HIP5600 has internal high voltage diodes in series with its input, it can be connected directly to an AC power line. This is an improvement over typical low current supplies constructed from a high voltage diode and voltage dropping resistor to bias a low voltage zener. The HIP5600 provides better line and load regulation, better efficiency and heat transfer. The latter because the TO-220 package permits easy heat sinking.

The efficiency of either supply is approximately the DC output voltage divided by the RMS input voltage. The resistor value, in the typical low current supply, is chosen such that for maximum load at minimum line voltage there is some current flowing into the zener. This resistor value results in excess power dissipation for lighter loads or higher line voltages.

Using the circuit in Figure 3 with a 1000µF output capacitor the HIP5600 only takes as much current from the power line as the load requires. For light loads, the HIP5600 is even more efficient due to it's interaction with the output capacitor. Immediately after the AC line goes positive, the HIP5600 tries to replace all the charge drained by the load during the negative half cycle at a rate limited by the short circuit current limit (see "A1" and "B1" Figure 10). Since most of this charge is replaced before the input voltage reaches its RMS value, the power dissipation for this charge is lower than it would be if the charge were transferred at a uniform rate during the cycle. When the product of the input voltage and current is averaged over a cycle, the average power is less than if the input current were constant. Figure 11 shows the HIP5600 efficiency as a function of load current for 80VRMS and 132VRMS inputs for a 15.6V output.

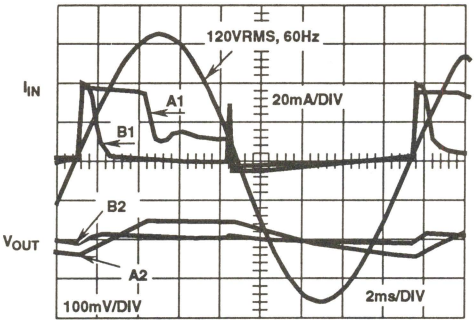


FIGURE 10. AC OPERATION

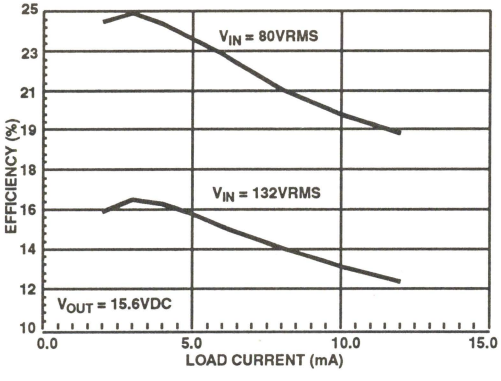


FIGURE 11. EFFICIENCY AS A FUNCTION OF LOAD CURRENT

Referring again to Figure 10, Curve "A1" shows the input current for a 10mA output load and curve "B1" with a 3mA output load. The input current spike just before the negative going zero crossing occurs while the input voltage is less than the minimum operating voltage but is so short it has no detrimental effect. The input current also includes the charging current for the 0.02µF input decoupling capacitor C1.

The maximum load current cannot be greater than 1/2 of the short circuit current because the HIP5600 only conducts over 1/2 of the line cycle. The short circuit current limit (Figure 39) depends on the case temperature, which is a function of the power dissipation. Figure 39 for a case temperature of +100°C (i.e. no heat sink) indicates for AC operation the maximum available output current is 10mA (1/2 x 20mA). Operation from full wave rectified input will increase the maximum output current to 20mA for the same +100°C case temperature.

As a reminder, since the HIP5600 is off during the negative half cycle, the output capacitor must be large enough to supply the maximum load current during this time with some acceptable level of droop. Figure 10 also shows the output ripple voltage, for both a 10mA and 3mA output loads "A2" and "B2", respectively.

Do's And Don'ts

DC Operation

1. Do not exceed the absolute maximum ratings.
2. The HIP5600 requires a minimum output current of 1mA. Minimum output current includes current through RF1. **Warning:** If there is less than 1mA load current, the output voltage will rise. If the possibility of no load exists, RF1 should be sized to sink 1mA under these conditions.

$$RF1_{MIN} = \frac{V_{REF}}{1mA} = \frac{1.07V}{1mA} = 1k\Omega$$

3. Do not "HOT" switch the input voltage without protecting the input voltage from exceeding ±650V. Note: inductance from supplies and wires along with the 0.02µF decoupling capacitor can form an under damped tank circuit that could result in voltages which exceed the maximum ±650V input voltage rating. Switch arcing can further aggravate the effects of the source inductance creating an over voltage condition.

   Recommendation: Adequate protection means (such as MOV, avalanche diode, surgector, etc.) may be needed to clamp transients to within the ±650V input limit of the HIP5600.
4. Do not operate the part with the input voltage below the minimum 50VDC recommended. **Low voltage operation:** For input voltages between 0VDC and +5VDC nothing happens ($I_{OUT} = 0$), for input voltages between +5VDC and +35VDC there is not enough voltage for the pass transistor to operate properly and therefore a high frequency (2MHz) oscillation occurs. For input voltages +35VDC to +50VDC proper operation can occur with some parts.
5. **Warning:** the output voltage will approach the input voltage if the adjust pin is disconnected, resulting in permanent damage to the low voltage output capacitor.

AC Operation

1. Do not exceed the absolute maximum ratings.
2. The HIP5600 requires a minimum output current of 0.5mA. Minimum output current includes current through RF1. **Warning:** If there is less than 0.5mA output current, the output voltage will rise. If the possibility of no load exists, RF1 should be sized to sink 0.5mA under these conditions.

$$RF1_{MIN} = \frac{V_{REF}}{0.5mA} = \frac{1.07V}{0.5mA} = 2k\Omega$$

3. If using a laboratory AC source (such as VARIACs or step-up transformers, etc.) be aware that they contain large inductances that can generate damaging high voltage transients when they are switched on or off.

   Recommendations

   (1) Preset VARIAC output voltage before applying power to part.

   (2) Adequate protection means (such as MOV, avalanche diode, surgector, etc.) may be needed to clamp transients to within the ±650V input limit of the HIP5600.

4. Do not operate the part with the input voltage below the minimum 50VRMS recommended. **Low voltage operation similar to DC operation** (reference step 4 under DC operation).
5. **Warning:** the output voltage will approach the input voltage if the adjust pin is disconnected, resulting in permanent damage to the low voltage output capacitor.

General Precautions

Instrumentation Effects

Background: Input to output parasitic impedances exist in most test equipment power supplies. The inter-winding capacitance of the transformer may result in substantial current flow (mA) from the equipment power lines to the DC ground of the HIP5600. This "ground loop" current can result in erroneous measurements of the circuits performance and in some cases lead to overstress of the HIP5600.

Recommendations for Evaluation of the HIP5600 in the Lab

a) The use of battery powered DVMs and scopes will eliminate ground loops.

b) When connecting test equipment, locate grounds as close to circuit ground as possible.

c) Input current measurements should be made with a non-contact current probe.

If AC powered test equipment is used, then the use of an isolated plug is recommended. The isolated plug eliminates any voltage difference between earth ground and AC ground. However, even though the earth ground is disconnected, ground loop currents can still flow through transformer of the test equipment. Ground loops can be **minimized** by connecting the test equipment ground as close to the circuit ground as possible.

CAUTION: Dangerous voltages may appear on exposed metal surfaces of AC powered test equipment.

Application Circuits

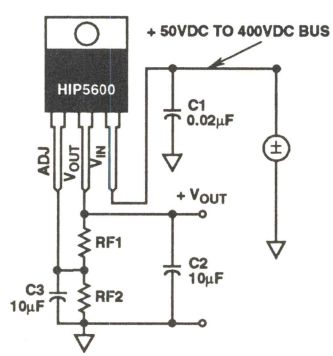


FIGURE 12. DC/DC CONVERTER

The HIP5600 can be configured in most common DC linear regulator applications circuits with an input voltage between 50VDC to 400VDC (above the output voltage) see Figure 12. A 10µF capacitor (C2) provides stabilization of the output stage. Heat sinking may be required depending upon the power dissipation. Normally, choose RF1 << V_{REF}/I_{ADJ}.

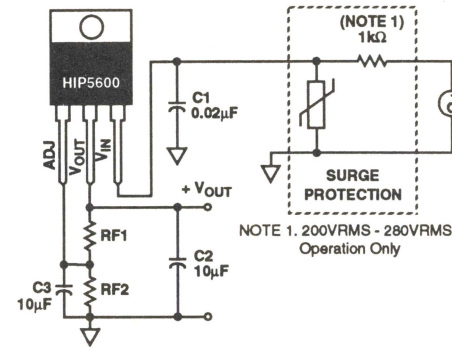


FIGURE 13. AC/DC CONVERTER

The HIP5600 can operate from an AC voltage between 50VRMS to 280VRMS, see Figure 13. The combination of a 1kΩ (2W) input resistor and a V275LA10B MOV provides input surge protection up to 6kV 1.2 x 50µs oscillating and pulse waveforms as defined in IEEE/ANSI C62.41.1980. When operating from 120VAC, a V130LA10B MOV provides protection **without** the 1kΩ resistor.

The output capacitor is larger for operation from AC than DC because the HIP5600 only conducts current during the positive half cycle of the AC line. The efficiency is approximately equal to V_{OUT}/V_{IN} (RMS), see Figure 11.

The HIP5600 provides an efficient and economical solution as a start-up supply for applications operating from either AC (50VRMS to 280VRMS) or DC (50VDC to 400VDC).

The HIP5600 has on chip thermal protection and output current limiting circuitry. These features eliminate the need for an in-line fuse and a large heat sink.

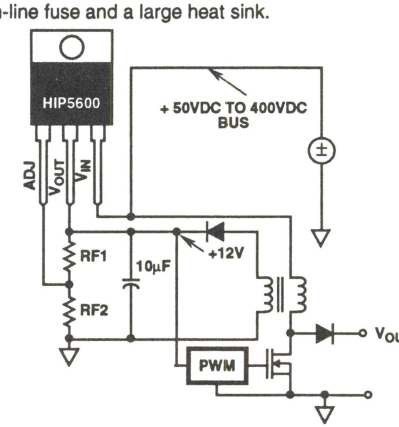


FIGURE 14. START UP CIRCUIT

The HIP5600 can provide up to 40mA for short periods of time to enable start up of a switch mode power supply's control circuit. The length of time that the HIP5600 will be on, prior to thermal shutdown, is a function of the power dissipation in the

part, the amount of heat sinking (if any) and the ambient temperature. For example; at 400VDC with no heat sink, it will provide 20mA for about 8s, see Figure 8.

Power supply efficiency is improved by turning off the HIP5600 when the SMPS is up and running. In this application the output of the HIP5600 would be set via RF1 and RF2 to be about 9V. The tickler winding would be adjusted to about 12V to insure that the HIP5600 is kept off during normal operating conditions.The input current under these conditions is approximately equal to I_{BIAS}. (See Figure 28).

The HIP5600 can supply a 450µA (±20%) constant current. (See Figure 15). It makes use of the internal bias network. See Figure 28 for bias current versus input voltage.

With the addition of a potentiometer and a 10µF capacitor the HIP5600 will provide a constant current source. I_{OUT} is given by Equation 13 in Figure 16.

The HIP5600 can be operated as a self-oscillating buck regulator for increased output currents and circuit efficiencies approaching 75%. The circuit shown (Figure 17) is capable of operating from either DC (50VDC to 400VDC) or AC (90VRMS to 264VRMS) and is optimized for a 24V 150mA output. The output voltage is set by RF1 and RF2 resistor values and is slightly higher than the value predicted in Equation 1A. The frequency of operation for the circuit is around 16kHz.

The circuit shown (Figure 18) is optimized for a 24V 250mA output with a 90VRMS to 132VRMS input. Output short circuit protection is provided by adding a pnp transistor and a small 0.22Ω sense resistor. A snubber circuit was also added to reduce the power dissipation in the P-IGBT. The frequency of operation for the circuit is around 18kHz.

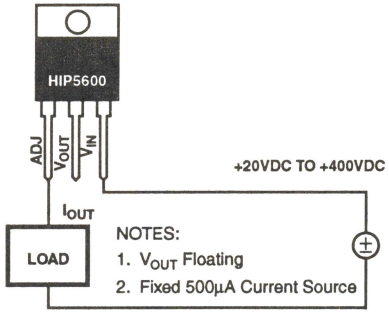
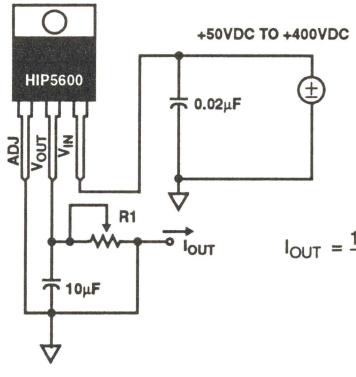


FIGURE 15. CONSTANT 450µA CURRENT SOURCE



$$I_{OUT} = \frac{1.21V}{R1} \quad \text{(EQ. 13)}$$

FIGURE 16. ADJUSTABLE CURRENT SOURCE

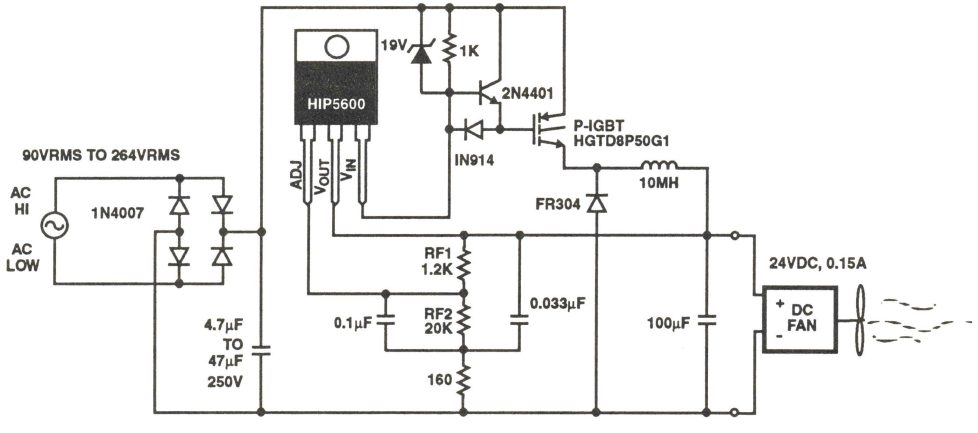


FIGURE 17. HIGH CURRENT "BUCK" REGULATOR

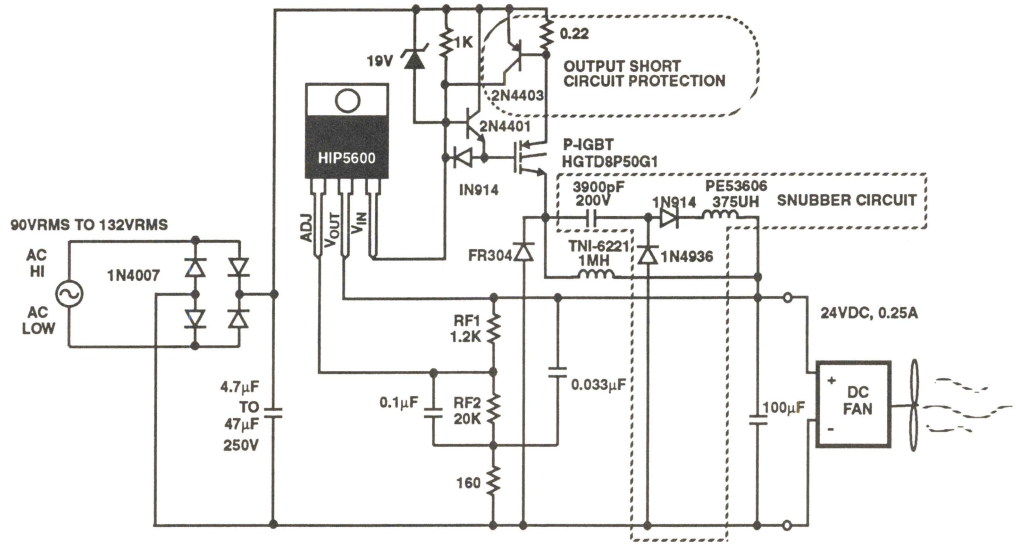


FIGURE 18. HIGH CURRENT "BUCK" REGULATOR WITH OUTPUT SHORT CIRCUIT PROTECTION AND SNUBBER

Typical Performance Curves

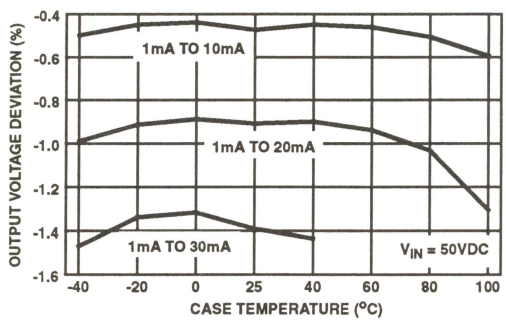


FIGURE 19. LOAD REGULATION vs TEMPERATURE

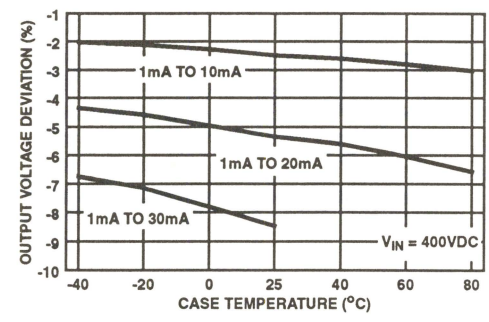


FIGURE 20. LOAD REGULATION VS. TEMPERATURE

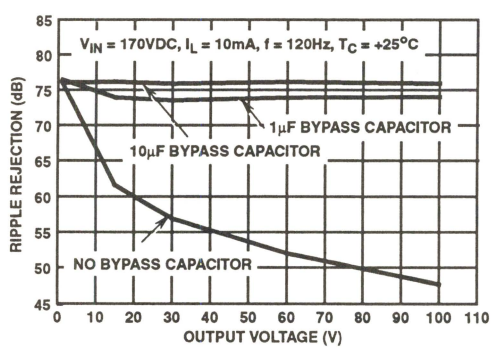


FIGURE 21. RIPPLE REJECTION RATIO (OUTPUT VOLTAGE)

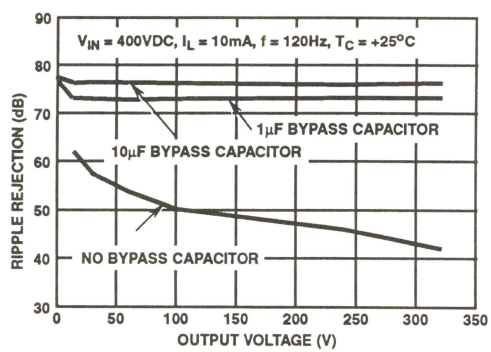


FIGURE 22. RIPPLE REJECTION RATIO (OUTPUT VOLTAGE)

Typical Performance Curves (Continued)

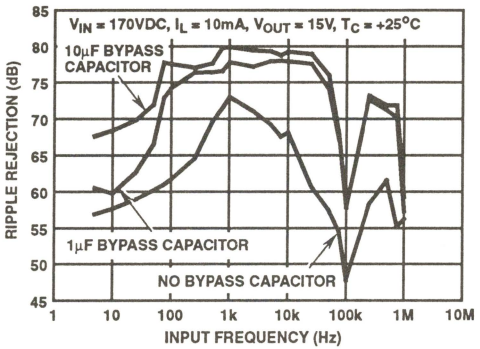


FIGURE 23. RIPPLE REJECTION RATIO (INPUT FREQUENCY)

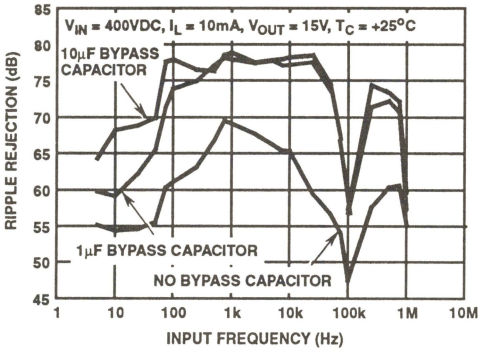


FIGURE 24. RIPPLE REJECTION RATIO (INPUT FREQUENCY)

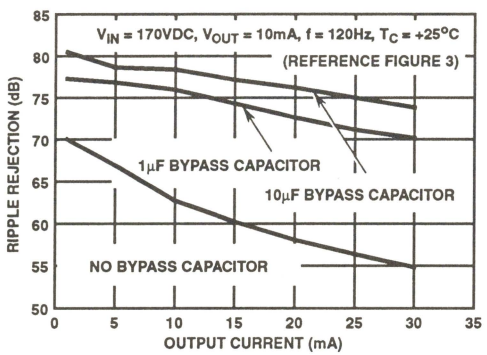


FIGURE 25. RIPPLE REJECTION RATIO (OUTPUT CURRENT)

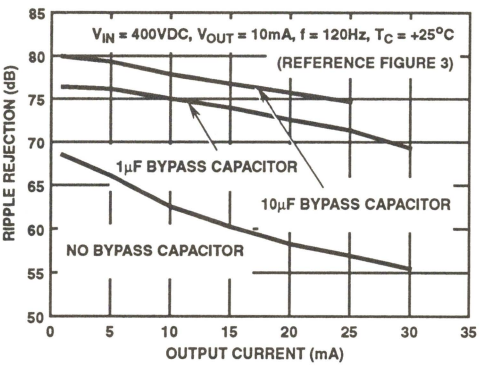


FIGURE 26. RIPPLE REJECTION RATIO (OUTPUT CURRENT)

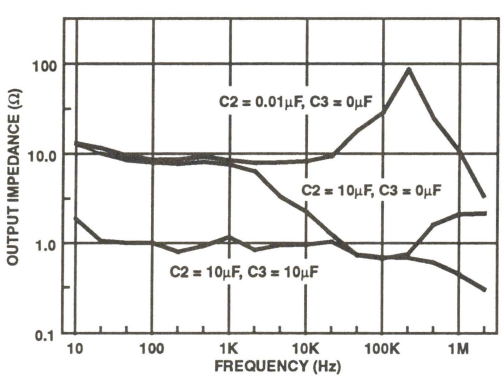


FIGURE 27. OUTPUT IMPEDANCE

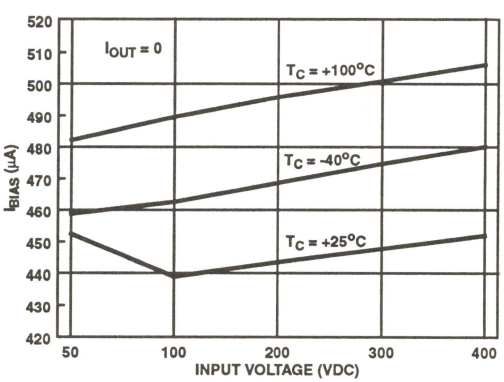


FIGURE 28. I_{BIAS} vs INPUT VOLTAGE

Typical Performance Curves (Continued)

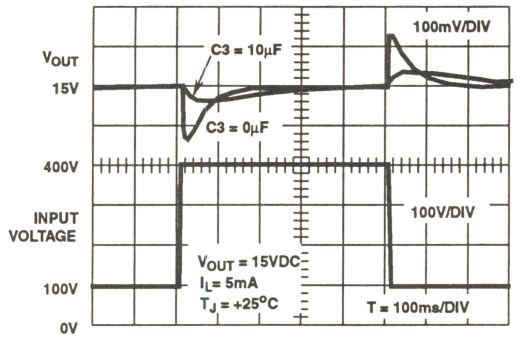


FIGURE 29. LINE TRANSIENT RESPONSE

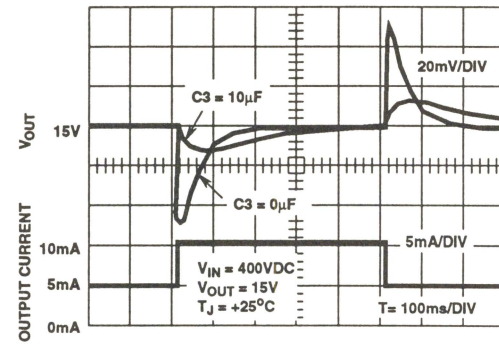


FIGURE 30. LOAD TRANSIENT RESPONSE

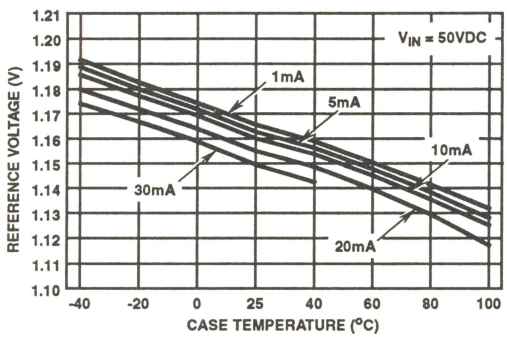


FIGURE 31. REFERENCE VOLTAGE vs TEMPERATURE

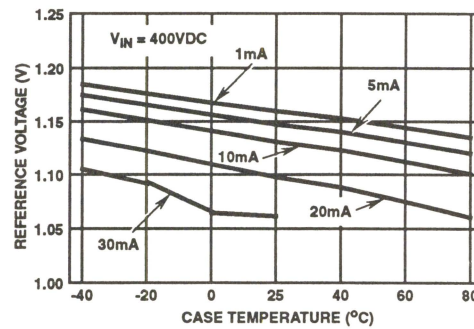


FIGURE 32. REFERENCE VOLTAGE vs TEMPERATURE

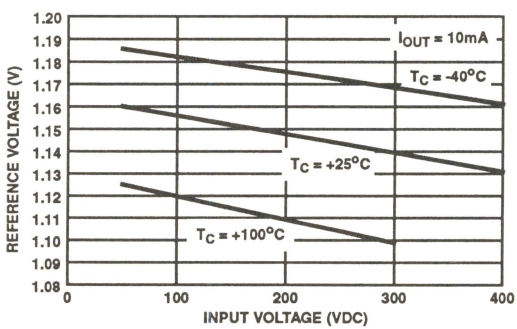


FIGURE 33. REFERENCE VOLTAGE vs INPUT VOLTAGE

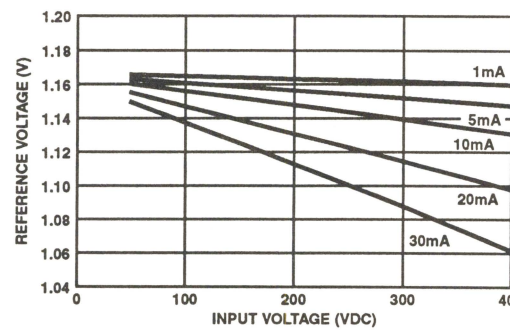


FIGURE 34. REFERENCE VOLTAGE vs V_{IN}; CASE TEMPERATURE OF +25°C

Typical Performance Curves (Continued)

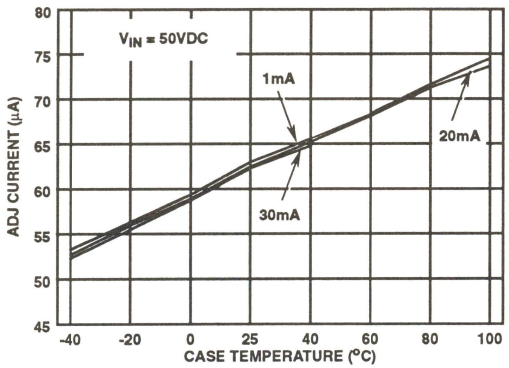


FIGURE 35. I_{ADJ} vs TEMPERATURE

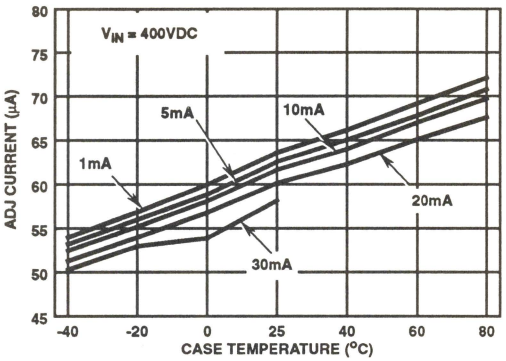


FIGURE 36. I_{ADJ} vs TEMPERATURE

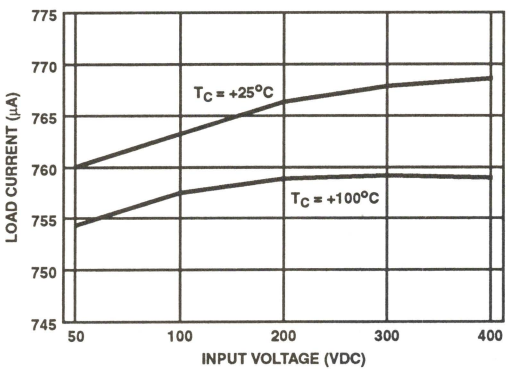


FIGURE 37. MINIMUM LOAD CURRENT vs V_{IN}

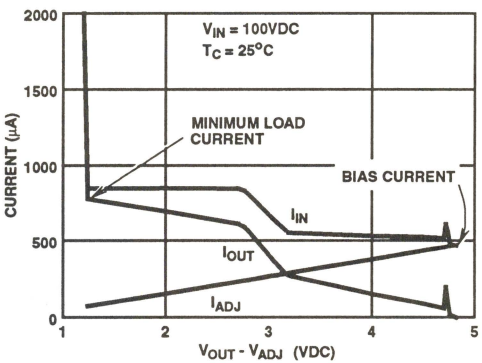


FIGURE 38. TERMINAL CURRENTS vs FORCED V_{REF}

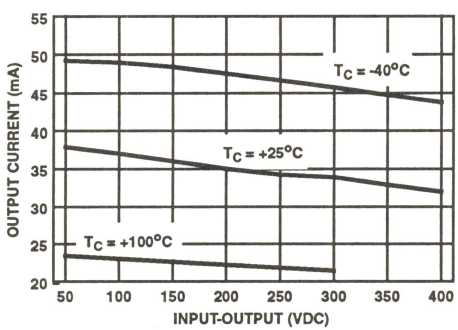


FIGURE 39. CURRENT LIMIT vs TEMPERATURE

Evaluation Boards

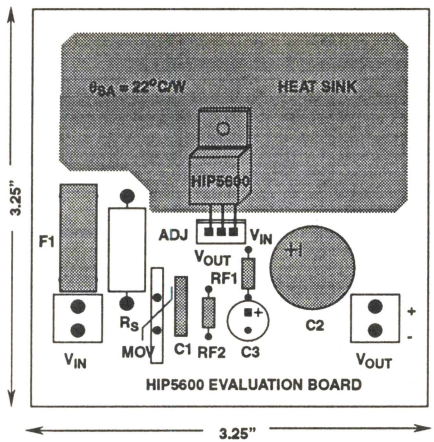


FIGURE 40. EVALUATION BOARD (TOP)

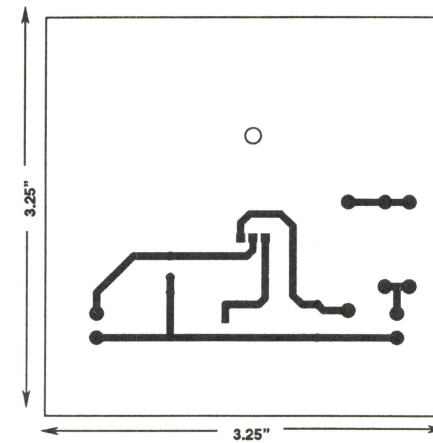


FIGURE 41. EVALUATION BOARD METAL MASK (BOTTOM)

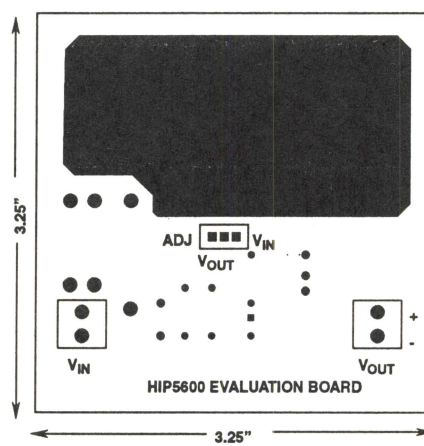


FIGURE 42. EVALUATION BOARD METAL MASK (TOP)

HARRIS SEMICONDUCTOR

ICL7660

April 1994

CMOS Voltage Converter

Features

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication ($V_{OUT} = (-) nV_{IN}$)
- Typical Open Circuit Voltage Conversion Efficiency 99.9%
- Typical Power Efficiency 98%
- Wide Operating Voltage Range 1.5V to 10.0V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temperature and Voltage Range

Applications

- On Board Negative Supply for Dynamic RAMs
- Localized µProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7660CTV	0°C to +70°C	8 Pin Metal Can
ICL7660CBA	0°C to +70°C	8 Lead SOIC (N)
ICL7660CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7660MTV (Note)	0°C to +70°C	8 Pin Metal Can

NOTE: Add /883B to part number if 883B processing is required.

Description

The Harris ICL7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complemetary output voltages of -1.5V to -10.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 can also be connected to function as a voltage doubler and will generate output voltages up to +18.6V with a +10V input.

Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

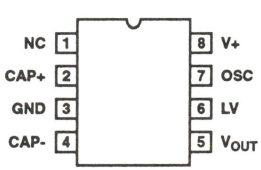
The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5V to +10.0V), the LV pin is left floating to prevent device latchup.

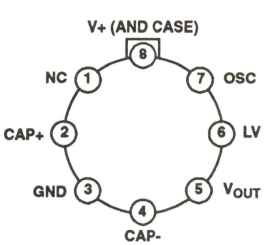
An enhanced direct replacement for this part, the ICL7660S, is now available and should be used for all new designs.

Pinouts

ICL7660 (PDIP, SOIC)
TOP VIEW



ICL7660 (CAN)
TOP VIEW



7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
Copyright © Harris Corporation 1994

File Number 3072.1

Absolute Maximum Ratings

Supply Voltage . . . . . +10.5V
LV and OSC Input Voltage . . . . . -0.3V to (V+ +0.3V) for V+ < 5.5V
(Note 1) (V+ -5.5V) to (V+ +0.3V) for V+ > 5.5V
Current into LV (Note 1) . . . . . 20µA for V+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) . . . . . Continuous

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	150°C/W	-
Plastic SOIC Package	170°C/W	-
Metal Can	156°C/W	68°C/W

Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL7660M . . . . . -55°C to +125°C ICL7660C . . . . . 0°C to +70°C

Electrical Specifications

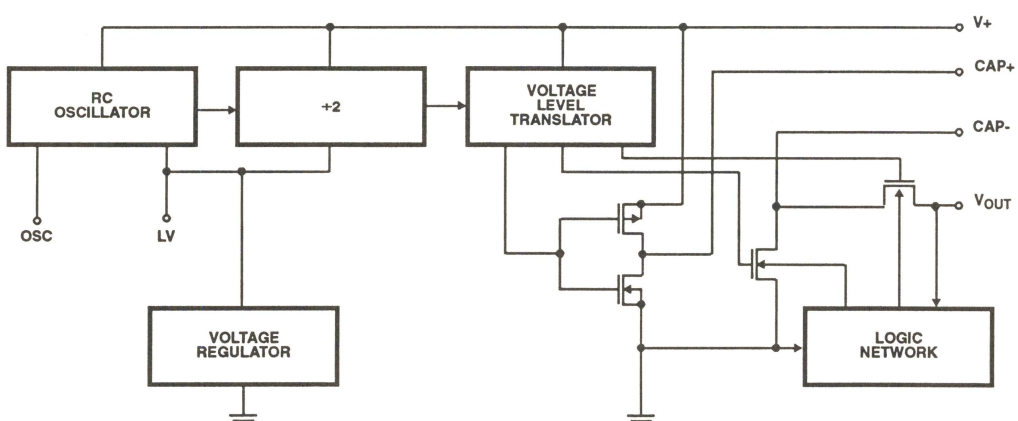
$V^+ = 5V$, $T_A = +25°C$, $C_{OSC} = 0$, Test Circuit Figure 11 (Unless Otherwise Specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I+	Supply Current	$R_L = \infty$	-	170	500	µA
V_L+	Supply Voltage Range - Lo	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND	1.5	-	3.5	V
V_H+	Supply Voltage Range - Hi	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to Open	3.0	-	10.0	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20mA, T_A = +25°C	-	55	100	Ω
		I_{OUT} = 20mA, 0°C ≤ T_A ≤ +70°C	-	-	120	Ω
		I_{OUT} = 20mA, -55°C ≤ T_A ≤ +125°C	-	-	150	Ω
		V^+ = 2V, I_{OUT} = 3mA, LV to GROUND 0°C ≤ T_A ≤ +70°C	-	-	300	Ω
		V+ = 2V, I_{OUT} = 3mA, LV to GROUND, -55°C ≤ T_A ≤ +125°C	-	-	400	Ω
f_{OSC}	Oscillator Frequency		-	10	-	kHz
P_{EF}	Power Efficiency	R_L = 5kΩ	95	98	-	%
$V_{OUT\ EF}$	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9	-	%
Z_{OSC}	Oscillator Impedance	V+ = 2 Volts	-	1.0	-	MΩ
		V = 5 Volts	-	100	-	kΩ

NOTES:

1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.

Functional Block Diagram



Typical Performance Curves (Test Circuit of Figure 11)

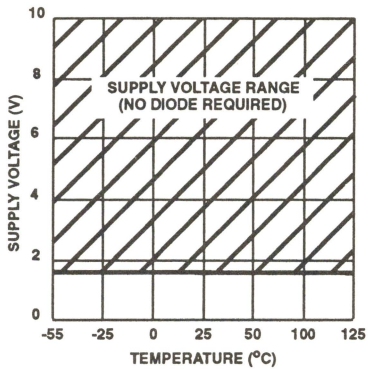


FIGURE 1. OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

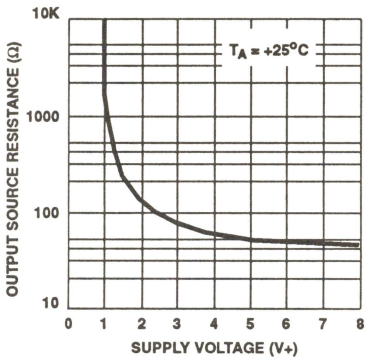


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

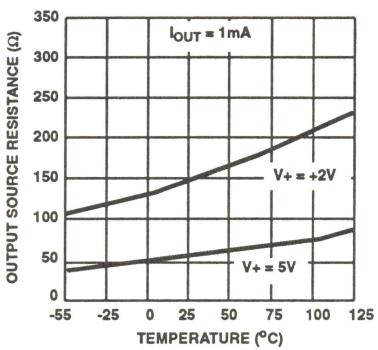


FIGURE 3. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

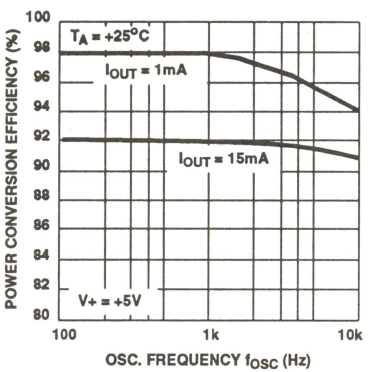


FIGURE 4. POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY

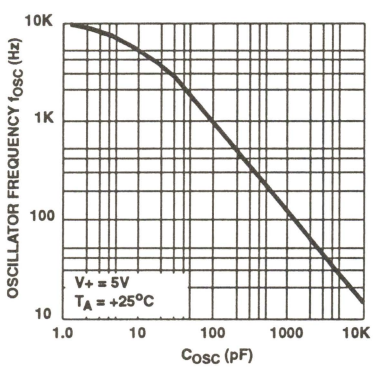


FIGURE 5. FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

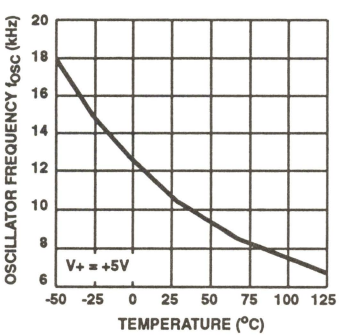


FIGURE 6. UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

Typical Performance Curves (Continued) (Test Circuit of Figure 11) (Continued)

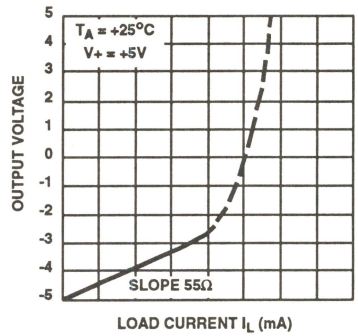


FIGURE 7. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

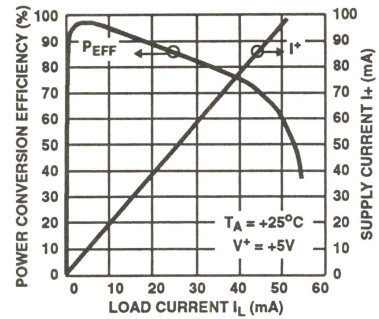


FIGURE 8. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS AFUNCTION OF LOAD CURRENT

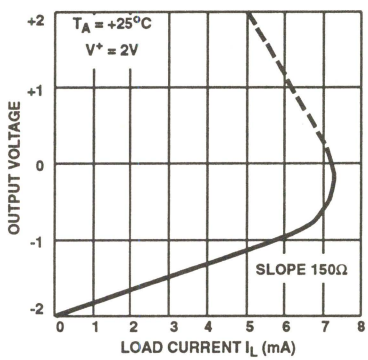


FIGURE 9. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

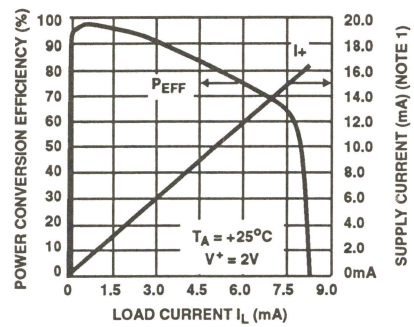
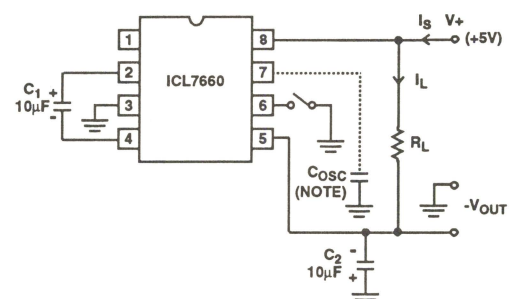


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

NOTE 3. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 11). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.



NOTE: For large values of C_{OSC} (>1000pF) the values of C_1 and C2 should be increased to 100µF.

FIGURE 11. ICL7660 TEST CIRCUIT

Detailed Description

The ICL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 12, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL 7660, the 4 switches of Figure 12 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start-up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

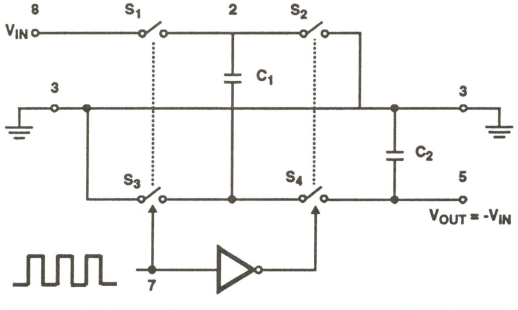


FIGURE 12. IDEALIZED NEGATIVE VOLTAGE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage converter can approach 100% efficiency if certain conditions are met.

A The driver circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 12) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's And Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5V.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
5. If the voltage supply driving the ICL7660 has a large source impedance (25Ω - 30Ω), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

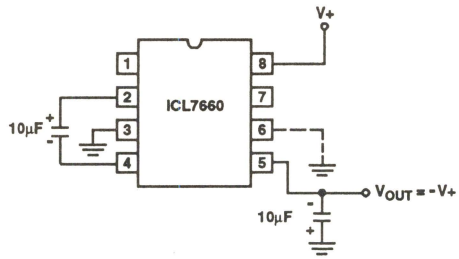


FIGURE 13A. CONFIGURATION

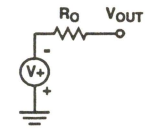


FIGURE 13B. THEVENIN EQUIVALENT

FIGURE 13. SIMPLE NEGATIVE CONVERTER

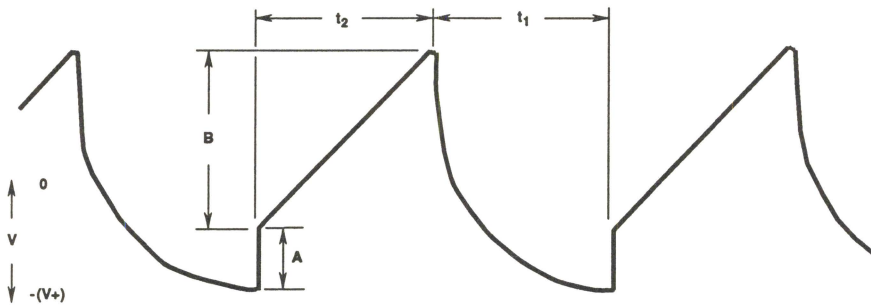


FIGURE 14. OUTPUT RIPPLE

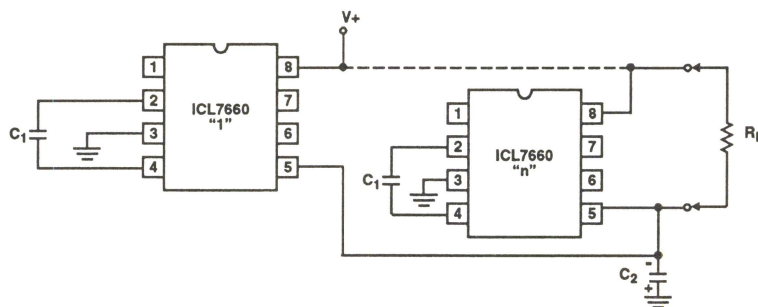


FIGURE 15. PARALLELING DEVICES

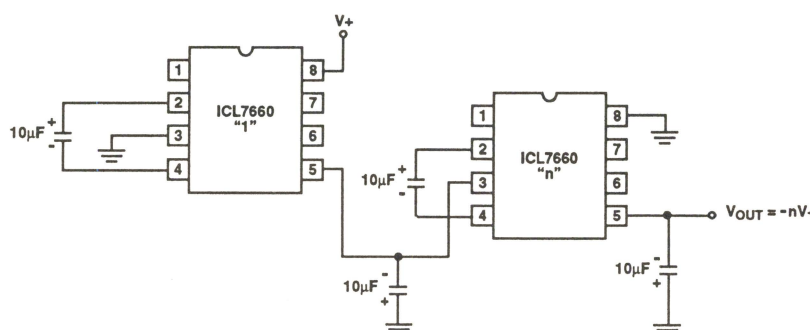


FIGURE 16. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 13 shows typical connections to provide a negative supply negative (GND) for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 13A can be approximated by an ideal voltage source in series with a resistance as shown in Figure 13B. The voltage source has a value of -V+. The output impedance (R_o) is a function of the ON resistance of the internal MOS switches (shown in Figure 12), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_o is:

$$R_0 \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{(f_{PUMP})(C1)} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2}, R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_0 \cong 2(R_{SW}) + \frac{1}{(f_{PUMP})(C1)} + 4(ESR_{C1}) + ESR_{C2}$$

RSW, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \bullet C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \bullet C1)$ term, but may have the side effect of a net increase in output impedance when $C_1 > 10\mu F$ and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10kHz and $C = C_1 = C_2 = 10\mu F$:

$$R_0 \cong 2(23) + \frac{1}{(5 \bullet 10^3)(10^{-5})} + 4(ESR_{C1}) + ESR_{C2}$$

$$R_0 \cong 46 + 20 + 5(ESR_C)$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \bullet C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

$$R_0 \cong 2(23) + \frac{1}{(5 \bullet 10^3)(10^{-5})} + 4(ESR_{C1}) + ESR_{C2}$$

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Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 14. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flow into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is $2 \bullet I_{OUT}$, hence the total drop is $2 \bullet I_{OUT} \bullet eSR_{C2}V$. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current to the load. The drop at B is $I_{OUT} \bullet t2/C_2V$. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left[\frac{1}{2(f_{PUMP})(C2)} + 2(ESR_{C2})\right] Iout$$

Again, a low ESR capacitor will reset in a higher performance output.

Paralleling Devices

Any number of ICL7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\text{ (of ICL7660)}}{n\text{ (number of devices)}}$$

Cascading Devices

The ICL7660 may be cascaded as shown to produced larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.

Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 17. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

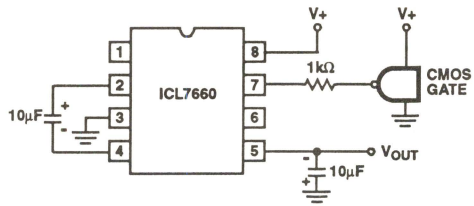


FIGURE 17. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 18. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

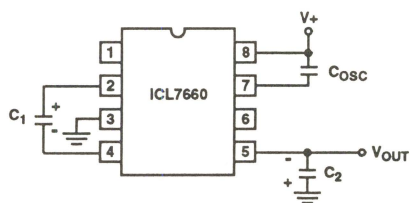


FIGURE 18. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure 19. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) - (2VF) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 5V and an output current of 10mA it will be approximately 60Ω.

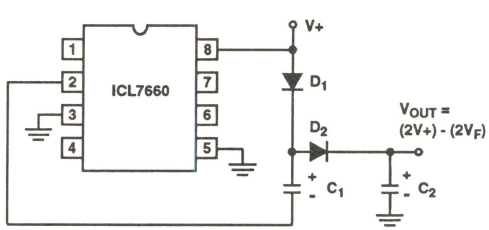


FIGURE 19. POSITIVE VOLTAGE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 20 combines the functions shown in Figures 13 and Figure 19 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

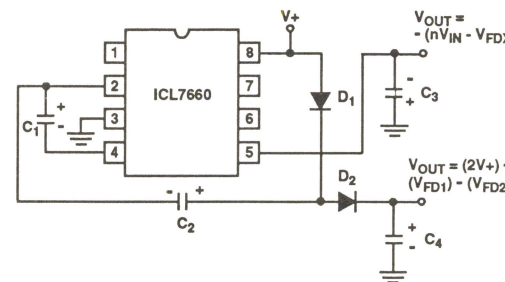


FIGURE 20. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 21. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 16, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250Ω).

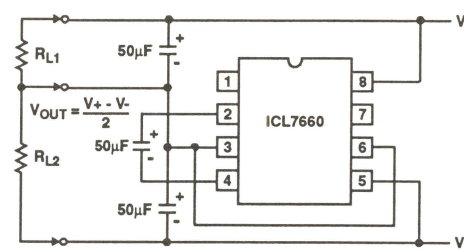


FIGURE 21. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 22 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660s output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

Other Applications

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

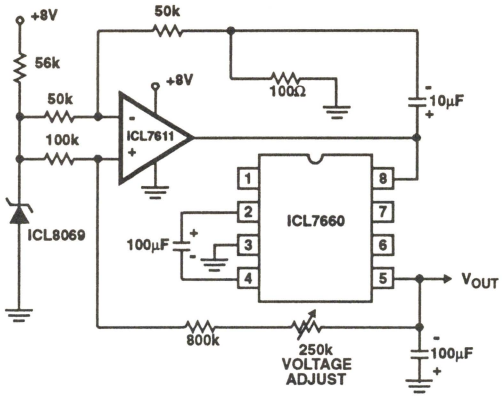


FIGURE 22. REGULATING THE OUTPUT VOLTAGE

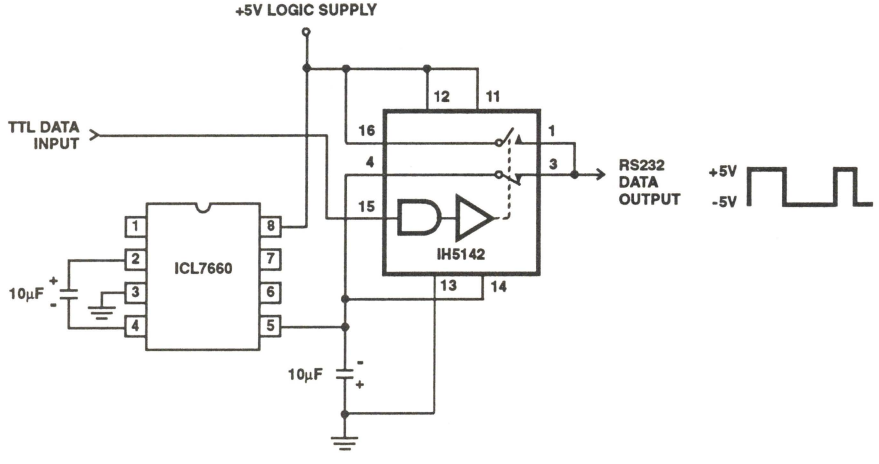


FIGURE 23. RS232 LEVELS FROM A SINGLE 5V SUPPLY

HARRIS SEMICONDUCTOR

ICL7660S

April 1994

Super Voltage Converter

Features

- **Guaranteed Lower Max Supply Current for All Temperature Ranges**
- **Wide Operating Voltage Range 1.5V to 12V**
- **100% Tested at 3V**
- **No External Diode Over Full Temperature and Voltage Range**
- **Boost Pin (Pin 1) for Higher Switching Frequency**
- **Guaranteed Minimum Power Efficiency of 96%**
- **Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%**
- **Improved SCR Latchup Protection**
- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication $V_{OUT} = (-)nV_{IN}$**
- **Easy to Use - Requires Only 2 External Non-Critical Passive Components**
- **Improved Direct Replacement for Industry Standard ICL7660 and Other Second Source Devices**

Applications

- **Simple Conversion of +5V to ±5V Supplies**
- **Voltage Multiplication $V_{OUT} = \pm nV_{IN}$**
- **Negative Supplies for Data Acquisition Systems and Instrumentation**
- **RS232 Power Supplies**
- **Supply Splitter, $V_{OUT} = \pm V_S/2$**

Description

The ICL7660S Super Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry standard ICL7660 offering an **extended** operating supply voltage range up to 12V, with **lower** supply current. **No external diode** is needed for the ICL7660S. In addition, a **Frequency Boost pin** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in the Electrical Specifications section. **Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.**

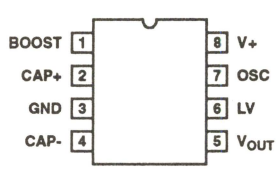
The ICL7660S performs supply voltage conversion from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of -1.5V to -12V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660S can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

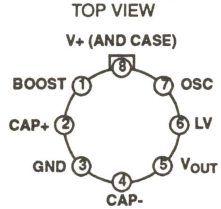
The "LV" terminal may be tied to GND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

Pinouts

ICL7660S (PDIP, SOIC)
TOP VIEW



ICL7660S (CAN)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
ICL7660SCBA	0°C to +70°C	8 Lead Plastic SOIC (N)
ICL7660SCPA	0°C to +70°C	8 Lead Plastic DIP
ICL7660SCTV	0°C to +70°C	8 Pin Metal Can
ICL7660SIBA	-40°C to +85°C	8 Lead Plastic SOIC (N)
ICL7660SIPA	-40°C to +85°C	8 Lead Plastic DIP
ICL7660SITV	-40°C to +85°C	8 Pin Metal Can
ICL7660SMTV (Note)	-55°C to +125°C	8 Pin Metal Can

NOTE: Add /883B to part number if 883B processing is required.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3179.1**

Absolute Maximum Ratings

Supply Voltage . . . . . +13.0V
LV and OSC Input Voltage (Note 1)
V+ < 5.5V . . . . . -0.3V to V+ + 0.3V
V+ > 5.5V . . . . . V+ -5.5V to V+ +0.3V
Current into LV (Note 1)
V+ > 3.5V 20µA
Output Short Duration
$V_{SUPPLY} \leq 5.5V$ . . . . . Continuous
Storage Temperature Range . . . . . -65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP	150°C/W	-
Plastic SOIC	170°C/W	-
Metal Can	155°C/W	70°C/W

Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL7660SM . . . . . -55°C to +125°C
ICL7660SI . . . . . -40°C to +85°C
ICL7660SC . . . . . 0°C to +70°C

Electrical Specifications

V+ = 5V, T_A = +25°C, OSC = Free running, Test Circuit Figure 12, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 3)	I+	$R_L = \infty$, +25°C	-	80	160	µA
		0°C < T_A < +70°C	-	-	180	µA
		-40°C < T_A < +85°C	-	-	180	µA
		-55°C < T_A < +125°C	-	-	200	µA
Supply Voltage Range - High (Note 4)	$V+_H$	R_L = 10K, LV Open, $T_{MIN} < T_A < T_{MAX}$	3.0	-	12	V
Supply Voltage Range - Low	$V+_L$	R_L = 10K, LV to GND, $T_{MIN} < T_A < T_{MAX}$	1.5	-	3.5	V
Output Source Resistance	R_{OUT}	I_{OUT} = 20mA	-	60	100	Ω
		I_{OUT} = 20mA, 0°C < T_A < +70°C	-	-	120	Ω
		I_{OUT} = 20mA, -25°C < T_A < +85°C	-	-	120	Ω
		I_{OUT} = 20mA, -55°C < T_A < +125°C	-	-	150	Ω
		I_{OUT} = 3mA, V+ = 2V, LV = GND, 0°C < T_A < +70°C	-	-	250	Ω
		I_{OUT} = 3mA, V+ = 2V, LV = GND, -40°C < T_A < +85°C	-	-	300	Ω
		I_{OUT} = 3mA, V+ = 2V, LV = GND, -55°C < T_A < +125°C	-	-	400	Ω
Oscillator Frequency (Note 3)	f_{OSC}	C_{OSC} = 0, Pin 1 Open or GND	5	10	-	kHz
		C_{OSC} = 0, Pin 1 = V+	-	35	-	kHz
Power Efficiency	P_{EFF}	R_L = 5kΩ	96	98	-	%
		$T_{MIN} < T_A < T_{MAX}$ R_L = 5kΩ	95	97	-	-
Voltage Conversion Efficiency	$V_{OUT}EFF$	$R_L = \infty$	99	99.9	-	%
Oscillator Impedance	Z_{OSC}	V+ = 2V	-	1	-	MΩ
		V+ = 5V	-	100	-	kΩ

NOTES:

1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660S.
2. Derate linearly above +50°C by 5.5mW/°C
3. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
4. The Harris ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.
5. All significant improvements over the industry standard ICL7660 are highlighted.

Electrical Specifications

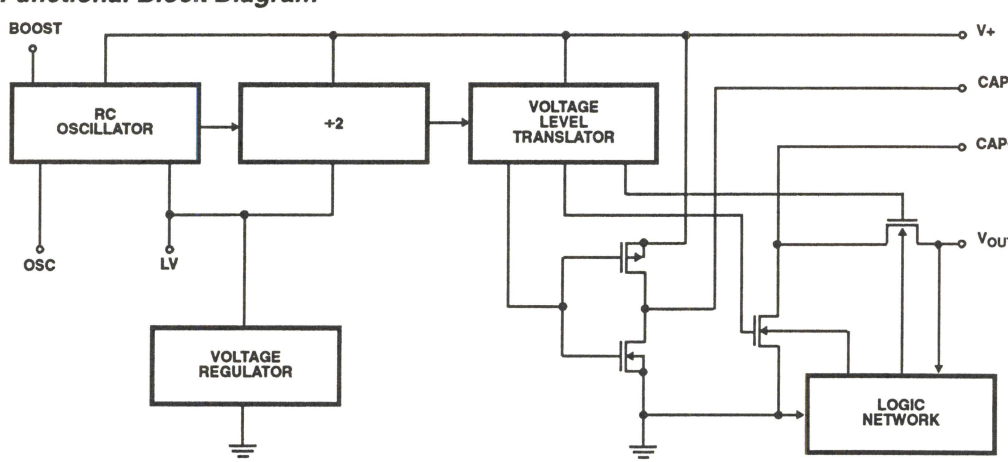
V+ = 3V, T_A = +25°C, OSC = Free running, Test Circuit Figure 12, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 3)	I+	V+ = 3V, R_L = ∞, +25°C	-	26	100	µA
		0°C < T_A < +70°C	-	-	125	µA
		-40°C < T_A < +85°C	-	-	125	µA
		-55°C < T_A < +125°C	-	-	150	µA
Output Source Resistance	R_{OUT}	V+ = 3V, I_{OUT} = 10mA	-	97	150	Ω
		0°C < T_A < +70°C	-	-	200	Ω
		-40°C < T_A < +85°C	-	-	200	Ω
		-55°C < T_A < +125°C	-	-	250	Ω
Oscillator Frequency (Note 3)	f_{OSC}	V+ = 3V (same as 5V conditions)	2.5	4	-	kHz
		0°C < T_A < +70°C	1.5	-	-	kHz
		-40°C < T_A < +85°C	1.5	-	-	kHz
		-55°C < T_A < +125°C	1.0	-	-	kHz
Voltage Conversion Efficiency	$V_{OUT}EFF$	V+ = 3V, R_L = ∞	99	-	-	%
		T_{MIN} < T_A < T_{MAX}	99	-	-	%
Power Efficiency	P_{EFF}	V+ = 3V, R_L = 5kΩ	96	-	-	%
		T_{MIN} < T_A < T_{MAX}	95	-	-	%

NOTES:

1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660S.
2. Derate linearly above +50°C by 5.5mW/°C
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Functional Block Diagram



Typical Performance Curves (Test Circuit Figure 12)

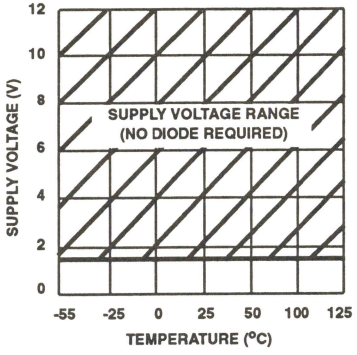


FIGURE 1. OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

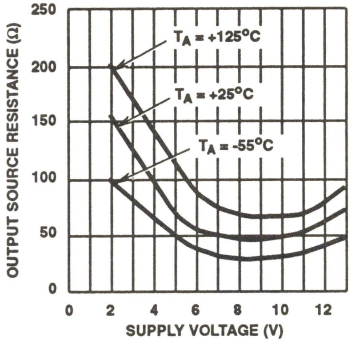


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

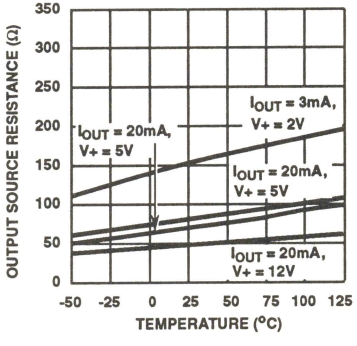


FIGURE 3. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

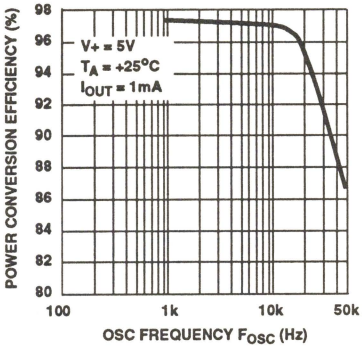


FIGURE 4. POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSCILLATOR FREQUENCY

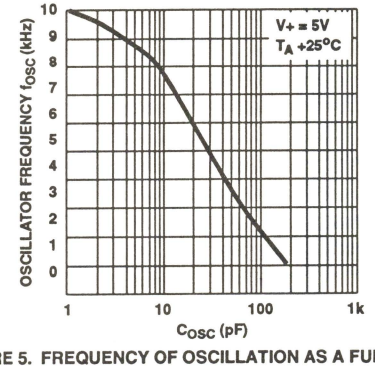


FIGURE 5. FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE

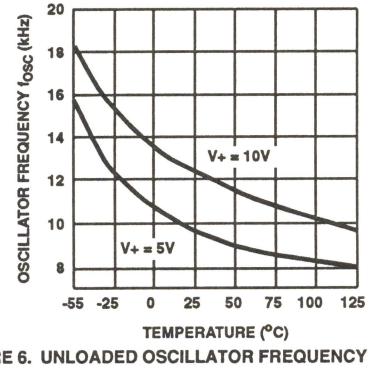


FIGURE 6. UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

Typical Performance Curves (Test Circuit Figure 12) (Continued)

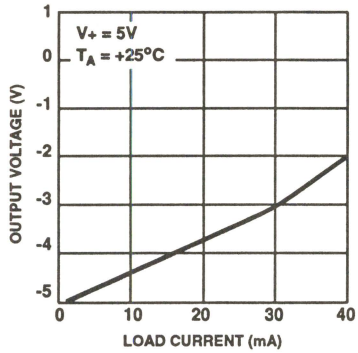


FIGURE 7. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

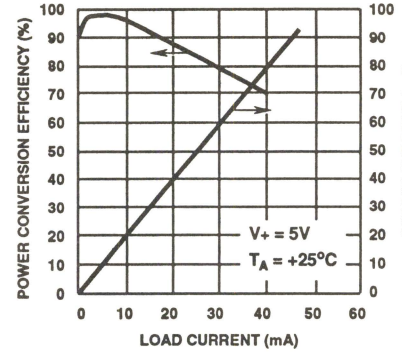


FIGURE 8. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

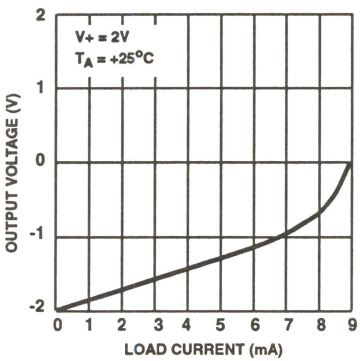


FIGURE 9. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

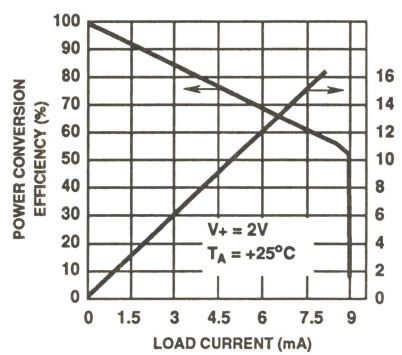


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

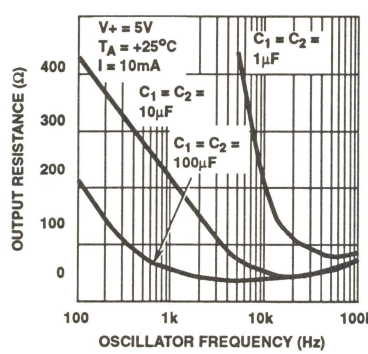
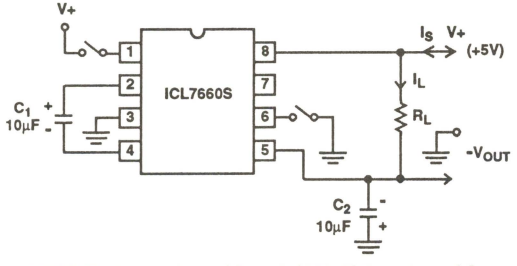


FIGURE 11. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY

NOTE 6. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 12). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660S, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.

Detailed Description

The ICL7660S contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 13, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7660S approaches this ideal situation more closely than existing non-mechanical circuits.



NOTE: For large values of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100µF

FIGURE 12. ICL7660S TEST CIRCUIT

In the ICL7660S, the 4 switches of Figure 13 are MOS power switches; S_1 is a P-Channel devices and S_2, S_3 and S_4 are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660S is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

Theoretical Power Efficiency Considerations

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

A. The drive circuitry consumes minimal power.

B. The output switches have extremely low ON resistance and virtually no offset.

C. The impedance of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660S approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = {}^1/_2 C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 13) compared to the value of R_L, there will be substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

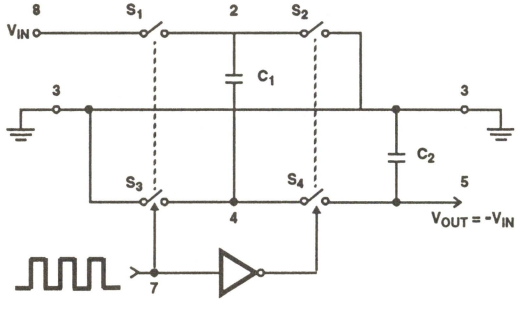


FIGURE 13. IDEALIZED NEGATIVE VOLTAGE CONVERTER

Do's and Don'ts

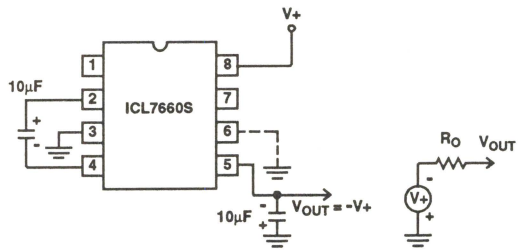
1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GND for supply voltage greater than 3.5V.
3. Do not short circuit the output to V^+ supply for supply voltages above 5.5V for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660S and the + terminal of C_2 must be connected to GND.
5. If the voltage supply driving the ICL7660S has a large source impedance (25Ω - 30Ω), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

   A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660S for generation of negative supply voltages. Figure 14 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltage below 3.5V.



14A. 14B.

FIGURE 14. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

The output characteristics of the circuit in Figure 14 can be approximated by an ideal voltage source in series with a resistance as shown in Figure 14B. The voltage source has a value of -(V+). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 13), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C_1 and C_2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW}4 + ESR_{C1}) + \frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESR_{C1} + ESR_{C2}\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C_1)$ term, but may have the side effect of a net increase in output impedance when $C_1 > 10\mu F$ and is not long enough to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10kHz and $C = C_1 = C_2 = 10\mu F$:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_O \cong 46 + 20 + 5 \times ESR_C\Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/f_{PUMP} \times C_1$) term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 15. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flowing into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is 2 x I_{OUT}, hence the total drop is 2 x I_{OUT} x ESR_{C2}V. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current the load. The drop at B is $I_{OUT} \times t_2/C_2$V. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \equiv \left(\frac{1}{2 \times f_{PUMP} \times C_2} + 2\ ESRC_2 \times I_{OUT} \right)$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7660S voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7660S})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7660S may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660S R_{OUT} values.

Changing the ICL7660S Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods described below.

By connecting the Boost Pin (Pin 1) to V+, the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately $3^1/_2$ times. The result is a decrease in the output impedance and ripple. This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller

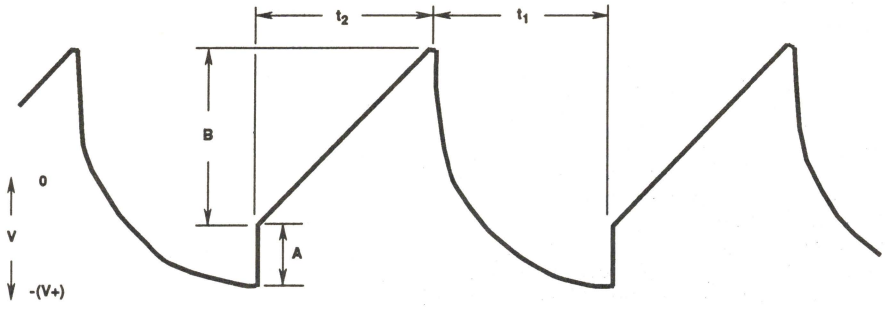


FIGURE 15. OUTPUT RIPPLE

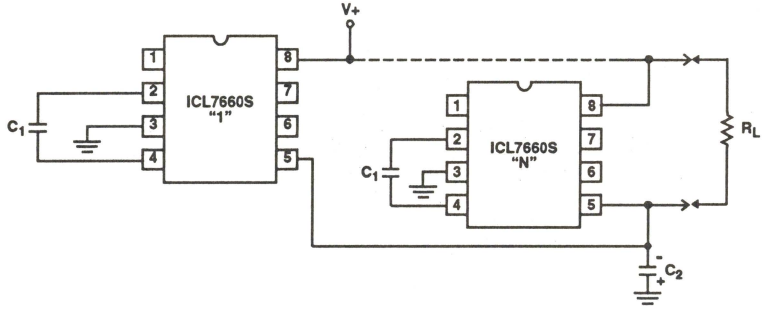
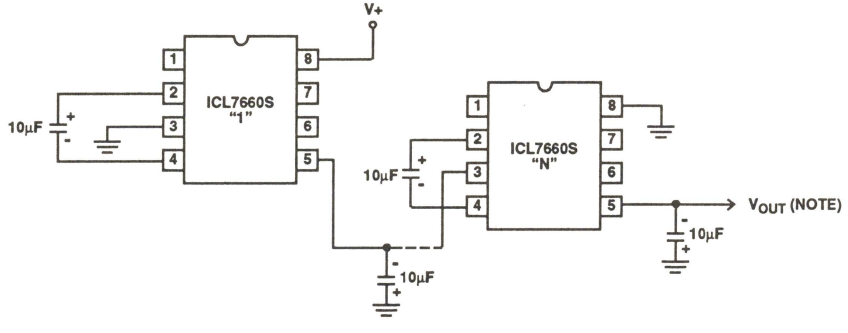


FIGURE 16. PARALLELING DEVICES



NOTE: $V_{OUT} = -nV$ for $1.5V \leq V+ \leq 12V$

FIGURE 17. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

capacitors, e.g. 0.1µF, can be used in conjunction with the Boost Pin in order to achieve similar output currents compared to the device free running with $C_1 = C_2 = 10\mu F$ or 100µF. (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 18. In order to prevent device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be $^1/_2$ of the clock frequency. Output transitions occur on the positive going edge of the clock.

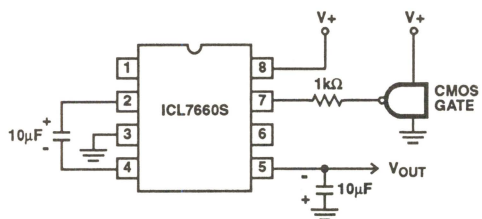


FIGURE 18. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the ICL7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 19. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

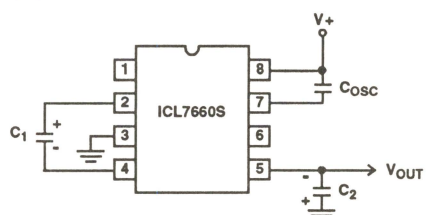
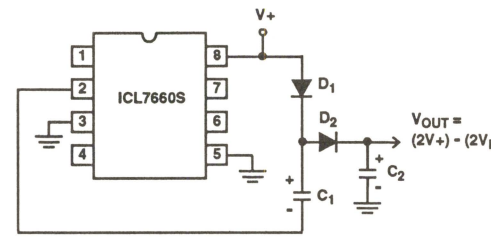


FIGURE 19. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7660S may be employed to achieve positive voltage doubling using the circuit shown in Figure 20. In this application, the pump inverter switches of the ICL7660S are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage on C_1 plus the supply voltage (V+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) - ($2V_F$) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 5V and an output current of 10mA it will be approximately 60Ω.



NOTE: D_1 and D_2 can be any suitable diode

FIGURE 20. POSITIVE VOLTAGE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 21 combines the functions shown in Figure 14 and Figure 20 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

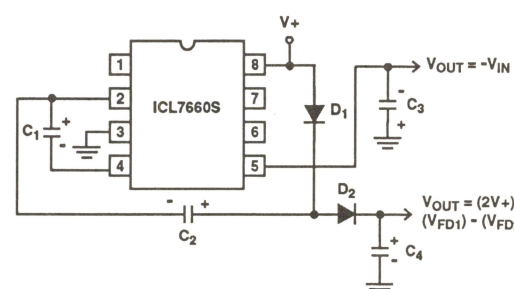


FIGURE 21. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

Voltage Splitting

The bidirectional characteristics can also be used to split a high supply in half, as shown in Figure 22. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents

can be drawn from the device. By using this circuit, and then the circuit of Figure 17, +15V can be converted (via +7.5, and -7.5 to a nominal -15V, although with rather high series output resistance (~250Ω).

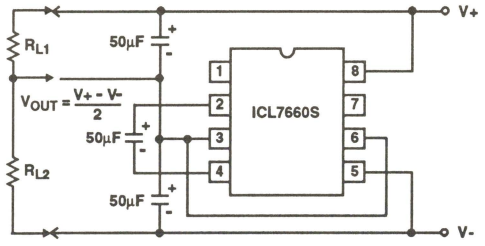


FIGURE 22. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In Some cases, the output impedance of the ICL7660S can be a problem, particularly if the load current varies substantially. The circuit of Figure 23 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660S's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660S, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

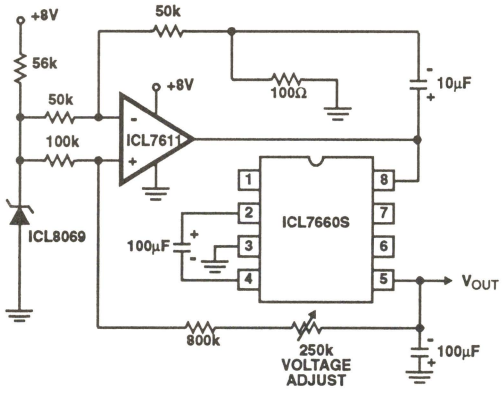


FIGURE 23. REGULATING THE OUTPUT VOLTAGE

Other Applications

Further information on the operation and use of the ICL7660S may be found in AN051 "Principles and Applications of the ICL7660 CMOS Voltage Converter".

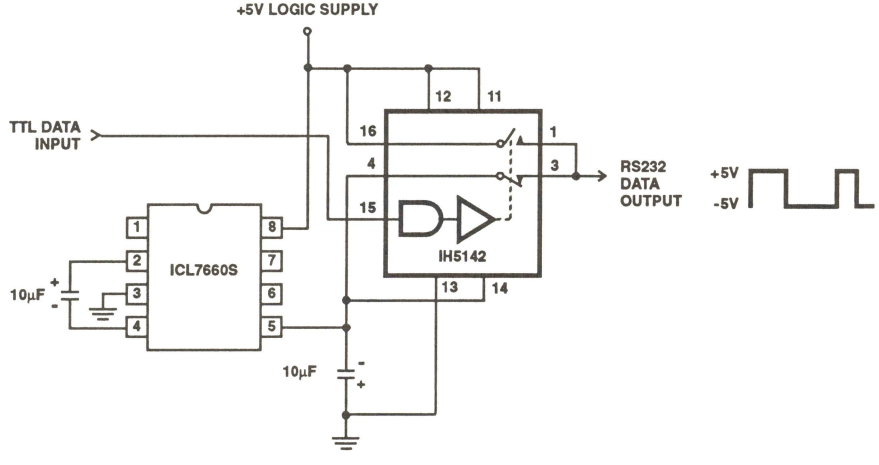


FIGURE 24. RS232 LEVELS FROM A SINGLE 5V SUPPLY

HARRIS SEMICONDUCTOR

ICL7662

April 1994

CMOS Voltage Converter

Features

- No External Diode Needed Over Entire Temperature Range
- Pin Compatible With ICL7660
- Simple Conversion of +15V Supply to -15V Supply
- Simple Voltage Multiplication ($V_{OUT} = (-)nV_{IN}$)
- 99.9% Typical Open Circuit Voltage Conversion Efficiency
- 96% Typical Power Efficiency
- Wide Operating Voltage Range 4.5V to 20.0V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components

Applications

- On Board Negative Supply for Dynamic RAMs
- Localized µProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- Up to -20V for Op Amps

Description

The Harris ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of -4.5V to -20V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V input.

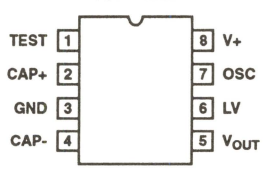
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0V. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

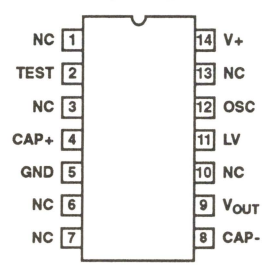
The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10V to +20V), the LV pin is left floating to prevent device latchup.

Pinouts

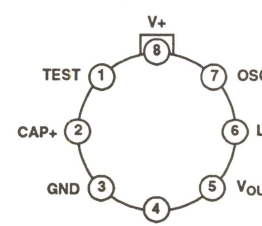
ICL7662 (PDIP)
TOP VIEW



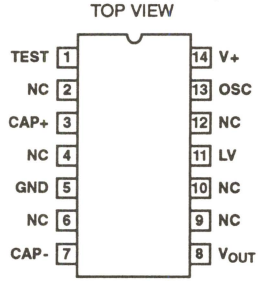
ICL7662CBD AND IBD (SOIC)
TOP VIEW



ICL7662 (CAN)
TOP VIEW



ICL7662CBD-0 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3181.2**

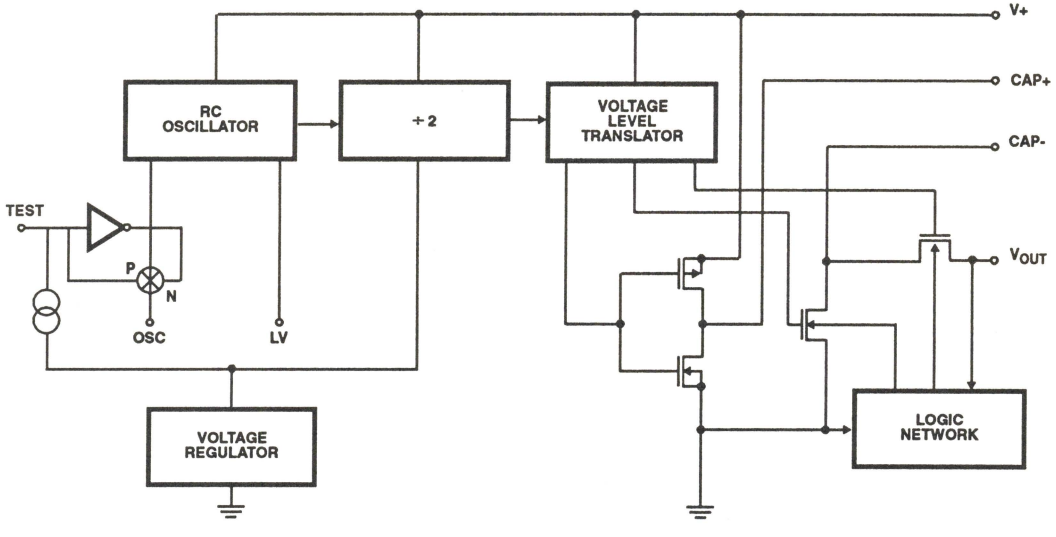
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7662CTV	0°C to +70°C	8 Pin Metal Can
ICL7662CPA		8 Lead Plastic DIP
ICL7662CBD-0		14 Lead SOIC (N)
ICL7662CBD		14 Lead SOIC (N)
ICL7662ITV	-40°C to +85°C	8 Pin Metal Can
ICL7662IPA		8 Lead Plastic DIP
ICL7662IBD		14 Lead SOIC (N)
ICL7662MTV (Note 1)	-55°C to +125°C	8 Pin Metal Can

NOTE:

1. Add /883 to part number if /883B processing is required.

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage 22V
Oscillator Input Voltage..... -0.3V to (V+ +0.3V) for V+ < 10V
.....(V+ -10V) to (V+ +0.3V) for V+ > 10V
(Note 1)
Current Into LV (Note 1) .....20µA for V+ > 10V
Output Short Duration..... Continuous

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	150°C/W	-
Plastic SOIC Package.....	120°C/W	-
Metal Can	156°C/W	68°C/W

Lead Temperature (Soldering, 10s)..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 15V, T_A = +25°C, C_{OSC} = 0, Unless Otherwise Specified. Refer to Figure 14.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range - Lo	V+L	R_L = 10kΩ, LV = GND	Min < T_A < Max	4.5	-	11	V
Supply Voltage Range - Hi	V+H	R_L = 10kΩ, LV = Open	Min < T_A < Max	9	-	20	V
Supply Current	I+	R_L = ∞, LV = Open	T_A = +25°C	-	0.25	0.60	mA
			0°C < T_A < +70°C -40°C < T_A < +85°C	-	0.30	0.85	mA
			-55°C < T_A < +125°C	-	0.40	1.0	mA
Output Source Resistance	R_O	I_O = 20mA, LV = Open	T_A = +25°C	-	60	100	Ω
			0°C < T_A < +70°C -40°C < T_A < +85°C	-	70	120	Ω
			-55°C < T_A < +125°C	-	90	150	Ω
Supply Current	I+	V+ = 5V, R_L = ∞, LV = GND	T_A = +25°C	-	20	150	µA
			0°C < T_A < +70°C -40°C < T_A < +85°C	-	25	200	µA
			-55°C < T_A < +125°C	-	30	250	µA
Output Source Resistance	R_O	V+ = 5V, I_O = 3mA, LV = GND	T_A = +25°C	-	125	200	Ω
			0°C < T_A < +70°C -40°C < T_A < +85°C	-	150	250	Ω
			-55°C < T_A < +125°C	-	200	350	Ω
Oscillator Frequency	FOSC			-	10	-	kHz
Power Efficiency	P_{EFF}	R_L = 2KΩ	T_A = +25°C	93	96	-	%
			Min < T_A < Max	90	95	-	%
Voltage Conversion Efficiency	VoEf	R_L = ∞	Min < T_A < Max	97	99.9	-	%
Oscillator Sink or Source Current	I_{OSC}	V+ = 5V (V_{OSC} = 0V to +5V)		-	0.5	-	µA
		V+ = 15V (V_{OSC} = +5V to +15V)		-	4.0	-	µA

NOTES:

1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660S.
2. Pin 1 is a Test pin and is not connected in normal use. When the TEST pin is connected to V+, an internal transmission gate disconnects any external parasitic capacitance from the oscillator which would otherwise reduce the oscillator frequency from its nominal value.

Performance Curves (See Figure 14, Test Circuit)

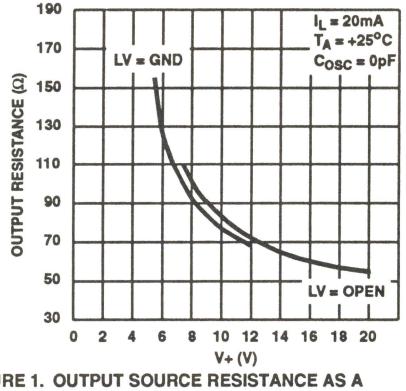


FIGURE 1. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

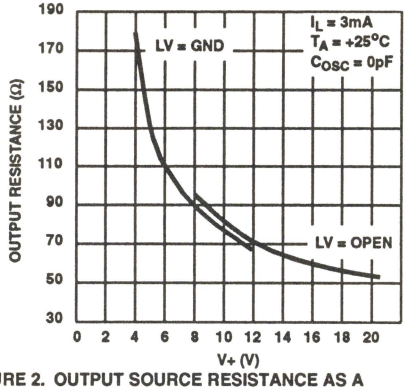


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

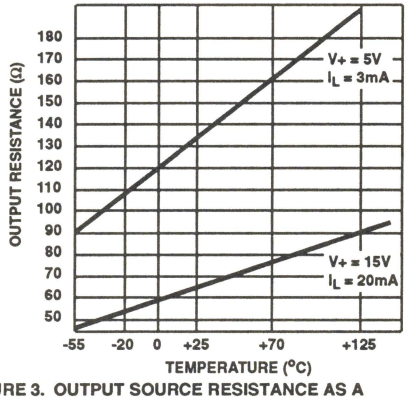


FIGURE 3. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

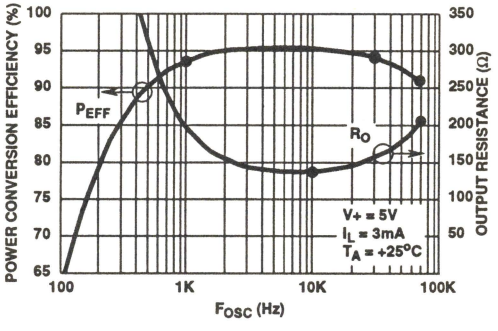


FIGURE 4. POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY

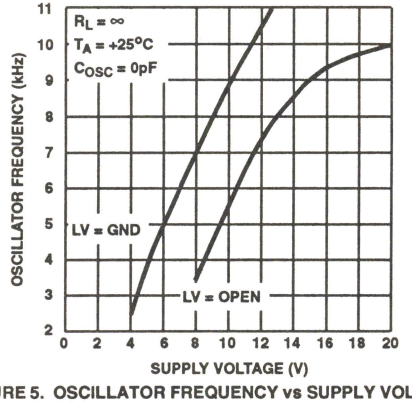


FIGURE 5. OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

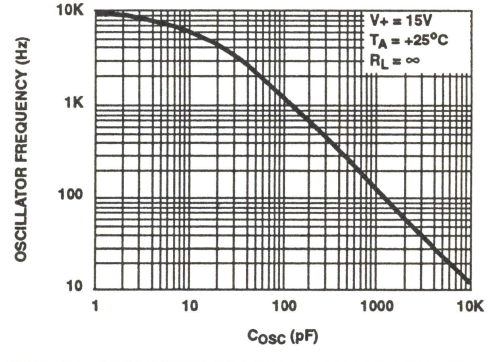


FIGURE 6. FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE

NOTE: All typical values have been characterized but are not tested.

Performance Curves (See Figure 14, Test Circuit) (Continued)

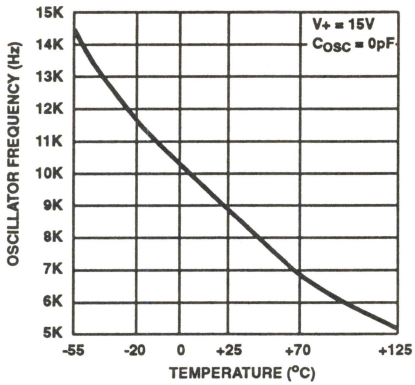


FIGURE 7. UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

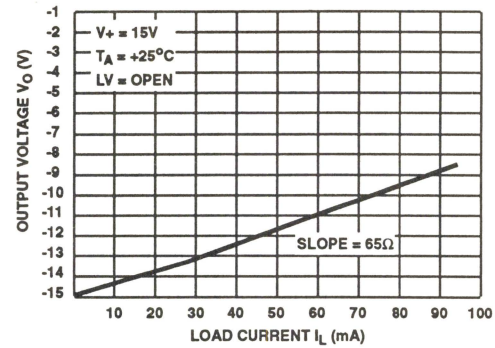


FIGURE 8. OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT

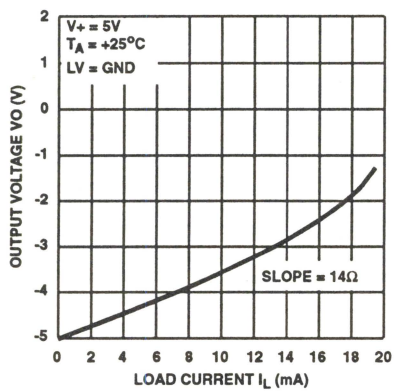


FIGURE 9. OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT

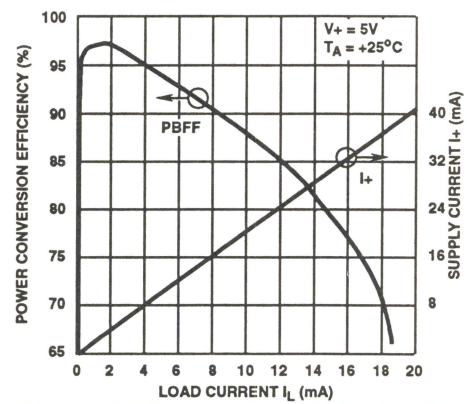


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD

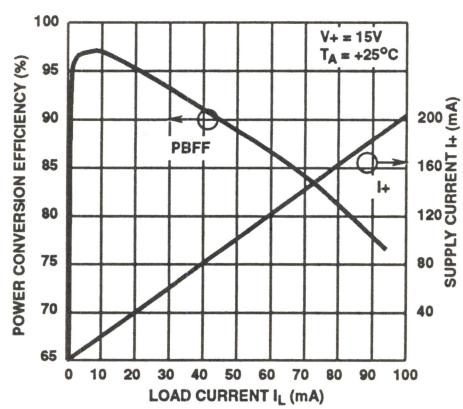


FIGURE 11. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

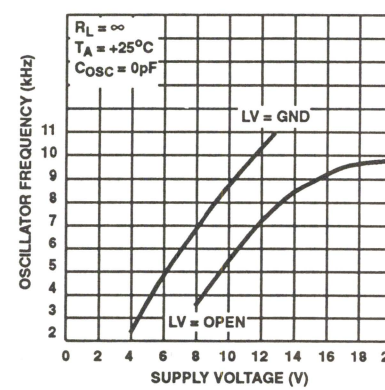


FIGURE 12. FREQUENCY OF OSCILLATION AS A FUNCTION OF SUPPLY VOLTAGE

Performance Curves (See Figure 14, Test Circuit) (Continued)

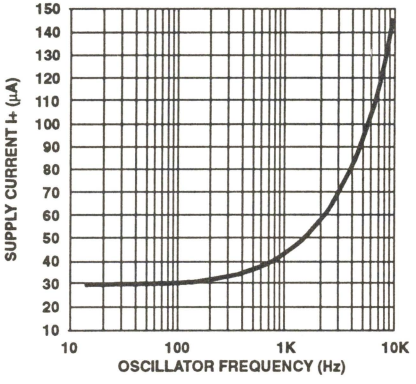


FIGURE 13. SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY

NOTE 4. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 14). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.

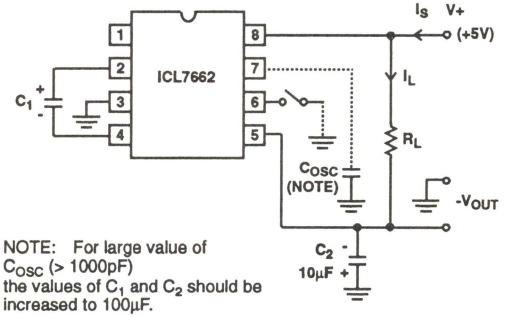
Circuit Description

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 15, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7662, the 4 switches of Figure 15 are MOS power switches; S_1 is a P-Channel device and S_2, S_3 and S_4 are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 10V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.



NOTE: For large value of C_{OSC} (> 1000pF) the values of C_1 and C_2 should be increased to 100µF.

FIGURE 14. ICL7662 TEST CIRCUIT

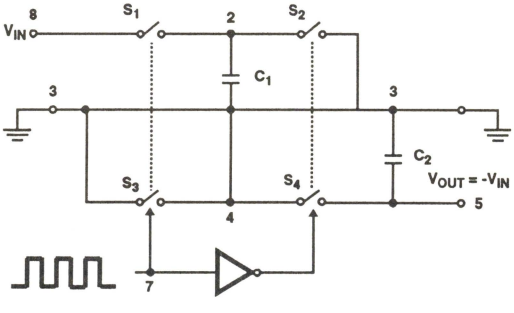


FIGURE 15. IDEALIZED NEGATIVE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 15) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's and Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 10V.
3. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7662 and the + terminal of C_2 must be connected to GROUND.
4. If the voltage supply driving the 7662 has a large source impedance (25Ω - 30Ω), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
5. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 16 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 10V.

The output characteristics of the circuit in Figure 16A can be approximated by an ideal voltage source in series with a resistance as shown in Figure 16B. The voltage source has a value of -(V+). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C_1 and C_2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESRC_1) + 2(R_{SW2} + R_{SW4} + ESRC_1) + \frac{1}{f_{PUMP} \times C_1} + ESRC_2$$

($f_{PUMP} = \frac{f_{OSC}}{2}$, R_{SWX} = MOSFET switch resistance)

Combining the four R_{SWX} terms as R_{SW}, we see that

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESRC_1 + ESRC_2\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 24Ω at +25°C and 15V, and 53Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C_1)$ component, and low FSR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C_1)$ term, but may have the side effect of a net increase in output impedance when $C_1 > 10\mu F$ and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10kHz and $C = C_1 = C_2 = 10\mu F$:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4\ ESRC_1 + ESRC_2$$

$$R_O \cong 46 + 20 + 5 \times ESR_C\Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

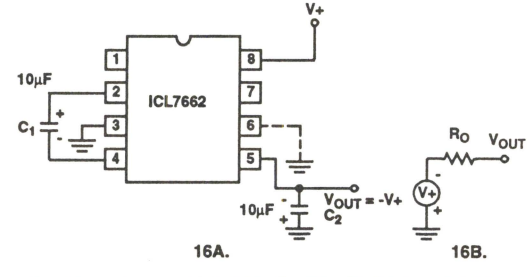


FIGURE 16. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2V, A and B, as shown in Figure 17. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flowing into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is 2 x I_{OUT}, hence the total drop is 2 x I_{OUT} x $ESRC_2$V. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current the load. The drop at B is I_{OUT} x t_2/C_2V. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left(\frac{1}{2 \times f_{PUMP} \times C_2} + 2\ ESRC_2 \times I_{OUT} \right)$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7662 voltage converters may be paralleled (Figure 18) to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7662})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7662 may be cascaded as shown in Figure 19 to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662 R_{OUT} values.

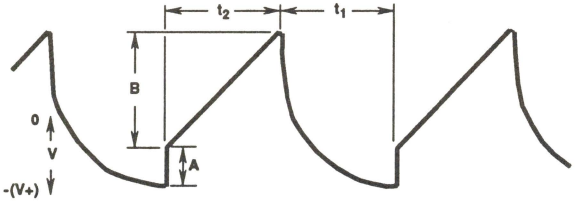


FIGURE 17. OUTPUT RIPPLE

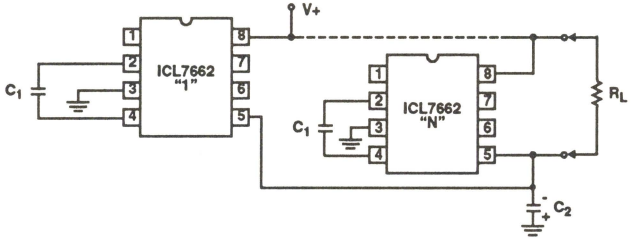


FIGURE 18. PARALLELING DEVICES

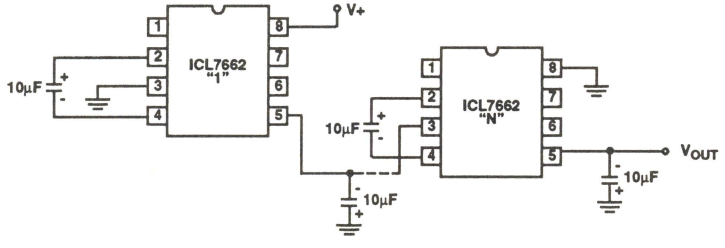


FIGURE 19. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Changing the ICL7662 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 20. In order to prevent possible device latchup, a 1kW resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kW pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, COSC, as shown in Figure 21. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10mF to 100mF).

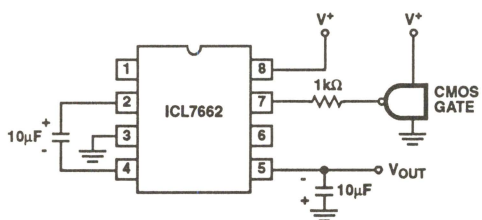


FIGURE 20. EXTERNAL CLOCKING

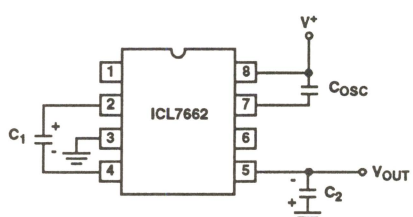
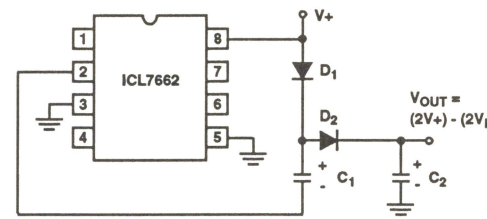


FIGURE 21. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 22. In this application, the pump inverter switches of the ICL7662 are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode C_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) ($2V_F$) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 15V and an output current of 10mA it will be approximately 70Ω.



NOTE: D_1 and D_2 can be any suitable diode.

FIGURE 22. POSITIVE VOLTAGE DOUBLER

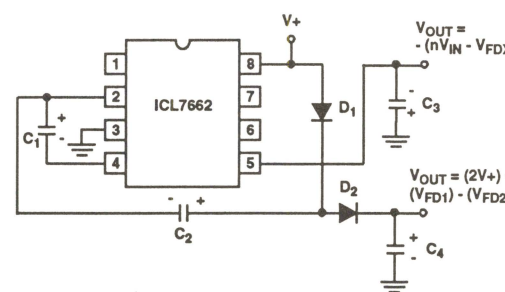


FIGURE 23. COMBINED NEGATIVE CONVERTER AND POSITIVE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 23 combines the functions shown in Figure 16 and Figure 22 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 24. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 19, +30V can be converted (via +15V, and -15V) to a nominal -30V, although with rather high series output resistance (~250Ω).

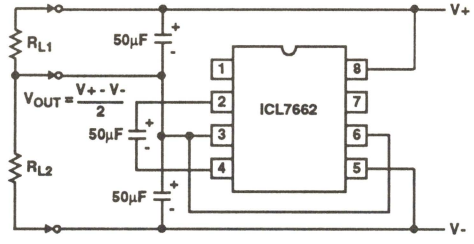


FIGURE 24. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 25 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662s output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

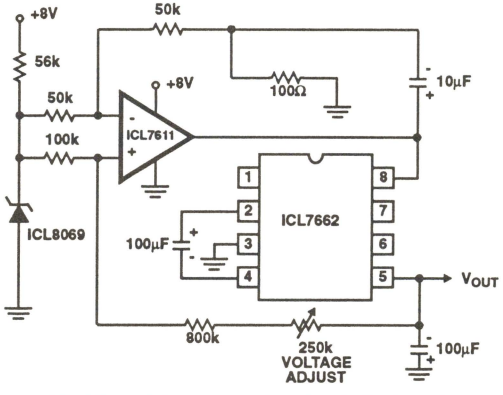


FIGURE 25. REGULATING THE OUTPUT VOLTAGE

Other Applications

Further information on the operation and use of the ICL7662 may be found in A051 "Principles and Applications of the ICL7660 CMOS Voltage Converter".

HARRIS SEMICONDUCTOR

ICL7663S

CMOS Programmable Micropower Positive Voltage Regulator

April 1994

Features

- *Guaranteed* 10μA Maximum Quiescent Current Over *All* Temperature Ranges
- *Wider* Operating Voltage Range - 1.6V to 16V
- *Guaranteed* Line and Load Regulation Over *Entire* Operating Temperature Range *Optional*
- 1% Output Voltage Accuracy (ICL7663SA)
- Output Voltage Programmable from 1.3V to 16V
- *Improved* Temperature Coefficient of Output Voltage
- 40mA Minimum Output Current with Current Limiting
- Output Voltages with Programmable Negative Temperature Coefficients
- Output Shutdown via Current-Limit Sensing or External Logic Level
- Low Input-to-Output Voltage Differential
- Improved Direct Replacement for Industry Standard ICL7663B and Other Second-Source Products

Applications

- Low-Power Portable Instrumentation
- Pagers
- Handheld Instruments
- LCD Display Modules
- Remote Data Loggers
- Battery-Powered Systems

Description

The ICL7663S Super Programmable Micropower Voltage Regulator is a low power, high efficiency positive voltage regulator which accepts 1.6V to 16V inputs and provides adjustable outputs from 1.3V to 16V at currents up to 40mA.

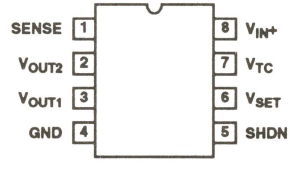
It is a direct replacement for the industry standard ICL7663B offering ***wider*** operating voltage and temperature ranges, ***improved*** output accuracy (ICL7663SA), better temperature coefficient, ***guaranteed*** maximum supply current, and guaranteed line and load regulation. All improvements are highlighted in the electrical characteristics section. ***Critical parameters are guaranteed over the entire commercial and industrial temperature ranges.*** The ICL7663S/SA programmable output voltage is set by two external resistors. The 1% reference accuracy of the ICL7663SA eliminates the need for trimming the output voltage in most applications.

The ICL7663S is well suited for battery powered supplies, featuring 4μA quiescent current, low V_{IN} to V_{OUT} differential, output current sensing and logic input level shutdown control. In addition, the ICL7663S has a negative temperature coefficient output suitable for generating a temperature compensated display drive voltage for LCD displays.

The ICL7663S is available in either an 8 lead Plastic DIP, Ceramic DIP, or SOIC package.

Pinout

ICL7663S (PDIP, CERDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7663SCBA	0°C to +70°C	8 Lead SOIC (N)
ICL7663SCPA		8 Lead Plastic DIP
ICL7663SCJA		8 Lead CerDIP
ICL7663SACBA		8 Lead SOIC (N)
ICL7663SACPA		8 Lead Plastic DIP
ICL7663SACJA		8 Lead CerDIP
ICL7663SIBA	-25°C to +85°C	8 Lead SOIC (N)
ICL7663SIPA		8 Lead Plastic DIP
ICL7663SIJA		8 Lead CerDIP
ICL7663SAIBA		8 Lead SOIC (N)
ICL7663SAIPA		8 Lead Plastic DIP
ICL7663SAIJA		8 Lead CerDIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3180.2**

Absolute Maximum Ratings

Input Supply Voltage . . . . . +18V
Any Input or Output Voltage (Note 1)
  Terminals 1, 2, 3, 5, 6, 7 . . . . . V_{IN}+0.3V to GND-0.3V
Output Source Current
  Terminal 2 . . . . . 50mA
  Terminal 3 . . . . . 25mA
Output Sinking Current
  Terminal 7 . . . . . -10mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	115°C/W	30°C/W
Plastic DIP Package	150°C/W	-
Plastic SOIC Package	180°C/W	-

Maximum Junction Temperature
  Plastic DIP Package . . . . . +150°C
  CerDIP Package . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
  (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
  ICL7663SC . . . . . 0°C to +70°C
  ICL7663SI . . . . . -25°C to +85°C

Electrical Specifications

Specifications Below Applicable to Both ICL7663S and ICL7663SA, Unless Otherwise Specified. $V+_{IN}$ = 9V, V_{OUT} = 5V, T_A = +25°C, Unless Otherwise Specified. Notes 4, 5. See Test Circuit, Figure 7

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	$V+_{IN}$	ICL7663S	T_A = +25°C	1.5	-	16	V
			0°C < T_A < +70°C	1.6	-	16	V
			-25°C < T_A < +85°C	1.6	-	16	V
		ICL7663SA	0°C < T_A < +70°C	1.6	-	16	V
			-25°C < T_A < +85°C	1.6	-	16	V
Quiescent Current	I_Q	1.4V ≤ V_{OUT} ≤ 8.5V, No Load					
		$V+_{IN}$ = 9V	0°C < T_A < +70°C	-	-	10	µA
			-25°C < T_A < +85°C	-	-	10	µA
		$V+_{IN}$ = 16V	0°C < T_A < +70°C	-	-	12	µA
			-25°C < T_A < +85°C	-	-	12	µA
Reference Voltage	V_{SET}	I_{OUT1} = 100µA, V_{OUT} = V_{SET}					
		ICL7663S	T_A = +25°C	1.2	1.3	1.4	V
		ICL7663SA	T_A = +25°C	1.275	1.29	1.305	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	0°C < T_A < +70°C		-	100	-	ppm
		-25°C < T_A < +85°C		-	100	-	ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET} \cdot \Delta V_{IN}}$	2V < V_{IN} < 15V	0°C < T_A < +70°C	-	0.03	-	%/V
			-25°C < T_A < +85°C	-	0.03	0.3	%/V
V_{SET} Input Current	I_{SET}	0°C < T_A < +70°C		-	0.01	10	nA
		-25°C < T_A < +85°C		-	0.01	10	nA
Shutdown Input Current	I_{SHDN}			-	±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN} HI: Both V_{OUT} Disabled		1.4	-	-	V
		V_{SHDN} LO: Both V_{OUT} Enable		-	-	0.3	V
Sense Pin Input Current	I_{SENSE}			-	0.01	10	nA
Sense Pin Input Threshold	V_{CL}			-	0.5	-	V
Input-Output Saturation Resistance (Note 2)	R_{SAT}	$V+_{IN}$ = 2V, I_{OUT1} = 1mA		-	170	350	Ω
		$V+_{IN}$ = 9V, I_{OUT1} = 2mA		-	50	100	Ω
		$V+_{IN}$ = 15V, I_{OUT1} = 5mA		-	35	70	Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	1mA < I_{OUT2} < 20mA		-	1	3	Ω
		50µA < I_{OUT1} < 5mA		-	2	10	Ω

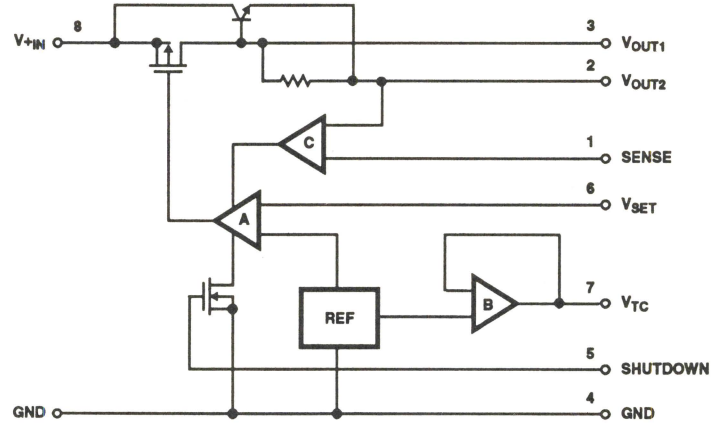
Electrical Specifications Specifications Below Applicable to Both ICL7663S and ICL7663SA, Unless Otherwise Specified. $V+_{IN}$ = 9V, V_{OUT} = 5V, T_A = +25°C, Unless Otherwise Specified. Notes 4, 5. See Test Circuit, Figure 7 **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Available Output Current (V_{OUT2})	I_{OUT2}	3V ≤ V_{IN} ≤ 16V, V_{IN} - V_{OUT2} = 1.5V		40	-	-	mA
Negative Tempco Output (Note 3)	V_{TC}	Open Circuit Voltage		-	0.9	-	V
	I_{TC}	Maximum Sink Current		0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		-	+2.5	-	mV/°C
Minimum Load Current	$I_{L(MIN)}$	Includes V_{SET} Divider	T_A = +25°C	-	-	1.0	µA
			0°C < T_A < +70°C	-	0.2	5.0	µA
			-25°C < T_A < +85°C	-	0.2	5.0	µA

NOTES:

1. Connecting any terminal to voltages greater than ($V+_{IN}$ + 0.3V) or less than (GND - 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663S power-up.
2. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.
3. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 9 for details. Pin will not source current.
4. All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V.
5. All significant improvements over the industry standard ICL7663 are highlighted.

Functional Diagram



Typical Performance Curves

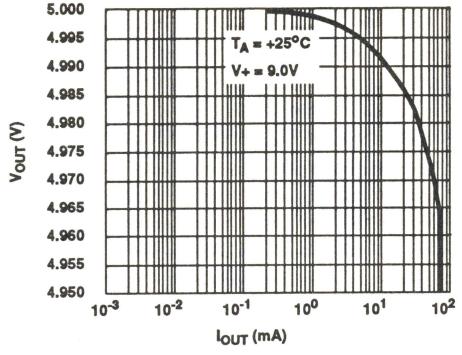


FIGURE 1. V_{OUT2} OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

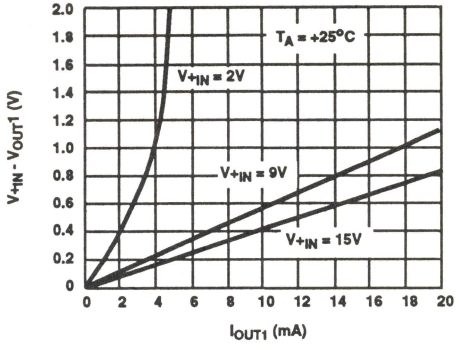


FIGURE 2. V_{OUT1} INPUT-OUTPUT DIFFERENTIAL vs OUTPUT CURRENT

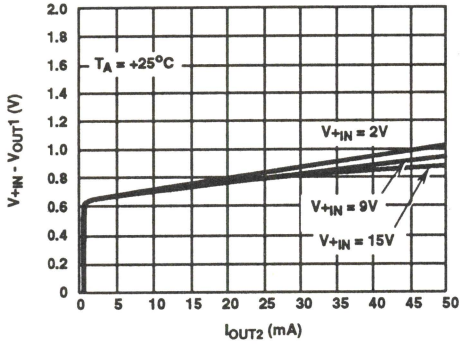


FIGURE 3. V_{OUT2} INPUT-OUTPUT DIFFERENTIAL vs OUTPUT CURRENT

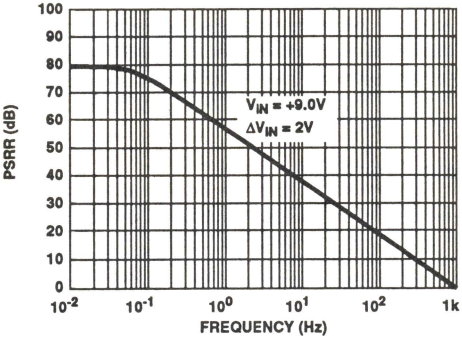


FIGURE 4. INPUT POWER SUPPLY REJECTION RATIO

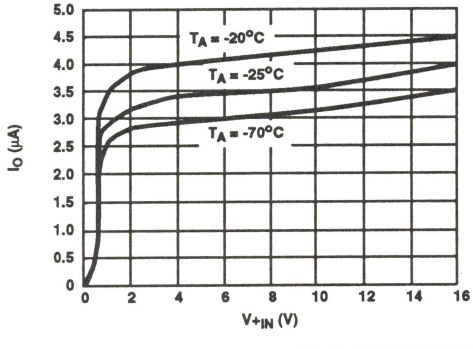


FIGURE 5. QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

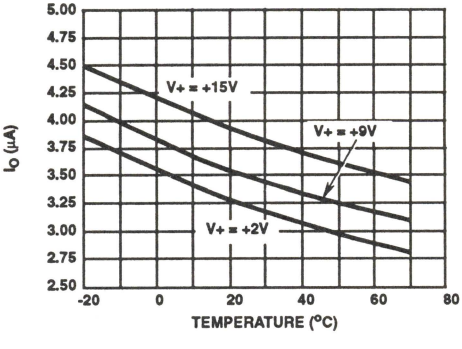


FIGURE 6. QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

Detailed Description

The ICL7663S is a CMOS integrated circuit incorporating all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the Functional Diagram, the main blocks are a bandgap-type voltage reference, an error amplifier, and an output driver with both PMOS and NPN pass transistors.

The bandgap output voltage, trimmed to 1.29V ± 15mV for the ICL7663SA, and the input voltage at the V_{SET} terminal are compared in amplifier A. Error amplifier A drives a P-channel pass transistor which is sufficient for low (under about 5mA) currents. The high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via a N-channel MOS transistor. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} terminal. The ICL7663S has an output (V_{TC}) from a buffer amplifier (B), which can be used in combination with amplifier A to generate programmable-temperature-coefficient output voltages.

The amplifier, reference and comparator circuitry all operate at bias levels well below 1µA to achieve extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

Basic Operation

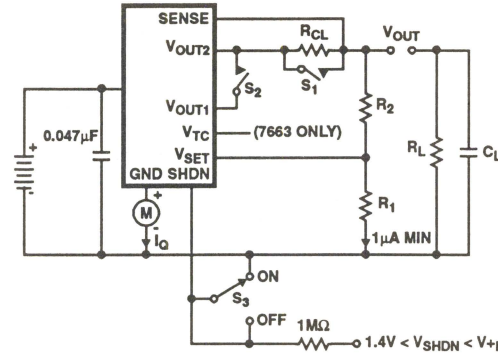
The ICL7663S is designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30mA clearly exceeds the power dissipation rating of the Mini-DIP:

$$(10 - 2)\ (30)\ (10^{-3}) = 240mW$$

The circuit of Figure 8 illustrates proper use of the device.

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or nonoperation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

Input Voltages - The ICL7663S accepts working inputs of 1.5V to 16V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047µF capacitor on the device side of the switch will limit inputs to a safe level around 2V/µs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDowN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.



NOTES:

1. S_1 when closed disables output current limiting.
2. Close S_2 for V_{OUT1}, open S_2 for V_{OUT2}.
3. $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$.
4. IQ quiescent currents measured at GND pin by meter M.
5. S_3 when ON, permits normal operation, when OFF, shuts down both V_{OUT1} and V_{OUT2}.

FIGURE 7. ICL7663S TEST CIRCUIT

Output Voltages - The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET}, to the desired output using the formula $V_{OUT} = (1 + R_2/R_1)\ V_{SET}$. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. In most applications the potentiometer may be eliminated by using the ICL7663SA. The ICL7663SA has V_{SET} voltage guaranteed to be 1.29V ±15mV and when used with ±1% tolerance resistors for R_1 and R_2 the initial output voltage will be within ±2.7% of ideal.

The low leakage current of the V_{SET} terminal allows R_1 and R_2 to be tens of megohms for minimum additional quiescent drain current. However, some load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1µA. This can include the current for R_2 and R_1.

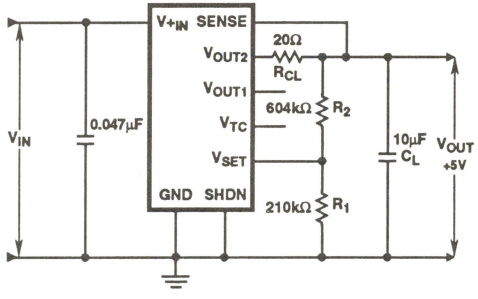
Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1}, terminal. The input-output differential increases to 1.5V when using V_{OUT2}.

Output Currents - Low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Where higher currents are needed, use V_{OUT2} (V_{OUT1}, should be left open in this case).

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing - The on-chip comparator (C in the Functional Diagram) permits shutdown of the regulator

output in the event of excessive current drain. As Figure 8 shows, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2} and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.5V) the voltage feedback is by-passed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.



$$V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET} = 5V$$

$$I_{CL} = \frac{V_{CL}}{R_{CL}} = 25mA$$

FIGURE 8. POSITIVE REGULATOR WITH CURRENT LIMIT

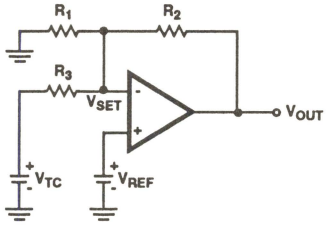
Logic-Controllable Shutdown - When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it is required. This usually means switches, with their unreliable contacts. Instead, the ICL7663S can be shut down by a logic signal, leaving only I_Q (under 4μA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663S will keep the regulator ON, and a voltage level of more than 1.4V but less than $V+_{IN}$ will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input ($V+_{IN}$) the current from this signal should be limited to 100μA maximum by a high value (1MΩ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

Additional Circuit Precautions - This regulator has poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From:

$$I = C\frac{\Delta V}{\Delta t}, C = I_{OUT}\frac{(20 \times 10^{-3})}{0.9V_{OUT}} = 0.022\frac{I_{OUT}}{V_{OUT}}$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see "Current-Limit Sensing").

Producing Output Voltages with Negative Temperature Coefficients - The ICL7663S has an additional output which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R_2/R_3 ratio (see Figure 9 and its design equations).



$$\text{EQ. 1: } V_{OUT} = V_{SET}\left(1 + \frac{R_2}{R_1}\right) + \frac{R_2}{R_3}(V_{SET} - V_{TC})$$

$$\text{EQ. 2: } TC\ V_{OUT} = -\frac{R_2}{R_3}(TC\ V_{TC}) \text{ in mV/°C}$$

Where: $V_{SET} = 1.3V$
$V_{TC} = 0.9V$
$TCV_{TC} = +2.5mV/°C$

FIGURE 9. GENERATING NEGATIVE TEMPERATURE COEFFICIENTS

Applications

Boosting Output Current with External Transistor

The maximum available output current from the ICL7663S is 40mA. To obtain output currents greater than 40mA, an external NPN transistor is used connected as shown in Figure 10.

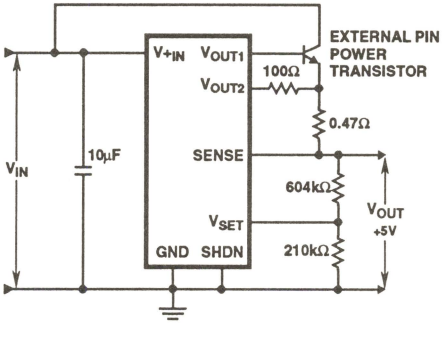


FIGURE 10. BOOSTING OUTPUT CURRENT WITH EXTERNAL TRANSISTOR

Generating a Temperature Compensated Display Drive Voltage

Temperature has an important effect in the variation of threshold voltage in multiplexed LCD displays. As temperature rises, the threshold voltage goes down. For applications where the display temperature varies widely, a temperature compensated display voltage, V_{DISP}, can be generated using the ICL7663S. This is shown in Figure 11 for the ICM7233 triplexed LCD display driver.

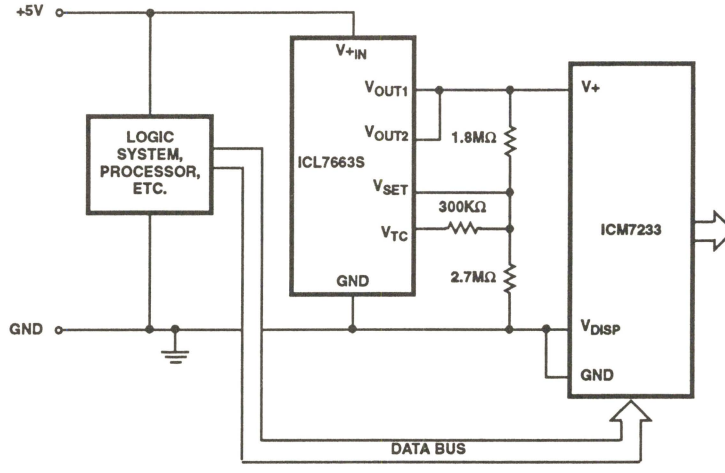


FIGURE 11. GENERATING A MULTIPLEXED LCD DISPLAY DRIVE VOLTAGE

HARRIS SEMICONDUCTOR

ICL7665S

CMOS Micropower Over/Under Voltage Detector

April 1994

Features

- Guaranteed 10μA Maximum Quiescent Current Over Temperature
- Guaranteed Wider Operating Voltage Range Over Entire Operating Temperature Range
- 2% Threshold Accuracy (ICL7665SA)
- Dual Comparator with Precision Internal Reference
- 100ppm/°C Temperature Coefficient of Threshold Voltage
- 100% Tested at 2V
- Output Current Sinking Ability . . . . . Up to 20mA
- Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels

Applications

- Pocket Pagers
- Portable Instrumentation
- Charging Systems
- Memory Power Back-Up
- Battery Operated Systems
- Portable Computers
- Level Detectors

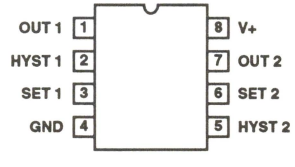
Description

The ICL7665S Super CMOS Micropower Over/Under Voltage Detector contains two low power, individually programmable Voltage detectors on a single CMOS chip. Requiring typically 3μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors. An internal bandgap-type reference provides an accurate threshold voltage while operating from any supply in the 1.6V to 16V range.

The ICL7665S, Super Programmable Over/Under Voltage Detector is a direct replacement for the industry standard ICL7665B offering ***wider*** operating voltage and temperature ranges, ***improved*** threshold accuracy (ICL7665SA), and temperature coefficient, and ***guaranteed*** maximum supply current. All improvements are highlighted in the electrical characteristics section. ***All critical parameters are guaranteed over the entire commercial and industrial temperature ranges.***

Pinout

ICL7665S (SOIC, PDIP, CerDIP)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665SCBA	0° to +70°C	8 Lead SOIC (N)
ICL7665SCPA		8 Lead Plastic DIP
ICL7665SCJA		8 Lead CerDIP
ICL7665SACBA		8 Lead SOIC (N)
ICL7665SACPA		8 Lead Plastic DIP
ICL7665SACJA		8 Lead CerDIP
ICL7665SIBA	-40°C to +85°C	8 Lead SOIC (N)
ICL7665SIPA		8 Lead Plastic DIP
ICL7665SIJA		8 Lead CerDIP
ICL7665SAIBA		8 Lead SOIC (N)
ICL7665SAIPA		8 Lead Plastic DIP
ICL7665SAIJA		8 Lead CerDIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3182.3**

Absolute Maximum Ratings

Supply Voltage (Note 2) ..... -0.3 to +18V
Output Voltages OUT1 and OUT2 ..... -0.3V to 18V (with respect to GND) (Note 2)
Output Voltages HYST1 and HYST2 ..... -0.3V to +18V (with respect to V+) (Note 2)
Input Voltages SET1 and SET2 .....(GND-0.3V) to (V+ V- +0.3V) (Note 2)
Maximum Sink Output OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2..... -25mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	115°C/W	30°C/W
Plastic DIP Package	150°C/W	-
Plastic SOIC Package	180°C/W	-

Maximum Junction Temperature (Plastic)..... +150°C
Maximum Junction Temperature (CerDIP) +175°CStorage Temperature Range .....-65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL7665SC ..... 0°C to +70°C ICL7665SI ..... -40°C to +85°C

Electrical Specifications The specifications below are applicable to both the ICL7665S and ICL7665SA. V+ = 5V, T_A = +25°C, Test Circuit Figure 7. Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+	ICL7665S	T_A = +25°C	1.6	-	16	V
			0°C ≤ T_A ≤ +70°C	1.8	-	16	V
			-25°C ≤ T_A ≤ +85°C	1.8	-	16	V
		ICL7665SA	0°C ≤ T_A ≤ +70°C	1.8	-	16	V
			-25°C ≤ T_A ≤ +85°C	1.8	-	16	V
Supply Current	I+	GND ≤ V_{SET1}, V_{SET2} ≤ V+, All Outputs Open Circuit					
		0°C ≤ T_A ≤ +70°C	V+ = 2V	-	2.5	10	µA
			V+ = 9V	-	2.6	10	µA
			V+ = 15V	-	2.9	10	µA
		-40°C ≤ T_A ≤ +85°C	V+ = 2V	-	2.5	10	µA
			V+ = 9V	-	2.6	10	µA
			V+ = 15V	-	2.9	10	µA
Input Trip Voltage	V_{SET1}	ICL7665S		1.20	1.30	1.40	V
	V_{SET2}			1.20	1.30	1.40	V
	V_{SET1}	ICL7665SA		1.275	1.30	1.325	V
	V_{SET2}			1.275	1.30	1.325	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$	ICL7665S		-	200	-	ppm
		ICL7665SA		-	100	-	ppm
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{2HYST2} = 1MΩ, 2V ≤ V+ ≤ 10V		-	0.03	-	%/V
Output Leakage Currents of OUT and HYST	I_{OLK}	V_{SET} = 0V or V_{SET} ≥ 2V		-	10	200	nA
	I_{HLK}			-	-10	-100	nA
	I_{OLK}	V+ = 15V, T_A = +70°C		-	-	2000	nA
	I_{HLK}			-	-	-500	nA
Output Saturation Voltages	V_{OUT1}	V_{SET1} = 2V, I_{OUT1} = 2mA	V+ = 2V	-	0.2	0.5	V
			V+ = 5V	-	0.1	0.3	V
			V+ = 15V	-	0.06	0.2	V

Electrical Specifications The specifications below are applicable to both the ICL7665S and ICL7665SA. V+ = 5V, T_A = +25°C, Test Circuit Figure 7. Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Saturation Voltages	V_{HYST1}	V_{SET1} = 2V, I_{HYST1} = -0.5mA	V+ = 2V	-	-0.15	-0.30	V
			V+ = 5V	-	-0.05	-0.15	V
			V+ = 15V	-	-0.02	-0.10	V
Output Saturation Voltages	V_{OUT2}	V_{SET2} = 0V, I_{OUT2} = 2mA	V+ = 2V	-	0.2	0.5	V
			V+ = 5V	-	0.15	0.3	V
			V+ = 15V	-	0.11	0.25	V
Output Saturation Voltages	V_{HYST2}	V_{SET2} = 2V	V+ = 2V, I_{HYST2} = -0.2mA	-	-0.25	-0.8	V
			V+ = 5V, I_{HYST2} = -0.5mA	-	-0.43	-1.0	V
			V+ = 15V, I_{HYST2} = -0.5mA	-	-0.35	-0.8	V
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V+		-	0.01	10	nA
Δ Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ, V_{OUT}LO = 1% V+, V_{OUT}HI = 99%V+	ICL7665S	-	1.0	-	mV
			ICL7665SA	-	0.1	-	mV
Difference in Trip Voltages	V_{SET1} - V_{SET2}	R_{OUT}, R_{HYST} = 1mW		-	±5	±50	mV
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1mW	ICL7665S	-	±1	-	mV
			ICL7665SA	-	±0.1	-	mV

NOTES:

1. Derate above +25°C ambient temperature at 4mW/°C
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For these reasons, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665S be turned on first. If this is not possible, current into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.
3. All significant improvements over the industry standard ICL7665 are highlighted.

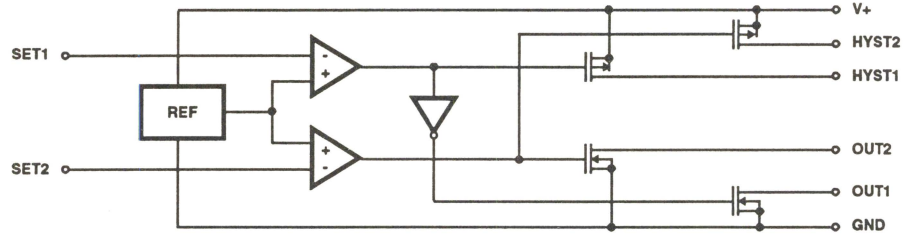
AC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DELAY TIMES						
Input Going HI	t_{SO1D}	V_{SET} Switched between 1.0V to 1.6V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ, C_L = 12pF	-	85	-	µs
	t_{SH1D}		-	90	-	µs
	t_{SO2D}		-	55	-	µs
	t_{SH2D}		-	55	-	µs
Input Going LO	$t_{\overline{S}O1D}$	V_{SET} Switched between 1.6V to 1.0V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ, C_L = 12pF	-	75	-	µs
	$t_{\overline{S}H1D}$		-	80	-	µs
	$t_{\overline{S}O2D}$		-	60	-	µs
	$t_{\overline{S}H2D}$		-	60	-	µs

AC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise Times	t_{O1R}	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF	-	0.6	-	µs
	t_{O2R}		-	0.8	-	µs
	t_{H1R}		-	7.5	-	µs
	t_{H2R}		-	0.7	-	µs
Output Fall Times	t_{O1F}	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF	-	0.6	-	µs
	t_{O2F}		-	0.7	-	µs
	t_{H1F}		-	4.0	-	µs
	t_{H2F}		-	1.8	-	µs

Functional Block Diagram



CONDITIONS (Note 1)
V_{SET1} > 1.3V, OUT1 Switch ON, HYST1 Switch ON
V_{SET1} < 1.3V, OUT1 Switch OFF, HYST1 Switch OFF
V_{SET2} > 1.3V, OUT2 Switch OFF, HYST2 Switch ON
V_{SET2} < 1.3V, OUT2 Switch ON, HYST2 Switch OFF

NOTE:

1. See Electrical Specificationsfor exact thresholds.

Typical Performance Curves

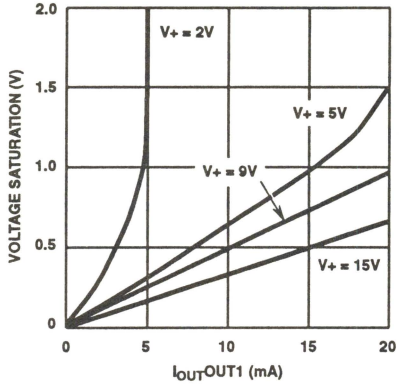


FIGURE 1. OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

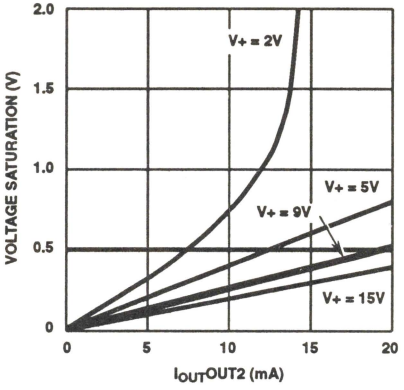


FIGURE 2. OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

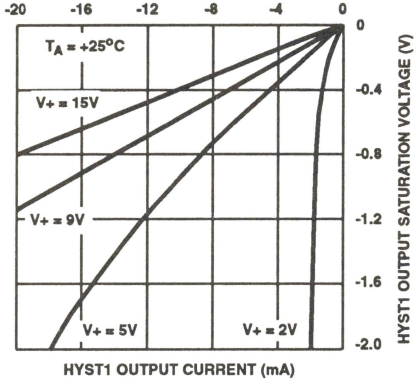


FIGURE 3. HYST1 OUTPUT SATURATION VOLTAGE vs HYST1 OUTPUT CURRENT

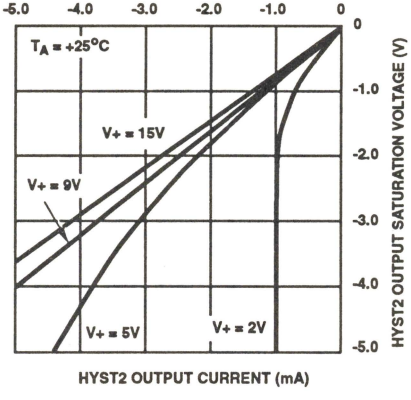


FIGURE 4. HYST2 OUTPUT SATURATION VOLTAGE vs HYST2 OUTPUT CURRENT

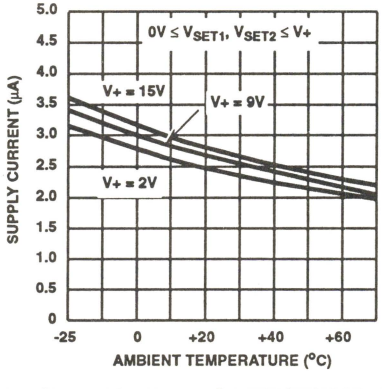


FIGURE 5. SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

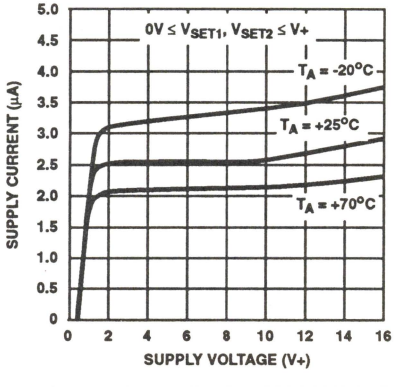


FIGURE 6. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

Detailed Description

As shown in the Functional Diagram, the ICL7665S consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V bandgap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under Voltage Detector and the Over Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal so V_{SET1} will generally not quite equal V_{SET2}.

The input impedance of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

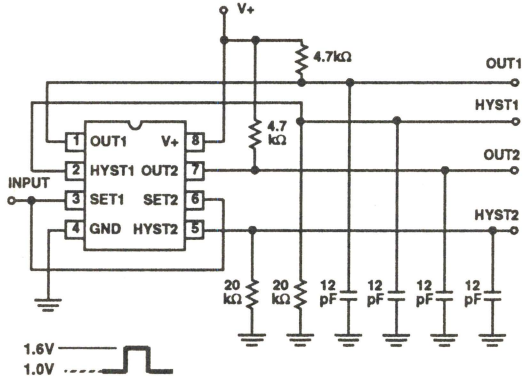


FIGURE 7. TEST CIRCUITS

Precautions

Junction isolated CMOS devices like the ICL7665S have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very low current analog circuits, such as the ICL7665S, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100V/µs in such a circuit. A low impedance capacitor (e.g., 0.05µF disc ceramic) between the V+ and GND pins of the ICL7665S can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

If the SET voltages must be applied before the supply voltage V+, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time.

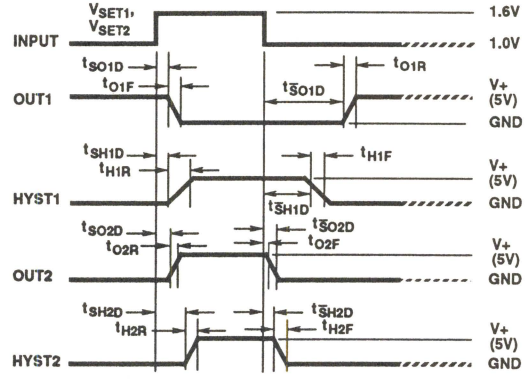


FIGURE 8. SWITCHING WAVEFORMS

Simple Threshold Detector

Figure 9 shows the simplest connection of the ICL7665S for threshold detection. From the graph 9B, it can be seen that at low input voltage OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g., at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equation giving V_{SET1} and V_{SET2} are from Figure 9A:

$$V_{SET1} = V_{IN}\frac{R_{11}}{(R_{11}+R_{21})}\ ;\ V_{SET2} = V_{IN}\frac{R_{12}}{(R_{12}+R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1}\frac{(R_{11}+R_{21})}{R_{11}} = 1.3\frac{(R_{11}+R_{21})}{R_{11}} \quad \text{for detector 1}$$

and

$$V_{TR2} = V_{SET2}\frac{(R_{12}+R_{22})}{R_{12}} = 1.3\frac{(R_{12}+R_{22})}{R_{12}} \quad \text{for detector 2}$$

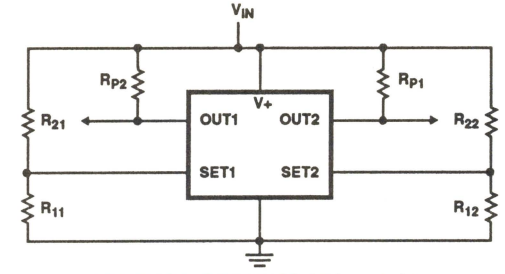


FIGURE 9A. CIRCUIT CONFIGURATION

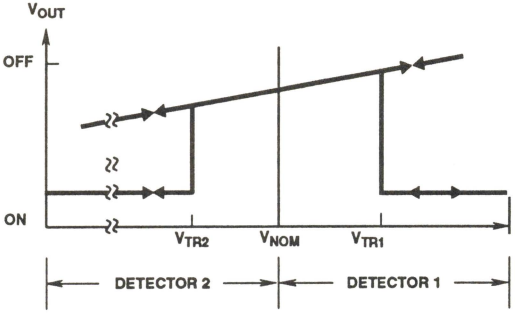


FIGURE 9B. TRANSFER CHARACTERISTICS

FIGURE 9. SIMPLE THRESHOLD DETECTOR

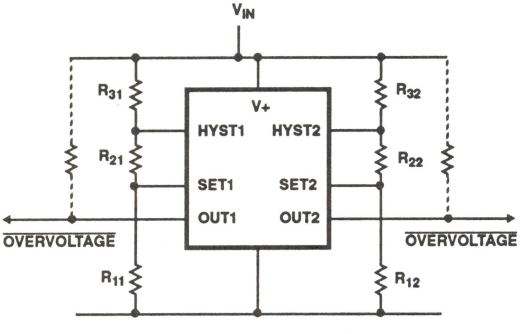


FIGURE 10A. CIRCUIT CONFIGURATION

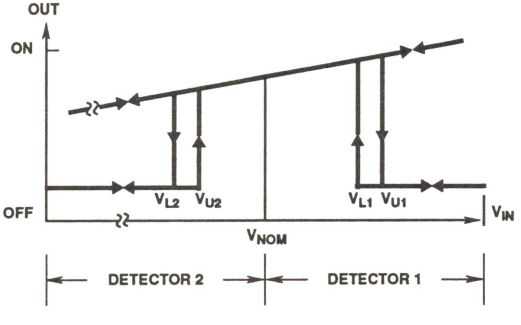


FIGURE 10B. TRANSFER CHARACTERISTICS

FIGURE 10. THRESHOLD DETECTOR WITH HYSTERESIS

Either detector may be used alone, as well as both together, in any of the circuits shown here.

When V_{IN} is very close to one of the trip voltage, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Threshold Detector with Hysteresis

Figure 10A shows how to set up such hysteresis, while Figure 10B shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicated direction of change. The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1N}, R_{2N}, and R_{3N}, until the trip point is reached. As this value is passed, the detector changes state, R_{3N} is shorted out, and the trip point becomes controlled by only R_{1N} and R_{2N}, a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 11. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100kΩ.

$$V_{TR2} = V_{SET2}\frac{(R_{12} + R_{22})}{R_{12}} = 1.3\frac{(R_{12} + R_{22})}{R_{12}} \quad \text{for detector 2}$$

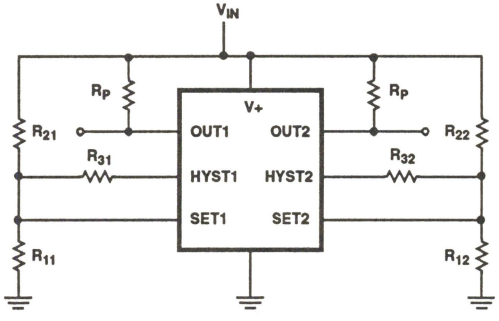


FIGURE 11. AN ALTERNATIVE HYSTERESIS CIRCUIT

TABLE 1. SET-POINT EQUATIONS

NO HYSTERESIS
Over-Voltage $V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Over-Voltage $V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
HYSTERESIS PER FIGURE 10A
$V_{U1} = \frac{R_{11} + R_{21} + R31}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}
$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
$V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$
Under-Voltage V_{TRIP}
$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
HYSTERESIS PER FIGURE 11
$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}
$V_{L1} = \frac{R_{11} + \frac{R_{21}R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$
$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
Over-Voltage V_{TRIP}
$V_{L2} = \frac{R_{12} + \frac{R_{22}R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$

Applications

Single Supply Fault Monitor

Figure 12 shows an over/under voltage fault monitor for a single supply. The over voltage trip point is centered around 5.5V and the under voltage trip point is centered around 4.5V. Both have some hysteresis to prevent erratic output ON and OFF conditions. The two outputs are connected in a wired OR configuration with a pullup resistor to generate a power OK signal.

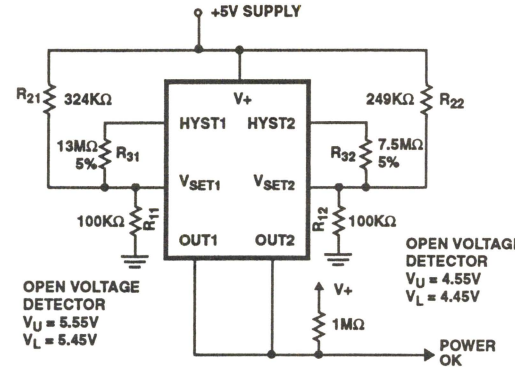


FIGURE 12. FAULT MONITOR FOR A SINGLE SUPPLY

Multiple Supply Fault Monitor

The ICL7665S can simultaneously monitor several supplies when connected as shown in Figure 13. The resistors are chosen such that the sum of the currents through R_{21A}, R_{21B}, and R_{31} is equal to the current through R_{11} when the two input voltage are at the desired low voltage detection point. The current through R_{11} at this point is equal to 1.3V/R_{11}. The voltage at the V_{SET} input depends on the voltage of both supplies being monitored. The trip voltage of one supply while the other supply is at the nominal voltage will be different that the trip voltage when both supplies are below their nominal voltages.

The other side of the ICL7665S can be used to detect the absence of negative supplies. The trip points for OUT1 depend on both the negative supply voltages and the actual voltage of the +5V supply.

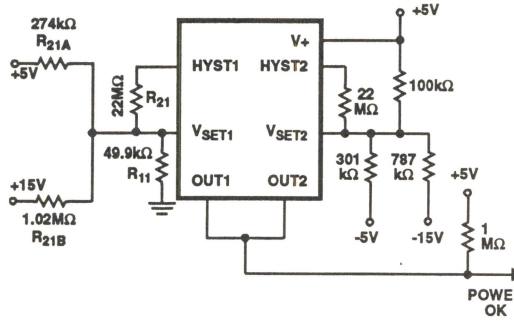


FIGURE 13. MULTIPLE SUPPLY FAULT MONITOR

Combination Low Battery Warning and Low Battery Disconnect

When using rechargeable batteries in a system, it is important to keep the batteries from being overdischarged. The circuit shown in Figure 14 provides a low battery warning and also disconnects the low battery from the rest of the system to prevent damage to the battery. OUT1 is used to shutdown the ICL7663S when the battery voltage drops to the value where the load should be disconnected. As long as V_{SET1} is greater than 1.3V, OUT1 is low, but when V_{SET1} drops below 1.3V, OUT1 goes high shutting off the ICL7663S. OUT2 is used for low battery warning. When V_{SET2} is greater than 1.3V, OUT2 is high and the low battery warning is on. When V_{SET2} drops below 1.3V, OUT2 is low and the low battery warning goes off. The trip voltage for low battery warning can be set higher than the trip voltage for shutdown to give advance low battery warning before the battery is disconnected.

Power Fail Warning and Powerup/Powerdown Reset

Figure 15 shows a power fail warning circuit with powerup/powerdown reset. When the unregulated DC input is above the trip point, OUT1 is low. When the DC input drops below the trip point, OUT1 shuts OFF and the power fail warning goes high. The voltage on the input of the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will provide a certain amount of warning before the 5V output begins to drop.

The ICL7665S OUT2 is used to prevent a microprocessor from writing spurious data to a CMOS battery backup memory by causing OUT2 to go low when the 7805 5V output drops below the ICL7665S trip point.

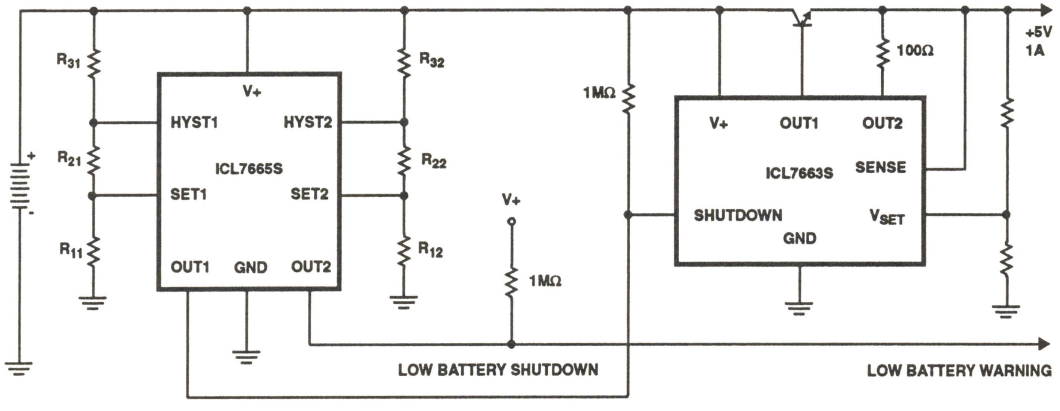


FIGURE 14. LOW BATTERY WARNING AND LOW BATTERY DISCONNECT

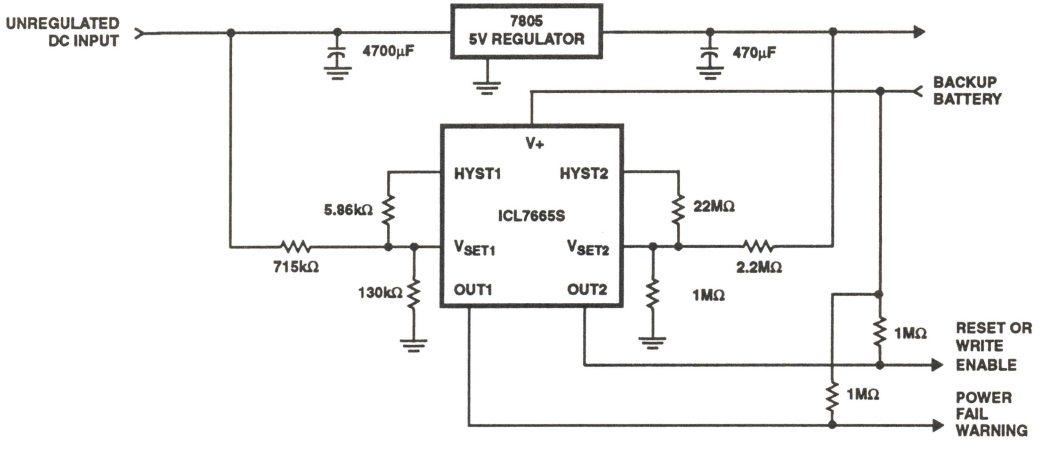


FIGURE 15. POWER FAIL WARNING AND POWERUP/POWERDOWN RESET

Simple High/Low Temperature Alarm

Figure 16 illustrates a simple high/low temperature alarm which uses the ICL7665S with an NPN transistor. The voltage at the top of R_1 is determined by the V_{BE} of the transistor and the position of R_1's wiper arm. This voltage has a negative temperature coefficient. R_1 is adjusted so that V_{SET2} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the high temperature alarm. When this occurs, OUT2 goes low. R_2 is adjusted so that V_{SET1} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the low temperature alarm. When the temperature drops below this limit, OUT1 goes low.

AC Power Fail and Brownout Detector

Figure 17 shows a circuit that detects AC undervoltage by monitoring the secondary side of the transformer. The capacitor, C_1, is charged through R_1 when OUT1 is OFF. With a normal 100 VAC input to the transformer, OUT1 will discharge C_1 once every cycle, approximately every 16.7ms. When the AC input voltage is reduced, OUT1 will stay OFF, so that C_1 does not discharge. When the voltage on C_1 reaches 1.3V, OUT2 turns OFF and the power fail warning goes high. The time constant, R_1C_1, is chosen such that it takes longer than 16.7ms to charge C_1 1.3V.

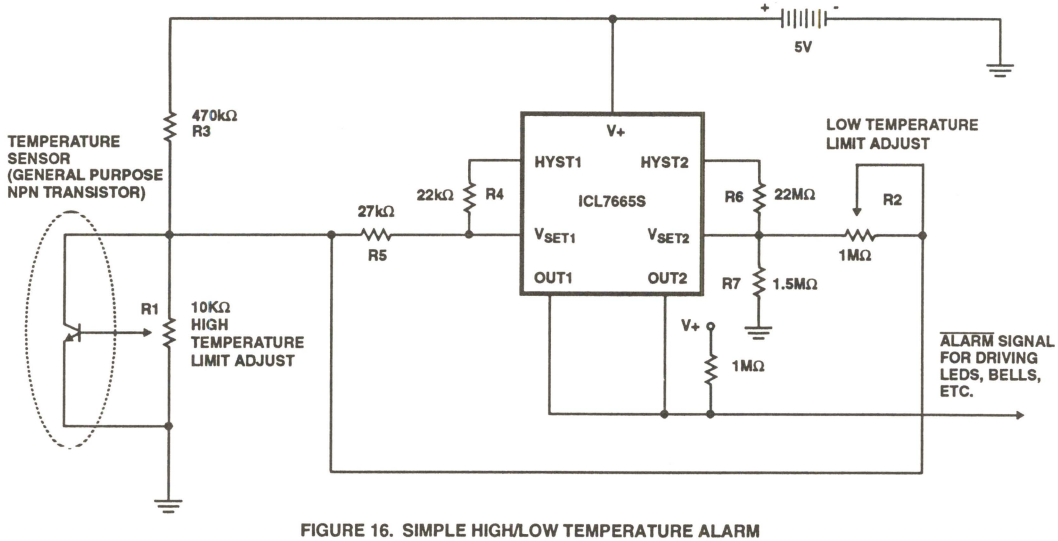


FIGURE 16. SIMPLE HIGH/LOW TEMPERATURE ALARM

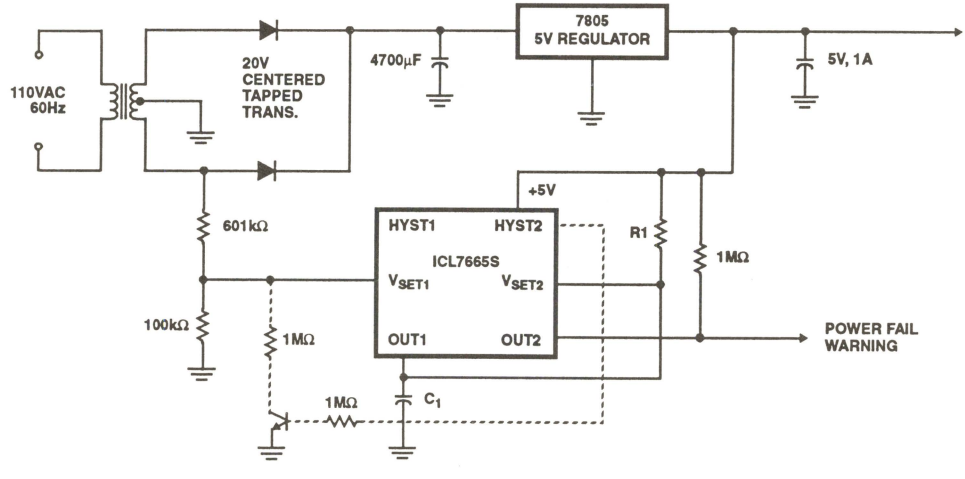


FIGURE 17. AC POWER FAIL AND BROWNOUT DETECTOR

HARRIS SEMICONDUCTOR

ICL7673

April 1994

Automatic Battery Back-Up Switch

Features

- Automatically Connects Output to the Greater of Either Input Supply Voltage
- If Main Power to External Equipment Is Lost, Circuit Will Automatically Connect Battery Backup
- Reconnects Main Power When Restored
- Logic Indicator Signaling Status of Main Power
- Low Impedance Connection Switches
- Low Internal Power Consumption
- Wide Supply Range: ..... 2.5V to 15V
- Low Leakage Between Inputs
- External Transistors May Be Added if Very Large Currents Need to Be Switched

Applications

- On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs
- Over/Under Voltage Detector
- Peak Voltage Detector
- Other Uses:
  - Portable Instruments, Portable Telephones, Line Operated Equipment

Description

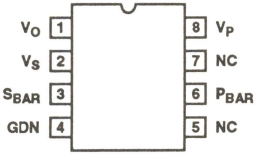
The Harris ICL7673 is a monolithic CMOS battery backup circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alive-battery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

Ordering Information

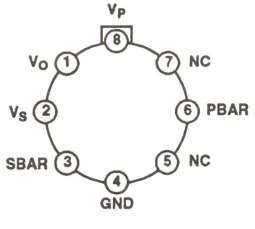
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7673CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7673CBA	0°C to +70°C	8 Lead SOIC (N)
ICL7673ITV	-25°C to +85°C	8 Pin Metal Can

Pinouts

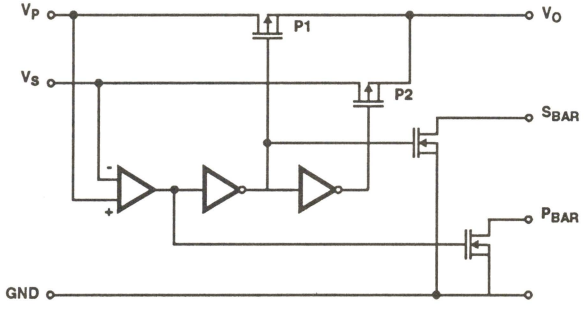
ICL7673 (SOIC, PDIP)
TOP VIEW



ICL7673 (CAN)
TOP VIEW



Functional Block Diagram



$V_P > V_S$, P1 SWITCH ON AND P_{BAR} SWITCH ON
$V_S > V_P$, P2 SWITCH ON AND S_{BAR} SWITCH ON

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3183.1

Absolute Maximum Ratings

Input Supply (V_P or V_S) Voltage ..... GND - 0.3V to +18V
Output Voltages P_{BAR} and S_{BAR} ..... GND - 0.3V to +18V
Peak Current
- Input V_P (at V_P = 5V) See Note. 38mA
- Input V_S (at V_S = 3V) 30mA
- P_{BAR} or S_{BAR} 150mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	150°C/W	-
Plastic SOIC Package	180°C/W	-
Metal Can	156°C/W	68°C/W

Lead Temperature (Soldering, 10sec) ..... 300°C
(SOIC - Lead Tips Only)

NOTE: Derate above +25°C by 0.38mA/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range:
ICL7673C ..... 0°C to +70°C
ICL7673I ..... -25°C to +85°C

Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Electrical Specifications T_A = +25°C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_P	V_S = 0V, I_{LOAD} = 0mA	2.5	-	15	V
	V_S	V_P = 0V, I_{LOAD} = 0mA	2.5	-	15	V
Quiescent Supply Current	I+	V_P = 0V, V_S = 3V, I_{LOAD} = 0mA	-	1.5	5	µA
Switch Resistance P1 (Note 1)	$R_{DS(ON)}P1$	V_P = 5V, V_S = 3V, I_{LOAD} = 15mA	-	8	15	Ω
		At T_A = +85°C	-	16	-	Ω
		V_P = 9V, V_S = 3V, I_{LOAD} = 15mA	-	6	-	Ω
		V_P = 12V, V_S = 3V, I_{LOAD} = 15mA	-	5	-	Ω
Temperature Coefficient of Switch Resistance P1	$T_{C(P1)}$	V_P = 5V, V_S = 3v, I_{LOAD} = 15mA	-	0.5	-	%/°C
Switch Resistance P2 (Note 1)	$R_{DS(ON)}P2$	V_P = 0V, V_S = 3V, I_{LOAD} = 1mA	-	40	100	Ω
		At T_A = +85°C	-	60	-	Ω
		V_P = 0V, V_S = 5V, I_{LOAD} = 1mA	-	26	-	Ω
		V_P = 0V, V_S = 9V, I_{LOAD} = 1mA	-	16	-	Ω
Temperature Coefficient of Switch Resistance P2	$T_{C(P2)}$	V_P = 0V, V_S = 3V, I_{LOAD} = 1mA	-	0.7	-	%/°C
Leakage Current (V_P to V_S)	$I_{L(PS)}$	V_P = 5V, V_S = 3V, I_{LOAD} = 10mA	-	0.01	20	nA
		At T_A = +85°C	-	35	-	nA
Leakage Current (V_P to V_S)	$I_{L(SP)}$	V_P = 0V, V_S = 3V, I_{LOAD} = 10mA	-	0.01	50	nA
		at T_A = +85°C	-	120	-	nA
Open Drain Output Saturation Voltages	V_{OPBAR}	V_P = 5V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	85	400	mV
		At T_A = +85°C	-	120	-	mV
		V_P = 9V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	50	-	mV
		V_P = 12V, V_S = 3V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	40	-	mV
Open Drain Output Saturation Voltages	V_{OSBAR}	V_P = 0V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	150	400	mV
		at T_A = +85°C	-	210	-	mV
		V_P = 0V, V_S = 5V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	85	-	mV
		V_P = 0V, V_S = 9V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	50	-	mV

Electrical Specifications T_A = +25°C Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Currents of P_{BAR} and S_{BAR}	I_{LPBAR}	V_P = 0V, V_S = 15V, I_{LOAD} = 0mA	-	50	500	nA
		at T_A = +85°C	-	900	-	nA
	I_{LSBAR}	V_P = 15V, V_S = 0V, I_{LOAD} = 0mA	-	50	500	nA
		at T_A = +85°C	-	900	-	nA
Switchover Uncertainty for Complete Switching of Inputs and Open Drain Outputs	V_P - V_S	V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 15mA	-	±10	±50	mV

NOTE:
1. The Minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

Typical Performance Curves

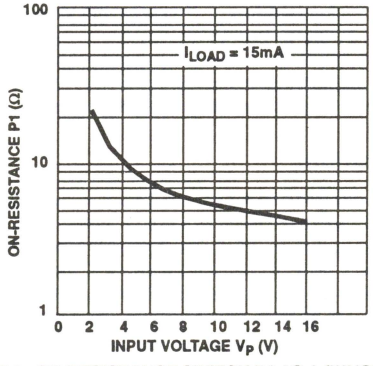


FIGURE 1. ON-RESISTANCE SWITCH P1 AS A FUNCTION OF INPUT VOLTAGE V_P

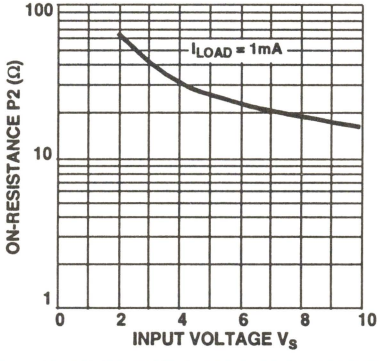


FIGURE 2. ON-RESISTANCE SWITCH P2 AS A FUNCTION OF INPUT VOLTAGE V_S

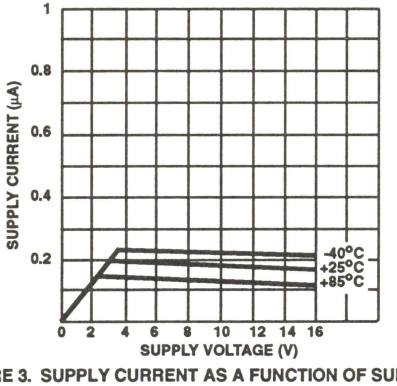


FIGURE 3. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

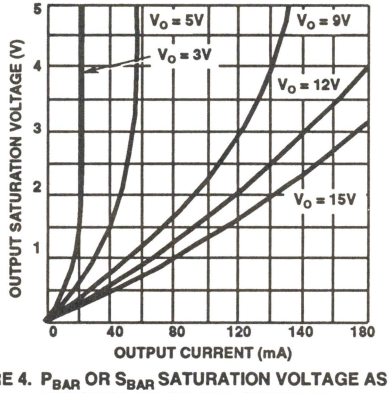


FIGURE 4. P_{BAR} OR S_{BAR} SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

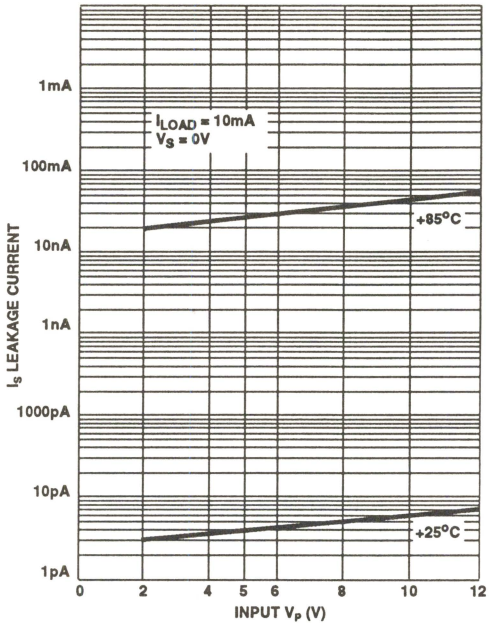


FIGURE 5. I_S LEAKAGE CURRENT V_P TO V_S AS A FUNCTION OF INPUT VOLTAGE

Detailed Description

As shown in the Functional Diagram, the ICL7673 includes a comparator which senses the input voltages V_P and V_S. The output of the comparator drives the first inverter and the open-drain N-Channel transistor P_{BAR}. The first inverter drives a large P-Channel switch, P1, a second inverter, and another open-drain N-Channel transistor, S_{BAR}. The second inverter drives another large P-Channel switch P2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-before-make switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs V_P and V_S must not be allowed to float, and, the difference in the two supplies must be greater than 50mV. The leakage current through the reverse biased parasitic diode of switch P_2 is very low.

Output Voltage

The output operating voltage range is 2.5V to 15V. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-Channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V_O. The ON-resistance of the P-Channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P1 or P2 is 0.5V, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50µs.

Input Voltage

The input operating voltage range for V_P or V_S is 2.5V to 15V. The input supply voltage (V_P or V_S) slew rate should be limited to 2V per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a 0.047µF disc ceramic can be used to reduce the rate-of-rise.

Status Indicator Outputs

The N-Channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

Applications

A typical discrete battery backup circuit is illustrated in Figure 6. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 7, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 8. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663S micropower voltage regulator as shown in Figure 9.

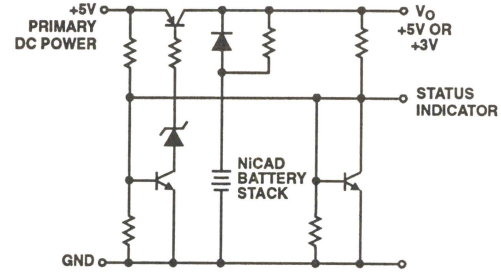


FIGURE 6. DISCRETE BATTERY BACKUP CIRCUIT

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under the voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

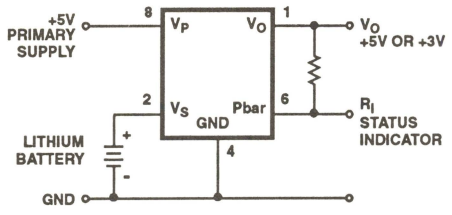


FIGURE 7. ICL7673 BATTERY BACKUP CIRCUIT

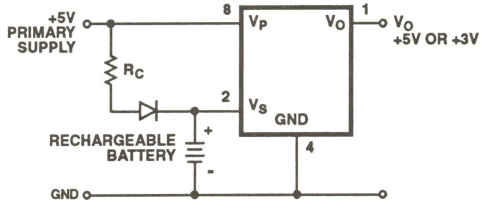


FIGURE 8. APPLICATION REQUIRING RECHARGEABLE BATTERY BACKUP

A typical application, as illustrated in Figure 12, would be a microprocessor system requiring a 5V supply. In the event of primary supply failure, the system is powered down, and a 3V battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to V_P and V_S, with the circuit output V_O supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than V_S and connect, via its internal MOS switches, V_P to output V_O. The backup input, V_S will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect V_P from V_O, and connect V_S.

Figure 11 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

If hysteresis is desired for a particular low power application, positive feedback can be applied between the input V_P and open drain output S_{BAR} through a resistor as illustrated in Figure 12. For high power applications hysteresis can be applied as shown in Figure 13.

The ICL7673 can also be used as a clipping circuit as illustrated in Figure 14. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

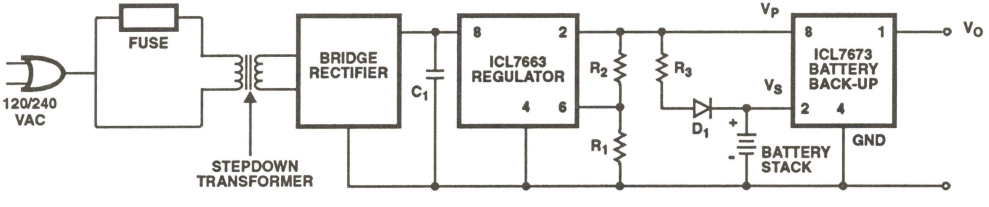


FIGURE 9. POWER SUPPLY FOR LOW POWER PORTABLE AC TO DC SYSTEMS

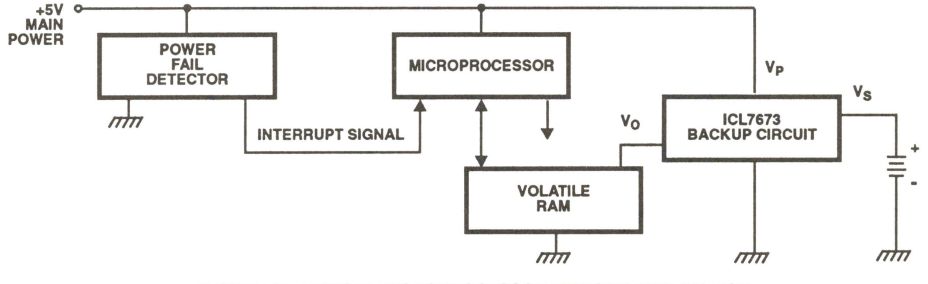


FIGURE 10. TYPICAL MICROPROCESSOR MEMORY APPLICATION

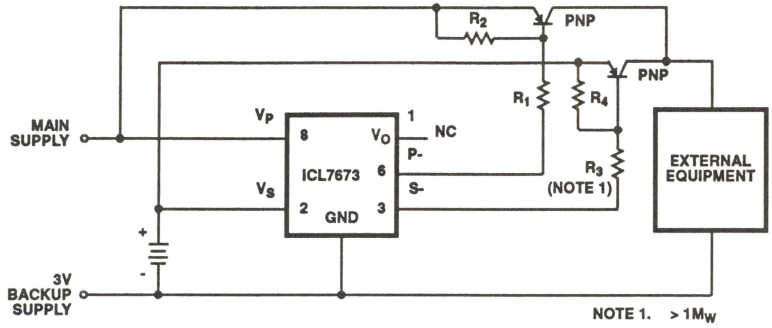


FIGURE 11. HIGH CURRENT BATTERY BACKUP SYSTEM

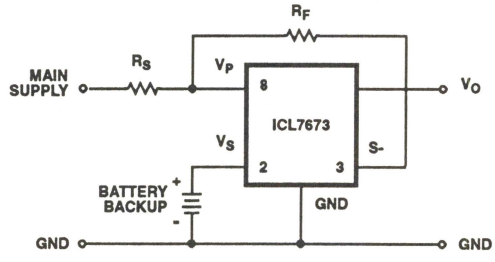


FIGURE 12. LOW CURRENT BATTERY BACKUP SYSTEM WITH HYSTERESIS

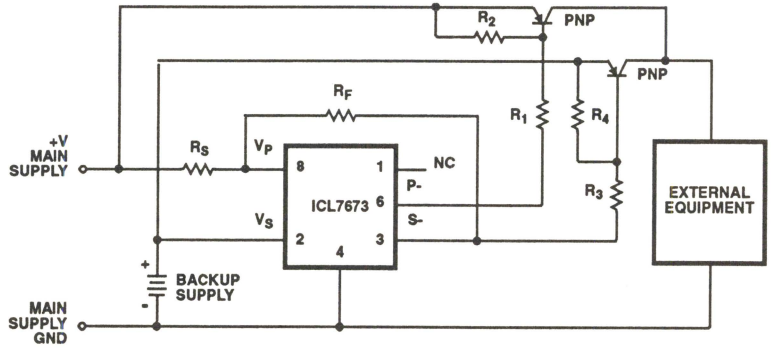


FIGURE 13. HIGH CURRENT BACKUP SYSTEM WITH HYSTERESIS

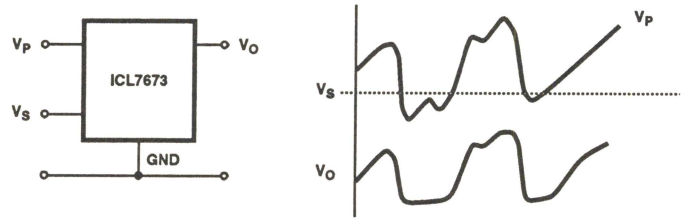


FIGURE 14. CLIPPLING CIRCUITS

ICL8211, ICL8212

April 1994

Programmable Voltage Detectors

Features

- High Accuracy Voltage Sensing and Generation
- Internal Reference 1.15V Typical
- Low Sensitivity to Supply Voltage and Temperature Variations
- Wide Supply Voltage Range Typ. 1.8V to 30V
- Essentially Constant Supply Current Over Full Supply Voltage Range
- Easy to Set Hysteresis Voltage Range
- Defined Output Current Limit ICL8211
- High Output Current Capability ICL8212

Applications

- Low Voltage Sensor/Indicator
- High Voltage Sensor/Indicator
- Nonvolatile Out-of-Voltage Range Sensor/Indicator
- Programmable Voltage Reference or Zener Diode
- Series or Shunt Power Supply Regulator
- Fixed Value Constant Current Source

Description

The Harris ICL8211/8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15V (the internal reference). The ICL8212 requires a voltage in excess of 1.15V to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Ordering Information

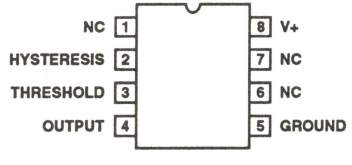
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8211CPA	0°C to +70°C	8 Lead Plastic DIP
ICL8211CBA	0°C to +70°C	8 Lead SOIC (N)
ICL8211CTY	0°C to +70°C	8 Pin Metal Can
ICL8211MTY (Note 1)	-55°C to +125°C	8 Pin Metal Can
ICL8212CPA	0°C to +70°C	8 Lead Plastic DIP
ICL8212CBA	0°C to +70°C	8 Lead SOIC (N)
ICL8212CTY	0°C to +70°C	8 Pin Metal Can
ICL8212MTY (Note 1)	-55°C to +125°C	8 Pin Metal Can

NOTE:

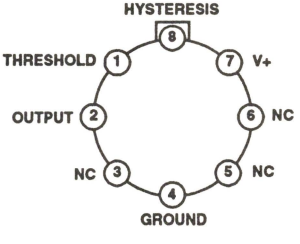
1. Add /883B to part number if 883B processing is required

Pinouts

ICL8211 (PDIP, SOIC)
TOP VIEW



ICL8211 (CAN)
TOP VIEW

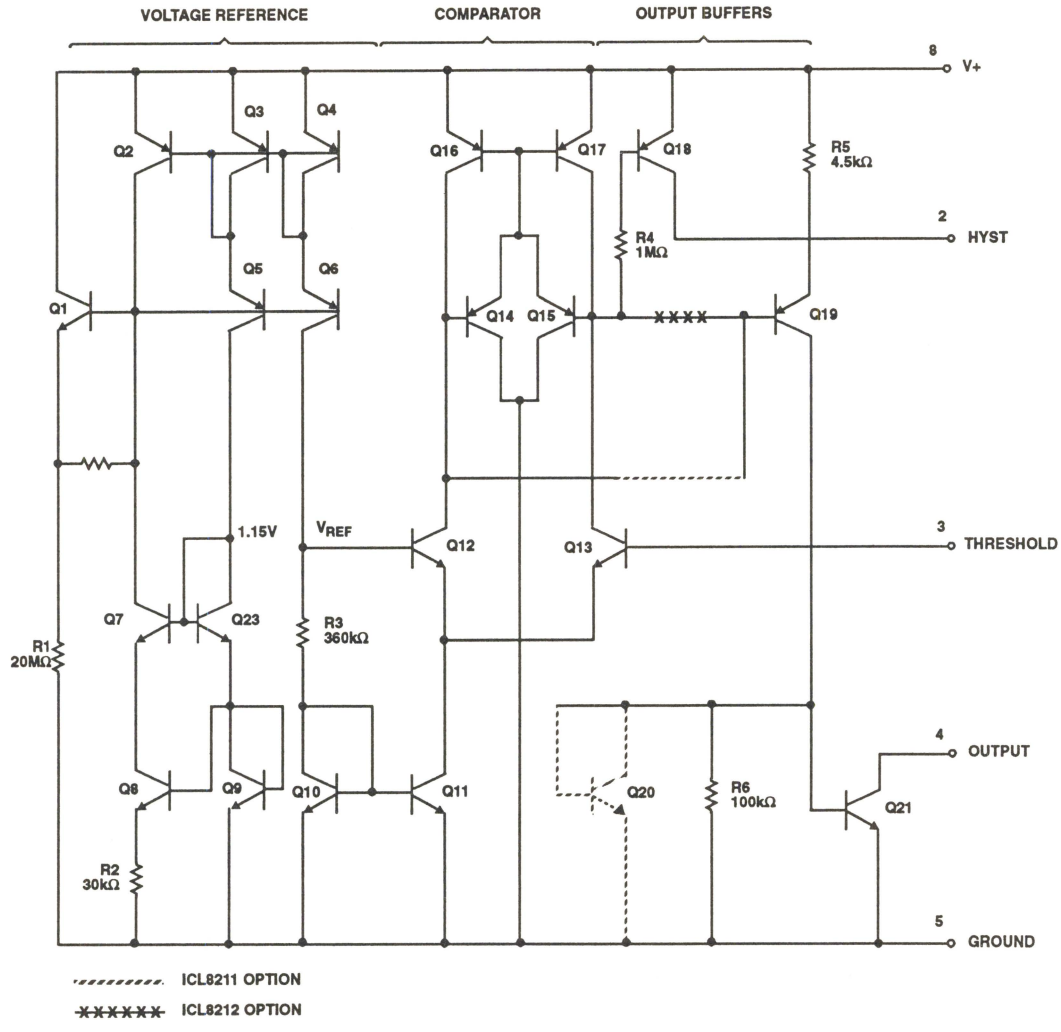


7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3184.1

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +30V
Output Voltage ..... -0.5V to +30V
Hysteresis Voltage ..... +0.5V to -10V
Threshold Input Voltage ..... +30V to -5V with respect to GROUND and +0V to -30V with respect to V+
Current into Any Terminal ..... ± 30mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	150°C/W	-
Plastic SOIC Package	180°C/W	-
Metal Can	156°C/W	68°C/W

Lead Temperature (Soldering, 10s) ..... 300°C
(SOIC - Lead Tips Only)
Current into Any Terminal ..... ± 30mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL8211M/8212M ..... -55°C to +125°C
ICL8211C/8212C ..... 0°C to +70°C

Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications $V+ = 5V$, $T_A = +25°C$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		ICL8211 MIN	ICL8211 TYP	ICL8211 MAX	ICL8212 MIN	ICL8212 TYP	ICL8212 MAX	UNITS
Supply Current	$I+$	$2.0 < V+ < 30$	$V_{TH} = 1.3V$	10	22	40	50	110	250	µA
			$V_{TH} = 0.9V$	50	140	250	10	20	40	µA
Threshold Trip Voltage	V_{TH}	$I_{OUT} = 4mA$, $V_{OUT} = 2V$	$V+ = 5V$	0.98	1.15	1.19	1.00	1.15	1.19	V
			$V+ = 2V$	0.98	1.145	1.19	1.00	1.145	1.19	V
			$V+ = 30V$	1.00	1.165	1.20	1.05	1.165	1.20	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	$I_{OUT} = 4mA$, $I_{HYST} = 7mA$, $V_{OUT} = 2V$, $V_{HYST} = 3V$		-	-0.8	-	-	-0.5	-	mV
Guaranteed Operating Supply Voltage Range	V_{SUPPLY}	+25°C (Note 3)		2.0	-	30	2.0	-	30	V
		0°C to +70°C (Note 3)		2.2	-	30	2.2	-	30	V
Minimum Operating Supply Voltage Range	V_{SUPPLY}	+25°C		-	1.8	-	-	1.8	-	V
		+125°C		-	1.4	-	-	1.4	-	V
		-55°C		-	1.5	-	-	2.5	-	V
Threshold Voltage Temperature Coefficient	$\Delta V_{TH}/\Delta T$	$I_{OUT} = 4mA$, $V_{OUT} = 2V$		-	± 200	-	-	± 200	-	ppm/°C
Variation of Threshold Voltage with Supply Voltage	$\Delta V_{TH}/\Delta V+$	$\Delta V+ = 10\%$ at $V+ = 5V$		-	1.0	-	-	1.0	-	mV
Threshold Input Current	I_{TH}	$V_{TH} = 1.15V$		-	100	250	-	100	250	nA
		$V_{TH} = 1.00V$		-	5	-	-	5	-	nA
Output Leakage Current	I_{OLK}	$V_{OUT} = 30V$	$V_{TH} = 0.9V$	-	-	-	-	-	10	µA
			$V_{TH} = 1.3V$	-	-	10	-	-	-	µA
		$V_{OUT} = 5V$	$V_{TH} = 0.9V$	-	-	-	-	-	1	µA
			$V_{TH} = 1.3V$	-	-	1	-	-	-	µA
Output Saturation Voltage	V_{SAT}	$I_{OUT} = 4mA$	$V_{TH} = 0.9V$	-	0.17	0.4	-	-	-	V
			$V_{TH} = 1.3V$	-	-	-	-	0.17	0.4	V
Max Available Output Current	I_{OH}	(Notes 3 & 4), $V_{OUT} = 5V$	$V_{TH} = 0.9V$	4	7.0	12	-	-	-	mA
			$V_{TH} = 1.3V$	-	-	-	15	35	-	mA
Hysteresis Leakage Current	I_{LHYS}	$V+ = 10V$, $V_{HYST} = GND$	$V_{TH} = 1.0V$	-	-	0.1	-	-	0.1	µA

Electrical Specifications $V+ = 5V$, $T_A = +25°C$ Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		ICL8211			ICL8212			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Hysteresis Sat Voltage	$V_{HYS(MAX)}$	$I_{HYST} = -7\mu A$, measured with respect to V+	$V_{TH} = 1.3V$	-	-0.1	-0.2	-	-0.1	-0.2	V
Max Available Hysteresis Current	$I_{HYS\ (MAX)}$		$V_{TH} = 1.3V$	-15	-21	-	-15	-21	-	µA

Electrical Specifications **ICL8211MTY/8212MTY** $V+ = 5V$, $T_A = -55°C$ to $+125°C$

PARAMETER	SYMBOL	TEST CONDITIONS		ICL8211			ICL8212			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I+	$2.8 < V+ < 30$		-	-	-	-	-	-	-
		$V_T = 1.3V$		-	-	100	-	350	350	µA
		$V_T = 0.8V$		-	-	350	-	100	100	µA
Threshold Trip Voltage	V_{TH}	$I_{OUT} = 2mA$, $V_{OUT} = 2V$	$V+ = 2.8V$	0.80	-	1.30	0.80	-	1.30	V
			$V+ = 30V$	0.80	-	1.30	0.80	-	1.30	V
Guaranteed Operating Supply Voltage Range	V_{SUPPLY}	(Note 5)		2.8	-	30	2.8	-	30	V
Threshold Input Current	I_{TH}	$V_{TH} = 1.15V$		-	-	400	-	-	400	nA
Output Leakage Current	I_{OLK}	$V_{OUT} = 30V$	$V_{TH} = 0.8V$	-	-	-	-	-	20	µA
			$V_{TH} = 1.3V$	-	-	20	-	-	-	µA
Output Saturation Voltage	V_{SAT}	$I_{OUT} = 3mA$	$V_{TH} = 0.8V$	-	-	0.5	-	-	-	V
			$V_{TH} = 1.3V$	-	-	-	-	-	0.5	V
Max Available Output Current	I_{OH}	(Notes 3 & 4) $V_{OUT} = 5V$	$V_{TH} = 0.8$	3	-	15	-	-	-	mA
			$V_{TH} = 1.3V$	-	-	-	9	-	-	mA
Hysteresis Leakage Current	I_{LHYS}	$V+ = 10V$, $V_{HYST} = GND$	$V_{TH} = 0.8V$	-	-	0.2	-	-	0.2	µA
Hysteresis Saturation Voltage	$V_{HYS(MAX)}$	$I_{HYST} = -7\mu A$ measured with respect to V+	$V_{TH} = 1.3V$	-	-	0.3	-	-	0.3	V
Max Available Hysteresis Current	$I_{HYS\ (MAX)}$		$V_{TH} = 1.3V$	10	-	-	10	-	-	µA

NOTES:

1. The maximum output current of the ICL8211 is limited by design to 15mA under any operating conditions. The output voltage may be sustained at any voltage up to +30V as long as the maximum power dissipation of the device is not exceeded.
2. The maximum output current of the ICL8212 is not defined. And systems using the ICL8212 must therefore ensure that the output current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.
3. Threshold Trip Voltage is 0.80V(min) to 1.30V(mas). At $I_{OUT} = 3mA$.

Typical Performance Curves (ICL8211 and ICL8212)

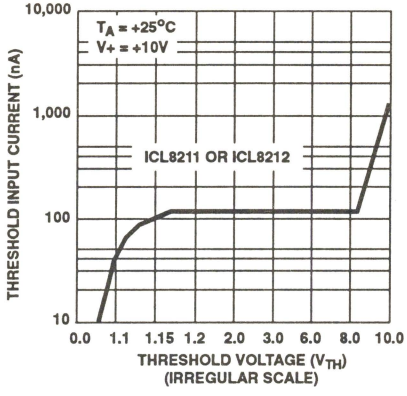


FIGURE 1. THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE

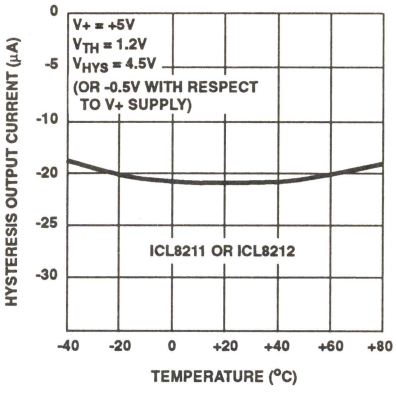


FIGURE 2. HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

Typical Performance Curves (ICL8211 ONLY)

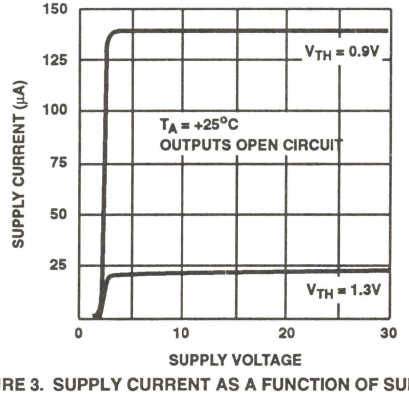


FIGURE 3. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

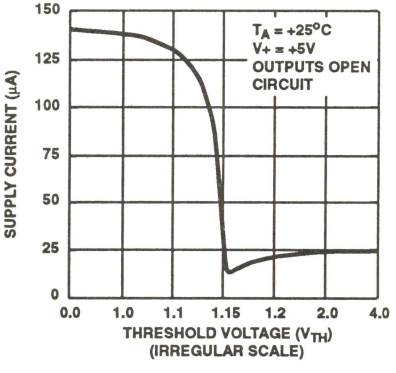


FIGURE 4. SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE

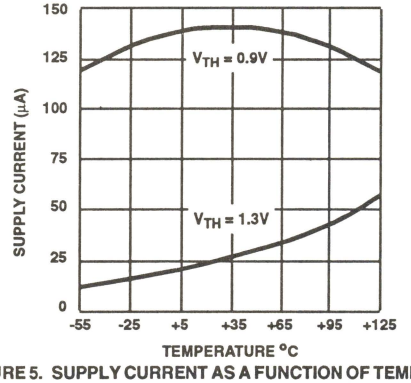


FIGURE 5. SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

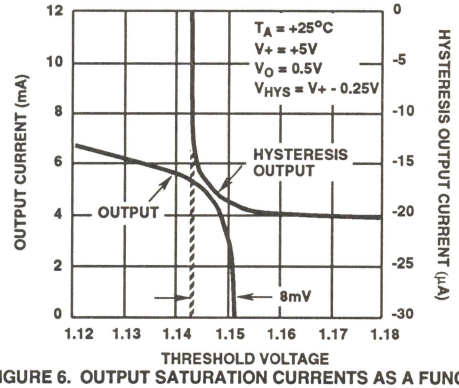


FIGURE 6. OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE

Typical Performance Curves (ICL8211 ONLY) (Continued)

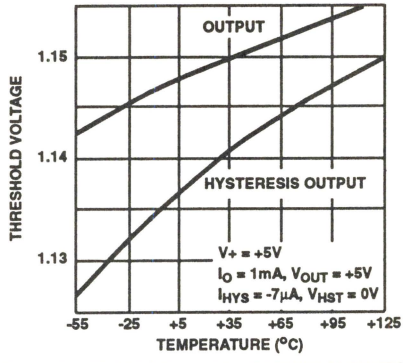


FIGURE 7. THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE

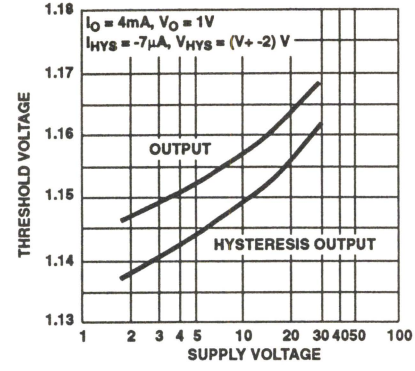


FIGURE 8. THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

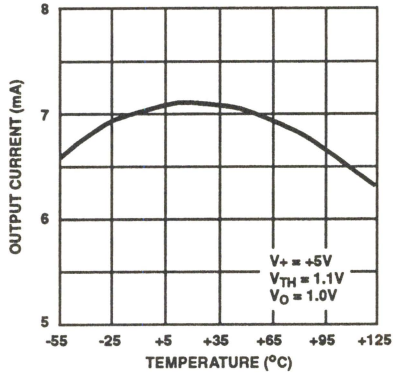


FIGURE 9. OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

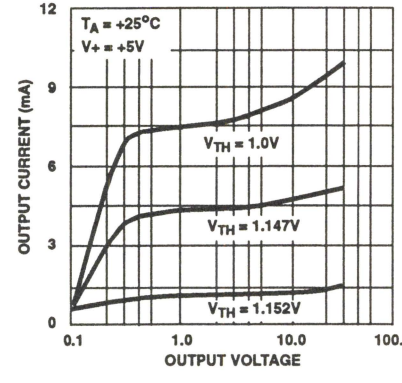


FIGURE 10. OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

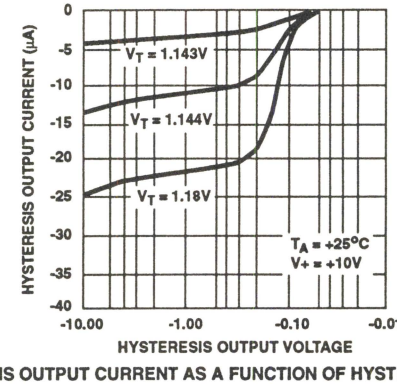


FIGURE 11. HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE

Typical Performance Curves (ICL8212 ONLY)

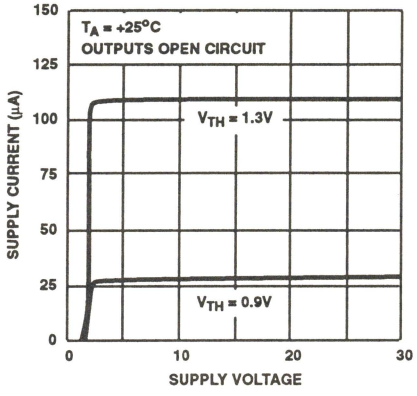


FIGURE 12. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

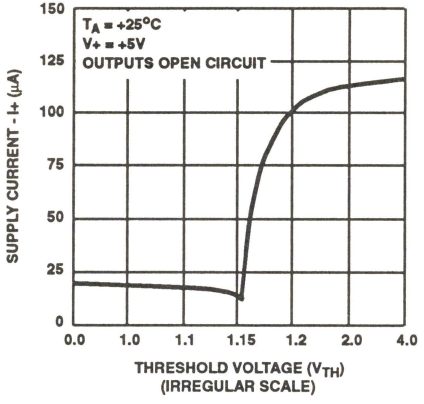


FIGURE 13. SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE

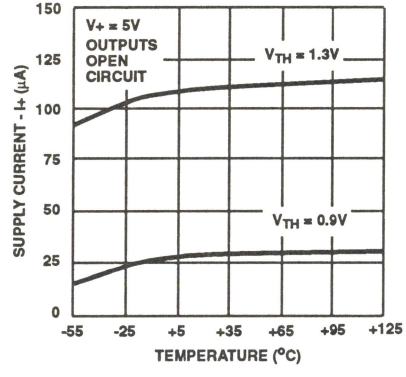


FIGURE 14. SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

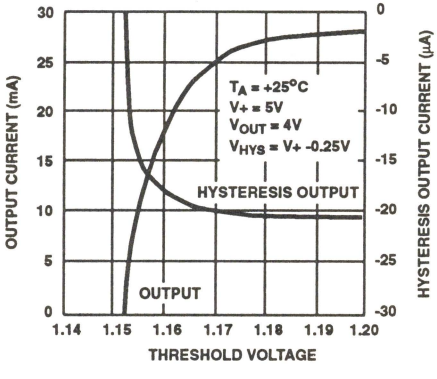


FIGURE 15. OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE

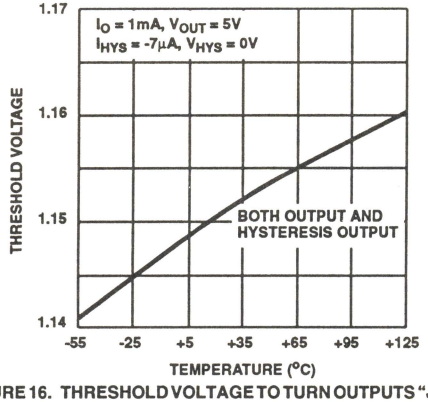


FIGURE 16. THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE

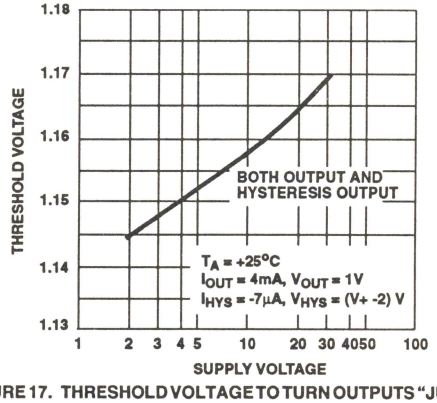


FIGURE 17. THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Curves

(ICL8212 ONLY) **(Continued)**

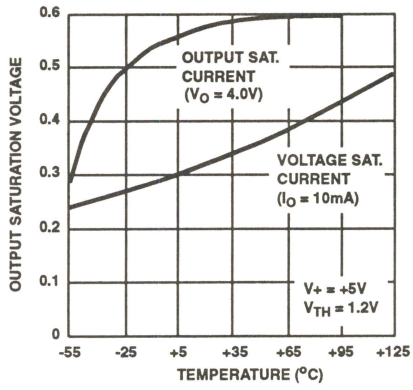


FIGURE 18. OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE

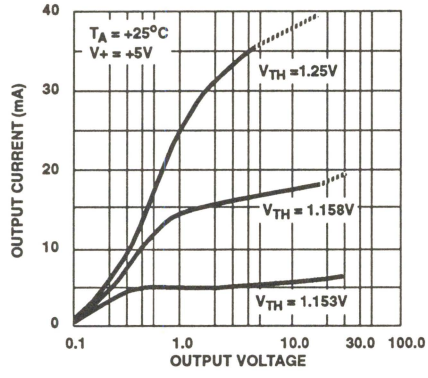


FIGURE 19. OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

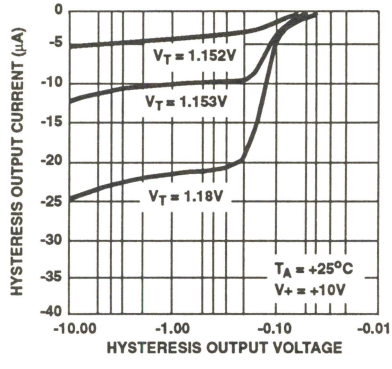


FIGURE 20. HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE

Detailed Description

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q_1 through Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15V. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (-5000 ppm per °C).

Components Q_2 through Q_9 and R_2 make up a constant current source; Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9, and due to the current mirror, the collector currents of Q_8 and Q_9 are forced to be equal and it can be shown that the collector current in Q_8 and Q_9 is

$$IC\ (Q_8 \text{ or } Q_9) = \frac{1}{R2} \times \frac{kT}{q} \ln 7$$

or approximately 1µA at +25°C

Where k = Boltzman's Constant
q = Charge on an Electron
and T = Absolute Temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the V_{CE} of Q_3, Q_4, and Q_9 remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of Q_1 provides sufficient start up current for the constant source; there being two stable states for this type of circuit - either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; Q_{10} is matched to Q_9. Thus the IC and V_{BE} of Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

$$\text{Thus } 1.5 = V_{BE}\ (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q}$$

$$\text{which provides: } \frac{R_3}{R_2} = 12 \text{ (approximately.)}$$

The total supply current consumed by the voltage reference section is approximately 6µA at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15V by the comparator consisting of transistors Q_{11} through Q_{17}. The outputs from the comparator are limited to two diode drops less than V+ or approximately 1.1V. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100µA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximately 7mA, whereas for the ICL8212

almost all the collector current of Q_{19} is available for base drive to Q_{21}, resulting in a maximum available collector current of the order of 30mA. It is advisable to externally limit this current to 25mA or less.

Applications

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

General Information

Threshold Input Considerations

Although any voltage between -5V and V+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6V since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

The outputs change states with an input THRESHOLD voltage of approximately 1.15V. Input and output waveforms are shown in Figure 21 for a simple 1.15V level detector.

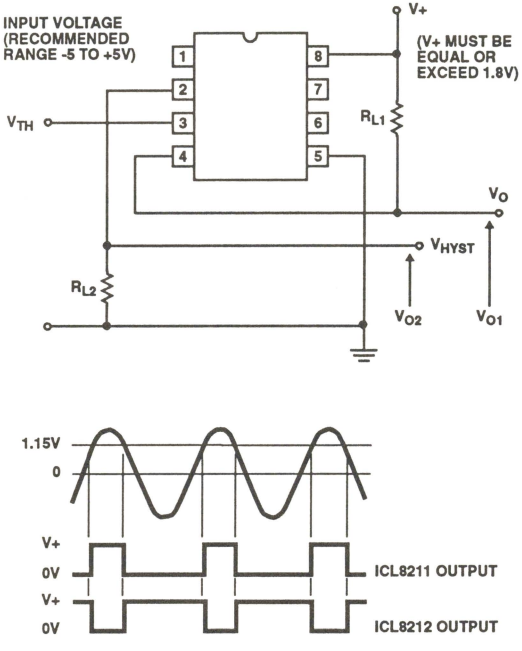


FIGURE 21. VOLTAGE LEVEL DETECTION

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10μA or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or CMOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for V_{TH}. For high accuracy, currents as large as 50μA may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as 6mA may be considered without a great loss of accuracy. 6mA represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.

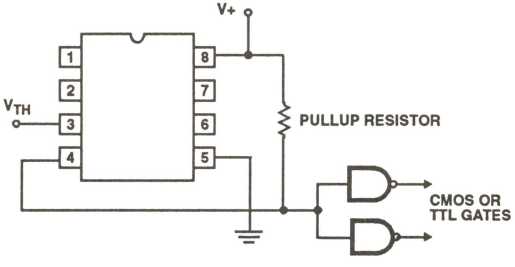


FIGURE 22. OUTPUT LOGIC INTERFACE

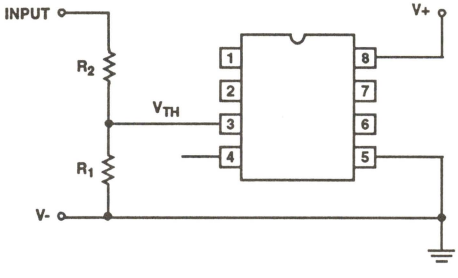


FIGURE 23. INPUT RESISTOR NETWORK CONSIDERATIONS

Case 1. High accuracy required, current in resistor network unimportant Set I = 50μA for V_{TH} = 1.15V ∴ $R_1 \rightarrow$ 20kΩ

Case 2. Good accuracy required, current in resistor network important Set I = 7.5μA for V_{TH} = 1.15V ∴ $R_1 \rightarrow$ 150kΩ

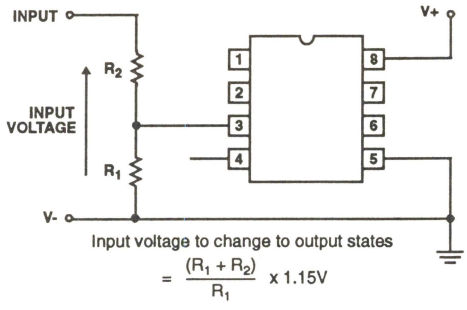


FIGURE 24. RANGE OF INPUT VOLTAGE GREATER THAN +1.15 VOLTS

Setup Procedures For Voltage Level Detection

Case 1. Simple voltage detection no hysteresis

Unless an input voltage of approximately 1.15V is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 25 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.

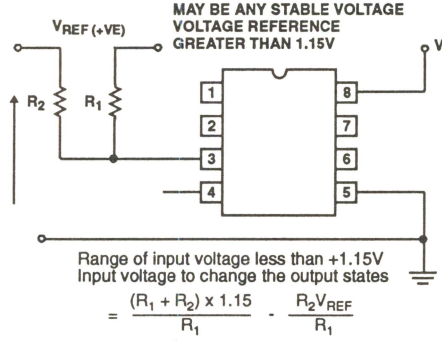


FIGURE 25. INPUT RESISTOR NETWORK SETUP PROCEDURES

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 26.

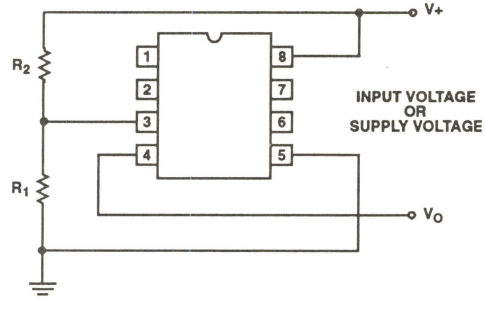


FIGURE 26. COMBINED INPUT AND SUPPLY VOLTAGES

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications-refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 27.

The circuit of Figure 27A requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output, whereas for circuit Figure 27B the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis, circuit Figure 27B is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

Practical Applications

Low Voltage Battery Indicator (Figure 28)

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35µA which will increase to 7mA when the lamp is turned on. R_3 will provide hysteresis if required.

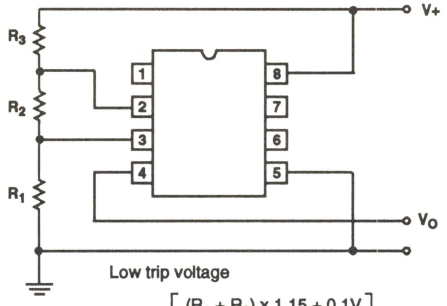
Nonvolatile Low Voltage Detector (Figure 29)

In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S_1 the operating point changes to B and will remain at B until the supply voltage drops below VTR1, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

Nonvolatile Power Supply Malfunction Recorde (Figure 30 and Figure 31)

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may



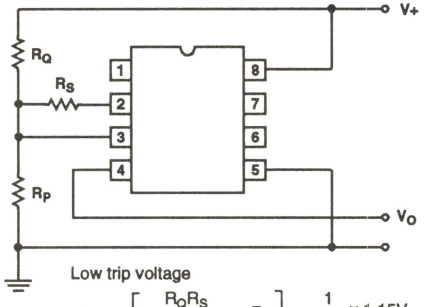
Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2) \times 1.15 + 0.1V}{R_1}\right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15V$$

FIGURE 27A.



Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + R_P\right] \times \frac{1}{R_P} \times 1.15V$$

High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15V$$

FIGURE 27B.

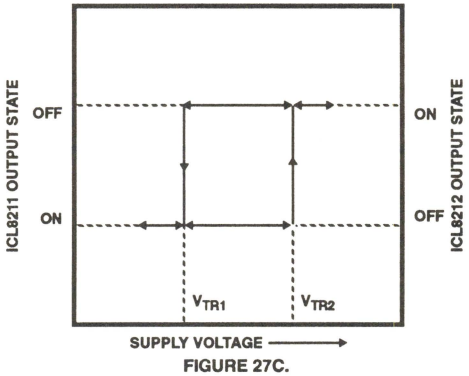
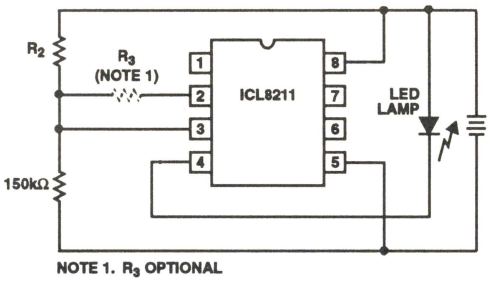


FIGURE 27C.

FIGURE 27. TWO ATERNATIVE VOLTAGE DETECTION CIRCUITS EMPLOYING HYSTERESIS TO PROVIDE PAIRS OF WELL DEFINED TRIP VOLTAGES



NOTE 1. R_3 OPTIMAL

FIGURE 28. LOW VOLTAGE BATTERY INDICATOR

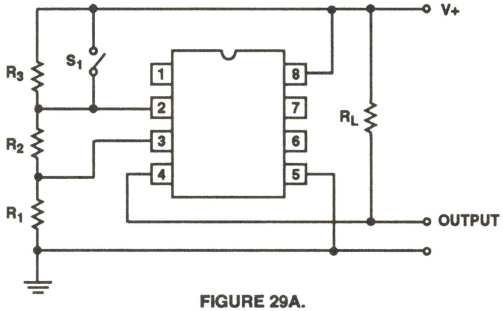


FIGURE 29A.

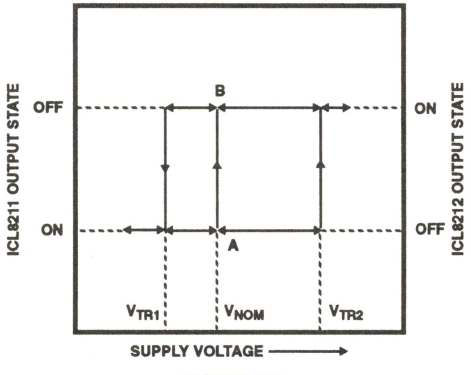


FIGURE 29B.

FIGURE 29. NON-VOLATILE LOW VOLTAGE INDICATOR

have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30V without exceeding the maximum ratings of the ICs. The two voltage limits defining the in range supply voltage may be set to any value between 2.0V and 30V.

The ICL8212 is used to detect a voltage, V_2, which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 - the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R3 for values of supply voltage between V_1 and V_2.

Constant Current Sources (Figure 32)

The ICL8212 may be used as a constant current source of value of approximately 25μA by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a 130μA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2V to 30V. These constant current sources may be used to provide basing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

Programmable Zener Voltage Reference (Figure 33)

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

$$V_{ZENER} = \frac{(R_1 + R_2)}{R_1} \times 1.15V.$$

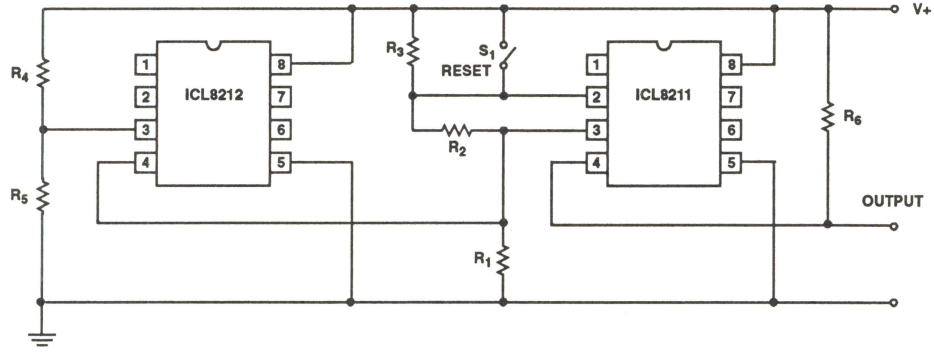


FIGURE 30. NON-VOLATILE POWER SUPPLY MALFUNCTION RECORDER

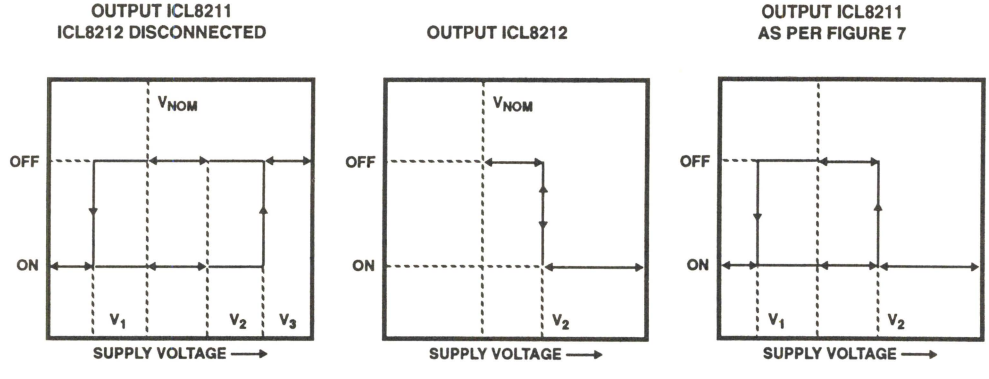


FIGURE 31. OUTPUT STATES OF THE ICL8211 AND ICL8212 AS A FUNCTION OF THE SUPPLY VOLTAGE

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2V to 30V may be programmed and typical impedance values between 300μA and 25μA will range from 4Ω to 7Ω. The knee is sharper and occurs at a significantly lower current than other similar devices available.

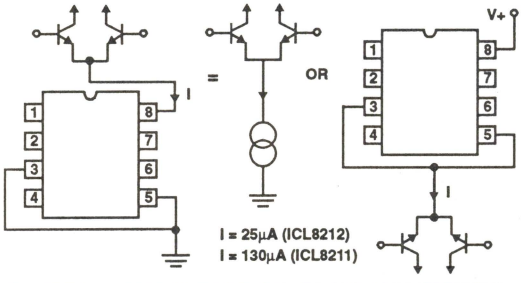


FIGURE 32. CONSTANT CURRENT SOURCE APPLICATIONS

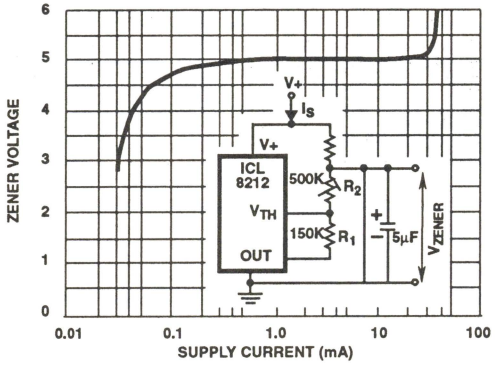


FIGURE 33. PROGRAMMABLE ZENER VOLTAGE REFERENCE

Precision Voltage Regulator (Figure 34)

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

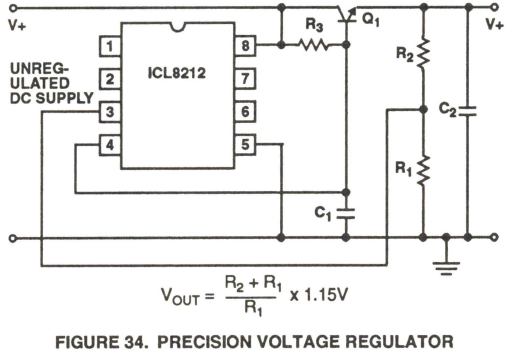


FIGURE 34. PRECISION VOLTAGE REGULATOR

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

High Supply Voltage Dump Circuit (Figure 35)

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

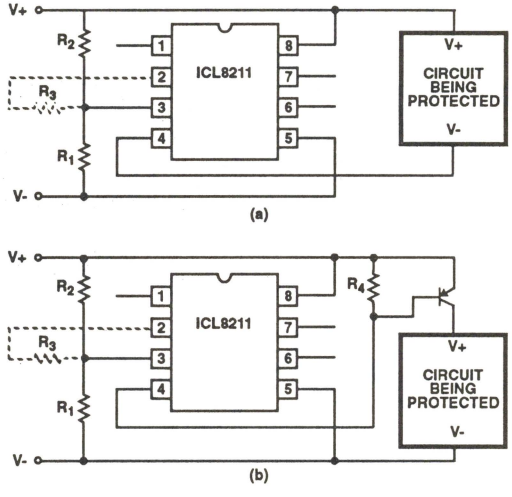


FIGURE 35. HIGH VOLTAGE DUMP CIRCUITS

Frequency Limit Detector (Figure 36)

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/8212. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3. The time constant of R_7 C_3 Is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

Switch Bounce Filter (Figure 37)

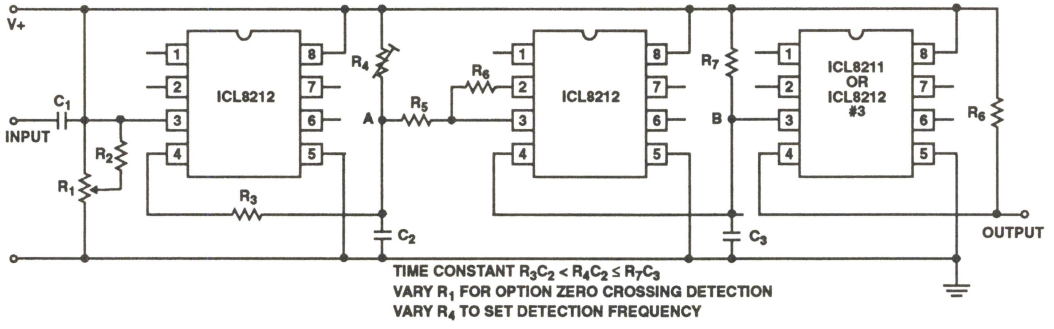
Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches.

SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times. The circuit shown in Figure 37 provides a rapid charge up of C_1 to close to the positive supply voltage (V_1) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of R_1 C_1 to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/8212 will be a single transition of state per desired switch closure

Low Voltage Power Disconnect (Figure 38)

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9V causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9V and turn the power supply off to the LM199 heater section below that voltage.

For further applications, see AN027 "Power Supply Design using the ICL8211 and ICL8212."



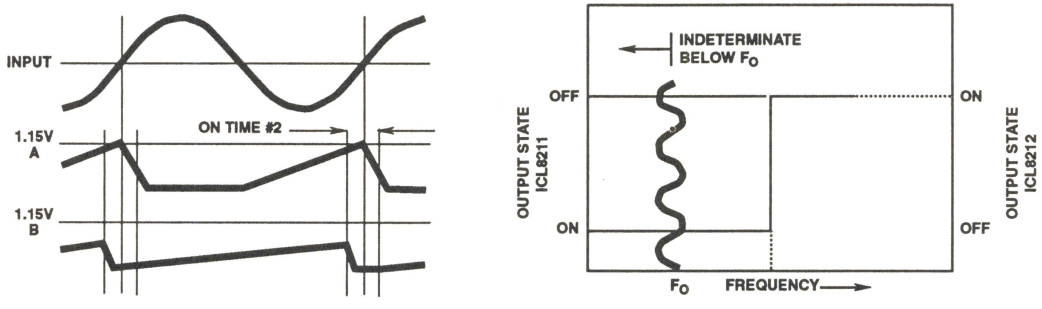


FIGURE 36. FREQUENCY LIMIT DETECTOR

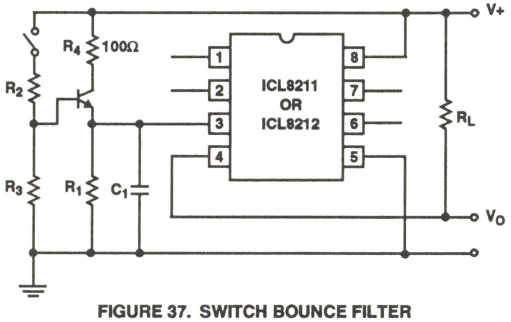


FIGURE 37. SWITCH BOUNCE FILTER

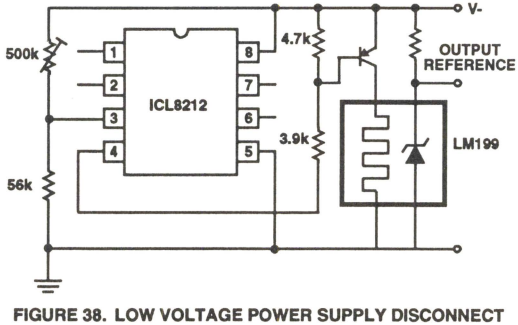


FIGURE 38. LOW VOLTAGE POWER SUPPLY DISCONNECT

INTELLIGENT POWER ICs

8

PROTECTION CIRCUITS

		PAGE
PROTECTION CIRCUITS SELECTION GUIDE		8-2
PROTECTION CIRCUITS DATA SHEETS		
SP710	Protected Power Switch with Transient Suppression	8-3
SP720	Electronic Protection Array for ESD and Overvoltage Protection	8-5
SP720MD-8, SP720MD, SP720MM-8, SP720MM	High Reliability Electronic Protection Array for ESD and Overvoltage Protection	8-8
SP721	Electronic Protection Array for ESD and Overvoltage Protection	8-14

Protection Circuits Selection Guide

PART NUMBER	DESCRIPTION	SUPPLY VOLTAGE RANGE	OVER-VOLTAGE TURN-ON THRESHOLD	TEMPERATURE RANGE	PACKAGE
SP710	Protected Power Switch	4V to 16V	16V to 18.5V	-40°C to +105°C	3 Lead TO-220
SP720	Protection Array	4.5V to 30V	$+V_{BE}$ Above V_{CC} or $-V_{BE}$ Below GND	-40°C to +105°C	16 Lead Plastic DIP and SOIC
SP720MD-8	Ceramic Packaged Harris Class B "Equivalent" SP720 Parts with Back-End Conformance to MIL-STD-883	4.5V to 30V	$+V_{BE}$ Above V_{CC} or $-V_{BE}$ Below GND	-55°C to +125°C	16 Lead Ceramic SBDIP
SP720MM-8					20 Pad Ceramic LCC
SP720MD	High Reliability Ceramic Packaged SP720 Parts	4.5V to 30V	$+V_{BE}$ Above V_{CC} or $-V_{BE}$ Below GND	-55°C to +125°C	16 Lead Ceramic SBDIP
SP720MM					20 Pad Ceramic LCC
SP721	Protection Array	4.5V to 30V	$+V_{BE}$ Above V_{CC} or $-V_{BE}$ Below GND	-40°C to +105°C	8 Lead Plastic DIP and SOIC
HIP1090	Protected Power Switch	4V to 16V	16V to 19V	-40°C to +105°C	3 Lead TO-220

HARRIS SEMICONDUCTOR

SP710

Protected Power Switch with Transient Suppression

April 1994

Features

- ±90V Transient Suppression
- 4V to 16V Operating Voltage
- 0.8A Current Load Capability
- Over-Voltage Shutdown Protected
- Short-Circuit Current Limiting
- Over-Temperature Protected Thermal Limiting at 150°C (T_J)
- -40°C to +105°C Operating Temperature Range

Applications

- Electronic Circuit Breaker
- Transient Suppressor
- Overvoltage Monitor

Description

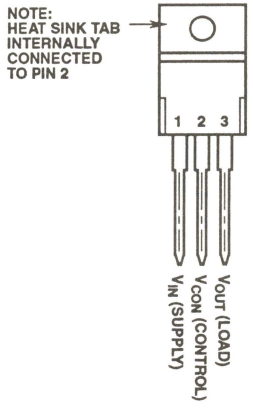
The SP710 is a Power Integrated Circuit designed to suppress potentially damaging overvoltage transients up to ±90V in amplitude. The device is designed to be operated in a pass-thru mode which allows the current to flow through the IC with minimal voltage drop. The protected load circuit is connected to the output of the SP710. As such, the protected power switch IC is designed to operate as a transient suppressor which is capable of driving resistive, inductive or lamp loads with minimum risk of damage under stress conditions of over voltage or over current. The SP710 is supplied in a 3 lead TO-220AB package.

Ordering Information

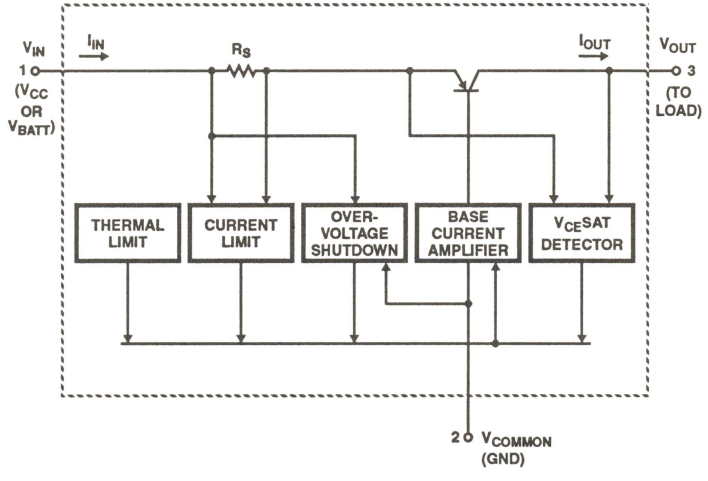
PART NUMBER	TEMPERATURE RANGE	PACKAGE
SP710AS	-40°C to +105°C	3 Lead Plastic SIP

Pinout

SP720 (SIP)
TOP VIEW



Functional Block Diagram



8 PROTECTION CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 2789.6

Absolute Maximum Ratings

Input Voltage, V_{IN} 24V
Load Current, I_{OUT} 800mA
Transient Max Voltage, V_{IN} (15ms) ..... ±90V

NOTE: $P_D = (V_{IN} - V_O)(I_O) + (V_{IN})(I_{COMMON})$
$T_J = T_A + (P_D)$ (Thermal Resistance)

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic SIP	60°C/W	4°C/W

Junction Temperature ..... 150°C
Ambient Operating Temperature ..... -40°C to +105°C
Storage Temperature ..... -40°C to +150°C
Lead Temperature (During Soldering) ..... 265°C
1/16in. ± 1/32in. (1.59mm ± 0.79mm) from case for 10s maximum

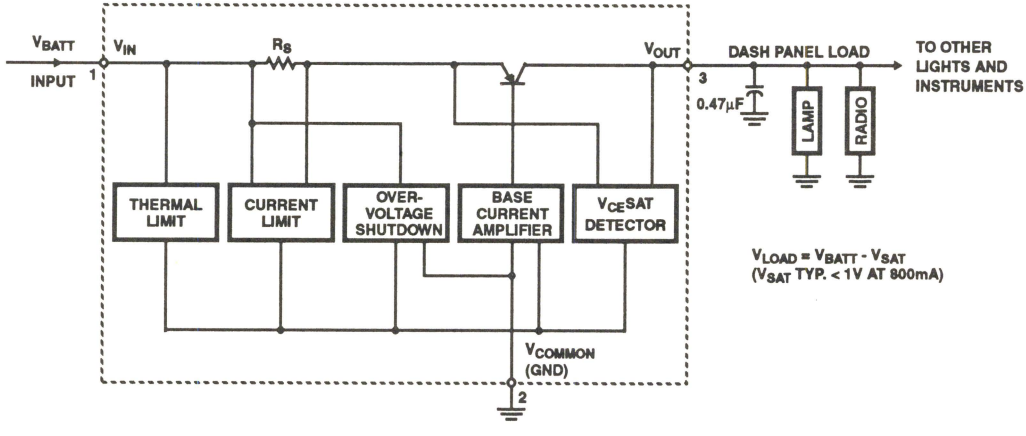
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +105°C, V_{IN} = 4V to 16V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Operating Voltage	V_{IN}		4	-	16	V
Shutdown Voltage	V_{SHSD}		16	-	18.5	V
Shutdown Temperature			-	150	-	°C
Transient Pulse	I_{OUT}	V_{IN} = ±90V for 15ms Pin 3 = 14V, Pin 2 = GND	-20	-	+20	mA
Short Circuit Current			1	-	2	A
V_{SAT} (Input-to-Output)		V_{IN} = 4V, I_{OUT} = 175mA	-	-	0.25	V
		V_{IN} = 9V, I_{OUT} = 500mA	-	-	0.65	V
		V_{IN} = 16V, I_{OUT} = 800mA	-	-	1.05	V
Common Current	I_{COM}	V_{IN} = 16V, I_{OUT} = 100mA	-	-	25	mA
		V_{IN} = 16V, I_{OUT} = 800mA	-	-	50	mA

Typical Application



HARRIS SEMICONDUCTOR

SP720

Electronic Protection Array for ESD and Overvoltage Protection

April 1994

Features

- ±2A Peak Current Capability
- Single-Ended Voltage Range to ..... +35V
- Differential Voltage Range to ..... +17.5V
- Designed to Provide Over-Voltage Protection
- Fast Switching ..... 6ns Risetime
- Low Input Leakages of 1nA at +25°C Typical
- Low Input Capacitance of 3pF Typical
- An Array of 14 SCR/Diode Pairs
- Proven Interface for ESD
- Operating Temperature Range ..... -40°C to +105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP720 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures per input. A total of 14 available inputs can be used to protect up to 14 external signal or bus lines. Over voltage protection is from the IN (pins 1-7 and 9-15) to V+ or V-. The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 16) or a $-V_{BE}$ diode threshold below V- (Pin 8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

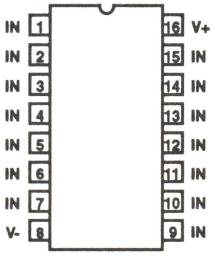
Refer to Application Note AN9304 for further information

Ordering Information

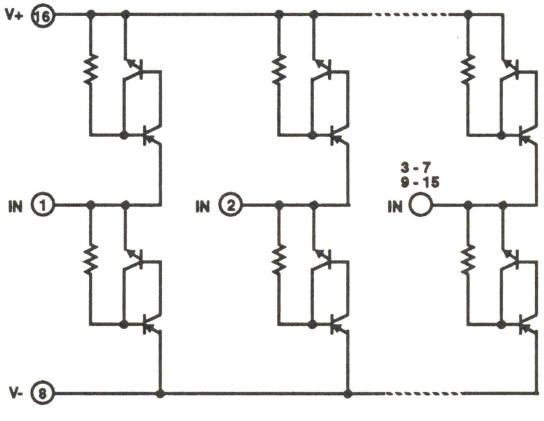
PART NUMBER	TEMPERATURE	PACKAGE
SP720AP	-40°C to +105°C	16 Lead Plastic DIP
SP720AB	-40°C to +105°C	16 Lead Plastic SOIC (N)
SP720ABT	-40°C to +105°C	16 Lead Plastic SOIC Tape and Reel

Pinout

SP720 (PDIP, SOIC)



Functional Block Diagram



8 PROTECTION CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 2791.5

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-) ..... +35V
Input Peak Current, I_{IN} ..... ±2A
Transient Ratings - See Note 2, Figure 1, Table 1

Thermal Information

Thermal Resistance θ_{JA}
16 Lead PDIP Package ..... 90°C/W
16 Lead SOIC Package ..... 170°C/W
Maximum Package Power Dissipation at +105°C:
Plastic DIP Package 500mW
Plastic SOIC Package 270mW
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +105°C; V_{IN} = 0.5V_{CC} Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	4.5 to 30	-	V
Forward Voltage Drop: IN to V- IN to V+	 V_{FWDL} V_{FWDH}	I_{IN} = 1A (Peak Pulse)	 - -	 2 2	 - -	 V V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}: Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	6	-	ns

NOTES:

1. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the supply and the SP720 pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
2. For ESD testing of the SP720 to MIL-STD-3015.7 Human Body Model (HBM), the results are typically better than 6KV (Condfition 1) (Figure 1, Table 1). Transient and ESD testing capability is highly dependent on the application. For conditions that are defined as an in-circuit method of ESD testing where the V+ and V- pins have a return path to ground, the ESD capability is typically greater than 15KV from 100pF through 1.5KΩ (Condition 2). For ESD testing of the SP720 to EIAJIC121 Machine Model (MM) standard, the results are typically better than 1KV (Condition 4). These values were measured by AT&T ESD Lab using the component testing procedures of both standards., Additional ESD testing for 200pF through 1.5KΩ with 6ns risetime was done with results better than 9KV (Condition 3).
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

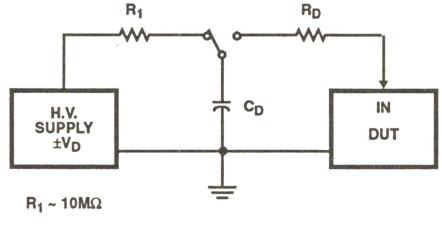


FIGURE 1. ELECTROSTATIC DISCHARGE TEST MIL-STD-883D, METHOD 3015.7

TABLE 1. ESD TEST CONDITIONS

TEST	±V_D	R_D	C_D	
Condition 1	6KV	1.5KΩ	100pF	(HBM)
Condition 2	15KV	1.5KΩ	100pF	(Mod. HBM)
Condition 3	9KV	1.5KΩ	200pF	(Mod. HBM)
Condition 4	1KV	0KΩ	200pF	(MM)

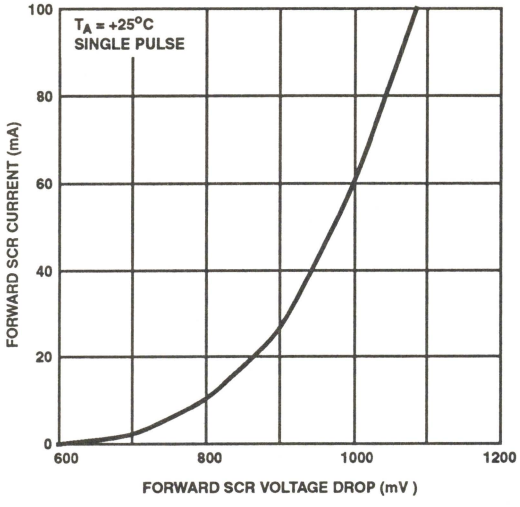


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

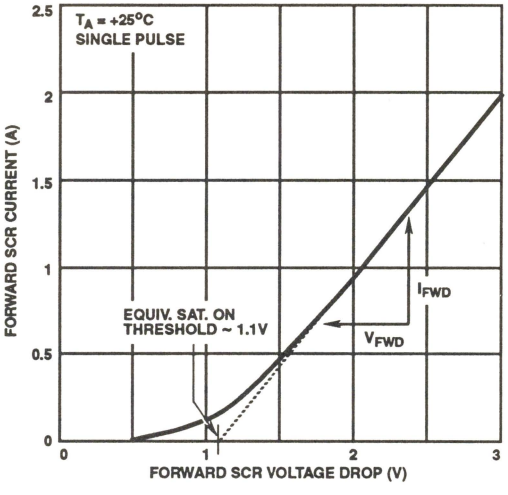


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

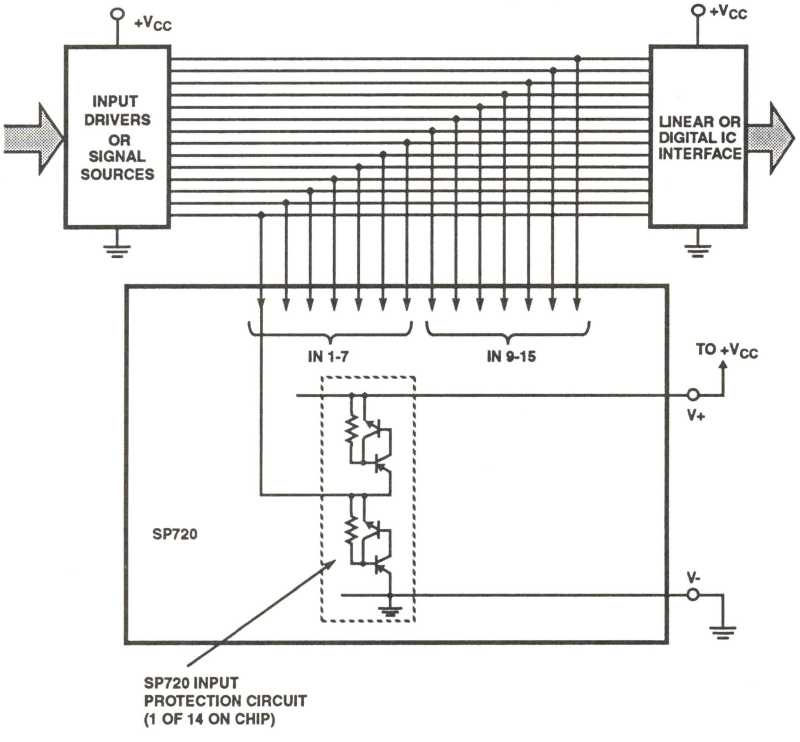


FIGURE 4. TYPICAL APPLICATION OF THE SP720 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-

HARRIS SEMICONDUCTOR

SP720MD-8, SP720MD
SP720MM-8, SP720MM

High Reliability Electronic Protection Array for ESD and Overvoltage Protection

PRELIMINARY

April 1994

Features

- **The SP720MD-8 and SP720MM-8 are Harris Class B "Equivalent" Parts with Back-End Conformance to Mil-Std-883 for Final Assembly, Electrical Testing, Burn-in and QC Inspection**
- **±2A Peak Current Capability**
- **Single-ended Voltage Range..... to +35V**
- **Differential Voltage Range ..... to ±17.5V**
- **Designed to Provide Over-Voltage Protection**
- **Fast Switching .....6ns Risetime**
- **Low Input Leakages of 1nA at 25°C Typical**
- **Low Input Capacitance of 3pF Typical**
- **An Array of 14 SCR/Diode Pairs**
- **Proven Interface for ESD**
- **Military Temperature Range ..... -55°C to +125°C**

Applications

- **Microprocessor/Logic Input Protection**
- **Data Bus Protection**
- **Analog Device Input Protection**
- **Voltage Clamp**

Description

The SP720 is a High Reliability Array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures at each IN input. A total of 14 available IN inputs can be used to protect up to 14 external signal or bus lines. Over voltage protection is from the IN to V+ or V-. The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ or at a $-V_{BE}$ diode threshold below V-. From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

The SP720MD-8 and SP720MM-8 Class B "Equivalent" Parts conform to Mil-Std-883 through final assembly, electrical test, burn-in and QC Inspection. The SP720MD and SP720MM are High Reliability Ceramic Packaged ICs.

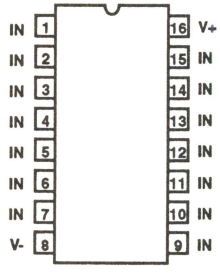
Refer to Application Note AN9304 for further information.

Ordering Information

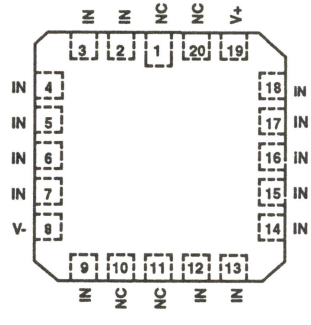
PART NUMBER	TEMPERATURE RANGE	PACKAGE
SP720MD-8	-55°C to +125°C	16 Lead Ceramic SBDIP
SP720MD	-55°C to +125°C	16 Lead Ceramic SBDIP
SP720MM-8	-55°C to +125°C	20 Pad Ceramic LCC
SP720MM	-55°C to +125°C	20 Pad Ceramic LCC

Pinouts

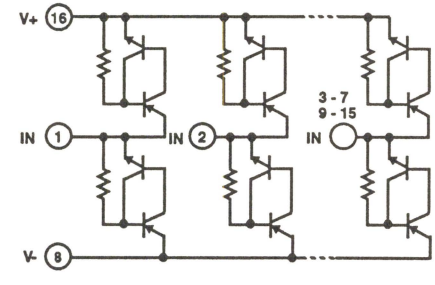
SP720MD (SBDIP)
TOP VIEW



SP720MM (CLCC)
TOP VIEW



Functional Block Diagram (SP720MD)



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File Number **3683**

Absolute Maximum Ratings

Continuous Supply Voltage, [(V+) - (V-)] ..... +35V
Input Peak Current, I_{IN} (non-repetitive, < 1ms) ..... ±2A
Max. DC Input Current, I_{IN} ..... ±70mA
For ESD Transient Capability - See Note 2, Figure 1, Table 1
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +265°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Sidebraze DIP Package	82°C/W	14°C/W
Ceramic LCC	70°C/W	19°C/W

Package Power Dissipation:
Sidebraze DIP Package, up to +93°C 1.0W
Ceramic LCC, up to +105°C 1.0W
Package Power Dissipation Derating Factor:
Sidebraze DIP Package, above +93°C ..... 12.2mW/°C
Ceramic LCC, above +105°C ..... 14.3mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range, Single Supply ..... +4.5V to +30V
Operating Voltage Range, Split Supply ..... ±2.25V to ±15V
Typical Quiescent Supply Current 50nA
Operating Temperature Range ..... -55°C to +125°C

Electrical Specifications

T_A = -55°C to +125°C; Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{SUPPLY}	V_{SUPPLY} = [(V+) - (V-)]	0	4.5 to 30	35	V
Peak Forward/Reverse Voltage Drop						
IN to V- (with V- Reference)	V_{IN} - (V-)	I_{IN} = -1A (1ms Peak Pulse)	-	-2	-	V
IN to V+ (with V+ Reference)	V_{IN} - (V+)	I_{IN} = +1A (1ms Peak Pulse)	-	+2	-	V
DC Forward/Reverse Voltage Drop						
IN to V- (with V- Reference)	V_{IN} - (V-)	I_{IN} = -100mA to V-	-1.5	-	-	V
IN to V+ (with V+ Reference)	V_{IN} - (V+)	I_{IN} = +100mA to V+	-	-	+1.5	V
Input Leakage Current	I_{IN}	V- < V_{IN} < V+, V_{SUPPLY} = 30V	-15	5	+15	nA
Quiescent Supply Current	$I_{QUIESCENT}$	V- < V_{IN} < V+, V_{SUPPLY} = 30V	-	50	150	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} (Note 3)	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	6	-	nS

NOTE:

1. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01 µF or larger from the V+ and V- pins to ground are recommended.
2. For ESD testing of the SP720 to MIL-STD 883, Method 3015.7, Human Body Model (HBM), the results are typically better than 6KV (Condition 1). Transient and ESD capability is highly dependent on the application. For conditions that are defined as an in-circuit method of ESD testing where the V+ and V- pins have a return path to ground, the ESD capability is typically greater than 15KV from 100pF through 1.5 KΩ (Condition 2). For ESD testing of the SP720 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1KV (Condition 4). These values were measured by AT&T ESD Lab using the component testing procedures of both standards. Additional ESD testing for 200pF through 1.5 KΩ with 6ns risetime was done with results better than 9KV (Condition 3).
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

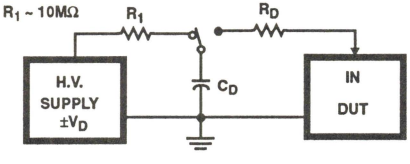


FIGURE 1. ELECTROSTATIC DISCHARGE TEST MIL-STD-883D, METHOD 3015.7

TABLE 1. ESD TEST CONDITIONS

TEST	±V_D	R_D	C_D	
Condition 1	6KV	1.5KΩ	100pF	(HBM)
Condition 2	15KV	1.5KΩ	100pF	(Mod. HBM)
Condition 3	9KV	1.5KΩ	200pF	(Mod. HBM)
Condition 4	1KV	0KΩ	200pF	(MM)

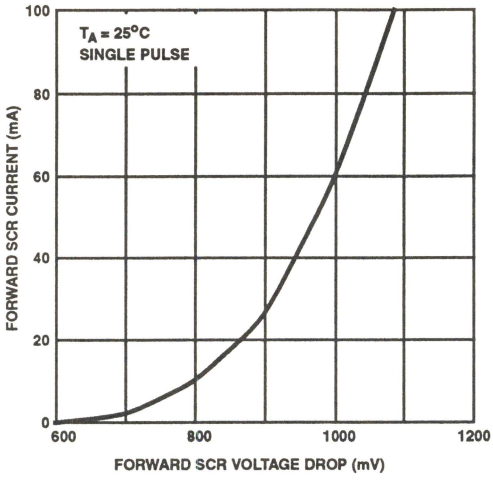


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

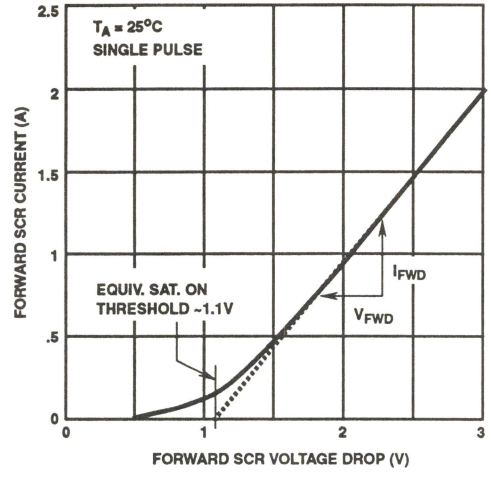


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

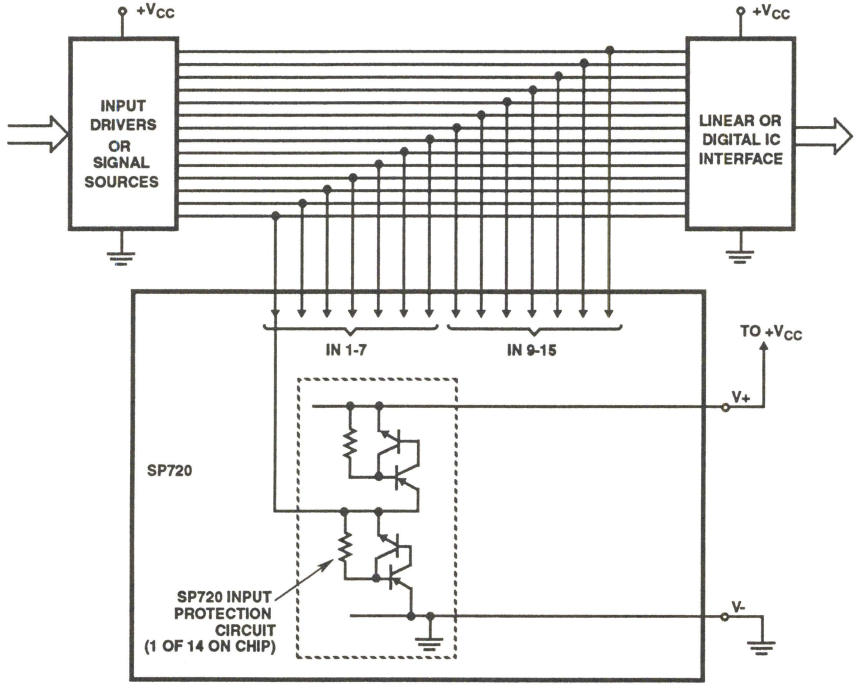


FIGURE 4. TYPICAL APPLICATION OF THE SP720 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-. PINOUT SHOWN IS FOR THE SP720MD PDIP PACKAGE.

Power Dissipation Derating Curves

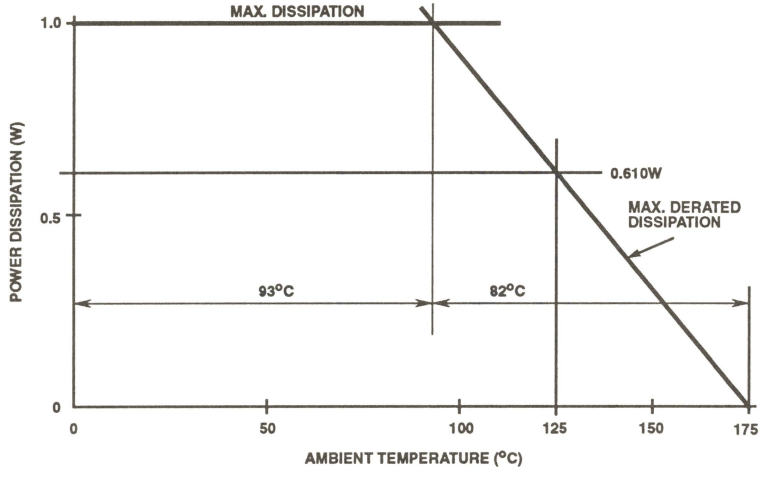


FIGURE 5. SP720MD DERATING CURVE FOR THE 82°C/W THERMAL RESISTANCE OF THE SIDEBRAZE 16 PIN CERAMIC PACKAGE, DERATED 12.2mW/°C FROM A MAXIMUM P_D OF 1.0W AT 93°C

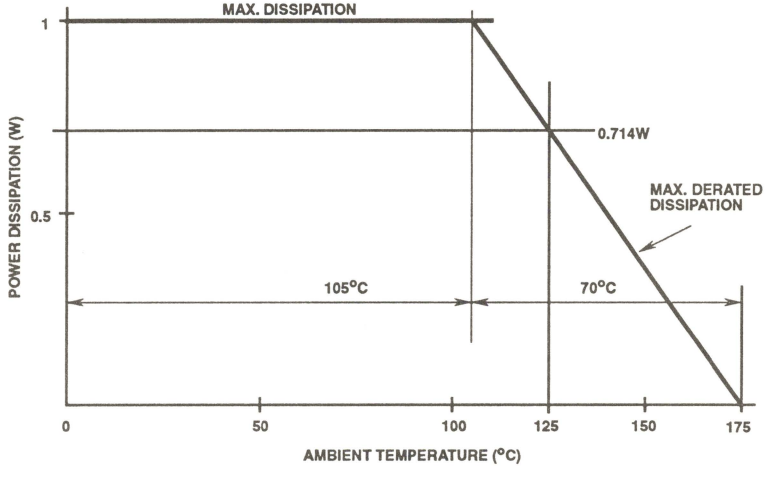
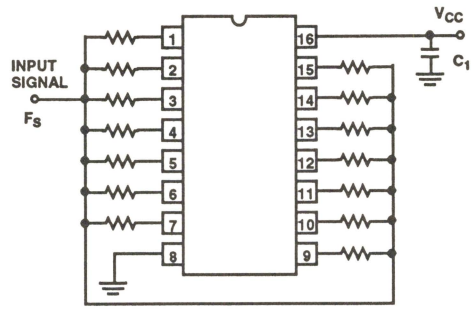


FIGURE 6. SP720MM DERATING CURVE FOR THE 70°C/W THERMAL RESISTANCE OF THE 20 PAD CERAMIC LCC PACKAGE, DERATED 14.3mW/°C FROM A MAXIMUM P_D OF 1.0W AT 105°C

SP720MD-8 and SP720MM-8 Dynamic Burn-In Circuits

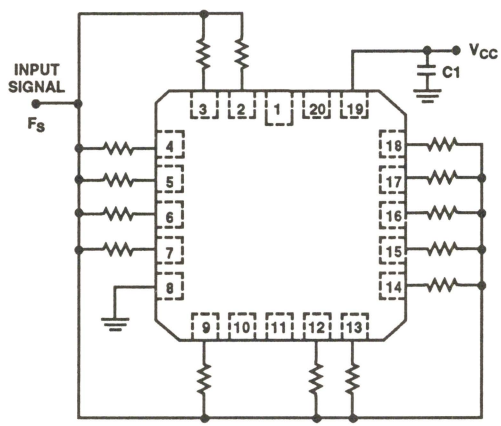
16 LEAD CERAMIC SBDIP



NOTES:

1. All resistors 1kΩ ±10%
2. V_{CC} = 30V ±1%
3. F_S = 0V to 30V ±1%, 50% Duty Cycle
4. C_1 = 22µF Min. Tantalum, 50WV (33WV at 125°C)
5. T_{AMB} = 125°C

20 PAD CLCC





Metallization Topology

DIE DIMENSIONS:
51 x 84 x 14 ± 1mils

METALLIZATION:
Type: Al
Thickness: 17.5kÅ ± 2.5kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

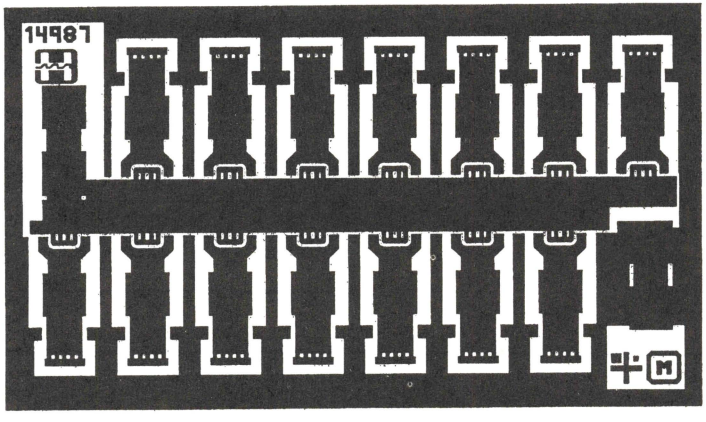
SUBSTRATE POTENTIAL (POWERED UP):
V-

WORST CASE CURRENT DENSITY:
9.18 x 10^4A/cm^2 at 70mA

PROCESS:
Bipolar

Metallization Mask Layout

SP720MD-8, SP720MD, SP720MM-8, SP720MM



HARRIS SEMICONDUCTOR

SP721

Electronic Protection Array for ESD and Overvoltage Protection

April 1994

Features

- ±2A Peak Current Capability
- Single-Ended Voltage Range ..... to +35V
- Differential Voltage Range ..... to ±17.5V
- Designed to Provide Overvoltage Protection
- Fast Switching ..... 6ns Risetime
- Low Input Leakages of 1nA at +25°C Typical
- Low Input Capacitance of 3pF Typical
- An Array of 6 SCR/Diode Pairs
- Proven Interface for ESD
- Operating Temperature Range ..... -40°C to +105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP721 is an array of SCR/Diode biploar structures for ESD and Overvoltage protection to sensitive input circuits. The SP721 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

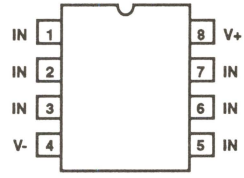
Further information is available in Application Note AN9304. AN9304 applies to both the SP720 and SP721

Ordering Information

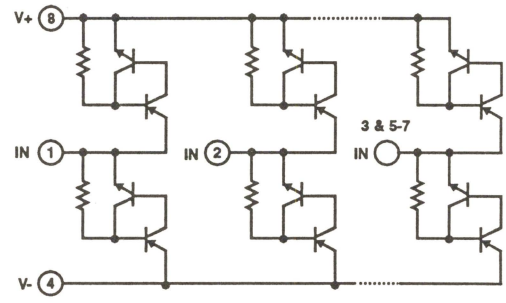
PART NUMBER	TEMPERATURE RANGE	PACKAGE
SP721AP	-40°C to +105°C	8 Lead Plastic DIP
SP721AB	-40°C to +105°C	8 Lead Plastic SOIC (N)
SP721ABT	-40°C to +105°C	8 Lead Plastic SOIC Tape and Reel

Pinout

SP721 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Copyright © Harris Corporation 1994

File Number **3590.1**

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-) ..... +35V
Input Peak Current, I_{IN} ..... ±2A
ESD Transient Ratings - See Note 2, Figure 1, Table 1

Thermal Information

Thermal Resistance, θ_{JA}
8 Lead DIP Package ..... 130°C/W
8 Lead SOIC Package ..... 170°C/W
Maximum Package Power Dissipation
8 Lead Plastic DIP Package, Up to +105°C 350mW
8 Lead Plastic SOIC Package, Up to +105°C 270mW
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +105°C, V_{IN} = 0.5V_{CC} Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	4.5 to 30	-	V
Forward Voltage Drop IN to V- IN to V+	 V_{FWDL} V_{FWDH}	I_{IN} = 1A (Peak Pulse)	-	 2 2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} ; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	6	-	ns

NOTES:

1. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP721 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- Pins to ground are recommended.
2. For ESD testing of the SP721 to MIL-STD 883, Method 3015.7, Human Body Model (HBM), the results are typically better than 6kV (Condition 1) (Figure 1, Table 1). Transient and ESD capability is highly dependent on the application. For conditions that are defined as an in-circuit method of ESD testing where the V+ and V- Pins have a return path to ground, the ESD capability is typically greater than 15kV from 100pF through 1.5kΩ (Condition 2) or 9kV from 200pF through 1.5kΩ (Condition 3). For ESD testing of the SP721 to EIAJ IC121 Machine Model (MM), the results are typically better than 1kV (Condition 4).
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

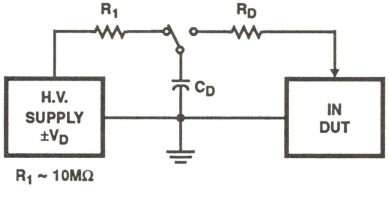


FIGURE 1. ELECTROSTATIC DISCHARGE TEST MIL-STD-883D, METHOD 3015.7

TABLE 1. ESD TEST CONDITIONS

TEST	±V_D	R_D	C_D	
Condition 1	6kV	1.5kΩ	100pF	(HBM)
Condition 2	15kV	1.5kΩ	100pF	(Mod. HBM)
Condition 3	9kV	1.5kΩ	200pF	(Mod. HBM)
Condition 4	1kV	0kΩ	200pF	(MM)

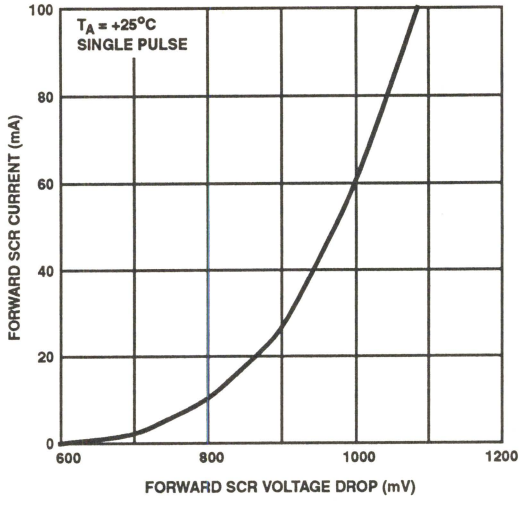


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

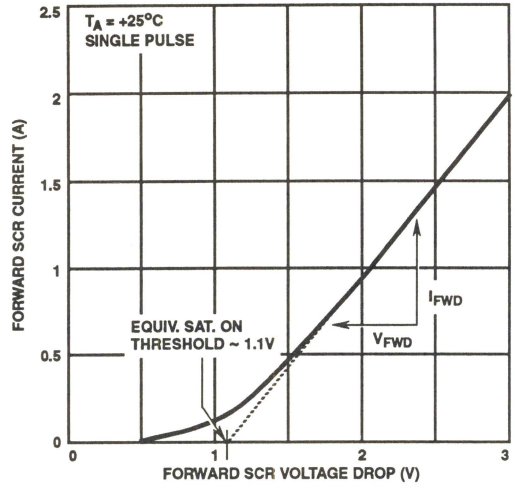


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

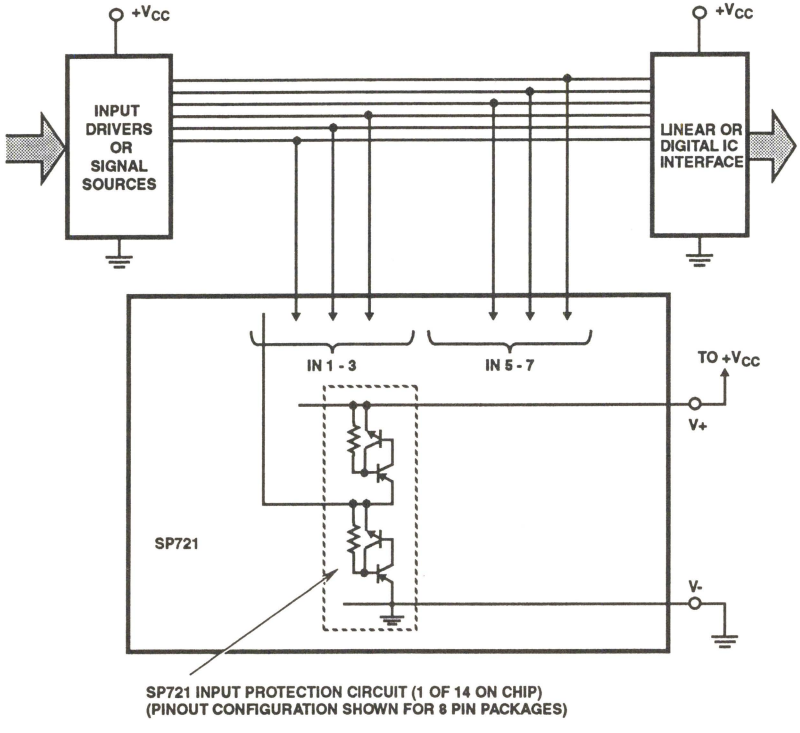


FIGURE 4. TYPICAL APPLICATION OF THE SP721 AS AN INPUT CLAMP FOR OVERVOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-

INTELLIGENT POWER ICs

9

MULTIPLEX COMMUNICATION CIRCUITS

		PAGE
MULTIPLEX COMMUNICATION CIRCUITS SELECTION GUIDE		9-2
MULTIPLEX COMMUNICATION CIRCUITS DATA SHEETS		
CDP68HC68S1	Serial Bus Interface	9-3
HIP7010	J1850 Byte Level Interface Circuit	9-17
HIP7020	J1850 Bus Transceiver I/O for Multiplex Wiring	9-33
HIP7030A0	J1850 8-Bit 68HC05 Microcontroller Emulator Version	9-40
HIP7030A2	J1850 8-Bit 68HC05 Microcontroller	9-50
HIP7038A8	J1850 8-Bit 68HC05 Microcontroller 8K EEPROM Version	9-99

Multiplex Communication Circuits Selection Guide

PART NUMBER	DESCRIPTION	APPLICATIONS	SUPPLY VOLTAGE	TEMPERATURE	PACKAGE
CDP68HC68S1	SPI Serial Bus Interface with Collision Detection and Arbitration	CCD 8/16-Bit Serial Bus	3V to 6V	-40°C to +105°C	14 Lead PDIP and 20 Lead SOIC
HIP7010	J1850 Byte Level Interface Circuit	J1850 Class B Variable Pulse Width (VPW)	3V to 6V	-40°C to +125°C	14 Lead PDIP and SOIC
HIP7020	J1850 Bus Transceiver I/O for Multiplex Wiring	J1850 Class B Variable Pulse Width (VPW)	6V to 24V	-40°C to +125°C	8 Lead PDIP and 8 Lead SOIC
HIP7030A0	J1850 8-Bit 68HC05 Microcontroller Emulator Version	J1850 Class B Variable Pulse Width (VPW)	3V to 6V	-40°C to +125°C	68 Lead PLCC
HIP7030A2	J1850 8-Bit 68HC05 Microcontroller	J1850 Class B Variable Pulse Width (VPW)	3V to 6V	-40°C to +125°C	28 Lead PDIP and 28 Lead SOIC
HIP7038A8	J1850 8-Bit 68HC05 Microcontroller 8K EEPROM Version	J1850 Class B Variable Pulse Width (VPW)	5V	-40°C to +125°C	28 Lead Ceramic SOIC Flatpack

CDP68HC68S1

April 1994

Serial Bus Interface

Features

- Differential Bus for Minimal EMI
- High Common Mode Noise Rejection
- Ideal for Twisted Pair Wiring
- Data Collision Detection
- Bus Arbitration
- Idle Detection
- Programmable Clock Divider
- Power-On Reset

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CDP68HC68S1E	-40°C to +105°C	14 Lead PDIP
CDP68HC68S1M	-40°C to +105°C	20 Lead SOIC (W)

Description

The CDP68HC6SS1 Serial Bus Interface Chip (SBIC) provides a means of interfacing in a Small Area Network configuration, various microcomputers (MCU's) containing serial ports. Such MCU's include the family of 68HC05 microcontrollers. The SBIC provides a connection from an MCU's Serial Communication Interface (asynchronous UART type interface) or Serial Peripheral Interface (synchronous) to a medium speed asynchronous two wire differential signal bus designed to minimize electromagnetic interference. This two wire bus forms the network bus to which all MCU's are connected (through SBI chips). See Figure 1. Each MCU operates independently and may be added or deleted from the bus with little or no impact on bus operation. Such a bus is ideal for inter-microcomputer communication in hazardous electrical environments such as automobiles, aircraft or industrial control systems.

In addition to acting as bus arbitor and interface for microcomputer SCI port to differential bus communication, the CDP68HC68S1 contains all the circuitry required to convert and synchronize Non-Return-to-Zero (NRZ) 8-bit data received on the differential bus and clock the data into a microcomputer's SPI port. Likewise, data to be sent by a microcomputer's SPI port is converted to asynchronous format by appending start and stop bits before transmitting to other microcomputers.

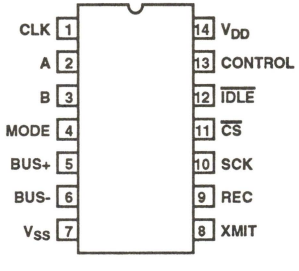
Refer to the data sheet for the CDP68HCO5C4 for additional information regarding CDP68HCO5 microcomputers and their Serial Communications and Serial Peripheral Interfaces.

The CDP68HC68S1 is supplied in a 14 lead dual-in-line plastic package (E suffix), and in a 20 lead small outline plastic package (M suffix).

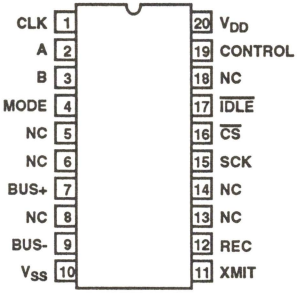
Operating voltage ranges from 4V to 7V and operating temperature ranges from -40°C to +105°C.

Pinouts

CD68HC68S1 (PDIP)
TOP VIEW



CD68HC68S1 (SOIC)
TOP VIEW



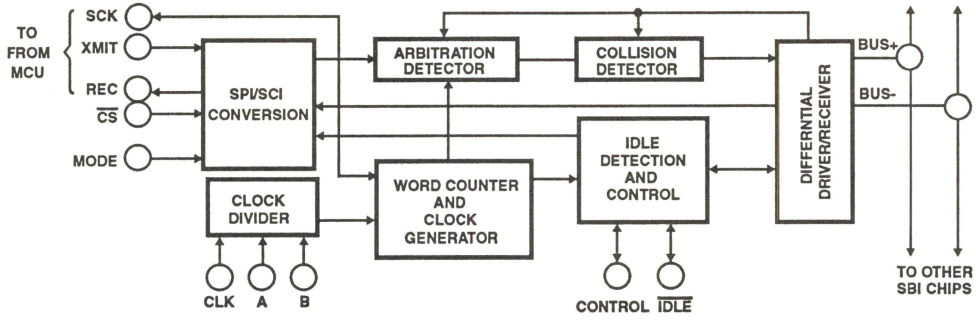
9 MULTIPLEX COMM. CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **1918.3**

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . -0.3V to +7.0V
Input Voltage (V_{IN}) . . . . . V_{SS} -0.3V to V_{DD}+0.3V_{DC}
DC Input Current (I_{IN}) . . . . . ±10mA

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package . . . . . 100°C/W
Plastic SOIC Package . . . . . 120°C/W
Storage Temperature Range (T_{STG}) . . . . . -55°C to +125°C
Lead Temperature (Soldering 10s) . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature (T_A) . . . . . -40°C to +105°C
DC Operating Voltage Range (V_{DD}) . . . . . +4V to +7V

DC Electrical Specifications

T_A = -40°C to +105°C Unless Otherwise Noted. External Bias (V_O) shall be 1.8V to 3.13V Unless Otherwise Noted.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
SIGNAL I/0 SECTION					
Output Voltage High Level	V_{OL}	Open Circuit	-	0.05	V_{DC}
Output Voltage Low Level	V_{OH}	Open Circuit	V_{DD}-0.05	-	V_{DC}
Input Voltage Low Level	V_{IL}		-	0.3V_{DD}	V_{DC}
Input Voltage High Level	V_{IH}		0.7V_{DD}	-	V_{DC}
Output High Drive (Source) Current (REC Pin)	I_{OH}	V_{OH} = 4.6V, V_{DD} = 5V	-0.12	-	mA
Output High Drive (Source) Current ($\overline{IDLE}$, Control Pins)	I_{OH}	V_{OH} = 4.6V, V_{DD} = 5V	-0.04	-	mA
Output Low Drive (Sink) Current ($\overline{IDLE}$, Control, REC)	I_{OL}	V_{OH} = 0.4V, V_{DD} = 5V	0.36	-	mA
DIFFERENTIAL TRANSCEIVER (SEE FIGURE 4) TRANSMITTER					
BUS+	I_{AOL}	V_O = V_{DD}/2, R_L = 120Ω	2.75	-	mA
	I_{AOH}	V_O = V_{DD}/2, R_L = 120Ω	-1.0	1.0	µA
BUS-	I_{BOL}	V_O = V_{DD}/2, R_L = 120Ω	-	-2.75	mA
	I_{BOH}	V_O = V_{DD}/2, R_L = 120Ω	-1.0	1.0	µA
I_{AOL} - I_{BOL} Match	I_M	V_O = V_{DD}/2, R_L = 120Ω, V_{DD} = 5V ±0.5V	-	5	%
Output Rise Time (BUS+)	t_R	V_{DD} = 5V, C_L = 25pF	-	1.5	µs
Output Fall Time (BUS-)	t_F	V_{DD} = 5V, C_L = 25pF	-	1.5	µs
Transition match (50% Point)	t_M	V_{DD} = 5V, C_L = 25pF	-50	50	ns
RECEIVER					
Differential Sensitivity	V_{IDH}	V_O = 2.5V, R_L = 120Ω, V_{DD} = 5V	-	120	mV
	V_{IDL}	V_O = 2.5V, R_L = 120Ω, V_{DD} = 5V	20	-	mV
Hysteresis (Within V_{IDH}, V_{IDL} Limits)	V_H	V_O = 2.5V, R_L = 120Ω, V_{DD} = 5V	20	-	mV
Propagation Delay	t_P	V_{IDH} =120mV, V_{DD} = 5V	-	700	ns
Out of Range	V_{AX}	V_{DD} = 5V	3.8	-	V
	V_{MIN}	V_{DD} = 5V	-	1.2	V
Quiescent Device Current	I_{DD}	V_{DD} = 0V, V_O = 2.5V	-10	10	µA
Clock Speed	f_{OP}	V_{DD} = 5, R_L = 120Ω, C_L = 25pF	-	TBD (Note)	MHz

NOTE: Although 1MHz is generally used as an example throughout this datasheet, the maximum speed limit may be higher and depends upon user's noise tolerance requirements.

The Serial Bus IC offers the user three possible modes of operation as defined by Table 1 - SCI (Note 1), SPI, and Buffered SPI. Also included is a "three-state mode" entered by pulling the CS pin high while in the Buffered SPI mode. As the name implies, the SCI mode is used when communicating through the microcomputer's SCI port. In this mode, asynchronous NRZ data format (1 start bit, 8 data bits 'least significant bit first', and 1 stop bit) and baud rate remain the same on each "side" of the SBIC, i.e. to and from the micro and to and from the differential network bus.

TABLE 1. MODE AND CHIP SELECT DEFINITION

SBI CHIP MODE	MODE PIN	CS PIN
SCI	1	1
SPI	1	0
Buffered SPI	0	0
Three-State (Note 2)	0	1

NOTES:

1. SCI is the UART interface of a 68HCO5 MCU. The CDP68HC68S1 is compatable with most UART devices.
2. The three-state mode is only entered when using the Buffered SPI mode. In the three-state mode, only the $\overline{\text{XMIT}}$, REC, and SCK pins are three-stated. The CONTROL and $\overline{\text{IDLE}}$ pins are always active.

During data transmission, while a byte is being transmitted from the MCU through the SBI chip onto the differential bus, it is also reflected and simultaneously received back at the micro, (this is required for bus arbitration as described later).

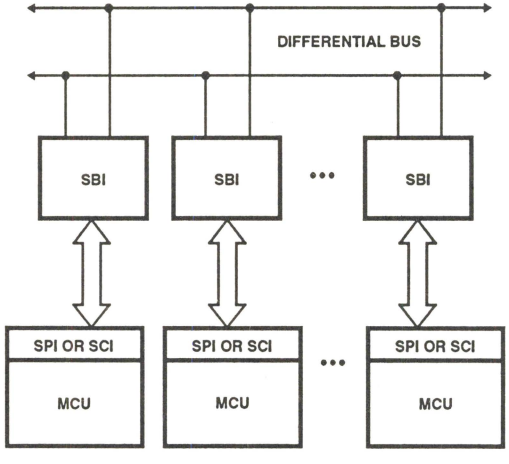


FIGURE 1. POSSIBLE NETWORK CONFIGURATION-VARIOUS MICROCOMPUTERS USING SBI CHIPS TO COMMUNICATE ALONG DIFFERENTIAL BUS.

In addition to performing a framing error check in the SCI mode, other advantages gained by using the SBIC (in any mode) include greater system EMI tolerance and automatic bus "monitoring". The Serial BUS Interface chip handles bus arbitration, data collision detection, and provides short circuit protection.

A 68HC0S MCU's SPI port may instead be used for bus communication. Two modes of SPI operation are available with the SBIC - one essentially places the 68HC05 microcomputer in the slave mode and the other allows the MCU to remain a master. In the normal SPI mode the SBIC acts as a master and supplies a data-synchronizing serial clock signal to the micro (which operates in the slave mode) for shifting data in or out of the micro's 8-bit SPI data register. Again, baud rates are the same on each side of the SBIC, however, the user must reverse the bit order of a byte transmitted or received via the SPI port due to the SPI's most significant bit first serial data nature. In addition, since the user microcomputer is operating in the slave mode it must signal the SBI chip (by pulling the CONTROL line low) to initiate a transmission. As in the SCI mode, during a transmission, the byte originally in the SPI data register is replaced by the byte reflected from the bus.

Transmission and reception of data in the Buffered SPI mode allows the user to free the micro's SPI port by allowing fast data communication (1M bits/second) between the SPI port and SBIC. For instance, if the MCU is transmitting, the SBIC converts the data stream from the MCU's SPI port to a slower speed for transmission along the differential bus when the bus becomes idle. Data speed conversion is accomplished via a 2 byte (16-bit) data buffer register residing in the serial bus chip. In this mode the MCU operates as a master and provides the serial clock signal to the slave SBIC peripheral. After fast data has been sent to or received from the SBIC, the micro can pull the SBIC's $\overline{\text{CS}}$ pin high (placing the SBIC chip in the three-state mode) and then use the SPI port to access other SPI peripherals.

All transfers between the user MCU and the SBIC in the Buffered SPI mode consist of 2 bytes, i.e. a message consists an even number of 8-bit transfers. A microcomputer wishing to transmit loads 2 bytes into the serial bus IC data register and then pulls the control pin low to initiate transmission. During transmission the 2 bytes placed into the buffer are replaced by the two reflected bytes received from the bus. After every 2 byte transmission the user micro should transfer the two reflected bytes out of the buffer and the next 2 bytes to be transmitted into the buffer.

TABLE 2. CLOCK PROGRAMMING

CLOCK INPUT DIVIDE FACTOR	A PIN	B PIN
÷ 1	0	0
÷ 2	0	1
÷ 4	1	0
÷ 10	1	1

Functional Pin Description

PIN NUMBER	SYMBOL	IN/OUT	DESCRIPTION
1	CLK	Input	This is the clock input that shall be divided by the SBIC (as described in Table 2) and used as an internal synchronizing clock. The internal clock is then further divided by 128 to determine baud rate, i.e. 128 internal clock periods constitute 1-bit length.
2, 3	A and B	Input	Programing inputs of the clock divider. These inputs are tied to $+V_{DD}$ or V_{SS} depending upon speed of external clock source. (See Table 2)
4	Mode	Input	This input shall be used in conjunction with $\overline{CS}$ input to define the mode of operation (see Table 1). It may be permanently wired to $+V_{DD}$ or V_{SS} or driven high or low by MCU I/O lines.
5, 6	BUS+ and BUS-	Input/Output	This is the two wire differential bus I/O used to transmit and receive data to and from the differential bus. BUS+ is both responsive to, or driven positive by sourcing current from an externally established bias point. This sourcing current matches the BUS- I/Os sinking current. BUS- is both responsive to, or driven negative by sinking current from an externally established bias point. This sinking current matches the BUS+ I/Os sourcing current.
14, 7	V_{DD} and V_{SS}	-	Power and ground reference are supplied to the device via these pins. V_{DD} is power and V_{SS} is ground.
8	XMIT	Input	In the SCI mode this data input shall come from the microcomputer standard NRZ asynchronous communications output port (68HC05 SCI port pin TxD). In the SPI modes, it shall come from the microcomputer's synchronous output port (68HC05 SPI port pin MOSI or MISO).
9	REC	Output	In the SCI mode this data output shall be fed into the microcomputer asynchronous communications input port (68HC05 SCI port pin RxD). In the SPI modes it shall be fed into the microcomputer's synchronous input port (6805 SP1 port pin MOSI or MISO).
10	SCK	Input/Output	In the SCI mode, this I/O is not required. In both SPI modes this pin is connected to the 68HC05's SPI port SCK pin. In the normal SPI mode, the SBIC shall produce shift clock pulses via this pin for synchronously shifting data into and out of the microcomputer. In the Buffered SPI mode this pin is an input and the microcomputer shall generate the shift clock pulses. Figure 3 shows the relationship between the serial clock signal and other SBIC signals in the SPI mode.
11	$\overline{CS}$	Input	This input shall be used in conjunction with the mode input and shall be used as a chip select (see Table 1). It may be permanently wired to $+V_{DD}$ or V_{SS} or driven high or low by MCU I/O lines.
12	$\overline{IDLE}$	Input/Output	The microcomputer shall monitor this signal to determine the bus condition and also pull this line low to generate a break. The $\overline{IDLE}$ signal goes low when the bus is idle (after sensing an End of Message condition) and high when the bus is active. On reset, this pin is set to a logic zero.
13	Control	Input/Output	The microcomputer shall monitor this I/O pin in the SPI mode to handle transmission and reception of data. In the SCI and SPI modes, as an output, this pin will go low to indicate that a data byte is currently active on the bus. In the Buffered SPI mode the control pin indicates whether the user microcomputer has current access to the SBI chip's internal 2 byte buffer (signified by a logic high on the control pin). In both SPI modes the control pin is also effective as an input. In these modes the control pin is pulled low by the user microcomputer to initiate a transmit operation by the SBIC. The control pin is normally high when the bus is inactive. On reset, this pin is set to a logic high.

Differential Transceiver Cell

The differential transceiver is a serial interface device which accepts digital signals and translates this information for transmitting on the two wire differential bus.

The transmitter section (shown in Figure 4), when transmitting, provides matched constant current sources to the bus "+" and bus "-" I/O sourcing and sinking respectively. When transmitting, a logic zero at the "transmit data" input causes the bus "+" I/O to provide source current and the bus "-" I/O to provide a matched sink current. A logic one at the "transmit data" input causes the bus "+" and bus "-" I/Os to simultaneously provide a high impedance state. The bus depends on external resistor components for bias and termination. Recommended resistor sizes are shown in Figure 4.

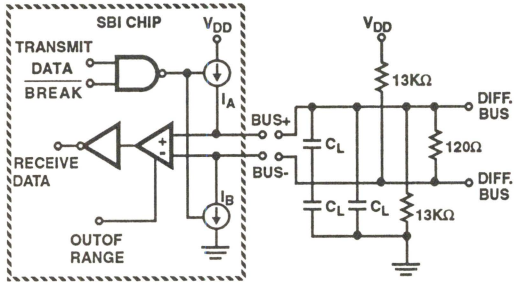
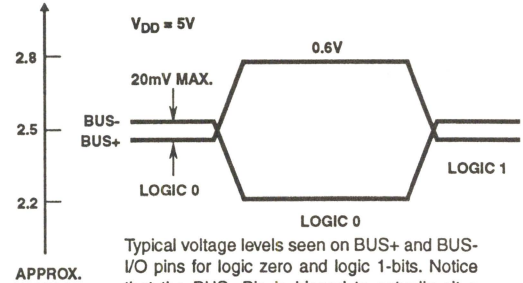


FIGURE 4. DIFFERENTIAL DRIVER/RECEIVER

A zero transmitted on the bus will appear as a large voltage drop across the BUS+ and BUS- pins, i.e. BUS+ might typically sit at +2.8V and BUS- at +2.2V for a logic zero. For a logic level one, the SBIC actually three-states the BUS+ and BUS- pins and relies on external resistors to bias the bus lines. The lines are both biased to sit at approximately 2.5V with a small (perhaps 20mV) voltage drop across the two lines. In this condition the BUS- line actually sits at a slightly higher potential than the BUS+ line. See Figure 5. Thus, the bus actually "floats" to a logic level one, but must be driven to a logic level zero. Logic 0-bits always dominate over logic 1-bits on the bus. If two MCU's simultaneously transmit a zero and a one on the bus, the zero will override the one and the bus will merely appear to be transmitting a zero. The "marking" or idle signal on the bus is a logic one. If the bus is idle or if a micro is sending a logic one, then a one will appear on the bus.

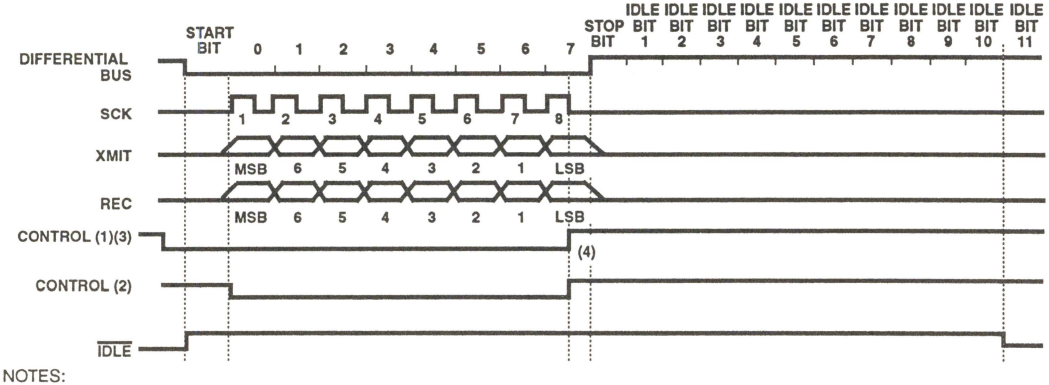
In addition to the transmission of data, the differential data transceiver accepts at its bus "+" and bus "-" I/Os, serial differential data which is translated into the standard digital logic levels. This reception of data also occurs while transmitting, thus reflecting the data seen on the bus back into the SBIC data register.



Typical voltage levels seen on BUS+ and BUS- I/O pins for logic zero and logic 1-bits. Notice that the BUS- Pin is biased to actually sit a higher voltage potential than the BUS+. Values shown are for V_{DD} = 5V

FIGURE 5.

The differential transceiver cell allows bus activity by other devices on the bus "+" and bus "-" I/Os when power to the cell is shut off. Therefore, this powered off condition places the transceiver outputs, BUS "+" and BUS "-", in a high impedance state. When the cell is either being powered up or down, with or without bus activity, SCR latch-up protection is provided such that this activity is not affected.



NOTES:

1. The control signal at the transmitting node.
2. The control signal at the receiving node.
3. There is a delay between the control pin being pulled low and the actual beginning of the start bit.
4. If the control pin is again puled low before the end of the stop bit, then the next start bit will begin at the end of the previous stop bit.

FIGURE 3. SCK, CONTROL, AND $\overline{IDLE}$ SIGNALS DURING THE SPI MODE OF OPERATION

Receive data is an output from the differential transceiver cell. It is the output of a differential amplifier which decodes the bus "+" and "-" I/O. When the bus "+" and "-" has been driven positive and negative respectively to a differential voltage value greater than V_{IDH}, the output of the differential amplifier is a logic one, which is inverted and considered a 0-bit from the bus. Otherwise, for level below V_{IDL} the differential amplifier output is a logic zero, which, in turn, is inverted and considered a 1-bit from the bus.

Twisted wire pair (or adjacent PC board traces) is recommended for the two differential bus lines.

The BREAK input, when held at a logic zero, (low) causes the differential transmitter driver to generate a continuous logic level zero on the differential bus. This action can generate a data collision which can be either used as a break or a request for arbitration by the system. When held at logic one, (high) this input has no effect on the operation of the cell.

The out of range output is normally a logic zero but goes to a logic one when the common mode voltage on both differential bus inputs exceeds a voltage value greater than V_{MAX} or less than V_{MIN} (see device specifications). This output is used by a latch to hold the received data at the logic level it was before the over range signal occurred.

Provided on chip is a power-on reset function. The transceiver cell's reset output is held to a logic zero on power up and switches to a logic one at or before V_{DD} rises to 4.0V. This output is used to ensure that other on-board logic has been properly initiated. During this reset time, the bus "+" and the bus "-" I/Os provide a high impedance state to the bus.

Bus Speed

SBIC systems typically use a bus speed of 7812.5 bits/second which is accomplished by using a 1MHz internal clock. However, no restriction on any other baud rate is designed into the chip, except its upper speed limit (see device specifications).

Bus Byte Format

All bytes transmitted on the bus follow the standard UART style asynchronous non-return-to zero data format consisting oft start bit (logical zero) followed by 8 data bits (LSB first), and 1 stop bit (logical one).

Bus Message Format

All messages transmitted on the bus consist of a number of bytes, from 1 to N, with no restriction on length. The user must be aware, however, that the longer the message length, the greater the probability of collision with messages being transmitted at random from other masters on the bus. Typical message lengths of systems now in use range from 1 to 4 bytes.

The actual definition of each byte sent is left for the user to determine, i.e. the user must define the system protocol. For instance, a typical (and recommended) protocol might dictate that the first byte of each message sent be a unique address/identification byte. The first byte sent by a node (an MCU coupled with an SBI chip) might contain address information telling where (to which node[s]) the message is targeted for or where the message came from.

Other possibilities would be to identify the type of message sent (e.g. an instruction or just information) or the length of the message. The remaining bytes in each message can be merely data bytes that comprise the actual message. The user can even use the last byte as a check sum so that all receiving nodes can check for errors in transmission.

Messages are normally received by all nodes on the bus and may be processed by one or more micros, i.e., each MCU may decide, after receiving the first byte (address/ID byte) that this particular message is not needed for its operation. The MCU can then ignore the remainder of the message.

Prioritization

Since simultaneous transmission of address/ID bytes from several microcomputers is a possibility, a system of prioritization should be determined for bus arbitration. Due to the electrical characteristics of the differential data bus, each unique address/ID byte can automatically contain priority information used for bus arbitration. Merely use "lower" value ID bytes for higher priority messages. "Lower" value, in the SBIC case, means an ID byte with more zero's in its least significant locations. To further explain, since the differential bus transmits data least significant bit first and a zero overrides a 1-bit simultaneously transmitted by different nodes, an ID byte with least significant bit equal to zero will override an ID byte from a micro whose least significant bit is a one. If this does occur on-chip bus arbitration will automatically allow only one SBIC chip (with the highest priority address/ID byte) to continue transmitting. In this case it is the micro who transmitted the 0-bit. Assuming both ID bytes contain identical LSBs (bit 0) then arbitration is carried on to the next bit (bit 1),and soon.

Reflected Data

Whenever a microcomputer sends data through the SBIC and onto the differential bus, it will always receive reflected data back. The reflected data is the data that was actually seen on the bus. Keep in mind that during data collisions between simultaneously transmitting micros, zeroes override ones. In addition, any noise that may have been induced on the bus may alter the resultant reflected byte.

Bus Arbitration

Bus arbitration is the attempted transmission onto the differential bus of an initial byte (preferably an address/ID byte) by one or more user microcomputers. The purpose of bus arbitration is to enable a single microcomputer to obtain sole usage of the bus for the purpose of transmitting a message.

Bus arbitration is accomplished via a combination of methods which include an MCU software comparison of transmitted bytes to reflected bytes, the SBIC's collision detection circuit, and its start bit arbitration detector circuits.

Collision Detection

The SBIC's collision detector circuit compares the bits being sent from a user microcomputer to the reflected byte simultaneously received back from the differential bus. If the collision detector detects a difference in the data, it immediately blocks the user microcomputer's transmitted data from fur-

ther reaching the bus. This will happen, as stated in the "Prioritization" section, when a micro with a higher priority address/ID byte attempts "simultaneous" transmission (actually, i.e. within a time window of 1/4 bit time).That micro, with a higher priority ID byte, is obviously sending a 0-bit and its reflected byte matches the byte it is sending. Not detecting a collision, it continues to transmit its message, while the lower priority MCU is cut off from transmitting on the bus. The lower priority micro will be inhibited from transmitting on the bus until the message presently on the bus has ended (EOM = "End of Message" condition).

End of Message Condition

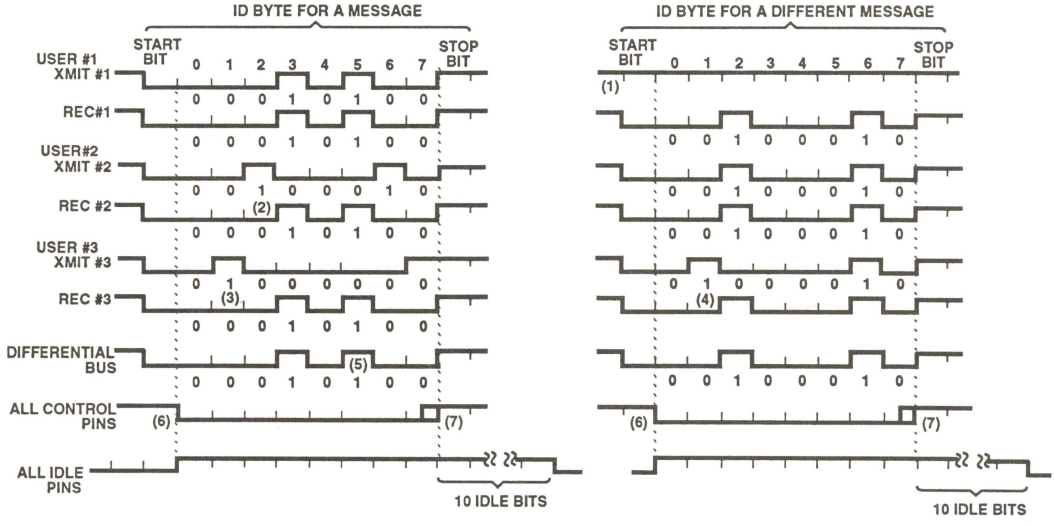
After transmitting the last byte of a message, the transmitting MCU must generate an End of Message (EOM) condition. An EOM condition is defined as a 10-bit length idle condition, i.e., the bus must remain idle (logic1) for a period of 10-bit times (1280 internal clock periods). This can be done by merely creating a 10-bit delay in MCU software.

Start Bit Arbitration Detection

Arbitration, as discussed above, is only necessary when two or more micros attempt to transmit within 1/4 bit time (32 internal clock periods) of each other. Otherwise, once a micro begins a transmission on the differential data bus, all other SBI chips sense the start bit and inhibit their microcomputers from transmitting (again, after a 32 clock period arbitration window delay). Once the arbitration detector circuit has blocked an MCU's transmission, access to the bus will be blocked until an End of Message condition.

Start of Message Delay

In order to properly synchronize various MCU's (which may be using different modes of operation) for impartial arbitration, each node must delay 2-bit times (256 internal clock periods) after detecting the $\overline{\text{IDLE}}$ signal drop low before transmitting, i.e., before the start bit of the next message reaches the bus. When using the SPI or Buffered SPI modes, this delay is automatically designed into the SBI chip. However, when using the SCI mode, the MCU must support this required delay. Fortunately, 68HC05 microcomputers using the SCI port will inherently experience a delay between the time that the SCI data register is loaded and the time that the start bit actually appears on the SCI port transmit pin (TxD). At a baud rate of 7812.5 bps this delay can be as long as 256 SBI chip internal clock periods. If this is so, then the user MCU does not have to worry about providing this delay.



NOTES:

1. USER #1 is note transmitting + marking.
2. Point at which USER #2 loses bus arbitration.
3. Point at which USER #3 loses bus arbitration.
4. Point at which USER #3 loses bus arbitration.
5. This '1' bit is not overridden by the '0' bits from users 2 and 3 because both users 2 and 3 have previously been blocked from bus access due to data collisions.
6. The control pin on the transmitting node goes low earlier in both SPI modes (it is pulled low by micro).
7. The control pin remains low until the end of the last data bit of the 2 byte set when using the buffered SPI mode, but goes high at the middle of the last data bit in other modes.

FIGURE 6. EXAMPLE OF THE SCI CHIP OPERATING DURING BUS ARBITRATION

Idle Detection

An idle detector circuit is used to detect when the differential bus is in the idle condition, i.e., no user microcomputer has control of the bus and the bus is sitting at a mark condition (a logic one). The idle detector senses a received stop bit and delays for a short idle period of 10-bit times, during which the bus must remain idle. The idle output pin is then set to a logic zero (true). It is later set to a logic one by receiving a start bit. During the 10-bit time delay, if a non-idle condition such as noise is detected on the bus, the delay period counter will be restarted.

Due to the 10-bit time idle delay period, once an MCU wins bus arbitration, it should send the next data byte to be transmitted within a period of 10-bit times (1280 internal clock periods). Each subsequent data byte to be sent should also not exceed the interbyte maximum of 10-bit times. If this maximum is exceeded, all SBIC chips will have detected the idle condition and now pull their idle lines low and reset their bus arbitration and collision detection circuits, thereby allowing other SBI chips with messages to send to arbitrate for the bus. Figure 6 shows the detailed operation of the serial bus interface chip during bus arbitration. This example shows the arbitration of a single byte (e.g. the address/ID byte) from three different user microcomputers. Two full arbitration cycles are shown.

Break Generator

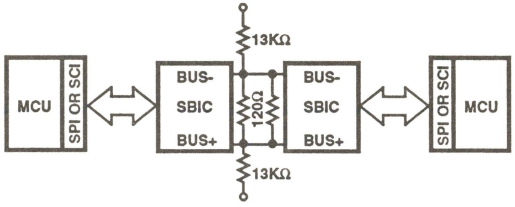
A request for arbitration can be generated by a node that needs to interrupt transmission of a long data string. This can be accomplished by forcing the SBIC's $\overline{\text{IDLE}}$ pin to a logic zero; this forces a data collision (by sending 0-bits) after three data bytes have been transmitted, and the transmitting MCU is required to detect this break condition and stop transmitting. It is, however, allowed to re-arbitrate for the bus and the interrupting mode may not generate a second break condition if it loses arbitration.

Using the CDP68HC68S1

Following are some hardware and software recommendations for using CDP68HC68S1 Serial Bus Interface Chip. Requirements may vary depending upon the user's system configuration.

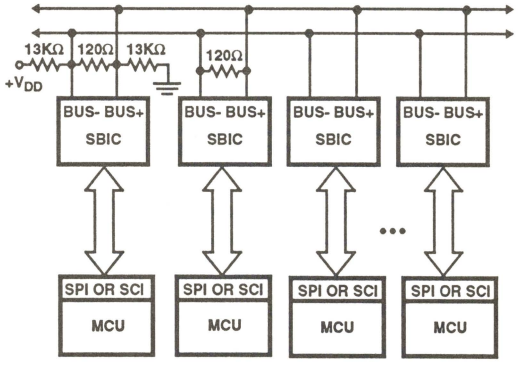
Hardware (General)

The differential bus lines (BUS+ and BUS-) must be terminated with external resistors as shown in Figure 4. This applies, however, only to one node (an MCU/SBIC pair) along the bus. Since all SBI chips are wired in parallel across the network bus, there is no need for additional 13K bias resistors at each node. The 120Ω termination resistors should, however, be present at two nodes if the network does indeed contain two or more nodes. The 120Ω resistor provides the voltage drop across which the SBI chip senses logic zero and logic 1-bits. If two nodes each utilize 120Ω termination resistors as shown in Figure 7A, the effective resistance across the BUS+ and BUS- pins drop to 60Ω total (due to the parallel wiring method). Any less resistance would not provide an ample voltage drop for the receiver cell op amp to sense. Following these guidelines, typical systems might look like those shown in Figure 7.



NOTE: Hardware configuration for a network consisting of two microcomputers. Notice that the pullup resistor is connected to the BUS- pin and the pulldown to BUS+.

FIGURE 7A.



NOTE: Hardware configuration for a network consisting of 3 or more MCU's. Notice that the bus utilizes no more than 1 set of 13K bias resistors and no more than two 120Ω termination resistors.

FIGURE 7B.

FIGURE 7. HARDWARE CONFIGURATION FOR A NETWORK OF MICROCOMPUTERS

Software (General)

Although each user's protocol may vary, the following general procedure should be followed when using the SBI chip in any mode:

When a microcomputer is preparing to transmit a message it should monitor the SBIC's $\overline{\text{IDLE}}$ pin and wait for it to go low (logic zero) indicating the bus is idle. Then the MCU attempts to transmit the first byte (preferably an Address/ID byte). If no other MCUs are transmitting at this time, or if this MCU has the highest priority ID byte, the SBI chip's collision detector circuit will permit transmission.

The microcomputer must then confirm transmission by reading the byte reflected back from the bus. If this byte matches the byte transmitted then the MCU has gained control of the bus and may continue to transmit the remainder of the message (if any).

If the reflected byte does not match the ID byte sent then the MCU has not gained control of the bus and may not presently transmit. It should, however, check the reflected ID byte to see if the incoming message (i.e. the message from the

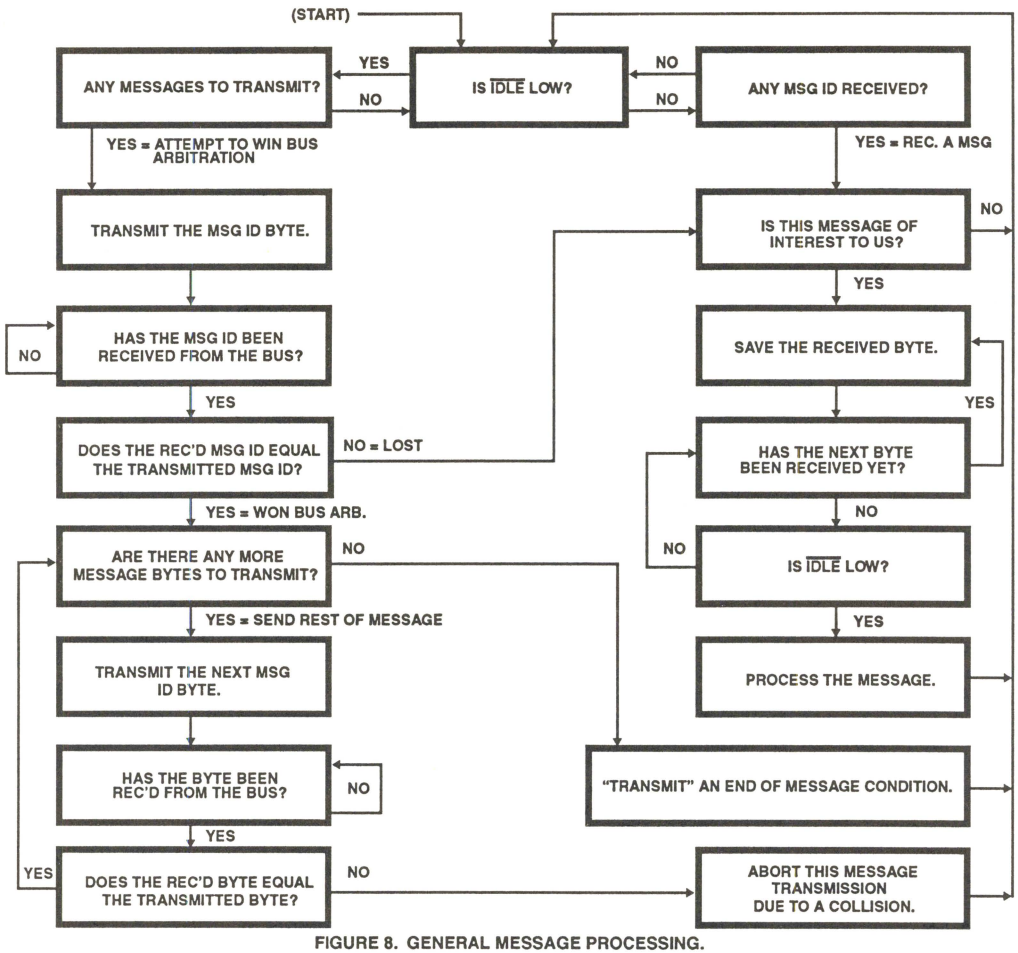


FIGURE 8. GENERAL MESSAGE PROCESSING.

arbitration-winning MCU) is of any interest. If so, it should save the incoming message (the length of which may be specified in the ID byte) and then wait for the $\overline{\text{IDLE}}$ line to go high before re-attempting transmission (if still desired). The flowchart in Figure 8 reflects this procedure.

The SCI Mode, Hardware

In the SCI mode, the TxD and RxD pins on the user microcomputer must be connected to the XMIT and REC pins on the SBIC chip, respectively, as shown in Figure 9. The MCU's SCI port should be configured for the same baud rate and character format as that used by the bus interface (i.e. 1 start bit, 8 data bits and 1 stop bit). The start and stop bits are used to synchronize the data, a byte transfers between the user microcomputer and the SBI chip. When using the SCI mode, the SBI chip should always be properly mode and chip selected. This can be accomplished by either a user microcomputer output signal or by permanent wiring. This is required in order to always be able to receive messages from other microcomputers on the bus, which can happen at random. For the SCI mode, the SBI chip's MODE pin must be set to1 and the $\overline{\text{CS}}$ pin to 1.

SCI Mode, Software

The procedure to follow for transmitting/receiving in the SCI mode is basically identical to that stated in the "Using the CDP68HC68S1-Software" section above, with the following exception:

Start of Message Delay

Transmitting a byte via the 68HC05 SCI port basically requires loading the byte into the MCU's SCI data register (once the SCI port is initialized). However, after the SBIC's $\overline{\text{IDLE}}$ pin drops low, the user may have to create a delay before transmitting the FIRST byte of a message; this necessary 2-bit time (256 internal clock periods) delay is called the Start of

Message (SOM) delay. Fortunately, SCI ports exhibit an inherent delay between the loading of the transmit data buffer and the actual beginning of the start bit appearing on the TXD pin. This delay, at 7812.5 Baud, can be as long as 256 SBI chip internal clock periods and can be used to synchronize SCI users with SPI and Buffered SPI users to ensure impartial bus arbitration. The delay for a particular microcomputer must be determined by the user. If this inherent delay is less than 256 clock periods, then the user must delay the loading of the first byte enough to ensure that the total delay including the inherent delay of the SCI port is 256 clock periods.

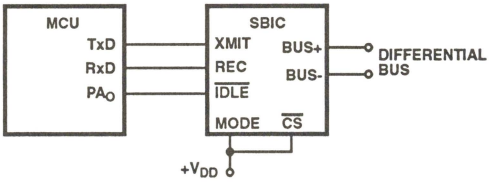


FIGURE 9. USING THE SCI MODE

Monitoring the $\overline{\text{IDLE}}$ Pin

The user microcomputer must monitor the $\overline{\text{IDLE}}$ pin on the SBIC chip in order to determine when a message ends, when the next received byte is a Msg ID byte, and when to attempt arbitration if the user microcomputer has a message to transmit.

The user microcomputer must be able to both detect when the $\overline{\text{IDLE}}$ signal goes from high to low and sense at other times whether it is either high or low. Detecting the change from high to low is necessary in order to know exactly when the bus goes idle. An MCU can then begin bus arbitration by attempting to transmit. Being able to sense the level of $\overline{\text{IDLE}}$ is necessary in order to be able to start transmitting a message sometime after $\overline{\text{IDLE}}$ has gone low but no other user on the bus has had a message to transmit for a length of time.

Instead of polling the $\overline{\text{IDLE}}$ pin via an MCU input pin, the user may wish to conserve CPU time by using interrupts to monitor bus activity. The user microcomputer's external interrupt pin (IRQ) can be used to edge detect the $\overline{\text{IDLE}}$ pin for high to low transitions.

Using 68HC05 SCI Port Flags

During message reception, the 68HC05 SCI port receive data register full flag (RDRF), and optionally its associated interrupt, can be used by the user microcomputer to determine when to unload the next received byte.

The user may wish to ignore the RDRF flag and disable the RDRF interrupt during reception of an unwanted message. In this case the user can merely wait for the $\overline{\text{IDLE}}$ pin to go low before attempting any further actions.

The normally available transmit data register empty flag (TDRE) can be used to determine when to load the next byte to be transmitted onto the bus. If there are no more bytes to be transmitted, then consider the last message as having been transmitted, and generate an End Of Message (EOM) (i.e. transmit a logic 1 for 10 contiguous bit times by creating a software delay).

Framing Errors

While in the SCI mode, the SBI chip is capable of detecting incoming framing errors. It will do this even though the incoming signal is also echoed to the user microcomputer, which should also detect the framing error via its' UART. When a framing error is detected by the SBI chip, the generation of the SCK pulses is terminated until and End Of Message is detected.

The SPI Mode Hardware

The Master Out Slave In, (MOSI), and Master In Slave Out, (MISO), pins on the user microcomputer are connected to the REC and XMIT pins of the SBI chip, respectively, as shown in Figure 10. The SCK pins on the user microcomputer and the SBI chip are connected together. Synchronization of data transferred between the user microcomputer and the SBI chip is done by using the SCK signal provided by the SBI chip.

In the SPI mode of operation the SBI chip should always be properly mode selected. This may be accomplished either by a user microcomputer output signal or by permanent wiring in order to guarantee that the SBI chip will always be able to receive messages from other microcomputers on the bus, which may happen at random. To select the SPI mode, set the MODE pin to a logic I and the $\overline{\text{CS}}$ pin to a logic 0.

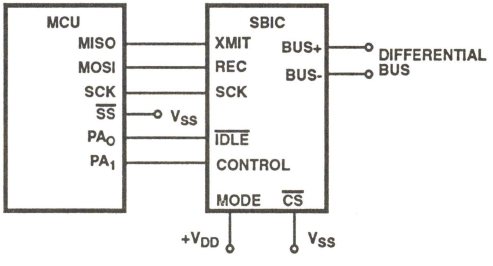


FIGURE 10. USING THE SPI MODE

The user microcomputer should configure its SPI port for slave mode operation with SCK positive polarity and data transfer on SCK leading edge (i.e. CPOL = 0, CPHA = 1, for 68HC05 microcomputers). 8-bit data transfers between the user microcomputer and the SBI chip occur at differential bus transfer speed.

In the SPI mode, the user microcomputer operates in the slave mode and the SBI chip operates as the master. The $\overline{\text{SS}}$ pin on the user microcomputer must be wired low or forced low whenever the SBI chip has incoming data. It may be useful to connect the CONTROL pin of the SBI chip to the Slave Select ($\overline{\text{SS}}$) pin of the 68HC05 microcomputer. The SBI chip will then control the user microcomputer's SPI port. The user microcomputer can request transmission of data onto the bus by the SBI chip by loading data into its SPI data register and then pulling the SBIC's CONTROL pin low (for at least 1µs). However, it must do so before the SBI chip has begun to receive data from another MCU.

SPI Mode, Software

The SPI mode is similar to SCI mode in that the user microcomputer sends/receives data to/from the SBI chip 1 byte at a time. In the SPI mode, however, the user microcomputer must reverse the bit order of transmitted and received bytes. When transmitting a message, each bit of a transmitted byte is simultaneously transmitted onto the bus and a reflected bit is simultaneously received from the bus.

Monitor and Control of the CONTROL Line

In the SPI mode, the user microcomputer monitors the CONTROL pin on the SBI chip in order to determine if the SBIC is ready to accept a transmit request. Actually, a data collision may still occur and the user microcomputer must always be ready to handle it.

The CONTROL signal is normally high and goes low when data is on the bus or when pulled low by the user microcomputer. After being pulled low by the user microcomputer, which signals a request to begin the transmission data, the CONTROL signal will latch low and stay low until the middle of the last data bit has been transmitted and appears on the bus.

The CONTROL signal will also go low at the beginning of the first data bit, when received from the bus. It will then go high at the middle of the last data bit.

When the SBI chip begins to receive a byte of data from the bus and the user microcomputer has not pulled the SBIC's CONTROL line low, the SBI chip will pull CONTROL low and start generating the SCK clock signal. As each data bit is received it is clocked out of the SBI chip and into the user microcomputer. Any data in the user microcomputer's SPI data register will be transferred out and into the SBI chip.

The CONTROL signal will go high at the midpoint of the eighth data bit. This will allow the user microcomputer to have enough time to review the just received SPI data and reload it, if further data is needed to be transmitted. However, it must again pull the CONTROL pin low to signal he SBI chip that it should begin transmitting. As a slave to he SBI chip, the user microcomputer must be able to and le the incoming data on the SPI port without affecting its other software routine functions.

Detecting $\overline{\text{IDLE}}$ via a User Microcomputer External Interrupt

The user microprocessor's external interrupt should be set to edge detect $\overline{\text{IDLE}}$ for falling transitions, i.e. EOM detection. If possible, detect CONTROL for rising transitions, for byte transmission/reception complete detection.

Use of Internal User Microcomputer Flags and Interrupts

The normally available SPI finished flag (SPIF) and optionally its associated interrupt may be used by the user microcomputer to know when a byte transmission/reception of is complete.

The user microcomputer should be ready to handle the Write Collision, WCOL, error flag. The WCOL flag is set when a collision is detected in the SPI port. This will occur when the user microcomputer tries to load a byte into the SPI data register after the SBI chip has already begun to load data into the SPI port.

Sending Messages to Other Microcomputers on the Bus

In order to send a message to other microcomputers on the bus while in the SPI mode the user microcomputer should:

1. Monitor the $\overline{\text{IDLE}}$ pin and determine if the bus is currently busy or if a transmission may be immediately started.
2. Monitor CONTROL to determine if it is ok to load the byte to be transmitted into the user microcomputer's SPI data register.
3. Load the byte to be transmitted into the SPI data register.
4. Pull the CONTROL pin low to signal the SBI chip to start a byte transmit cycle.
5. Wait until the byte transmit cycle is completed as signaled by the SPI Finished, SPIF, flag/interrupt in the SPI port or by the CONTROL signal going high.
6. Compare the received byte with the last transmitted byte.
7. If the received byte equals the last transmitted byte, and more bytes remain to be transmitted, then continue the cycle with step #3. If there are more messages to transmit, then go to step #1. If there are no more bytes to be transmitted, then consider the message as having been transmitted, and generate an End Of Message (EOM) (i.e. delay for 10 contiguous bit times). Go to step #1.
8. If the received byte does not equal the last transmitted byte and this is the first byte of a message, then treat the received byte as the first byte of a received message (i.e. the ID byte). Attempt to retransmit the previous message after the $\overline{\text{IDLE}}$ signal has gone low again. If this happens during the transmission of a later message byte, other than the ID byte, then consider it due to either an erroneous data collision on the bus or due to noise collisions on the bus causing the message to have to be re-transmitted. Go to step #1.

Framing Errors

While in the SPI mode, the SBI chip is capable of detecting incoming framing errors. If one is detected, generation of the SCK pulses to the user microcomputer is terminated. The SBI chip essentially quits receiving data and starts looking for an End Of Message. Resetting of the SCK generator will occur upon receiving an EOM. Meanwhile, software must be prepared to resynchronize the micro's SPI port; this can be done by disabling and then reinitializing it.

Even though the SBI chip can detect framing errors, it can not flag the user microcomputer that one has occurred. Since the previously received byte has already been transferred to the user microcomputer, the SBI chip will simply refuse to accept any further incoming data until an EOM occurs. Thus, one way that the user microcomputer may detect that the received data is valid, is via using a check sum byte imbedded within each message. Another way would be to compare the number of bytes received fora particular ID to the number expected for that ID.

Buffered SPI Mode, Hardware

The MOSI and MISO pins on the user microcomputer should be connected to the XMIT and REC pins of the SBI chip respectively. The SCK pins on the user microcomputer and

the SBI chip should also be connected together, as shown in Figure 11. Synchronization of the data that is transferred between the user microcomputer and the SBI chip is done by the SCK signal which is provided by the user microcomputer.

The Slave Select ($\overline{SS}$) pin on the user microcomputer must be wired high or forced high whenever the SBI chip is selected.

The user microcomputer should configure its SPI port for master mode operation, SCK low polarity, and data transfer on first edge (i.e. CPOL = 0, CPHA = 1 for 68HC05 microcomputers).

The SBI chip must be chip selected either by a user microcomputer output signal or by permanent wiring of its pins. To select the Buffered SPI mode, set the MODE pin and the $\overline{CS}$ pin to logic zero. This is required in order to transfer data between the SBI chip and the user microcomputer. However, in the Buffered SPI mode, since the MCU is operating as a master and controls the SPI port, chip selection is only required during when the SPI transfers are actually occurring.

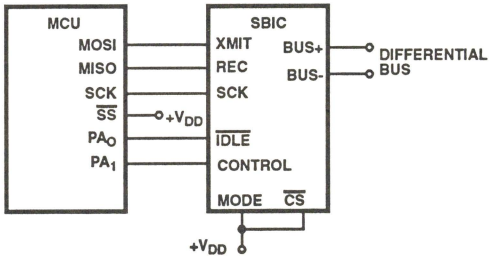


FIGURE 11. USING THE BUFFERED SPI MODE

Buffered SPI Mode, Software

The principle difference between the Buffered SPI mode and the normal SPI mode is the use of a 2 byte internal buffer. Also, the Buffered SPI mode allows the user microcomputer to operate in the master mode, instead of the slave mode, which allows high speed transferring of data between the SBI chip's buffer and the user microcomputer.

For typical operation, the user microcomputer loads the SBI's 2 byte buffer, at a high speed, using its SPI interface. The 68HC05's SPI Finished flag (SPIF), and optionally its associated interrupt, may be used by the user microcomputer to know when the transfer of a byte between the user microcomputer and the SBI chip is complete. Then it signals the SBI chip, by pulling its CONTROL line low, to transmit the data in the buffer onto the differential bus.

The SBI chip, at a differential bus speed, then attempts to transmit the buffered data onto the bus. During this attempt, the SBI chip will receive two reflected bytes of data back from the bus, store them in the buffer and then disable the buffer from receiving further data from the differential bus until this received data is later unloaded by the user microcomputer at high SPI transfer speeds. The MCU should also, at this time, simultaneously load the next 2 bytes of data to be transmitted into the buffer.

While it is transmitting and receiving the 2 bytes of data on the differential bus the SBI chip will not allow transfer of data to and from the user microcomputer. In fact, the SBI chip does not need to be chip selected during this time.

The bus will override the user microcomputer if incoming data is received during the time when the user microcomputer is performing a data transfer, after having unloaded the previous 2 bytes. The data from the differential bus will be loaded into the SBIC buffer, while the data from the user microcomputer will be lost. The data that the user microcomputer will receive during this transfer, is undefined. The user microcomputer has no way of knowing its transfer has been aborted unless it either monitors the CONTROL signal for a rising transition or by detecting that CONTROL was not high at completion of the SPI transfer.

Monitoring the Control Signal

The user microcomputer should monitor the CONTROL signal on the SBI chip, in order to determine whether it is actively transmitting or receiving data. The CONTROL signal is used to determine who has access to the 2 byte buffer. During data reception or transmission to the differential bus by the SBIC its CONTROL pin is low signifying that the differential bus now has access to the SBIC and the MCU is locked out from accessing the SBIC. Then when 2 bytes of data have been received from the differential bus, the SBI chip will pull its CONTROL line high, signaling to the MCU that the MCU can now access the SBIC's 2 byte buffer. The MCU may now read the 2 bytes received and simultaneously transmit two more bytes (if desired) by performing a 2 byte transfer (a swap of data), via the MCU SPI port, with the SBIC; then the MCU pulls the SBIC's CONTROL pin low to transmit the two new bytes. The CONTROL pin will remain latched low (by the SBIC) until the two new bytes are transmitted.

The user microcomputer should also monitor the $\overline{IDLE}$ signal in order to accurately know when the bus is idle or when bus arbitration is occurring, when a received message has finished, and when the next bytes to be received are the beginning bytes of a new message. Preferably, the user microcomputer's external interrupt should be set up to edge detect falling $\overline{IDLE}$ and rising CONTROL transitions.

When the CONTROL pin goes high, it signals that the buffer is full and that the user microcomputer currently has access. When the $\overline{IDLE}$ pin goes low, it is signaling that the current message has been completed, and an MCU may now arbitrate for the bus.

Size of Messages that can be Transmitted or Received

In the Buffered SPI mode, the user microcomputer can only send messages in 2 byte multiples. Transmitting messages with an odd number of bytes, to other microcomputers on the bus, is NOT supported by the SBI chip in Buffered SPI mode. However, reception of any number of bytes is supported.

In the Buffered SPI mode, the user microcomputer can receive messages of any length. For odd length messages, the user microcomputer must know when the message is finished either from the message ID byte or via the $\overline{IDLE}$ signal. Since the SBI chip will give no indication as to whether the buffer contains one or 2 bytes of information from the bus, the message length should be contained within the message data bytes.

When a single byte is received from the bus, followed by a bus idle condition, the SBI chip will, as it normally does when the buffer has received 2 bytes, set the CONTROL signal high. It will then relinquish control of the buffer for data transferral via the user microcomputer, and restrict access to the buffer from incoming bus data until the 2 byte data transfer has been completed.

If only 1 byte is received from the bus, the user microcomputer will receive it first when performing the 2 byte data transfer. The second byte received by the user microcomputer, during this transfer, is undefined. A 2 byte transfer is still required in order to return control of the buffer back to the SBI chip, to gather further incoming data from the bus.

Power On/Reset

The SBI chip is reset internally, at power on. After reset, the CONTROL pin is set high and $\overline{IDLE}$ is set low. The buffer access is set as though 2 bytes have just been received from the bus. A 2 byte transfer must be performed, via the user microcomputer, in order to initalize the SBI chip for general operation.

Sending Messages to Other Microcomputers on the Bus

In order to send a message to other microcomputers on the bus, while in the Buffered SPI mode, the user microcomputer should:

1. Monitor the SBIC CONTROL pin to know when it is ok to perform the 2 byte transfer between the user microcomputer and the SBI chip.
2. Perform the 2 byte transfer between the user microcomputer and the SBI chip for the first 2 bytes of the message.
3. Pull CONTROL low to tell the SBI chip to start a 2 byte bus transmit cycle.
4. Wait until CONTROL goes high again indicating that the 2 byte transmit cycle has completed.
5. Perform another 2 byte transfer between the user microcomputer and the SBI chip, thus giving it the next 2 bytes to be transmitted and giving the user microcomputer the 2 bytes just received.
6. Compare the just received 2 bytes with the 2 bytes which were attempted to be transmitted.
7. If the received and last transmitted bytes are equal and more bytes remain to be sent, then continue the cycle with step #3.
8. If the received and last transmitted 2 bytes are unequal, then restart with step #2.

Creating an EOM after a Message Transmission

There must be at least a 10-bit interval of bus idle between the stop bit of the last byte of one message and the detection of the start bit of the first byte of the next message. This can be implemented by either:

1. Including a 10-bit interval time out, via using a timer or software loop.
2. The user microprocessor can simply wait until it senses $\overline{IDLE}$ going low.

Receiving Messages from Other Microcomputers on the Bus

If the user microcomputer loses arbitration, or if it has no message to transmit and another microcomputer begins to send its message onto the bus, the SBI chip will begin to receive a message from the bus.

The SBIC CONTROL pin will go low at the beginning of the first data bit that is received from the bus. It will go high either whenever 2 bytes have been received, or when 1 byte has been received followed by the bus going idle (i.e. when $\overline{IDLE}$ goes low).

The transition of CONTROL from low to high indicates that the SBI chip has 2 bytes in its internal buffer for the user microcomputer to retrieve. Whether the SBI chip has received either 1 or 2 bytes, the user microcomputer must perform a 2 byte transfer in order to return control of the buffer back to the SBI chip.

The user microcomputer must detect CONTROL going high and transfer the 16-bits from the SBI chip before the beginning of the first data bit of the next message or else the bus will be locked out of accessing the buffer until after both the next 16-bit transfer is complete and $\overline{IDLE}$ goes low. Thus, if there was further incoming data and this did occur, some of the incoming data may be lost.

Framing Errors

While in the Buffered SPI mode, the SBI chip is capable of detecting incoming framing errors, however it is unable to flag this to the user microcomputer. When the SBI chip detectsaframing error, anyfu rther loading of the SBI chip's internal buffer is terminated. The SBI chip essentially quits receiving data and starts looking for an End Of Message. Resetting of the framing error will occur upon receiving an EOM.

Even though the SBI chip can detect framing errors, it can not flag the user microcomputer that one has occurred. Since the previously received byte has already been loaded into the SBI chip's buffer, the user microcomputer must determine whether this data is valid. If a framing error occurs during the first byte of a 2 byte reception, access to the buffer will be restricted from the user microcomputer until and EOM occurs. If a framing error occurs during the second byte of a 2 byte reception, the user microcomputer will be given access to the buffer. However, even if the user microcomputer unloads the buffer, the SBI chip will not load any further data into the buffer until an EOM occurs. Basically, when a framing error occurs, no further data is read from the bus and buffer access is given to the user microcomputer either immediately or upon an EOM.

One way that the user microcomputer may detect that the received data is valid, is by using a check sum byte imbedded within each message. Another way would be to compare the number of bytes received for a particular ID to the number expected for that ID.

References

Portions of the information contained in this document were taken and condensed from Chrysler Corporation's "CCD USER'S MANUAL" issued April 15,1987.

HARRIS SEMICONDUCTOR

HIP7010

ADVANCE INFORMATION

April 1994

J1850 Byte Level Interface Circuit

Features

- Fully Supports VPW (Variable Pulse Width) Messaging Practices of SAE Recommended Practice J1850 for Class B Multiplexed Wiring
- 3-Wire, High-Speed, Synchronous, Serial Interface
- Reduces Wiring Overhead
- Directly Interfaces with 68HC05 and 68HC11 Style SPI Ports
- 1MHz, 8-Bit Transfers Between Host and HIP7010 Minimize Host Service Requirements
- Automatically Transmits Properly Framed Messages
- Prepends SOF to First Byte and Appends CRC to Last Byte
- Fail-Safe Design Including, Slow Clock Detection Circuitry, Prevents J1850 Bus Lockup Due to System Errors or Loss of Input Clock
- Automatic Collision Detection
- End of Data (EOD), Break, Idle Bus, and Invalid Symbol (Noise/Illegal Symbols) Detection
- Supports In-Frame Responses with Generation of Normalization Bits (NB) for Type 1, Type 2, and Type 3 Messages
- Wait-For-Next-Idle Mode Reduces Host Overhead During Non-Applicable Messages
- Status Register Flags Provide Information on Current Status of J1850 Bus
- Serial I/O Pins are Active Only During Transfers - Bus Available for Other Devices 95% of the Time
- High Speed (4X) Receive Mode for Production and Diagnostic Testing/Programming
- TEST Pin Provides Built-in-Test Capabilities for In-System Diagnostics and Factory Testing
- Operates with Wide Range of Input Clock Frequencies
- Power-Saving Power-Down Mode
- Full -40°C to +125°C Operating Range
- Single 3.0V to 6.0V Supply

Description

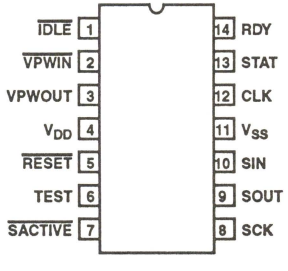
The Harris HIP7010, J1850 Byte Level Interface Circuit, is a member of the Harris family of low-cost multiplexed wiring ICs. The integrated functions of the HIP7010 provide the system designer with components key to building a "Class B" multiplexed communications network interface, which fully conforms to the VPW Multiplexed Wiring protocol specified in SAE Recommended Practice J1850. The HIP7010 is designed to interface with a wide variety of Host microcontrollers via a standard three wire, high-speed (1MHz), synchronous, serial interface. The HIP7010 automatically produces properly framed VPW messages, appending the Start of Frame (SOF) symbol and calculating and appending the CRC check byte. All circuitry needed to decode incoming messages, to validate CRC bytes, and to detect Breaks, End of Data (EOD), Idle bus, and illegal symbols is included. In-Frame Responses (IFRs) are fully supported for Type 1, Type 2, and Type 3 messages, with the appropriate Normalization Bit automatically generated. The HCMOS design allows proper operation at various input frequencies from 2MHz to 12MHz. Connection to the J1850 Bus is via a Harris HIP7020.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP7010P	-40°C +125°C	14 Lead Plastic DIP
HIP7010B	-40°C +125°C	14 Lead Plastic SOIC (N)

Pinout

HIP7010 (SOIC, PDIP)
TOP VIEW



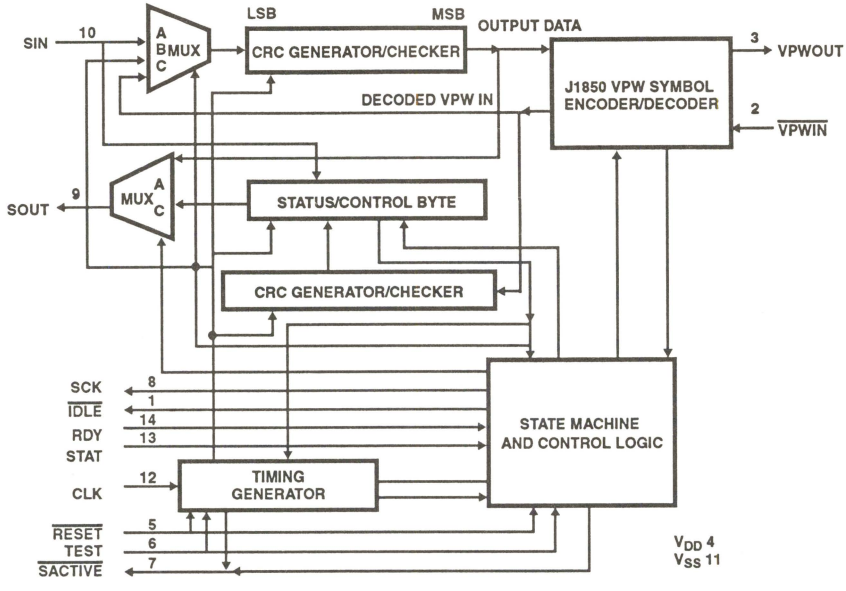
9 MULTIPLEX COMM. CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3644.1

Block Diagram



Pin Description

PIN NUMBER	PIN NAME	IN/OUT	PIN DESCRIPTION
1	$\overline{\text{IDLE}}$	OUT	CMOS Output
2	$\overline{\text{VPWIN}}$	IN	CMOS Schmitt (No V_{DD} Diode)
3	VPWOUT	OUT	CMOS Output
4	V_{DD}	-	Power Supply
5	$\overline{\text{RESET}}$	IN	CMOS Schmitt (No V_{DD} Diode)
6	TEST	IN	CMOS Input with Pull-Down
7	$\overline{\text{SACTIVE}}$	OUT	CMOS Output
8	SCK	OUT	Three-State with Pull-Down
9	SOUT	OUT	Three-State with Pull-Down
10	SIN	IN	CMOS Input with Pull-Down
11	V_{SS}	-	Ground
12	CLK	IN	CMOS Schmitt (No V_{DD} Diode)
13	STAT	IN	CMOS Input with Pull-Down
14	RDY	IN	CMOS Input with Pull-Down

Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... -0.3V to +7.0V
Input or Output Voltage
  Pins with V_{DD} Diode ..... -0.3V to V_{DD} +0.3V
  Pins without V_{DD} Diode ..... -0.3V to +10.0V
ESD Classification ..... Class 2
Gate Count ..... +2500 Gates

Thermal Information

Thermal Resistance θ_{JA}
  Plastic DIP Package ..... +100°C/W
  SOIC Package ..... +120°C/W
Maximum Package Power Dissipation at +125°C
  DIP Package 250mW
  SOIC Package 200mW
Operating Temperature Range (T_A) ..... -40°C to +125°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +3.0V to +5.5V
Operating Temperature Range ..... -40°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... ($0.8V_{DD}$) to V_{DD}
Input Rise and Fall Time
  CMOS Inputs ..... 100ns Max
  CMOS Schmitt Inputs ..... Unlimited

Electrical Specifications

T_A = -40°C to +125°C, V_{DD} = $5V_{DC}$ ±10%, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Operating Current	I_{OP}	CLK = 2.0 MHz	-	1.0	-	mA
Power-Down Mode (Note 1)	I_{PD}	PD = 1	-	5.0	-	µA
Clock Stopped (Note 2)	I_{STOP}	CLK = V_{SS} or V_{DD}	-	5.0	-	µA
Input High Voltage						
CMOS Level (SIN, STAT, RDY, TEST)	V_{IH}		$0.7V_{DD}$	-	V_{DD}	V
Schmitt Trigger ($\overline{RESET}$, CLK, $\overline{VPWIN}$)			$0.8V_{DD}$	-	V_{DD}	V
Input Low Voltage						
CMOS Level (SIN, STAT, RDY, TEST)	V_{IL}		V_{SS}	-	$0.3V_{DD}$	V
Schmitt Trigger ($\overline{RESET}$, CLK, $\overline{VPWIN}$)			V_{SS}	-	$0.2V_{DD}$	V
High Level Input Current						
(CLK, $\overline{VPWIN}$, $\overline{RESET}$)	I_{IH}	$V_{IN} = V_{DD}$	-1	0.001	1	µA
Input Buffer with Pull-down (SIN, TEST, STAT, RDY)			100	TBD	500	µA
Low Level Input Current						
(SIN, CLK, STAT, RDY, $\overline{VPWIN}$, $\overline{RESET}$, TEST)	I_{IL}	$V_{IN} = V_{SS}$	-1	-0.001	1	µA
Output High Voltage						
(SCK, SOUT, VPWOUT, $\overline{IDLE}$, $\overline{SACTIVE}$)	V_{OH}	I_{LOAD} = 0.8 mA	V_{DD} -0.8	-	-	V
Output Low Voltage						
(SCK, SOUT, VPWOUT, $\overline{IDLE}$, $\overline{SACTIVE}$)	V_{OL}	I_{LOAD} = -1.6 mA	-	-	0.4	V
High Impedance Leakage Current						
Three-State with Pull-down (SCK, SOUT)	I_{OZ}	$V_{OUT} = V_{DD}$	100	-0.01	500	µA
		$V_{OUT} = V_{SS}$	-10		10	µA
Schmitt Trigger Hysteresis Voltage ($\overline{RESET}$, CLK, $\overline{VPWIN}$)	V_{HYS}		0.2	0.5	2.0	V

NOTES:

1. SIN, STAT, RDY, and TEST = V_{SS}; $\overline{VPWIN}$ = V_{DD}; CLK = 10MHz
2. SIN, STAT, RDY, and TEST = V_{SS}; $\overline{SACTIVE}$ and $\overline{VPWIN}$ = V_{DD}

Serial Interface Timing (See Figure 1- Figure 7) T_A = -40°C to +125°C, V_{DD} = $5V_{DC}$ ±10%, Unless Otherwise Specified

NUMBER	SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS
-	-	Operating Frequency	2	8	12	MHz
(1)	t_{CYC}	SCK Cycle Time	-	1.0	-	MHz
(2)	t_{LEAD}	$\overline{SACTIVE}$ Lead Time				
		Before Status/Control Transfer	450	718	850	ns
		Before DataTransfer	1200	1250	1350	ns
(3)	t_{LAG}	$\overline{SACTIVE}$ Lag Time				
		After Status/Control Transfer	650	750	850	ns
		After Data Transfer	1200	1250	1350	ns
(4)	t_{SCKH}	Clock (SCK) HIGH Time	450	500	550	ns
(5)	t_{SCKL}	Clock (SCK) LOW Time	450	500	550	ns
(6)	t_{DVSCK}	Required Data In Setup Time (SIN to SCK)	-	10	40	ns
(7)	t_{SCKDX}	Required Data In Hold Time (SIN after SCK)	-	10	40	ns
(8)	t_{DZDA}	Data Active from High Impedance Delay ($\overline{SACTIVE}$ to SOUT Active)	0	10	-	ns
(9)	t_{DADZ}	Data Active to High Impedance Delay ($\overline{SACTIVE}$ to SOUT High Impedance)	-	10	40	ns
(10)	t_{SCKDV}	Data Out Setup Time (SCK to SOUT)	375	475	-	ns
(11)	t_{DXSCK}	Data Out Hold Time (SOUT after SCK)	375	475	-	ns
(12)	t_{RISE}	Output Rise Time ($0.3V_{DD}$ to $0.7V_{DD}$, C_L = 100pF)	20	50	75	ns
(13)	t_{FALL}	Output Fall Time ($0.7V_{DD}$ to $0.3V_{DD}$, C_L = 100pF)	20	50	75	ns
(14)	t_{STATH}	Required STAT Pulse Width	-	20	75	ns
(15)	t_{RDYH}	Required RDY Pulse Width	-	20	75	ns
(16)	$t_{SACTIVE}$	$\overline{SACTIVE}$ Delay from RDY ($\overline{IDLE}$ = V_{SS}) $\overline{SACTIVE}$ Delay from STAT (FTU = 0)	1150 5	1750 285	2350 850	ns
(17)	t_{RDYSCK}	Required RDY Removal Time Prior to Last SCK for Short RDY	-	25	100	ns
(18)	t_{SCKRDY}	Required RDY Hold Time after Last SCK for Long RDY	-	0	50	ns
(19)	t_{REC}	Required SERIAL Recovery Time (Minimum Time after $\overline{SACTIVE}$ Until Next RDY/STAT)	-	0	100	ns

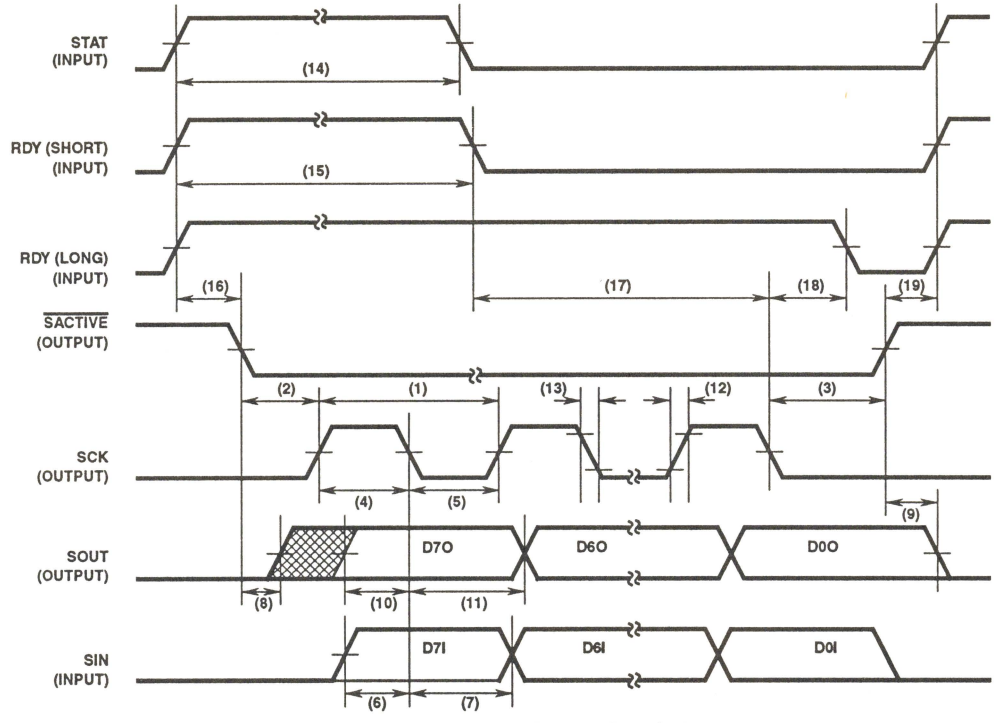


FIGURE 1. SERIAL INTERFACE TIMING DIAGRAM

NOTES:

1. Measurement points are from $V_{DD}/2$, except 12 and 13 which are measured between V_{IL} and V_{IH}.
2. All timings assume proper CLK frequency and Divide Select values to generate 1MHz SCK.

Functional Pin Description

This section provides a description of each of the 14 pins of the HIP7010 as shown in Figure 2.

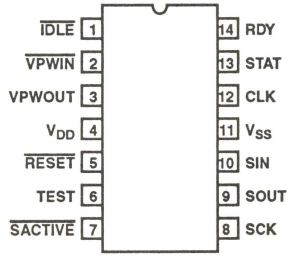


FIGURE 2. 14 PIN DIP AND SO TERMINAL ASSIGNMENTS

V_{DD} and V_{SS} (Power)

Power is supplied to the HIP7010 using these two pins. V_{DD} is connected to the positive supply and V_{SS} is connected to the negative supply.

CLK (Clock - Input)

The Clock input (CLK) provides the basic time base reference for all J1850 symbol detection and generation. Serial Bus transfers between the HIP7010 and the Host microcontroller are also timed based on the Clock input. Proper VPW symbol detection and generation requires a 2MHz clock which is internally derived from the CLK input. Various CLK input frequencies can be accommodated via the Divide Select bits in the Status/Control Register (see **Status/Control Register** for details).

An internal Slow Clock Detect circuit monitors the CLK input signal and generates a HIP7010 reset if the clock is inactive for more than 2µs. This is a safety mechanism to prevent blocking the J1850 and Serial busses in the event of a clock failure. The Slow Clock Detect reset can also be intentionally invoked by externally inhibiting CLK input transitions.

Power can be reduced under Host control via the Power-Down bit in the Status/Control Register (see Status/Control Register for details). Setting the Power-Down bit effectively stops internal clocking of the HIP7010.

For enhanced noise immunity, the CLK input is a CMOS Schmitt trigger input. See **Electrical Specifications** for input levels.

VPWOUT (Variable Pulse Width Out - Output), VPWIN (Variable Pulse Width In - Input)

These two lines are used to interface to a J1850 bus transceiver, such as the Harris HIP7020. VPWOUT is the variable pulse width modulated output of the HIP7010's symbol encoder circuit. VPWIN is the inverted input to the symbol decoder of the HIP7010. VPWIN is a schmitt input.

SIN (Serial In - Input), SOUT (Serial Out - Output), SCK (Serial Clock - Output), SACTIVE (Serial Bus Active - Output)

These four lines constitute the synchronous Serial Interface **(SERIAL)** interface of the HIP7010. See the **Serial Interface (SERIAL) System** for details. SIN, SOUT, and SCK provide the three principal connections to the Host controller. SIN is a CMOS input. SOUT and SCK are three-state outputs which are only activated during serial transfers. The SIN, SOUT, and SCK pins contain integrated pull-down load devices which provide termination on the bus whenever it is in a high impedance state. The SACTIVE pin is a CMOS output, which pulls low when the HIP7010 is communicating on the serial bus. See **Serial Interface (SERIAL) System** and **Applications Information** for more details.

RDY (Byte Ready - Input)

The Byte Ready (RDY) line is a "handshaking" input from the Host. Each rising edge on the RDY pin signifies that the Host has loaded a byte into its SERIAL transmit register and the HIP7010 can retrieve it (by generating clocks on SCK) when the HIP7010 is ready for the data. See **Serial Interface (SERIAL) System** and **Applications Information** for more details.

The RDY pin contains an integrated pull-down load device which will hold the pin low if it is left unconnected.

IDLE (Idle/Service Request - Output)

The IDLE output pin indicates that the J1850 Bus has been in a passive state for at least 300µs and is now idle. If the bus has been passive for a minimum of 239µs and another node initiates a new message, IDLE will pulse low for 1µs.

In its role as a Service Request pin, a reset forces IDLE high. Following the reset, IDLE remains high for 17 CLK cycles and is then driven low. IDLE will remain low until 40 CLK cycles +1.5µs after completion of the first Status/Control byte transfer. The IDLE pin will then resume its normal role, remaining high until a 300µs lull (or 239µs plus a passive to active transition) has been detected on the J1850 bus. This provides a handshake mechanism to ensure the Host will reinitialize the HIP7010 each time the HIP7010 is reset via POR, RESET, or Slow Clock Detect.

If IDLE is low when an echo failure causes the ERR bit to be set in the Status byte, the IDLE pin will pulse high for 2µs and then return low (see Status/Control Register).

If IDLE is low when the host sets the NXT bit in the control byte, the IDLE pin will pulse high for 2µs and then return low (see Status/Control Register).

In general a Status/Control byte transfer should be performed each time IDLE goes low. See **Effects of Resets and Power-Down** and **Applications Information** for more details.

The IDLE pin is an active low CMOS output. See **Operation of the HIP7010** for more details.

STAT (Request Status/Control - Input)

The Request Status/Control (STAT) input pin is used by the Host microcontroller to initiate an exchange of the Host's control byte and the HIP7010's status byte. A low to high transition on the STAT input signals the HIP7010 that the Host has placed a control word in it's SERIAL output register and is ready to exchange it with the HIP7010's status word. The HIP7010 controls the exchange by generating the 8 SCKs required. See **Serial Interface (SERIAL) System** and **Applications Information** for more details.

The STAT pin contains an integrated pull-down load device which will hold the pin low if it is left unconnected.

RESET (Reset - Input)

The RESET input is a low level active input, which resets the HIP7010. Resetting the HIP7010 forces SACTIVE high, disables the SOUT and SCK pins, forces the VPWOUT output low, drives IDLE high, and returns the internal state machine to its initial state. Following reset, the HIP7010 is inhibited from transmitting or receiving J1850 messages until a Status/Control Register transfer has been completed (see **Effects Of Resets And Power-Down** for more details).

The HIP7010 is also reset during initial power-on, by an internal power-on-reset (POR) circuit.

Loss of a clock on the CLK input will cause a reset as described previously under **CLK**.

If not used, the RESET pin should be tied to V_{DD}.

For enhanced noise immunity, the CLK input is a CMOS Schmitt trigger input. See **Electrical Specifications** for input levels.

TEST (Test Mode - Input)

The TEST input provides a convenient method to test the HIP7010 at the component level. Raising the TEST pin to a high level causes the HIP7010 to enter a special TEST mode. In the TEST mode, a special portion of the state machine is activated which provides access to the Built-in-Test and diagnostic capabilities of the HIP7010 (see **Test Mode** for more details).

The TEST pin contains an integrated pull-down load device which will hold the pin low if it is left unconnected. In many applications the TEST pin will be left unconnected, to allow access via a board level ATE tester.

J1850 VPW Messaging

This section provides an introduction to J1850 multiplexed communications. It is assumed that the user is or will become familiar with the appropriate documents published by the Society of Automotive Engineering (SAE). The following discussion is not comprehensive.

Overview

The **SAE Recommended Practice J1850** (Note 1) (J1850) establishes the requirements for communications on a Class B multiplexed wiring network for automotive applications. The J1850 document details the requirements in a three layer description which separately specifies the characteristics of the *physical layer*, the *data link layer*, and the *application layer*. There are several options within each layer which allows vehicle manufacturers to customize the network while still maintaining a level of universality.

NOTE:

1. **SAE Recommended Practice J1850, Class B Data Communication Network Interface**, September 1, 1993, Society of Automotive Engineers Inc.

The hardware of the Harris HIP7010 provides features which facilitate implementation of the 10.4Kbps Variable Pulse Width Modulated (VPW) physical layer option of J1850. In combination with a bus transceiver, such as the Harris J1850 Bus Transceiver HIP7020, and appropriate software algorithms the HIP7010 circuitry enables the designer to completely implement a 10.4Kbps VPW Class B Communications Network Interface per J1850. Features of such an implementation include:

- Single Wire 10.4Kbps Communications
- Bit-by-Bit Bus Arbitration
- Industry Standard Protocol
- Message Acknowledgment ("In-Frame Response") Capabilities
- Exceptionally Tolerant of Clock Skew, System Noise, and Ground Offsets
- Meets CARB and EPA Diagnostic Requirements
- Supports up to 32 Nodes
- Low Error Rates
- Excellent EMC Levels (when interfaced via Harris J1850 Bus Transceiver HIP7020)

In addition to the standard J1850 features, the HIP7010 hardware provides a high speed mode, (intended for receive only use) which can significantly enhance vehicle maintenance capabilities. The high speed mode provides a 41.6Kbps communications path to any node built with the HIP7010.

Anatomy of a J1850 VPW Message

All messages in a J1850 VPW system are sent along a single wire, shared bus. At any given moment the bus can be in either of two states: *active* (high) or *passive* (low). Multiple nodes are connected to the bus as a "wired-OR" network in which the bus is high if *any* one (or more) node is generating an active output. The bus is only low when *no* nodes are generating active outputs. It follows that, when no communications are taking place the bus will rest in the passive state. A message begins when the bus is first driven to the high state. Each succeeding state transition (i.e. - a change from active to passive or passive to active) transfers one bit of information (*symbol*) until the message is complete and the bus once again rests at the passive state. The interpretation of each symbol in the message is dependent on its duration (and state), hence the descriptor Variable Pulse Width (VPW).

Each message has a beginning and an end, the span of which encompasses the entire *message* or *frame* (refer to Figure 3). A frame consists of an active *start of frame* (SOF) symbol and a passive *end of frame* (EOF) symbol sandwiched around a series of byte sized (8-bit) groups of symbols. The first byte of the frame contents is always a *header* byte, followed by possibly additional header bytes, followed by one or more *data* bytes, followed by an integrity check byte (*CRC* byte), followed by a passive *end of data* (EOD) symbol, followed by possibly one or more *in-frame-response* (IFR) bytes. To keep waiting times low, messages are limited to 12 bytes total (including header, data, check, and IFR bytes). All message bytes are transmitted most significant bit (MSB) first.

VPW Symbol Definitions

Within the J1850 scheme, symbols are defined in terms of both duration and state (passive or active). The duration is measured as the time between successive transitions. There is one transition per symbol and one symbol per transition. The end of one symbol marks the beginning of the next. Since the bus is passive when a message begins and must return to that same state when the message completes, all frames have an even number of transitions and hence an even number of symbols.

There are unique definitions for data bit symbols (all the symbols which occur within the header, data, and check bytes) and protocol symbols (including SOF, EOD, and EOF). The duration of each symbol is expressed in terms of VPW Timing Pulses (TV values). Table 1 summarizes the TV definitions. Each TV is specified in terms of a *nominal* (or ideal) duration and a *minimum* and *maximum* duration. The span between the minimum and maximum limits accommodates system noise sources such as node to node clock skew, ground offsets, clock jitter, and electromechanical noise. There are no dead zones between the maximum of one TV and the minimum of the next.

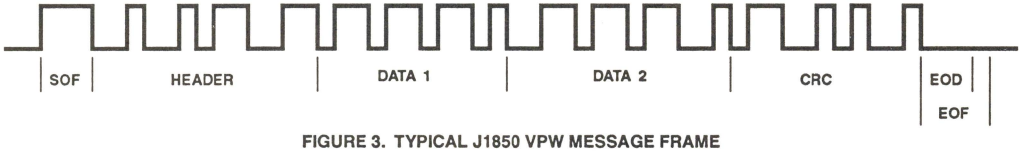


FIGURE 3. TYPICAL J1850 VPW MESSAGE FRAME

The terms *short* and *long* are often used to refer to pulses of duration TV1 and TV2 respectively.

TABLE 1. J1850 TV DEFINITIONS

TV ID	DURATION (ALL TIMES IN μs)		
	MINIMUM	NOMINAL	MAXIMUM
Illegal	0	NA	≤34
TV1	>34	64	≤96
TV2	>96	128	≤163
TV3	>163	200	≤239
TV4	>239	280	NA
TV5	>239	300	NA
TV6	>280	300	NA

VPW is a non-return-to-zero (NRZ) protocol in which each transition represents a complete bit of information. Accordingly, a *0* data bit will sometimes be transmitted as a passive pulse and sometimes as an active pulse. Similarly, a *1* data bit will sometimes be transmitted as a passive pulse and sometimes as an active pulse. In order to accommodate arbitration (see **Bus Arbitration**) a *long active* pulse represents a 0 data bit and a *short active* pulse represents a 1 data bit. Complementing this fact, a *short passive* pulse represents a 0 and a *long passive* pulse represents a 1. Starting from a transition to the active state, a 0 data bit will maintain the active level longer than a 1. Similarly, starting from a transition to the passive state, a 0 data bit will return to the active level quicker than a 1. These facts give rise to the dominance of 0's over 1's on the J1850 bus as depicted in Figure 4. See **Bus Arbitration** for additional details.

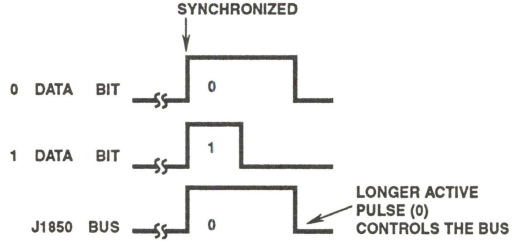


FIGURE 4A. DOMINANCE OF ACTIVE 0 DATA BIT

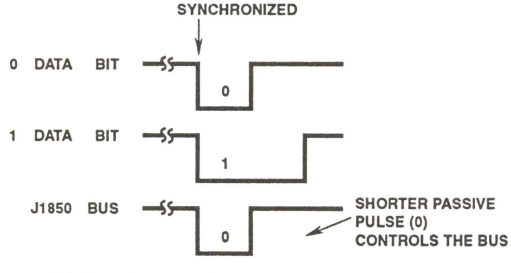


FIGURE 4B. DOMINANCE OF PASSIVE 0 DATA BIT

FIGURE 4.

Table 2 summarizes the complete set of symbol definitions based on duration and state.

TABLE 2. J1850 SYMBOL DEFINITIONS

SYMBOL	DEFINITION
0 Data	Passive TV1 or Active TV2
1 Data	Active TV1 or Passive TV2
SOF (Start of Frame)	Active TV3
EOD (End of Data)	Passive TV3
EOF (End of Frame)	Passive TV4
IFS (Inter-Frame Separation)	Passive TV6
IDLE (Idle Bus)	Passive >TV6 Nominal
NB (Normalization Bit)	ActiveTV1 or Active TV2
BRK (Break)	Active TV5

In Frame Response (IFR)

The distinction between two of the passive symbols, EOD and EOF, is subtle but important (refer to Figure 5). The EOD (TV3) interval signifies that the originator of the message is done broadcasting and any nodes which have been requested to respond (i.e. - to acknowledge receipt of the message) can now do so. The EOD interval begins when the transmitting node has completed sending the eighth bit of the check byte. The transmitter simply releases the bus and allows it to revert to a passive state. In the course of normal messaging, no node can seize the bus until an EOD time has been detected. Once an EOD has elapsed, any nodes which are scheduled to produce an IFR will arbitrate for control of the bus (see **Bus Arbitration**) and respond appropriately. If no responses are forthcoming the bus remains in the passive state until an EOF (TV4) interval has elapsed. After the EOF has been generated, the frame is considered closed and the next communications on the bus will represent a totally new message.

IFRs can consist of multiple bytes from a single respondent, one byte from a single respondent, or one byte from multiple respondents. In all cases the first response byte must be preceded by a *normalization bit (NB)* which serves as a *start of response* symbol and places the bus in an active state so that following the IFR byte(s) the bus will be left in the passive state.

The NB symbol is by definition active, but can be either TV1 or TV2 in duration. The long variety (TV2) signifies the IFR contains a CRC byte. The short variety (TV1) precedes an IFR without CRC.

Message Types

Messages are classified into one of four *Types* according to whether the message has an IFR and what kind of IFR it is. The definitions are:

- Type 0 - No IFR
- Type 1 - One byte IFR from a single respondent (no CRC byte)
- Type 2 - One byte IFRs from multiple respondents (no CRC byte)
- Type 3 - Multiple byte IFR from a single respondent (CRC appended)

Bus Arbitration

The nature of multiplexed communications leads to contention issues when two or more nodes attempt to transmit on the bus simultaneously. Within J1850 VPW systems, messages are assigned varying levels of priority which allows implementation of an arbitration scheme to resolve potential contentions. The specified arbitration is performed on a symbol by symbol basis throughout the duration of every message.

Arbitration begins with the rising edge of the SOF pulse. No node should attempt to issue an SOF until an Idle bus has been detected (i.e. - an *Inter-Frame Separation (IFS)* symbol with a period of TV6 has been received). If multiple nodes are ready to access the bus and are all waiting for an IFS to elapse, invariable skews in timing components will cause one arbitrary node to detect the Idle condition before all others and start transmission first. For this reason, all nodes waiting for an IFS will consider an IFS to have occurred if either:

1. An IFS nominal period has elapsed

   or

2. An EOF minimum period has elapsed *and* a rising edge has been detected

Arbitrating devices will all be synchronized during the SOF. Beginning with the first data bit and continuing to the EOF, every transmitting device is responsible for verifying that the symbol it sent was the symbol which appeared on the bus. Each transition, every transmitting node must decode the symbol, verify the received symbol matches the one sent, and begin timing of the next symbol. Since timing of the next symbol begins with the last transition detected on the bus, all transmitters are re-synchronized each symbol. When the received symbol doesn't match the symbol sent, a conflict (*bit collision*) occurs. Any device detecting a collision will assume it has lost arbitration and immediately relinquish the bus. Typically, after losing arbitration, a device will attempt retransmission of the message when the bus once again becomes idle.

The definition of 1 and 0 data bits (see Table 2 and discussion under **VPW Symbol Definitions**) leads to 0's having priority over 1's in this arbitration scheme. Header bytes are generally assigned such that arbitration is completed before the first data byte is transmitted. Because of the dominance of 0 bits and the MSB first bit order, a header with the hexadecimal value $00 will have highest priority, then $01, $02, $03, etc. An example of two nodes arbitrating for control of the bus is shown in Figure 6.

Arbitration also takes place during the IFR portion of a message, if more than one node is attempting to generate a response. Arbitration begins with the NB symbol, which follows the EOD and precedes the first IFR byte.

For Type 1 and Type 3 messages only, the respondent which successfully arbitrates for control of the bus produces an IFR. All other respondents abort their IFRs.

For Type 2 messages, all respondents which lose arbitration must count symbols and re-attempt transmission at the end of each byte. Each node, which successfully responds, eliminates itself from the subsequent arbitration until all nodes have responded. This arbitration scheme limits each respondent to a single byte during a Type 2 IFR.

Break

To force a message to be aborted before EOF is reached, a break (BRK) symbol can be transmitted by any node. The BRK symbol is an active pulse of duration TV5. Reception of a break causes all nodes to reset to a *ready-to-receive* state and to re-arbitrate for control following an IFS.

HIP7010 Architectural Overview

The HIP7010 consists of three major functional blocks: the Serial Interface System (SERIAL) block; the State Machine (STATE) block; and the Symbol Encoder/Decoder (SENDEC) block. Transfers between the Host and the HIP7010 are controlled by the SERIAL block, while transfers between the J1850 bus and the HIP7010 are handled by the SENDEC

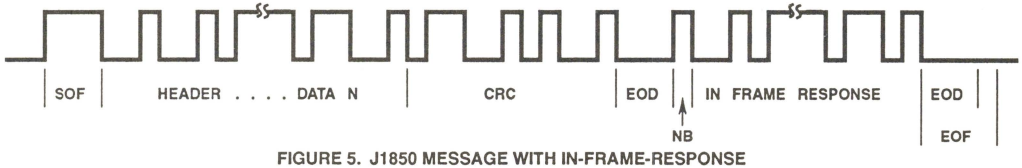


FIGURE 5. J1850 MESSAGE WITH IN-FRAME-RESPONSE

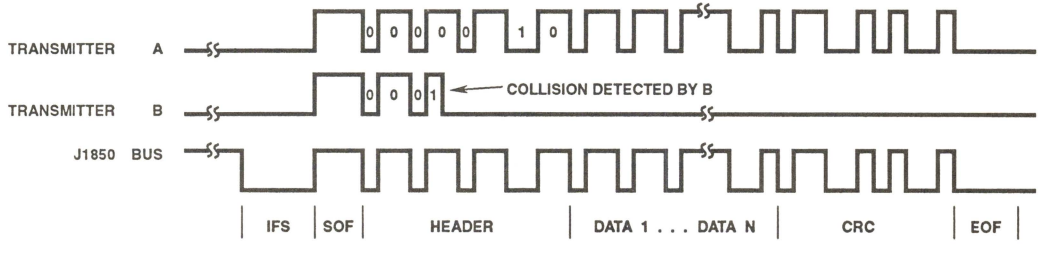


FIGURE 6. TWO NODES ARBITRATING FOR CONTROL OF J1850 BUS

block. The STATE block controls the flow of all data between the SERIAL and SENDEC blocks. The STATE block also controls Host/HIP7010 handshaking, automatic J1850 bus arbitration, break recognition, CRC checking, and many other features. In addition to the three major blocks the HIP7010 includes CRC generator/checker hardware, a Status/Control Register, and a Timing generator.

Timing Generator

The timing generator, as its name suggests, generates all internal timing pulses required for the SERIAL, SENDEC, STATE, and CRC circuits. The CLK input pin is appropriately divided to produce an internal 2MHz clock which results in a 1MHz SERIAL transfer rate and VPW J1850 symbol timing with 1µs accuracy. The CLK pin of the HIP7010 can be driven with a variety of common microcontroller frequencies. Frequency selection is accomplished via three bits in the Status/Control register. See **Status/Control Register** for more details.

The Serial Interface (SERIAL) System

Overview

The SERIAL system handles all interface between the Host microcontroller and the HIP7010. The SERIAL system is designed to interface directly with the Serial Peripheral Interface (SPI) systems of the Harris CDP68HC05 family of microcontrollers. Identical interfaces are found on the 68HC11 and HC16 families. Compatible systems are found on most popular microcontrollers.

Serial data words are simultaneously transmitted and received over the SOUT/SIN lines, synchronized to the SCK clock stream. The word size is fixed at 8-bits. A series of eight clocks is required to transfer one word. With the exception of Status/Control Register transfers (described later), all SERIAL transfers use a single eight bit shift register within the HIP7010. The serial bits are "shifted out" on the SOUT pin, most significant bit (MSB) first, from the shift register. As each bit shifts out one end of the shift register, the data on the SIN input pin is, usually, shifted into the other end of the same shift register. After eight clocks, the original contents of the shift register have been entirely transmitted on the SOUT pin and replaced by the byte received on the SIN pin.

Most Host micros which include a synchronous serial interface, operate their interface in a manner compatible with the HIP7010s implementation. The result of each 8-bit SERIAL transfer is that the contents of the HIP7010s shift register and the Host's shift register have effectively been "swapped".

SERIAL Bus Timing

The SCK output of the HIP7010 is used to synchronize the movement of data both into and out of the device on its SIN and SOUT lines. As stated above, the Host and the HIP7010 are capable of exchanging a byte of information during a sequence of eight clocks generated on the SCK pin. The relationship between the clock signal on SCK and the data on SIN and SOUT is shown in Figure 7.

Approximately 750ns prior to each series of eight clocks, the $\overline{\text{SACTIVE}}$ output of the HIP7010 is driven low. $\overline{\text{SACTIVE}}$ remains low until a minimum of 1200ns after the last clock transition. When interfacing to a CDP68HC05 SPI compatible Host, the $\overline{\text{SACTIVE}}$ output would normally be connected to the $\overline{\text{SS}}$ input of the Host. The trailing edge of the $\overline{\text{SACTIVE}}$ signal can also be used as a flag to Hosts which don't automatically recognize the transfer of a serial byte.

The quiescent state of SCK is low. Once a transfer is initiated, the rising edge of each SCK pulse places the next bit on the SOUT line and the falling edge is used to latch the bit input on SIN.

The Host must adhere to this same timing, by meeting the input setup time requirements of SIN valid before the trailing edge of SCK (see **Electrical Specification** for details) and latching the SOUT data on the same edge. When interfacing the HIP7010 to a CDP68HC05 SPI compatible Host, the SPI interface should be programmed with CPHA = 1 and CPOL = 0.

At all times, other than during an actual SERIAL transfer between the HIP7010 and its Host, the SCK and SOUT pins are held in a high impedance state. This allows other devices connected to the Host via the SERIAL bus to be accessed when the HIP7010 is not transferring data. Utilization of the SERIAL bus by the HIP7010 is less than 5%, leaving significant bandwidth for other transfers. When held in the high impedance state, a pair of integrated pull-down devices on the SCK and SOUT pull the pins to ground, if they are not driven by another source. See **Applications Information** for a detailed discussion of SERIAL bus utilization.

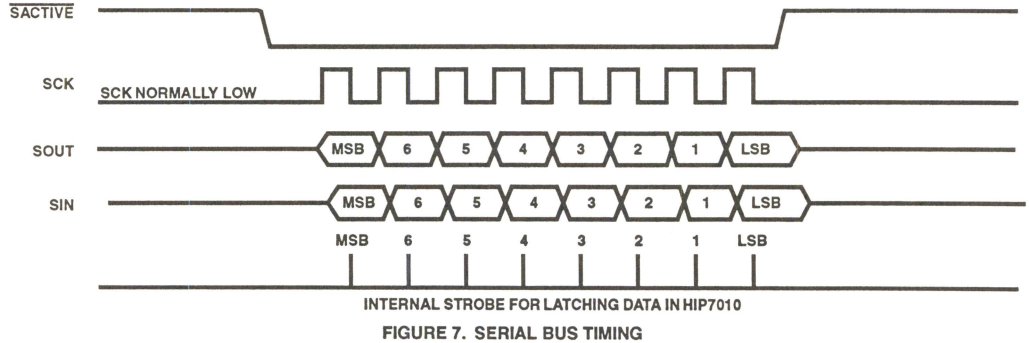


FIGURE 7. SERIAL BUS TIMING

SERIAL Bus Transfers

The HIP7010 is always configured as a SERIAL "master". As a master, the HIP7010 generates the transfer-synchronizing clock on the SCK pin, transmits data on the SOUT pin, and receives data on the SIN pin.

Whenever the HIP7010 receives a complete byte from the J1850 bus via the $\overline{\text{VPWIN}}$ line, it automatically initiates an *unsolicited* SERIAL transfer. The unsolicited transfer transmits the received (or reflected) byte to the Host and, if in the midst of transmitting a message, retrieves the next byte from the Host. While these unsolicited transfers are, strictly speaking, asynchronous to the Host's activities, there are well defined rules which govern the minimum time between unsolicited transfers (i.e. - no two unsolicited transfers can occur in less time than it takes to transfer one J1850 byte (8 x 64 = 512µs). See **Applications Information** for more details.

In addition to the unsolicited transfers which are based on receipt of incoming J1850 messages, the Host can initiate certain transfers in a more synchronous fashion. *Handshaking* between the Host and the HIP7010 is provided by the Byte Ready (RDY) and Request Status (STAT) pins. These two pins are driven by the Host and trigger the HIP7010 to initiate one of the two, unique, *solicited* SERIAL transfers.

The Byte Ready (RDY) line is the first of two handshaking inputs from the Host. Each rising edge on the RDY pin signifies that the Host has loaded a byte into its serial transmit register and the HIP7010 can retrieve it. If the J1850 bus is available (i.e. - IFS has elapsed) the rising edge of RDY is interpreted as signalling the first byte of a new message. The HIP7010 immediately performs a solicited SERIAL transfer to load the first byte. Prior to performing the transfer, the HIP7010 drives the J1850 bus high to initiate an SOF symbol. The SOF is then followed by the eight symbols which represent the transferred byte. If a J1850 message is already in progress, the rising edge of RDY is interpreted as signalling that the next byte of the message or of an IFR is ready to be transferred from the Host. The HIP7010 will initiate the transfer, as an unsolicited transfer, when conditions on the J1850 bus warrant the transfer (i.e. - when the previously retrieved byte has been completely transmitted on the J1850 bus or after EOD for an IFR).

While the rising edge of RDY is used to notify the HIP7010 that the Host is ready to supply the next byte, the level of RDY following the actual serial transfer provides additional information. Figure 1 depicts the use of RDY. By driving the RDY line high and returning it low before the transfer has been completed, the HIP7010 will detect a low. This is referred to as a *short RDY*. If the RDY line is brought high and held high until the transfer is complete, a high level is detected by the HIP7010. This is referred to as a long *RDY*.

A short RDY signals a normal transfer, but a long RDY has special significance. A long RDY indicates that the byte currently sitting within the Host is the last byte of a message or of an IFR. When transmitting the body of a message or a Type 3 IFR the HIP7010 will automatically append the CRC after the byte for which the long RDY was used. When responding with a Type 1 or Type 2 IFR the response is a single byte, and as such it is always the last byte. For sake of consistency the HIP7010 requires a long RDY for Type 1 and Type 2 IFRs. See **Status/Control Register** and **Application Information** for more details.

The other handshaking input is the Request Status/Control (STAT) input pin. STAT is used by the Host microcontroller to initiate an exchange of the Host's *control byte* and the HIP7010's *status byte*. A low to high transition on the STAT input signals the HIP7010 that the Host has placed a control word in it's serial output register and is ready to exchange it with the HIP7010's status word. The HIP7010 will generate the eight SCKs for the solicited transfer as soon as feasible. To avoid confusion with the transfer of a received J1850 byte, STAT should generally be pulsed shortly after receiving each data byte from the HIP7010. This technique is safe, because once a J1850 message byte has been received from or sent to the HIP7010, another unsolicited transfer is guaranteed not to happen for at least 500µs. A Control/Status byte transfer should also be performed in response to each high to low transition on the $\overline{\text{IDLE}}$ line. See **Application Information** for more details.

Status/Control Register

The Status/Control Register is actually a pair of registers: the Status Register and the Control Register. When the Host initiates a Status/Control Register transfer by raising the STAT input, the HIP7010 sends the contents of the Status Register to the Host and simultaneously loads the Control register with the byte received from the Host.

Status Register

The Status Register contains eight, read-only, status bits.

7	6	5	4	3	2	1	0
EOD	MACK	0	FTU	4X	CRC	ERR	BRK

B7, EOD — When an EOD symbol has been received on $\overline{\text{VPWIN}}$ and an IFR byte is received from the J1850 bus, the End-of-Data flag (EOD) is set, during the unsolicited transfer of the byte from the HIP7010 to the Host. EOD remains set, until the unsolicited transfer of the first byte of the next frame.

EOD can be used to distinguish the IFR portion of a frame from the message portion.

EOD is cleared by reset.

B6, MACK — If MACK (Multi-byte ACKnowledge) is high, either the MACK control bit has been set during a previous Status/Control Register transfer or a long normalization bit has been received following an EOD. When both MACK is set and the EOD flag (see B7, EOD) is set, the most recent data byte transferred is part of a Type 3 IFR. Mask remains set until the unsolicited transfer of the first byte of the next frame.

MACK is cleared by reset.

B5, 0 — Bit 5 of the Status byte is not used and will **always** read as a 0.

B4, FTU — When First Time Up (FTU) is high, it indicates that a reset has occurred since the last Status/Control Register transfer. FTU is high during the first Status/Control Register transfer after a reset and low thereafter.

FTU can be used to recognize that a Slow Clock Detect reset has occurred or to insure that a Status/Control Register transfer has been successfully completed since the last reset.

B3, 4X — The 4X status flag indicates that the 4X mode bit has been set in the Control Register. This bit reflects the contents of the Control Register not the current mode of the HIP7010's SENDEC. The SENDEC only changes modes synchronously with an edge detected on the $\overline{\text{VPWIN}}$ pin.

4X is cleared by reset.

B2, CRC — The CRC Error flag (CRC) is set when a CRC error has been detected in the current frame.

CRC is cleared by reset and at the conclusion of the Status/Control Register transfer.

B1, ERR — The Error flag (ERR) is set when an illegal symbol or other, non-CRC error has been detected on the $\overline{\text{VPWIN}}$ pin. Following are some of the many errors which will cause ERR to be set: 1. An illegal symbol, (i.e. - a symbol other than a TV1, TV2, or Break in the middle of a data byte); 2. Receipt of a truncated byte (i.e. - less than 8 symbols); 3. The Host attempting to initiate a message more than 96µs after the $\overline{\text{IDLE}}$ line goes high; 4. An improperly framed message (i.e. - SOF not equal to TV3, wrong EOD, EOF, or NB widths); 5. Failure by the Host to use the long form of RDY to indicate the last byte of a message; 6. An attempt by the Host to transmit a single byte (Type 1 or Type 2) IFR by setting ACK but without using the long form of RDY for the byte transfer; 7. Setting the Host asserting STAT during a data byte transfer; 8. A transition has occurred on the VPWOUT pin and the reflected transition has not been detected on $\overline{\text{VPWIN}}$ (echo fail).

ERR is cleared by a reset and at the conclusion of the Status/Control Register transfer.

B0, BRK — The break flag (BRK) is set on the first rising edge of $\overline{\text{VPWIN}}$ after a BRK symbol has been detected on the J1850 bus. If the Host was transmitting or has a message to transmit, it should re-arbitrate for the bus following an IFS ($\overline{\text{IDLE}}$ goes low).

BRK automatically clears the 4X mode of the SENDEC and resets the 4X bit in the Status byte.

BRK is cleared by a reset or at the conclusion of the Status/Control Register transfer.

Control Register

The Control Register contains eight, write-only, control bits. The PD, NXT, MACK, and ACK bits can only be set high they are cleared by hardware under specific conditions. The other four bits can be both set and reset by the Host. All bits in the Control Register are cleared by reset.

7	6	5	4	3	2	1	0
ACK	MACK	NXT	PD	4X	DS2	DS1	DS0

B7, ACK — Setting the Acknowledgment (ACK) bit signals the HIP7010 that, following the EOD, an IFR response is to be sent. Once set, the ACK bit cannot be cleared by the Host. ACK is cleared upon successful transmission of the IFR or at the next Idle.

The ACK bit can be set anytime prior to the final byte of a message. The first IFR byte must be loaded into the Host's serial output register, and the RDY line set **after** the HIP7010 transfers the next-to-last byte to the Host, and **before** the HIP7010 transfers the last byte (CRC) of the J1850 message to the Host. When the CRC byte is sent to the Host from the HIP7010, the IFR byte will be simultaneously loaded into the HIP7010.

To send a single byte (Type 1 or Type 2) IFR the Host must leave MACK (B6 of the Control Register) low and use the long RDY line format.

When sending a single byte (Type 1 or Type 2) IFR, the possibility of losing arbitration exists. In the case of a Type 1 IFR no further action should be taken. The standard protocol for handling loss of arbitration during a Type 2 IFR is to reattempt the transmission until successful. To ensure proper transmission of the IFR the Host must repeatedly load it's serial output register with the desired IFR byte, and set RDY (using the short format), until the IFR has been properly received back. There is no danger of inadvertently sending the IFR byte twice. The HIP7010 monitors the arbitration results and will transmit the IFR byte only once. The ACK bit is automatically cleared upon the first successful transmission thus preventing a second transmission. The Host controls when the ACK bit is set. During normal operation the Host must only set ACK once per IFR.

To send a Type 3 IFR the Host must set MACK high and use the short format of the RDY for all bytes except the last, when the long format is used. A CRC will automatically be appended to the last byte of a Type 3 IFR. A Type 3 IFR, consisting of a single byte plus CRC, can be created by setting MACK high and using the long RDY line format for loading the single data byte.

When sending a Type 3 IFR, the possibility of losing arbitration during the IFR also exists. In the case of Type 3 IFRs, once arbitration has been lost the Host no longer needs to continue transmitting bytes. As in the case of Type 2 IFRs, the Host cannot know arbitration has been lost until after the next byte to transmit has been loaded. Again, there is no danger of sending extra bytes because the HIP7010 automatically suspends transmissions once arbitration is lost.

B6, MACK The Multi-byte Acknowledge (MACK) bit, in conjunction with the ACK bit, signals the HIP7010 that, following the EOD, a Type 3 IFR with CRC response is to be sent. Once set, the MACK bit cannot be cleared by the Host. MACK is cleared upon detection of an Idle following the transmission of the IFR. Setting MACK without also setting ACK will result in no IFR being transmitted.

The MACK bit can be set anytime prior to the final byte of a message. The first IFR byte must be loaded into the Host's serial output register, and the RDY line set **after** the HIP7010 transfers the next-to-last byte to the Host, and **before** the HIP7010 transfers the last byte (CRC) of the J1850 message to the Host. When the CRC byte is sent to the Host from the HIP7010, the first IFR byte will be simultaneously loaded into the HIP7010. To send a Type 3 IFR the Host uses the short format of the RDY for all bytes except the last, when the long format is used.

B5, NXT If the Wait for Next Idle (NXT) bit is asserted high during a Status/Control Register transfer, the HIP7010 State Machine is re-initialized to a "wait for Idle" state. The VPWOUT pin is driven low and the $\overline{\text{IDLE}}$ pin is reset high. Activity on the $\overline{\text{VPWIN}}$ pin is ignored until a valid Idle is detected. When NXT is asserted the $\overline{\text{IDLE}}$ pin will go high for a minimum of 6µs. If the bus is Idle at the end of the 6µs period, $\overline{\text{IDLE}}$ will be driven low and the HIP7010 will be ready to transmit or receive a J1850 message. If the bus is not Idle, current activity on the $\overline{\text{VPWIN}}$ pin is ignored until a new Idle is detected.

The NXT bit enables the Host to ignore the balance of the current message. Unsolicited transfers from the HIP7010 are guaranteed not to occur until the next Idle occurs. Transfers resume following the first byte of the next message.

B4, PD The Power-Down (PD) bit is used to halt internal clocks to the HIP7010 to minimize power. A low level on the $\overline{\text{VPWIN}}$, a low to high edge on the STAT pin, or a high level on the RDY pin will clear the PD bit and normal HIP7010 functions will resume.

PD can only be set if the $\overline{\text{IDLE}}$ pin is low or during the first Status/Control Register transfer following a reset. The CLK input is internally gated off at the end of the Status/Control Register transfer.

There are two situations which can cause the PD bit to be cleared prematurely: 1. The RDY input is high during the Status/Control Register transfer (since this is under control of the Host it should be avoided); 2. A noise pulse of less than 8µs duration occurs on the $\overline{\text{VPWIN}}$ line.

If either of these situations occur, the PD will be cleared, the HIP7010 will awake and look for a valid edge on $\overline{\text{VPWIN}}$, RDY, or STAT. If no valid edge has occurred the HIP7010 will recycle to the top of the State Machine, pulsing $\overline{\text{IDLE}}$ high for a minimum of 2µs. It is the responsibility of the Host to monitor the $\overline{\text{IDLE}}$ pin after setting PD to ensure that the POWER-DOWN mode has been successfully entered.

See **Effects of Resets and Power-Down** for a detailed discussion of the Power-Down mode.

B3, 4X Setting the High Speed Mode (4X) bit causes the HIP7010's SENDEC to decode symbols received on the J1850 bus at 0.25X the normal durations. The 4X mode is designed to allowed receipt of messages at 4X the normal J1850 rate. It is intended for manufacturing and diagnostic use, not normal "down the road" vehicle communications. Transmission is inhibited while the 4X bit is set.

The 4X bit can only be written to when the $\overline{\text{IDLE}}$ pin is low or during the first Status/Control Register transfer following a reset. The SENDEC begins operating at the 4X rate upon receipt of the next edge. The system must provide sufficient time for all nodes to detect the Idle, interpret the "shift to high speed" message, and change their mode bits before issuing a high speed SOF.

4X is cleared by receipt of a Break symbol on the J1850 bus and it can also be cleared by performing a Status/Control Register transfer with the 4X bit low. When cleared via a Status/Control Register transfer, $\overline{\text{IDLE}}$ must be low. The SENDEC reverts to operating at the normal rate upon receipt of the next edge.

B2, DS2
B1, DS1
B0, DS1 The three Divide Select bits (DS2-DS0) are used to match the internal clock divider with the input frequency on the CLK input to produce the required 2MHz internal time base. Table 3 shows the clock divide values and nominal input frequency for the eight combinations of DS2-DS0.

During a HIP7010 reset caused by a POR, a Slow Clock Detect, or a low on the $\overline{\text{RESET}}$ line, the Clock Divider is inhibited and a fixed divide-by sixteen clock divider is activated. This is greater than any selectable divide-by and guarantees proper operation of the SERIAL interface for all valid operating frequencies (although the transfer rate will be below 1MHz). The CLK divide-by remains at sixteen and operation of the HIP7010 is suspended until the Host performs a Status/Control Register transfer to set the proper divide value. The State Machine and SENDEC are held in a reset state (passive) until the first Status/Control Register transfer has been completed. This insures proper setting of the divide selects prior to generation or receipt of any symbols.

TABLE 3. DS2-DS0 CLOCK DIVIDER SELECTIONS

DS2	DS1	DS0	CLK INPUT FREQ. (MHZ)	INTERNAL HIP7010 CLK DIVIDE-BY
0	0	0	24 (Note 1)	12
0	0	1	12 (Note 1)	6
0	1	0	20	10
0	1	1	10	5
1	0	0	16 (Note 1)	8
1	0	1	8	4
1	1	0	4	2
1	1	1	2	1

NOTE:

1. Objective Specification

Once DS2-DS0 have been set following a reset, they must not be altered. Each Status/Control Register transfer must properly reassert the same DS2-DS0 values to maintain proper clocking. Selecting a DS2-DS0 combination which is too low for the given CLK frequency can result in loss of SERIAL communications, due to excessive clocking rates. In such instances the only recovery mechanism is to force a HIP7010 reset by pulling the $\overline{\text{RESET}}$ input low, interrupting the CLK input, or performing a power-on reset. A well behaved Host will avoid changes to DS2-DS0. System fault tolerance can be maximized by using the lowest possible frequency at the CLK input.

Power-down does **not** reset DS2-DS0, allowing rapid "wake-up" from the Power-down state.

Symbol Encoder/Decoder (SENDEC) Operation

The Symbol Encoder/Decoder (SENDEC) hardware integrated in the HIP7010 handles generation and reception of J1850 messages on a symbol by symbol basis. Symbols are output from the SENDEC, as a digital signal, on the VPWOUT pin and input, as a digital signal, on the $\overline{\text{VPWIN}}$ pin. These two lines must be connected through a bus transceiver (such as the Harris J1850 Bus Transceiver HIP7020) to the single wire J1850 bus. The transceiver is responsible for generating and receiving waveforms consistent with the physical layer specifications of J1850. In addition, the transceiver is responsible for providing isolation from bus transients.

Every symbol sent out on the VPWOUT is, in effect, inverted and *reflected* back on the $\overline{\text{VPWIN}}$ pin after some finite delay through the transceiver. In actuality. Only active symbols are guaranteed to be reflected unchanged. If the transmitted symbol is passive and another node is simultaneously sending an active symbol, the active symbol will dominate and pull the bus to a high level. The SENDEC circuitry includes a 3-bit digital filter which effectively filters out noise pulses less than 8µs in duration.

The STATE logic transfers data bits between the SERIAL system and the SENDEC and handles addition of required frame elements such as the SOF symbol and the CRC byte. When transmitting bytes, bits are taken from the SERIAL shift register and translated into the required symbols, bit by bit. **Timing of each symbol is calculated from the last transition on the $\overline{\text{VPWIN}}$ line** which keeps all nodes on the J1850 bus "in synch" during arbitration periods.

Decoding of received symbols is automatically performed by the SENDEC. The decoded symbol is translated to a 0 or 1 value and transferred by the STATE logic into the SERIAL shift register. As each symbol is decoded it is shifted into the SERIAL shift register and, if transmitting, the next bit to transmit on the J1850 bus is shifted out. Once an entire byte has been loaded into the SERIAL shift register the STATE logic automatically generates an unsolicited transfer of the byte to the Host.

Whenever the SENDEC is transmitting, it is simultaneously monitoring the "reflected" symbol on the $\overline{\text{VPWIN}}$ line. At each transition the reflected symbol is read and compared to the sent one. If the reflected symbol doesn't match the symbol sent, a collision has occurred and the HIP7010 automatically disables transmissions until the next Idle/IFR period. If there was no collision, the HIP7010 continues transmitting until the entire byte has been sent. Once the byte has been sent, a full byte will also have been reflected and received by the HIP7010. As discussed above, the HIP7010 initiates a transfer of the received byte to the Host, which allows the Host the opportunity to compare the sent and reflected bytes, and to transfer the next byte of the message.

In addition to features already discussed, the SENDEC includes, noise detection, Idle bus detection, a wake-up facility, "no echo" detection, and a high speed receive mode. Symbol timing is based on the main CLK input. The programmable prescaler, controlled by the DS0-DS2 bits in the Control Register, allows proper SENDEC operation with a variety of CLK input frequencies (see **DS2-DS0** under **Status/Control Register** for prescaler details). The high speed mode is a J1850 extension which allows production and/or maintenance equipment to transmit messages at 4X the normal 10.4Kbps rate (see **4X** under **Status/Control Register** for prescaler details).

Software algorithms can be implemented in the Host to provide message buffering and filtering and other needed features to create a complete J1850 VPW node. See the **Applications Information** section for typical algorithms.

The State Machine Logic (STATE)

The State Machine Logic (STATE) of the HIP7010, is a sequential state machine implementation of the J1850 VPW data link layer. STATE controls data flows within the HIP7010 and between the Host and the J1850 bus.

When receiving messages, STATE monitors the input from the SENDEC, building byte sized chunks to send to the Host. As each byte is assembled, STATE transfers the result to the Host via the Serial interface, as an unsolicited transfer. Upon receipt of a complete message (recognized by EOD), STATE verifies both the CRC and bit counts and sets appropriate Status Register flags.

When transmitting messages from the Host to the J1850 bus, STATE waits for the first RDY input transition, after which it retrieves the first byte from the Host and initiates the message with an SOF. Each bit of the Host's message byte is transferred to the J1850 bus via the SENDEC. When the transfer of a byte is complete, STATE checks for a new RDY (if there is one), retrieves the associated byte, and again transfers the byte via the SENDEC to the J1850 bus. After retrieving each byte from the Host, STATE checks to see if the long RDY format was used, which indicates this is the end of the Host's message. If the message is complete, STATE transfers the final byte to the J1850 Bus and then, automatically, sends the computed CRC to the J1850 bus.

Throughout the transmission of a message from the Host to the J1850 bus, STATE monitors the symbols reflected back via the SENDEC and handles all bus conditions such as loss of arbitration, illegal bits, Break, bad CRC, and missing bits. STATE also catches Host errors including failure to set the RDY line in time for the next byte transfer, attempting to initiate a new message more than 96µs after $\overline{\text{IDLE}}$ has gone away, and inappropriate use of the STAT line (i.e. - requesting a Status/Control Register transfer during an unsolicited transfer of the reflected data).

The Control Register bits influence STATE. If ACK is set, STATE handles sequencing of the requested IFR. The flow consists of waiting for an EOD, sending the appropriate Normalization Bit (Type 1/2 vs Type 3 IFR), transferring the IFR byte(s) from the Host to the J1850 bus, handling arbitration, and finally adding the CRC to Type 3 IFRs. As with normal transmissions, STATE contains error handling to react appropriately to all J1850 bus conditions.

Detection of an Idle on the bus causes STATE to set the $\overline{\text{IDLE}}$ pin. STATE clears the $\overline{\text{IDLE}}$ pin upon receipt of a transition on the $\overline{\text{VPWIN}}$ line or when the Host initiates a new message.

Detection of a Break on the J1850 bus causes an interrupt input to STATE which causes the HIP7010 to cease any current transmission and enter a *wait for $\overline{\text{IDLE}}$* mode.

Effects of Resets and Power-Down

Resets

A Power-On reset, a Slow Clock Detect reset, and a low on the $\overline{\text{RESET}}$ pin all have an identical effect on the operation of the HIP7010. All resets are asynchronous and *immediately* do the following:

- VPWOUT is forced low.
- The HIP7010 is set to *RESTART mode.*
- The internal divide-by is set to sixteen and held at that value until the RESTART mode ends.
- $\overline{\text{SACTIVE}}$ is forced high and SCK and SOUT are set to a high impedance state.
- The ACK, MACK, NXT, PD, and 4X bits are cleared in the Control Register.
- All Status Register bits are cleared (except bit 4, FTU, which is set to a 1).
- $\overline{\text{IDLE}}$ is forced high and held high for 17 CLKs after the source of the reset is removed. After 17 CLKs, $\overline{\text{IDLE}}$ is forced low. $\overline{\text{IDLE}}$ Remains low until 40 CLKs +1.5µs after the first Status/Control Register transfer.
- The SENDEC is reset, holding the symbol timer at a count of 0 and clearing the 3-bit $\overline{\text{VPWIN}}$ filter to all 0's, until the RESTART mode ends.
- STATE is held in a *reset loop* until the RESTART mode ends. While STATE is in the reset loop, transitions on the RDY pin are ignored.

The RESTART mode is entered by any reset and ends when the first Status/Control Register transfer has been completed. Upon exiting the RESTART mode the HIP7010 enters its normal *RUN mode.* This is reflected in the clearing of the FTU bit of the Status Register.

When the RESTART mode ends and the RUN mode begins, the internal divide-by is set to the value programmed via DS2-DS0 in the Control Register. The $\overline{\text{IDLE}}$ pin is driven high after 40 CLKs, the SENDECs counter and $\overline{\text{VPWIN}}$ filter begin operating, and STATE begins monitoring the outputs of SENDEC looking for an Idle.

The HIP7010 remains in RUN mode until another reset occurs or the POWER-DOWN mode is entered.

Power-Down

The *POWER-DOWN mode* of the HIP7010 is entered by setting the PD bit in the Control Register (see **Control Register** for more information). Setting the PD bit can only be done when the HIP7010 is driving the $\overline{\text{IDLE}}$ pin low. Once set, the PD forces the HIP7010 to the POWER-DOWN mode 2µs after the completion of the Status/Control Register transfer. While in the POWER-DOWN mode the CLK input is internally gated off, minimizing power dissipation. The Slow Clock Detect is inhibited while in the POWER-DOWN mode.

A return to the RUN mode from the POWER-DOWN mode is normally caused by a low level on $\overline{\text{VPWIN}}$. During POWER-DOWN the input signal is not filtered via the 7µs digital filter (no clocks are available to drive the digital filter). Without filtering in place it is possible for a noise spike, less than 8µs wide, to *wake-up* the HIP7010. In such a case the HIP7010 returns to RUN mode, but the spike is rejected by the now running, digital filter and the bus continues in the Idle state. To notify the Host when such spurious wake-ups occur, STATE monitors the output of the digital filter and if, within 12µs after the wake-up, the digital filter doesn't indicate $\overline{\text{VPWIN}}$ is low, STATE pulses $\overline{\text{IDLE}}$ high for 2µs and then drives it low again. The HIP7010 is now in the RUN mode. It is the responsibility of the Host to recognize the pulse on the $\overline{\text{IDLE}}$ pin and set PD in the Control Register to reenter the POWER-DOWN mode. In systems where the Host directly monitors the $\overline{\text{VPWIN}}$ pin during POWER-DOWN, monitoring the $\overline{\text{IDLE}}$ pin may not be necessary.

One of the mechanisms to exit POWER-DOWN is to provide a high level on the RDY pin. Since this is a level sensitive event the HOST must ensure that RDY is not already high when the PD bit is set in the Control Register. A well behaved Host will control this properly. However, in the event RDY is high when PD is set, a 12µs timeout will occur similar to that described for waking-up with a noise pulse on $\overline{\text{VPWIN}}$. After the timeout, IDLE will pulse high for 2µs then low again. The Host should react to this pulse appropriately.

Test Mode

Overview

The *TEST mode* is entered by raising the TEST input pin on the HIP7010. Depending on the current STATE contents, the TEST mode may or may not be entered immediately. To insure direct entry into TEST mode, the TEST pin should be driven high before or immediately following a reset (i.e. - before the first Status/Control Register transfer). TEST mode can also be quickly entered by raising the TEST pin and setting the NXT bit in the Control Register.

The TEST mode allows the Host (or factory Automated Test Equipment, ATE) to run one of several *test blocks*. Once TEST mode has been entered a specific test block can be selected by using the RDY and STAT lines and setting the Control Register contents appropriately.

While in Test mode, the $\overline{\text{VPWIN}}$ pin is internally connected to the VPWOUT (with proper polarity). This provides a means of isolating faults.

Test Block 1

Upon entering TEST mode, the HIP7010 is set to run Test Block 1 (TB1). TB1 provides a means to test the SERIAL block of the HIP7010. It also tests proper functionality of the $\overline{\text{IDLE}}$ pin. TB1 is equally useful for in-system or component level testing.

Using the short form of the RDY pulse, the Host requests the HIP7010 to swap the contents of the SERIAL block's shift register with the serial register of the HOST. The Host can continue requesting serial transfers indefinitely while in TB1.

Following a reset the contents of the SERIAL shift register will be $00. Each time a swap is performed the JLBIC will *echo back* to the HOST the byte which the HOST provided during the previous transfer. Following each transfer the $\overline{\text{IDLE}}$ pin is pulsed low for 1µs.

Test Block 2

Test Block 2 (TB2) is entered from TB1 by using the long form of RDY. A final TB1 transfer will be completed and then the HIP7010 will enter TB2.

Additional Test Blocks

Additional Test Blocks are currently being defined and descriptions will be included in the next release of this document.

Applications Information

Typical Flowcharts for HIP7010 Based J1850 Messaging

The previous discussions have detailed the operating details of the HIP7010 features. The techniques for utilizing the features to send and receive J1850 messages was presented in a somewhat fractured manner. The following descriptions are intended to provide a more unified look at the operations and to serve as a template for use of the HIP7010 in implementing standard J1850 protocols.

This section will be included in the next release of this document. Harris TechBriefs pertaining to the HIP7010 are available from Harris Applications Engineers.

HARRIS SEMICONDUCTOR

HIP7020

ADVANCE INFORMATION

April 1994

J1850 Bus Transceiver I/O for Multiplex Wiring

Features

- J1850 Bus Transceiver I/O for MX Wiring
- 5V CMOS/TTL Logic Interface
- Current Controlled Transmitter Driver
- Controlled Rise/Fall Time of Bus Drive for Both Voltage and Current
- Filtered BUS Input Receiver
- Ground Fault Tolerant for Bus Isolation
- Protection for Reverse Battery, Load Dump and Latch-up
- ±9kV ESD Protection -BUS OUT and BATTERY Pins
- -40°C to +125°C Operating Range
- Loop-Back Fault Detection Mode
- 4x (41.6kHz) Receive Speed

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP7020AB	-40°C to +125°C	8 Lead Plastic SOIC (N)
HIP7020AP	-40°C to +125°C	8 Lead Plastic DIP

Description

The HIP7020 IC is an Integrated I/O Bus Transceiver designed for the SAE Standard **J1850 Class B Data Communication Network Interface**. The Bus transmits and receives data on a single wire using a 10.4 kHz VPWM (Variable Pulse Width Modulated) signal. The HIP7020 is intended as an I/O buffer interfacing to 5V CMOS logic and is designed to operate directly from the 12V battery line of an automobile. The normal Bus voltage swing capability is from 0V to 7.75V at currents greater than 30mA.

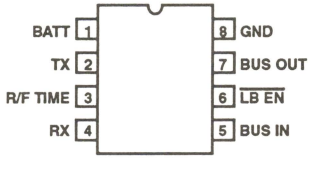
As shown in the block diagram, the Transmitter TX Input and the RX Output of the Bus Transceiver Circuit interface to the control logic. The TX input signal is wave shaped for rise time, fall time and amplitude before it is converted from voltage to current. The Waveshaper with an external programming resistor, R_S controls the rise and fall time of the BUSOUT output signal. The current source drive to the Bus is voltage controlled by the Wave Shaped Voltage Reference to a maximum limit as specified for the J1850 Bus and includes short-circuit current limiting.

The HIP7020 Receiver is connected to the J1850 Bus through an external resistor, R_F and has a trip point at one-half of the Bus signal voltage which is nominally 3.875V. The Receiver input is filtered to remove high frequency Bus noise by the external resistor and an internal capacitor. The bus signal is output at the Receiver RX Output. The RX interface to the control logic incorporates blocking circuitry to prevent power-up of the logic circuits when the battery power is off.

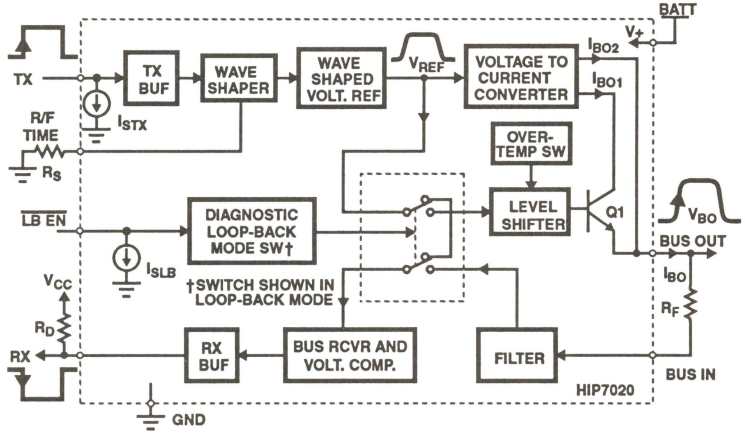
The HIP7020 has a Loop-Back Enable Mode Switch to return diagnostic information for the Bus Transceiver node. For an active low or an open $\overline{\text{LB EN}}$ input, the Transmit/Receive signals are internally "Looped-Back" to provide a TX to RX return signal path independent of signals on the Bus. A return path validation indicates proper action of the Bus Transceiver apart from the J1850 Bus.

Pinout

HIP7020 (PDIP, SOIC)
TOP VIEW



Block Diagram



9 MULTIPLEX COMM. CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3642.1**

Absolute Maximum Ratings

Supply Voltage, V_{BATT} ..... $\pm 24V_{DC}$
J1850 BUS Input Voltage, V_{BUSIN} ..... $\pm 20V$
J1850 BUS Load Current, V_{BUSOUT} ..... Self-Limiting
TX Logic Input Voltage ..... GND-0.3V to 7V
RX Logic Output Current 5mA
Load Dump (Note 1) 40V
BUS Transient Susceptibility ..... (Note 2)
ESD: BUS OUT, BATTERY Pins, (Air Gap, Note 3) ..... $\pm 9KV$
BUS OUT, BATTERY Pins, (Direct, Note 3) ..... $\pm 4.5KV$
All Other Pins (Direct, Note 3) ..... $\pm 2KV$

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package, ... 150°C/W
Plastic SOIC Package, ... 165°C/W
Maximum Package Power Dissipation, P_D (SOIC)
At +85°C 395mW
Above +85°C, derate at ..... 6.1mW/°C
Maximum Package Power Dissipation, P_D (PDIP)
At +85°C 433mW
Above +85°C, derate at ..... 6.67mW/°C
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +125°C; 9.5V ≤ V_{BATT} ≤ 16V; Unless Otherwise Specified; Refer to Block Diagram and Figure 1, Figure 2, Figure 3 and Figure 4 for Waveforms and Test Circuit.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Idle Supply Current	I_{BATT}	No Bus Signal; V_{BATT} = 12.6V; V_{TX} Low		100	-	200	µA
Operating Voltage Range	V_{BATT}	(Note 4)		6	-	24	V
Supply Current, BUS OUT Short to GND	$I_{BATT(SG)}$	BUS OUT Short to GND, V_{TX} High		40	-	50	mA
Supply Current, BUS OUT Short to BATT	$I_{BATT(SB)}$	BUS OUT to V_{BATT}; (No I_{BO} Current)	V_{TX} High	2	-	5	mA
			V_{TX} Low	100	-	200	µA
Thermal Shutdown Temperature	T_{SD}	(Note 5)		150	-	170	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	(Note 5)		10	15	20	°C
Noise Isolation; BATTERY and GND to BUS OUT	N_{ISO}	Figure 3, Test Circuit		60	-	-	dB
TX CMOS/TTL INPUT WITH/PULL DOWN							
Input Bias Current, TX	I_{TX}	V_{TX} = 7V; (Note 6)		10	-	30	µA
Input Low Voltage	V_{IL}			-	-	0.8	V
Input High Voltage	V_{IH}			2.0	-	-	V
BUS OUT							
BUS OUT High Voltage	V_{BOH}	Bus Load, R_{BS} = 240Ω to 2500Ω; V_{TX} High		7.5	7.75	8	V
BUS OUT Low Voltage	V_{BOL}	Bus Load, R_{BS} = 10KΩ; V_{TX} Low		-	-	0.1	V
BUS OUT Voltage, Low BATTERY	$V_{BOH(PSL)}$	6V ≤ V_{BATT} ≤ 9.5V; V_{TX} High		(V_{BATT} -1.5V)	-	8	V
Source Current, Bus Low	I_{BO}	-20V ≤ V_{BUS} ≤ V_{BOH}; V_{TX} High		40	-	50	mA
Source Current, Bus High	I_{BO2}	V_{BOH} ≤ V_{BUS} ≤ (V_{BATT} -1.5V); V_{TX} High		0.25	0.5	0.75	mA
Current Limit, Short Circuit	$I_{BO(SC)}$	-2V ≤ V_{BUS} ≤ V_{BOH}; V_{TX} High		40	-	50	mA
Leakage Currents	I_{BO_LEAK}						
BATTERY Low/OFF		V_{BATT} ≤ 2V; V_{TX} High or Low		-10	-	10	µA
Bus High		(V_{BATT} -1.5V) ≤ V_{BUS} ≤ +20V; V_{TX} High		-10	-	10	µA
TX Low		-20V ≤ V_{BUS} ≤ +20V; 0V ≤ V_{BATT} ≤16V; V_{TX} Low		-10	-	10	µA
With Loss of BATTERY		-20V ≤ V_{BUS} ≤ +20V; 0V ≤ V_{BATT} ≤ 16V; V_{TX} High or Low		-10	-	10	µA
With Loss of Ground				-10	-	10	µA

Electrical Specifications T_A = -40°C to +125°C; 9.5V ≤ V_{BATT} ≤ 16V; Unless Otherwise Specified; Refer to Block Diagram and Figure 1, Figure 2, Figure 3 and Figure 4 for Waveforms and Test Circuit. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TX to BUS OUT Propagation Delays	t_{DTXHBO}, t_{DTXLBO}	R_{BS} = 10kΩ; C_{BS} = 470pF; R_S = 62kΩ; (Note 7)	10.7	13.75	17.5	µs
BUS OUT Transition Times, Rise and Fall	t_R, t_F		14	16	18	µs
BUS IN						
Input High Voltage	V_{BIH}		4.1	-	20	V
Input Low Voltage	V_{BIL}		-2	-	3.65	V
Input Hysteresis	$V_{B(HYS)}$		50	100	150	mV
Input Bias Current	I_{BIN}	-20V ≤ V_{BUS} ≤ 20V	-5	-	5	µA
Max. Input Current with Loss of Ground	$I_{BIN(MAX)}$	-20V ≤ V_{BUS} ≤ +20V; 0V ≤ V_{BATT} ≤ 16V; V_{TX} High or Low	-200	-	200	µA
Input Resistance	R_{BIN}		200	-	-	kΩ
Input Capacitance	C_{BIN}		10	-	25	pF
Filter Bandwidth	f_{BW} (3dB)	Measure with Ext. Series Resistor, R_F = 15kΩ	500	750	1000	kHz
RX OUTPUT						
Output Voltage, Low	V_{IL}	I_{OUT} = 1.6mA	0.05	-	0.4	V
Output Current	I_{RX}	V_{OUT} = 5V	2	5	8	mA
Output Leakage Current	$I_{RX(LK)}$	V_{OUT} = 5V, R_D = 10kΩ; BUS IN Low	-10	-	10	µA
Receive Propagation Delay	t_{DRXON}, t_{DRXOFF}	Meas. at Bus 50% Level	0.1	0.65	1.2	µs
$\overline{\text{LB EN}}$ CMOS/TTL INPUT WITH/PULL DOWN						
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Input Bias Current, LB	I_{LB}	V_{LB} = 7V; (Note 8)	10	-	30	µA
TX to RX Turn ON, OFF; Delay In Loop-Back Mode	t_{DLBON}, t_{DLBOFF}	V_{LB} Low; Toggle TX; Meas. RX	10.7	-	17.5	µs
$\overline{\text{LB EN}}$ Turn ON, OFF; TX to BUS OUT	$t_{D(LH)}$, $t_{D(HL)}$	V_{TX} High; Toggle $\overline{\text{LB EN}}$; Meas. BUS OUT	0.1	-	2	µs

NOTES:

1. Load Dump -40V (Fault capability of the J1850 Bus Transceiver includes reverse BATTERY, load dump and latch-up tolerance to ±200mA on any terminal.)
2. Transient Susceptibility Bus and BATTERY Pins Per SAE J1113, Aug 1987, Figure 1, Figure 2, Figure 3A and Figure 3B of -100V, +150V and ±200V.
3. ESD Conditions - SAE J1113; Aug 1987. BUS OUT and BATTERY Pins: Air Gap and Direct Contact Discharge; R = 2kΩ, C = 150pF
   All Other Pins: Direct Contact Discharge; R = 1.5kΩ, C = 100pF.
4. In the operating voltage range from 6V to 9.5V the BUS OUT, V_{BOH} is limited by the low power supply. In the operating voltage range from 16V to 24V the maximum bus load is limited by the device dissipation ratings.
5. Over-temperature shutdown with hysteresis is incorporated to protect the IC under system failure conditions.
6. Measured Current into the TX terminal is determined by Pull-Down Current Sink plus Leakage, $I_{TX} = I_{STX} + I_{LK}$.
7. Propagation Delay limits are measured at the 50% level which is referenced to 3.875V. Rise, Fall Times are referenced to 1.5V Low threshold point and 6.25V High threshold point.
8. Measured Current into the LB terminal is determined by Pull-Down Current Sink plus Leakage, $I_{LB} = I_{SLB} + I_{LK}$.

HIP7020 Signal Interface

The HIP7020 is a member of the Harris family of low cost multiplexed wiring ICs. As a Bus Transceiver IC, it interfaces the module and system control logic to the vehicle signal bus wiring. The integrated functions of the Bus Transceiver serve as an interface for a "Class B" multiplexed communications network. The TX digital interface is designed to accept CMOS/TTL logic levels and convert them to the appropriate J1850 analog serial data levels. This is accomplished using an internally generated reference waveform and voltage driver with a controlled current source to supply an analog signal output to the J1850 bus load of 300Ω (typical). Because of the special wave shaping used to control the J1850 bus waveform, it is regarded as an analog signal.

In the receive mode the incoming bus analog signals are input to the receiver at the BUS IN terminal. The bus data is converted to logic information by comparing it to an on-chip reference voltage. The received signal is provided as digital output from an open collector transistor driver at the RX output.

In the transmit mode a CMOS/TTL digital signal is received at the TX input. It is then rise and fall time controlled, wave shaped and level adjusted. A voltage controlled current driver circuit transmits the signal from the BUS OUT terminal to the J1850 Bus with current limiting protection.

Functional Blocks

The Bus Transceiver IC functional blocks, as shown in the Block Diagram, are as follows:

TX BUF (Transmit Input Buffer Interface)

The TX Buffer input function is a data interface to the Waveshaper reference circuit. The CMOS/TTL logic levels to be transmitted are input to the TX pin.

Waveshaper Circuit

This stage defines the transitions of high and low signal levels to provide a uniform rise and fall time. The input signal to the Waveshaper is the TX Buffer output and is an active high signal. In the Waveshaper the Transmit signal is amplified and compared to an internal reference voltage. The Waveshaper also provides waveform corner shaping on both the positive and negative going transitions. The rise and fall time of the serial waveform is set by the Waveshaper circuit and an external programming resistor, R_S that sets an internal current reference for control of the rise and fall slopes of the waveform.

Wave Shaped Voltage Reference Drive, V_{REF}

The Wave Shaped Voltage Reference circuit sets a scaled analog signal level and maintains a constant peak-to-peak voltage during worst case BATTERY voltage conditions, including cold cranking. The analog signal from the Wave Shaped Voltage Reference circuit drives the Voltage-to-Current Converter and a Level Shifter Interface to the bus driver transistor, Q1. The Voltage-to-Current Converter, in addition to the waveform leveling, helps to preserve low RFI and drive integrity. The edges of the wave shaped waveform, V_{REF} have well defined rise and fall times and the knees of the waveform are smooth and rounded as signal conditioning to reduce RFI.

Voltage-to-Current Converter

The Voltage-to-Current Converter determines the maximum current to be sourced out to the J1850 bus and is designed to source current proportional to the input signal from the Wave Shaped Voltage Reference, V_{REF}. The output of the Voltage-to-Current Converter maintains drive integrity of the V_{REF} waveform without the use of feedback.

A small quiescent current source is supplied to maintain a fixed minimum for each bus node. This precisely fixes the quiescent current at low input signal drive to the Voltage-to-Current Converter.

Voltage Controlled Current Driver, Q1

The Voltage Controlled Current Driver, Q1, controls the amount of current sourced out to the J1850 Bus. The Wave Shaped Voltage Reference, V_{REF}, drives the base of Q1 and the Voltage-to-Current Converter drives the collector of Q1. Both voltage and current determine the drive level which is supplied to the bus. When the Bus voltage is below the level determined by the Voltage Reference, V_{REF}, the Voltage Controlled Current Driver allows more current to be sourced out to the J1850 Bus. Voltage drive may increase as needed until the Bus voltage and the Voltage Reference match or until the maximum current limit is reached, as set by the Voltage-to-Current Converter. When the Bus voltage is above the Voltage Reference the Voltage Controlled Current Drive to the J1850 Bus is decreased. Decreasing correction occurs until the Bus voltage and the Voltage Reference match or until zero current is being sourced.

Filter, Bus Receiver and Voltage Comparator

The Filter limits the high frequency bandwidth by external resistor, R_F, and the input capacitance of the Filter Block. The on-chip Filter network and the external resistor, R_F, form a low pass filter to reject high frequency noise that may be present on the bus. Resistor, R_F, also provides isolation protection from transients. The analog bus signal is passed to the Bus Receiver and Voltage Comparator which determine when the bus is high or low as referenced to half the nominal bus voltage at the BUS IN pin.

RX BUF (Receiver Output Buffer Interface)

The RX BUF function is a buffer for the logic output as determined by the Bus Receiver and Voltage Comparator. An open collector transistor supplies current switched output to an external load resistor, R_D. BUS IN data is converted to serial CMOS/TTL logic data which is output at the RX pin of the HIP7020. Resistor, R_D, is biased from the digital 5V supply for optimum output drive levels to the logic circuits.

Thermal Shutdown

Over-temperature shutdown with hysteresis is incorporated to protect the IC under system failure conditions. Temperature is sensed at the transistor, Q1. Thermal shutdown will occur when the temperature of the chip reaches +150°C (minimum) and will latch-off the HIP7020 Bus Receiver operation. A reset occurs on the first positive edge transition of the next transmit data bit after ~15°C decrease in chip temperature. Hysteresis in the thermal shutdown threshold is necessary to allow the temperature to decrease to a safe operating temperature, typically less than +140°C.

Diagnostic Loop-Back Mode Switch

The HIP7020 has an active low Loop-Back Enabled Mode Switch which controls an internal signal path to provide diagnostic information. When Enabled, the Transmit/Receive signals are internally "Looped-Back" independent of the signal conditions on the J1850 Bus. A return path validation indicates proper action of the Bus Transceiver apart from the J1850 Bus. In the Loop-Back Mode, the transistor, Q1 output is forced low, preventing the output from sourcing current to the bus. Loop-Back is not affected by thermal shutdown.

Note: The Block Diagram switch position is shown for Loop-Back operation. A pull-down at the $\overline{LB\ EN}$ input forces an active low Loop-Back mode as the default position when no connection is applied.

Operational Description

Bus Output Signal

The BUS OUT output drive from the HIP7020 conforms to the SAE Standard **J1850 Class B Data Communication Network Interface** document specifications. It meets these requirements without oscillation, glitches or overshoots. The digital signal to be transmitted is wave shaped and amplitude controlled to produce an analog serial data waveform with precisely defined rise and fall edges. Operational capability covers a wide range of bus load resistances, capacitances and characteristic impedance while complying with the arbitration requirements of the Bus. Transient noise interference on the bus is minimized by the bus interface filtering and control circuitry of the Bus Transceiver IC.

The HIP7020 maintains a uniform and consistent bus waveform having specific transition times and propagation delays to preserve a J1850 analog data stream. Transmitted bus data is encoded by a J1850 PCI Controller (Programmable Communications Interface, see Figure 3) where "1's" and "0's" are defined by the length of time in which the bus voltage is high or low. Precise waveform control is necessary for a receiving node to accurately decode the difference between "1's" and "0's" by the time duration of high levels and low levels on the bus. In order to retain bus data integrity, digital information to be transmitted on the bus is wave shaped and amplitude controlled in the Bus Transceiver. The transmitted signal output to the J1850 Bus is a waveform with uniform edge control and precisely defined voltage levels.

Bus Current and Voltage Control

The Bus Transceiver has a Wave Shaped Voltage Reference which controls both the Voltage-to-Current Converter and the Bus Voltage Driver, Q1. The Voltage-to-Current Converter supplies a limited current feed to the collector of Q1. Together this provides the function of a Voltage Controlled Current Driver which controls the bus voltage drive level while supplying limited current to drive the bus load.

Wave Shaped Voltage Reference, V_{REF}

The output of the Wave Shaped Voltage Reference is a uniform signal which is a scaled waveform of the desired bus signal and is shown as V_{REF} in Block Diagram. This signal controls the output current driver and is the input to the Voltage-to-Current Converter. The internal reference voltage, V_{REF} is isolated from the J1850 Bus and is totally unaffected by the signal conditions on the bus. This isolation provides superior Bus stability in the vehicle environment. The bus drive control interface maintains the integrity of the V_{REF} waveform supplied to the bus. This is done without feedback control which is inherently susceptible to oscillation.

Voltage-to-Current Converter

The Voltage-to-Current Converter generates a current, I_{BO1} which is proportional to the Wave Shaped Voltage Reference magnitude and waveshape. This is the maximum current that can be supplied to the bus and is limited to a value of 45mA.

The Voltage-to-Current Converter also generates a sustained marginal current, I_{BO2} which bypasses the output driver direct to the BUS OUT pin. This current is proportional to the Voltage Reference magnitude and waveshape but is otherwise limited to 0.75mA. The purpose of this low level current source is to minimize reverse current conditions in the event of a bus collision. For example: With Node 1 and Node 2 in a state of Bus arbitration (both Nodes ON), a positive ground bounce interference at Node1 will attempt to assume full control and cause reverse current conditions at Node 2. The sustained marginal current sourced at Node 2 will assure a minimum level of output from Node 2 and will also reduce RFI on the bus.

Voltage Controller Current Driver

The Voltage Controller Current Driver, Q1, is the device which controls the amount of the available current which will be sourced out to the bus as determined by the Voltage Reference and allowed by the Voltage-to-Current Converter.

When the Bus voltage is below the Voltage Reference, Q1 allows more current to be sourced out to the J1850 Bus; until the Bus voltage and the Voltage Reference match or until the maximum current limit is reached as set by the Voltage-to-Current Converter.

When the Bus voltage is above the Voltage Reference, Q1 allows less current sourced out to the J1850 Bus; until the Bus voltage and the Voltage Reference match or until zero current is being sourced from Q1.

Bus Output Waveform

The bus output waveform shown in Figure 1 is controlled by the internal Waveshaper and has a tightly controlled rise and fall time with rounded corners. The RISE/FALL TIMES t_R and t_F are defined between V_{BOL} and V_{BOH}. The timing to reach the 50% voltage level of the bus signal is typically 13.75µs from the start of TX input going high.

Constant Propagation Time Delay

There is a constant propagation time delay from the TX going high or low to the Bus output signal (measured at 3.875V). This time delay is nominally 13.75µs. The propagation time delay signals are shown in Figure 2.

The BUS IN input signals, as shown in Figure 2, are characterized by the V_{BIH} and V_{BIL} specifications which include hysteresis. There is a constant propagation delay for the Bus to RX receive channel of the Bus Transceiver. The received propagation delay time is typically 1µs as measured in reference to the 50% voltage level on the rising or falling edge of the BUS IN input signal to the rising or falling edge of the RX output signal.

Low Pass Filter Input

The BUS input has an on-chip input filter to strip off the unwanted incoming high frequency noise. The 3dB point of this filter is nominally 750kHz.

Diagnostic Bus-Isolated Loop-back

An on-chip Bus-Isolated Diagnostic Loop-Back function is controlled by the $\overline{\text{LB EN}}$ pin. The Loop-Back function is a mode switch that is enabled by placing a logic low on the $\overline{\text{LB EN}}$ pin. When activated, the signal flow is cross-switched to open the Bus Receive Input and connect the Voltage Reference, V_{REF} output to the input of the Bus Receiver. This "Loops-Back" the TX signal to the RX output while maintaining isolation from the signal on the J1850 Bus. When the Loop-Back is enabled, diagnostic trouble shooting can be done at each individual node regardless of fault conditions on the bus.

Thermal Shut Down Protection

On-chip Thermal Shutdown Protection is designed to shutdown source drive to the J1850 bus and protect the Bus Transceiver IC output. The temperature shutdown threshold is set to protect the absolute maximum junction temperature of the chip and is nominally set for +160°C with 15°C to 20°C of hysteresis. Thermal shutdown may occur when over-load conditions exist on the bus. (See Function Blocks - Thermal Shutdown).

Package Pinout

BATT Pin

The BATT pin is connected directly to the vehicle Battery (Ignition) line. The Battery supply connection (V_{BATT}) provides voltage for all on-chip functions, including the voltage reference. As such, the BATT input is designed to withstand transient power supply conditions.

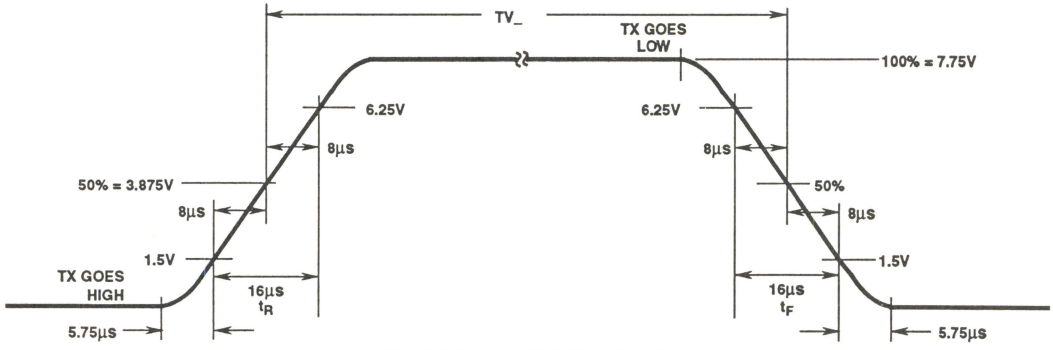


FIGURE 1. J1850 BUS WAVEFORM

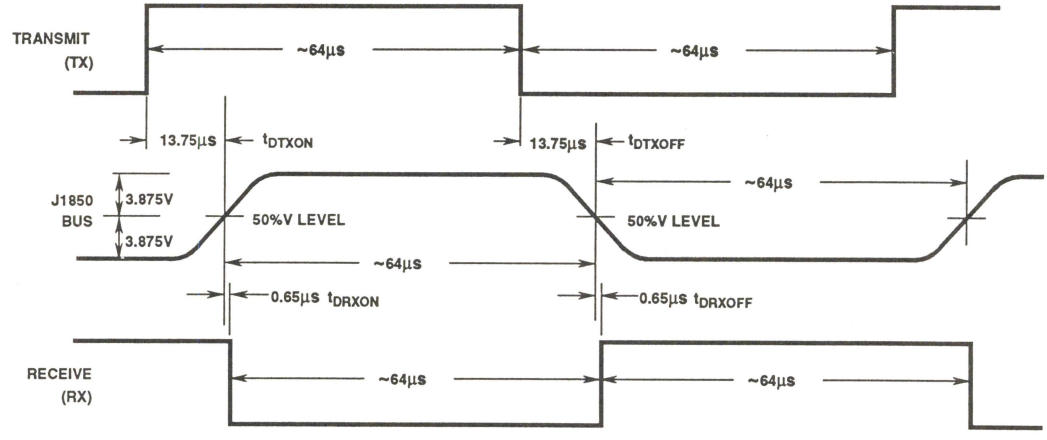


FIGURE 2. PROPAGATION TIME DELAYS

TRANSMIT (TX) Pin

The TRANSMIT pin will accept standard CMOS/TTL logic level input data. Logic level data is input at the TRANSMIT (TX) pin in a serial format, such as provided by a Harris J1850 PCI Controller, and is output on the J1850 Bus at the BUS OUT pin. The TX input has an active pull down current sink to insure that a logic level low will be maintained when no signal drive is present.

Receive (RX) Pin

The RX pin is the output for J1850 Bus data and interfaces to an open collector transistor output driver. The RX digital data output is inverted from the analog bus data input at the BUS IN pin. The data from the RX pin is output to a Harris HIP7010 Byte Level I/O or a HIP7030A2 Protocol Microcontroller IC where the 10.4Kbps VPWM messages from the J1850 network are decoded.

Ground Pin

This is the HIP7020 Bus Transceiver IC ground reference for all the signals which interface to the control logic and the J1850 bus. It is also the ground return path for the BATTERY power supply to IC.

R/F Time Pin

The R/F (Rise/Fall) Time pin connects the external resistor, R_S, from the wave shaped voltage reference to ground. The Rise and Fall Time is controlled by the transition slope of the signal waveform. The resistor, R_S, sets an internal current reference to control the rise and fall slope.

BUS IN Pin

The BUS IN pin is the receive input of the SAE J1850 Bus signal. It receives the 10.4kHz VPWM (Variable pulse width modulated) data from the single wire analog serial bus through an external Resistor, R_F.

BUS OUTPUT Pin

The BUS OUTPUT pin transmits the SAE J1850 10.4kHz VPWM (Variable Pulse Width Modulated) data to the serial bus. Data is transmitted to the serial J1850 bus with the same polarity as the TX input signal.

$\overline{\text{LB EN}}$ Pin

The $\overline{\text{LB EN}}$ Loop-Back Enable pin controls the Diagnostic Loop- Back Mode Switch function. A logic low on the $\overline{\text{LB EN}}$ pin connects the output of the Wave Shaped Voltage Reference to the Bus Receiver & Voltage Comparator while disconnecting the filtered input of J1850 Bus. This feature provides the means to trouble shoot system problems.

Test/Application Circuit

The circuit of Figure 3 illustrates the essential elements of the J1850 Bus Transceiver in a normal application. For normal J1850 applications, a Bus Transceiver is used at each system node. The Electrical Specifications Table also refers to the peripheral components shown in Figure 3 and the Block Diagram for the HIP7020 Bus Transceiver.

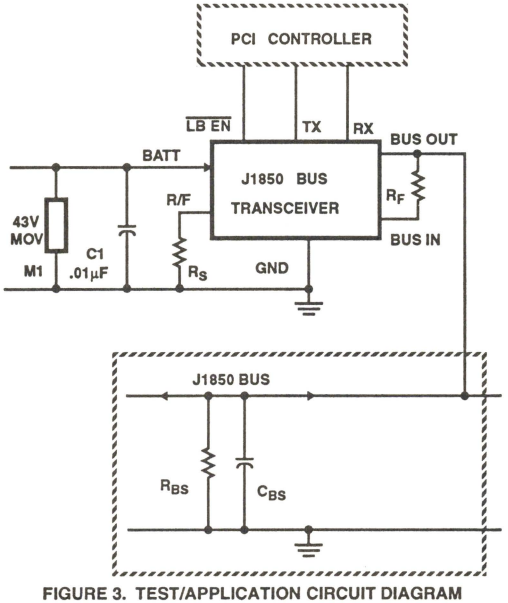


FIGURE 3. TEST/APPLICATION CIRCUIT DIAGRAM

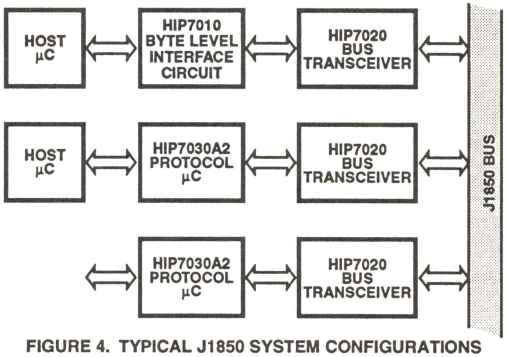


FIGURE 4. TYPICAL J1850 SYSTEM CONFIGURATIONS

HARRIS SEMICONDUCTOR

HIP7030A0

PRELIMINARY

April 1994

J1850 8-Bit 68HC05 Microcontroller Emulator Version

Features

- HIP7030A2 Microcontroller Emulation
  - All HIP7030A2 Hardware and Software Features
  - Timing and Performance Equivalent to HIP7030A2
- On-Chip Memory
  - 176 Bytes of RAM - No ROM
- Full 8K Byte Address Space Available Externally
- Non-Multiplexed External Address and Data Lines
  - I/O Memory Interface Matches Industry Standard EPROM/EEPROMS for True Emulation with Two Chips
- FS Line Identifies Fetch Cycles for Breakpoint Logic
- -40°C to +125°C Operating Range
- Single 3.0V to 6.0V Supply
- Available in 68 Lead PLCC Packages

Description

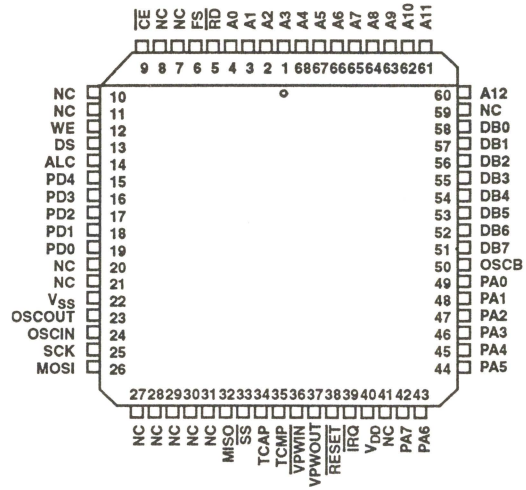
The HIP7030A0 Emulator is functionally equivalent to the HIP7030A2 microcontroller with the addition of external data bus, address bus, and control signals which provide off chip address capability. It is designed to permit prototype and pre-production development of systems for mask programmed applications. The HIP7030A0 is also intended for construction of development systems for the HIP7030A2.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP7030A0M	-40°C to +125°C	68 Lead Plastic LCC

Pinout

HIP7030A0 (PLCC)
TOP VIEW

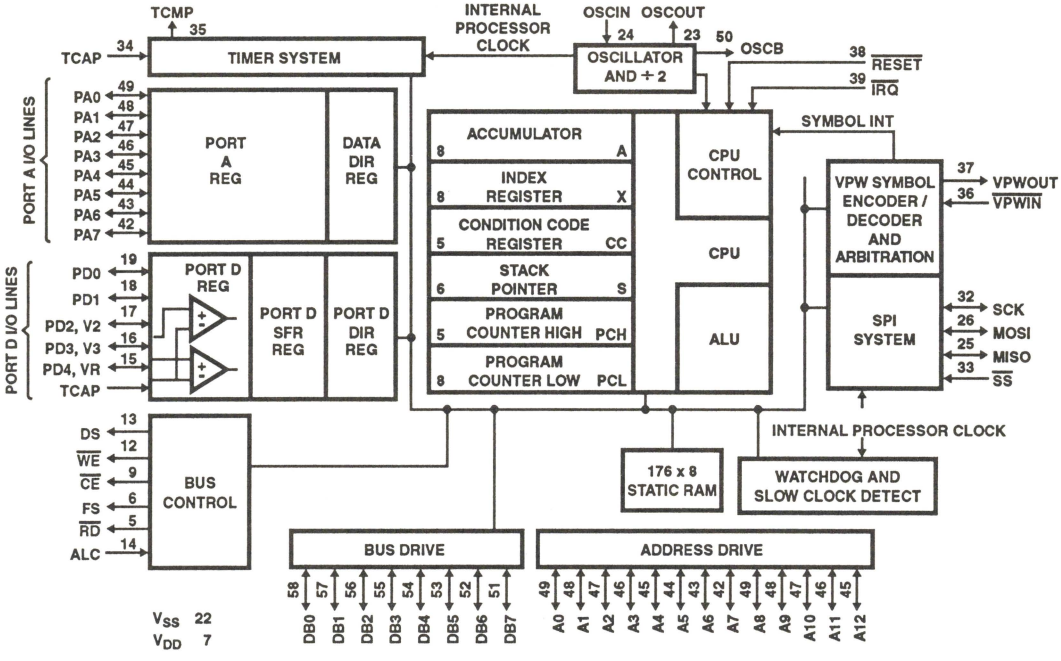


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3645

Block Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{DD} . . . . . -0.5 to +7V
Input Voltage, V_{IN} (Note 1) . . . . . (V_{SS}-0.3) to (V_{DD}+0.3)V
Self-Check Mode ($\overline{IRQ}$ Pin Only), V_{IN}. . . (V_{SS}-0.3) to 2•(V_{DD}+0.3)V
Current Drain Per Pin (Excluding V_{DD} and V_{SS}) 25mA

Thermal Information

Thermal Resistance θ_{JA}
Plastic LCC Package . . . . . 55°C/W
Maximum Package Power Dissipation, P_D at 125°C 450mW
Operating Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range, T_{STG} . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Control Timing

V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
FREQUENCY OF OPERATION						
Crystal Option	f_{OSC}		1	-	10	MHz
External Clock Option			1	-	10	MHz
INTERNAL OPERATING FREQUENCY						
Crystal (f_{OSC} + 2)	f_{OP}		0.5	-	5	MHz
External Clock (f_{OSC} + 2)			0.5	-	5	MHz
Cycle Time	t_{CYC}		200	-	-	ns

DC Electrical Specifications

V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} < 10mA	-	-	0.1	V
	V_{OH}	I_{LOAD} > -10mA	V_{DD} -0.1	-	-	V
Output High Voltage: A0-A12, DB0-DB7, $\overline{CE}$, $\overline{RD}$, $\overline{WE}$, FS	V_{OH}	I_{LOAD} = 0.8mA	V_{DD} -0.8	-	-	V
Output Low Voltage: A0-A12, DB0-DB7, $\overline{CE}$, $\overline{RD}$, $\overline{WE}$, FS	V_{OH}	I_{LOAD} = 1.6mA	-	-	0.4	V
Input High Voltage: DB0-DB7	V_{IH}		-	0.5•V_{DD}	0.7•V_{DD}	V
Input Low Voltage: DB0-DB7	V_{IL}		0.3•V_{DD}	-	-	V
DB0-7 High Impedance Leakage Current:	I_{IL}		-10	-	+10	µA
Input Current	I_{IN}		-1	-	+1	µA
Capacitance	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Supply Current: RUN	I_{RUN}		-	8	TBD	mA

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})
2. Characteristics are listed for the signals unique to the Emulator IC. For details on the other signal pins see the HIP7030A2 data sheet.
3. Minimum frequency applies when ALC is low.

Read Cycle Timing (ALC = 0) (See Figure 1) $V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40°C$ to $+125°C$ Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency	1	10	MHz
(1)	t_{CYC}	Read Cycle Time	200	2000	ns
(2)	t_{AVCEL}	Address Setup Time Before $\overline{CE}$	-10	-	ns
(3)	t_{DVCEL}	Access Time From $\overline{CE}$	-	$t_{CYC} - 80$	ns
(4)	t_{DVRDL}	Access Time From $\overline{RD}$	-	$0.75t_{CYC} - 80$	ns
(5)	t_{DVAV}	Access Time From Address Change	-	$t_{CYC} - 80$	ns
(6)	t_{CEHAX}	Address Hold Time After $\overline{CE}$	0	-	ns
(7)	t_{CEHAX}	Data Hold Time After $\overline{CE}$	0	-	ns
(8)	t_{RDLDX}	Data Bus Driven From $\overline{RD}$ (Time to Data Active from High Impedance State)	0	-	ns
(9)	t_{RDHAX}	Data Hold Time After $\overline{RD}$ (Hold Time to High Impedance State)	0	-	ns
(10)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

Minimum frequency applies when ALC is low.

Write Cycle Timing (ALC = 0) (See Figure 2) $V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40°C$ to $+125°C$ Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency	1	10	MHz
(1)	t_{CYC}	Write Cycle Time	200	2000	ns
(2)	t_{AVCEL}	Address Setup Time Before $\overline{CE}$	-10	-	ns
(3)	t_{AVWEL}	Address Setup Time Before $\overline{WE}$	$0.25t_{CYC} - 25$	-	-
(4)	t_{WEWE}	$\overline{WE}$ Pulse Width	$0.5t_{CYC} - 10$	-	ns
(5)	t_{DVWEH}	Data Set-up Time to $\overline{WE}$ Trailing Edge	$0.75t_{CYC} - 75$	-	ns
(6)	t_{WEHDX}	Data Hold Time After $\overline{WE}$ Trailing Edge	$0.25t_{CYC} - 20$	-	ns
(7)	t_{WEHAX}	Address Hold Time After $\overline{WE}$ Trailing Edge	$0.25t_{CYC} - 20$	-	ns
(8)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

1. Minimum frequency applies when ALC is low.

Read Cycle Timing (ALC = 1) (See Figure 3) $V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40°C$ to $+125°C$ Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency		10	MHz
(1)	t_{CYC}	Read Cycle Time	200	-	ns
(2)	t_{RDOSC}	$\overline{RD}$, FS Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(3)	t_{DVCEL}	Access Time From $\overline{CE}$	-	t_{CYC}-80	ns
(4)	t_{DVOSC}	Access Time From OSCB	-	t_{CYC}-70	ns
(5)	t_{OSCAV}	Address Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(6)	t_{OSCAX}	Address Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(7)	t_{OSCAX}	Data Hold Time After OSCB	10	-	ns
(8)	t_{RDLDX}	Data Bus Driven From $\overline{CE}$ (Time to Data Active from High Impedance State)	0	-	ns
(9)	t_{OSCRD}	$\overline{RD}$, FS Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(10)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

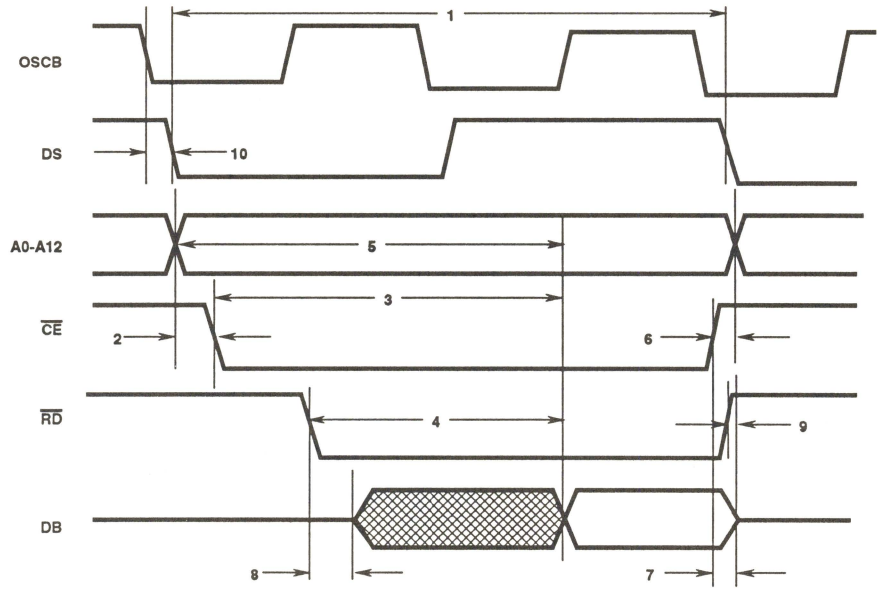
1. Minimum frequency applies when ALC is high.

Write Cycle Timing (ALC = 1) (See Figure 4) $V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40°C$ to $+125°C$ Unless Otherwise Specified.

NUMBER	SYMBOL	PARAMETER	MIN	MAX	UNITS
	f_{OSC}	OSCB Operating Frequency		10	MHz
(1)	t_{CYC}	Write Cycle Time	200	-	ns
(2)	t_{RDOSC}	$\overline{RD}$, FS Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(3)	t_{DVOSC}	Data Setup Time Before OSCB		$0.75t_{CYC}$-95	ns
(4)	t_{OSCAV}	Address Setup Time Before OSCB	$0.5t_{CYC}$-25	-	ns
(5)	t_{OSCAX}	Address Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(6)	t_{OSCAX}	Data Hold Time After OSCB	10	-	ns
(7)	t_{OSCDX}	Data Bus Driven From OSCB (Time to Data Active from High Impedance State)	$.25t_{CYC}$-25	-	ns
(8)	t_{OSCRD}	$\overline{RD}$, FS Hold Time After OSCB	$0.5t_{CYC}$	-	ns
(9)	t_{OSCDS}	OSCB to DS Propagation Delay	5	25	ns

NOTE:

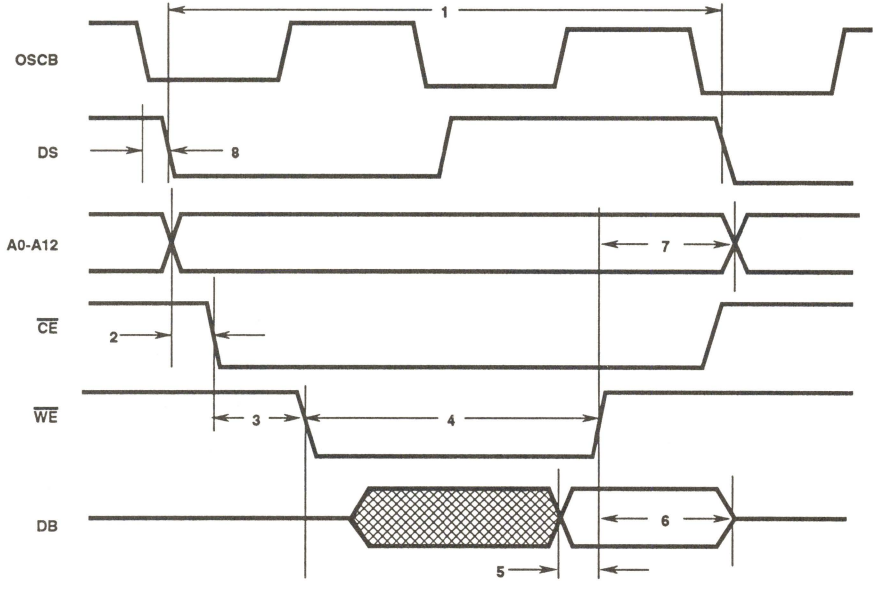
1. Minimum frequency applies when ALC is high.



NOTE:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.

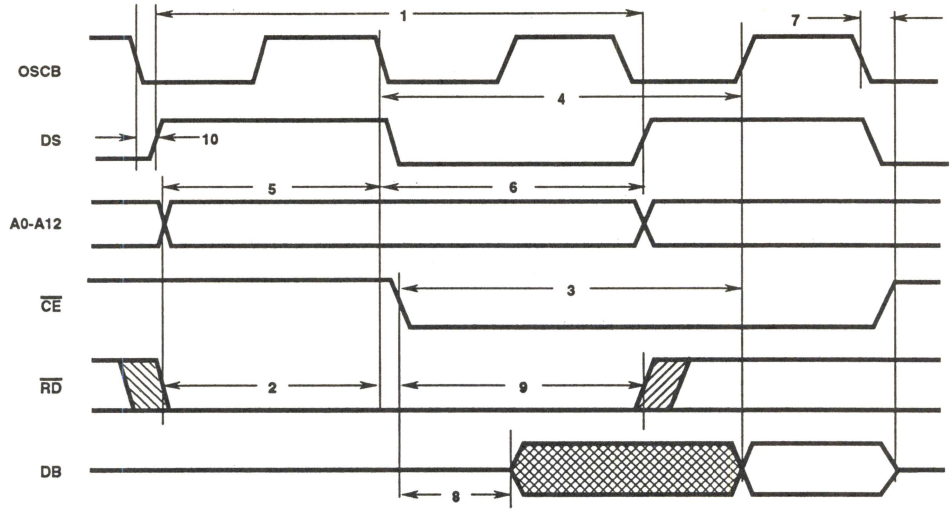
FIGURE 1. READ CYCLE TIMING DIAGRAM (ALC = 0)



NOTE:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.

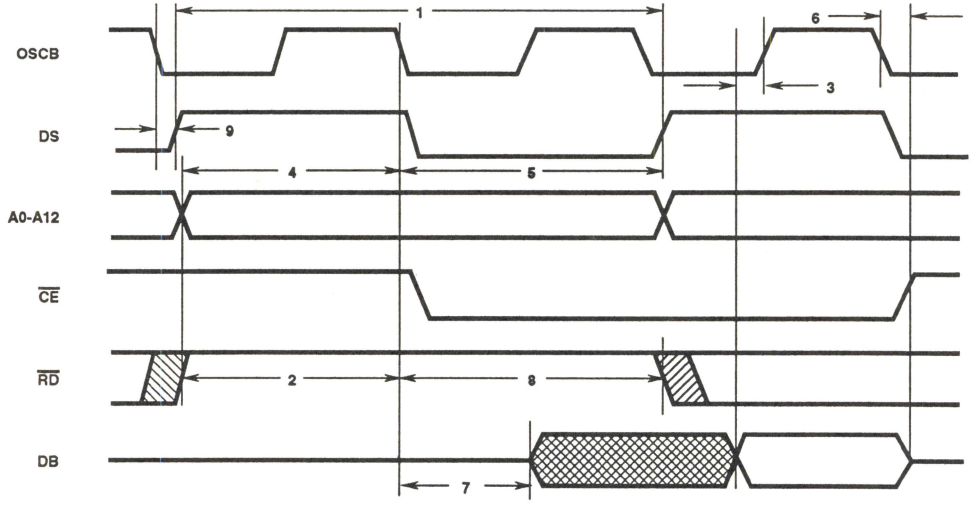
FIGURE 2. WRITE CYCLE TIMING DIAGRAM (ALC = 0)



NOTES:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.
2. Timing for FS is identical to RD timing.

FIGURE 3. READ CYCLE TIMING DIAGRAM (ALC = 1)



NOTES:

1. Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}.
2. Timing for FS is identical to RD timing.

FIGURE 4. WRITE CYCLE TIMING DIAGRAM (ALC = 1)

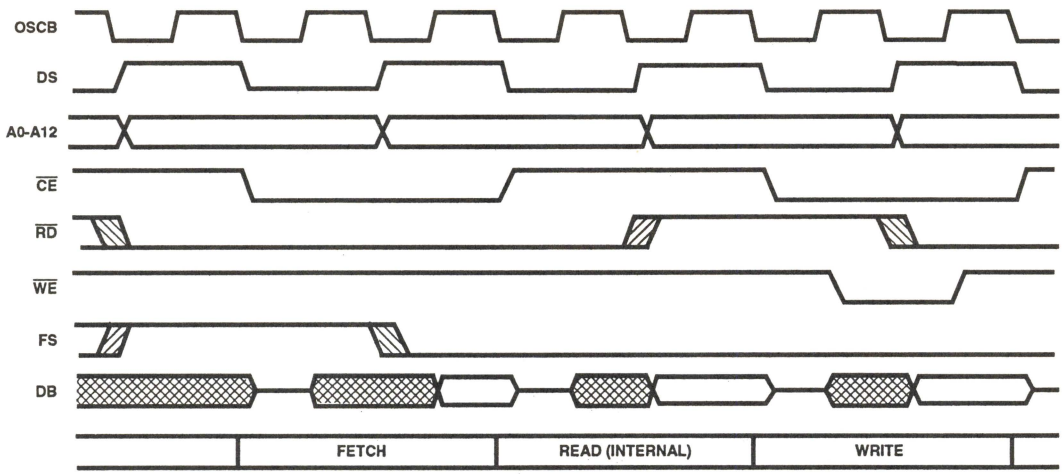


FIGURE 5. SIGNAL TIMING DIAGRAM (ALC = 1)

Functional Pin Description

This section provides a brief description of each of the pins of the HIP7030A0 microcontroller. A more detailed discussion is contained in the HIP7030A2 data sheet.

V_{DD} and V_{SS} (Power)

Power is supplied to the MCU using these two pins. V_{DD} is connected to the positive supply and V_{SS} is connected to the negative supply.

$\overline{IRQ}$ (Maskable Interrupt Request - Input)

The $\overline{IRQ}$ pin is negative edge-sensitive triggering. A high to low transition on the input to the $\overline{IRQ}$ pin will produce an interrupt.

In the event of an interrupt request, the MCU always completes the current instruction before it responds to the request. An internal mask can be used to inhibit the MCU from responding to $\overline{IRQ}$ interrupts.

An edge-sensitive $\overline{IRQ}$ interrupt is generated if the $\overline{IRQ}$ pin is pulled low for at least one t_{ILIH}. The occurrence of the low going pulse is registered in a flip-flop and the $\overline{IRQ}$ interrupt will be recognized even if the $\overline{IRQ}$ pin has returned to a high state before the interrupt can be serviced.

Once the edge-sensitive flip-flop is cleared (it is automatically cleared at the start of the interrupt service routine) the interrupt request is removed until the $\overline{IRQ}$ pin returns to a high level and once again goes low.

$\overline{RESET}$ (Master Reset - Input)

The HIP7030A2 contains an integrated Power-On Reset (POR) circuit and the $\overline{RESET}$ input is therefore not required for start-up. It can be used to reset the MCU internal state and provides for an orderly re-start of the software after initial power-up. A low level on the $\overline{RESET}$ pin will reset the HIP7030A0.

TCAP (Timer Capture - Input)

The TCAP input controls the input capture feature for the on-chip programmable timer system. The TCAP input is also used as the strobe signal to the Port D strobed outputs.

TCMP (Timer Compare - Output)

The TCMP pin provides an output for the output compare feature of the on-chip timer system.

OSCIN (Oscillator Input - Input),
OSCOUT (Oscillator Output - Output),
OSCB (Oscillator Buffered Output - Output)

OSCIN is the input and OSCOUT is the output of an inverter/amplifier which can be used to build either a quartz crystal or ceramic resonator based clock oscillator. Alternatively the OSCIN input can be driven from any external clock source which satisfies the CMOS schmitt trigger input level requirements of the OSCIN pin. OSCB is a squared, buffered version of the OSCIN signal, available for driving one external CMOS load. See Electrical Specifications of the HIP7030A2 for output drive and input level specifications.

The fundamental internal clock is derived by a divide-by-two of the external oscillator frequency (fOSC). All other internal clocks are also derived from the external frequency. These clocks include the input to the 16-bit Timer, the SPI Serial Clock (SCK), and the VPW Symbol Encoder/Decoder (SENDEC).

PA0-PA7 (Port A - Input/Output)

These eight I/O lines comprise Port A. The mode (i.e. - input or output) of each pin is software programmable. All Port A I/O lines are configured as inputs during power-on or $\overline{RESET}$.

PD0-PD4 (Port D - Input/Output)

These five I/O lines comprise Port D. As with PA0-PA7, the mode (i.e. - input or output) of each pin is software programmable. In addition a Special Function Register (SFRD) allows configuring PD0 and PD1 as "strobed" outputs, and/or PD2,PD3, and PD4 as inputs to an on-chip analog comparator.

All Port D I/O lines are configured as inputs during power-on or $\overline{\text{RESET}}$.

VPWOUT (Variable Pulse Width Out - Output),
$\overline{\text{VPWIN}}$ (Variable Pulse Width In - Input)

These two lines are used to interface to the J1850 bus transceiver.

VPWOUT is the pulse width modulated output of the SENDEC encoder block.

$\overline{\text{VPWIN}}$ is the inverted input to the SENDEC decoder block.

MISO (Master-in/Slave-out - Input/Output),
MOSI (Master-out/Slave-in - Input/Output),
SCK (Serial Clock - Input/Output),
$\overline{\text{SS}}$ (Slave Select - Input)

These four lines constitute the Serial Peripheral Interface (SPI) communications port. The MCU can be configured as a SPI "master" or as a SPI "slave". In master mode MOSI and SCK function as outputs and MISO functions as an input. In slave mode MOSI and SCK are inputs and MISO is an output. SS is always an input.

Serial data words are transmitted and received over the MISO/MOSI lines synchronously with the SCK clock stream. The word size is fixed at 8 bits. Single buffering is used which results in an inherent inter-byte delay. The master device always provides the synchronizing clock.

A low on the $\overline{\text{SS}}$ line causes the MCU to immediately assume the role of slave, regardless of it's current mode. This allows multi-master systems to be constructed with appropriate arbitration protocols.

ALC (Address Latch Control - Input)

The ALC input controls the timing and function of the address and memory control lines ($\overline{\text{CE}}$, $\overline{\text{RD}}$, $\overline{\text{WE}}$, and FS). For more information on each of these lines refer to the appropriate section.

When ALC is low the address and control lines are produced coincident with data bus transitions of the HIP7030A0's machine cycle. This mode allows direct interfacing to industry standard memory devices. Refer to the timing diagrams in **Electrical Specifications** for more details.

Driving ALC high causes several changes in the behavior of the address and control lines. These changes are intended to facilitate design of development systems for the HIP7030A2. When ALC is high the following occur:

- The Internal RAM is disabled and accesses to RAM space are mapped off-chip.
- A0-A12, FS, and $\overline{\text{RD}}$ are produced t_{CYC} cycle (i.e. 100ns with a 10MHz clock) ahead of data bus transitions of the HIP7030A0's machine cycle. The earlier availability of these address and control lines facilitates implementation of break detection and bus tracing logic. External latching of the address and control signals is required for interfacing to the memory of the development tool. The timing of $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are not affected by ALC, and remain synchronized with data bus transfers.
- The $\overline{\text{RD}}$ signal is no longer gated with $\overline{\text{CE}}$ and is a full cycle wide, when ALC is high. $\overline{\text{RD}}$ indicates whether the ensuing data bus cycle will be a ***read of*** or ***write to*** memory-I/O space. It can be viewed as a R/$\overline{\text{W}}$ signal. $\overline{\text{RD}}$ provides R/$\overline{\text{W}}$ information for all cycles, internal as well as external.
- Resetting the HIP7030A0 with ALC = 1 disables the Slow Clock Detect circuits. The Watchdog can be disabled by writing to the Watchdog Status Register (WSR - location $1E), which has special features when ALC is high. The Slow Clock circuit is permanently disabled when ALC = 1. If the Slow Clock detect circuitry were allowed to run, stopping the CPU clock during breakpoint servicing would not be possible. The watchdog should be reset by the tool while interrogating the CPU.

The ALC input has an integrated pull-down device which allows floating this pin when interfacing to industry standard memory devices.

A0-A12

Address lines 0 through 12. When ALC = 0, A0-A12 are coincident with data bus transfers. When ALC = 1, A0-A12 change t_{CYC} ahead of the data bus transfers and must be externally latched. See the timing diagrams in the **Electrical Specifications** section for more details.

DB0-DB7

Bidirectional 8-bit non-multiplexed data bus lines. The data bus is an input during all reads from external memory-I/O space and during the first t_{CYC} of every machine cycle. At all other times it is an output. See the timing diagrams in the **Electrical Specifications** section for more details.

$\overline{\text{CE}}$ (Chip Enable - Output)

Chip Enable is an output signal used for selecting external memory or I/O. A low level indicates when external memory or I/O is being accessed. Note that the $\overline{\text{CE}}$ signal will not go true when addressing the unused locations of Page 0 I/O space even though the address lines will be valid.

$\overline{\text{RD}}$ (Read - Output)

$\overline{\text{RD}}$ is a status output signal which indicates direction of data flow with respect to external or internal memory space (a low level indicates a read from memory space). A read from internal memory or I/O will place data on the external data

bus. When ALC = 0, $\overline{RD}$ is internally gated with $\overline{CE}$, and generated in synchronization with data bus cycles. With ALC = 0, standard RAM, ROM, and EPROM devices can be directly connected to the HIP7030A0 with no additional components. When ALC = 1, $\overline{RD}$ is not gated by $\overline{CE}$ and is produced t_{CYC} cycle (i.e. 100ns with a 10MHz clock) ahead of data bus transitions of the HIP7030A0's machine cycle.

$\overline{WE}$ (Write Enable - Output)

Write Enable is an active low output pulse for use in writing data to external RAM memory. A low level indicates valid data on the data bus. $\overline{WE}$ is internally gated with $\overline{CE}$ for writing to external memory. Since, in most systems, external memory is substituting for mask programmed ROM, $\overline{WE}$ is frequently not used.

DS (Data Strobe - Output)

The Data Strobe output provides a pulse when address and data are valid. DS can be used to transfer data to or from a peripheral or memory and occurs every cycle and is also used for synchronizing development tools to the oscillator clock. DS is a continuous signal at $f_{OSC} \div 2$, except when the Emulator is in the WAIT or STOP mode. See the timing diagrams in the **Electrical Specifications** section for more details.

FS (Fetch Status - Output)

The FS output signal goes true to indicate an opcode fetch cycle is in progress. When ALC = 0, FS will be coincident with the data transfer of the fetch. When ALC = 1, FS is produced t_{CYC} cycle (i.e. 100ns with a 10MHz clock) ahead of data bus transitions of the HIP7030A0's machine cycle. See the timing diagrams in the **Electrical Specifications** section for more details.

Watchdog Status Register

When ALC is high, the HIP7030A0's Watchdog Status Register (WSR - location $1E) provides the ability to selectively enable and disable the Watchdog Timer logic of the HIP7030A0.

The user of a development tool should be cautioned against accidently clearing the WDE bit of this register during final code prove-out. During initial code development the user may want to intentionally clear this bit to eliminate the need to insert watchdog handling routines. The clearing of the bit must be done following every reset.

Reset presets the WDE bit of the WSR to enable the Watchdog Timer.

7	6	5	4	3	2	1	0
-	-	-	-	-	-	WDE	WDF

WATCHDOG STATUS REGISTER

Bit 7,6,5,4,3,2 - Unused

Bit 1 - WDE

When WDE (WatchDog Enable) is low, the Watchdog Timer is disabled. When ALC is high, WDE is forced high by any reset. The WDE bit should normally be cleared when servicing a breakpoint (if OSCIN is being clocked), to avoid a Watchdog Reset while interrogating the CPU.

The WDE bit controls the Watchdog Reset, but it doesn't inhibit the Watchdog Timer from advancing. Prior to re-enabling the WDE bit, the Watchdog Timer should normally be reset by writing $55, $AA to the Watchdog Reset Register (WDRR, location $1D). This implies that each breakpoint should generate a Watchdog Reset. To verify proper watchdog action the user should run final code with no breaks. In some cases the number of CPU cycles utilized in the break may be low enough to allow the watchdog to run without causing premature watchdog timeouts.

Bit 0 - WDF

The WatchDog flag (WDF), is set when a Watchdog timeout causes a COP Reset. This flag is used to distinguish a Slow Clock Detect from a Watchdog Timeout in the COP Reset service routine.

Writing a 0 to the Watchdog Reset Register (WDRR, location $1D) clears the WDF flag. WDF is cleared by Power-on Reset, but unaffected by all other types of resets. For this reason, WDF should normally be cleared (by writing a 0 to the WDRR) following each read of the WSR.

HARRIS SEMICONDUCTOR

HIP7030A2

ADVANCE INFORMATION

April 1994

J1850 8-Bit 68HC05 Microcontroller

Features

- Fully Supports VPW Specifications of SAE Recommended Practice J1850 for Class B Multiplexed Wiring
- On-Chip Memory
- 176 Bytes of RAM
- 2110 Bytes of User ROM
- 13 Bidirectional I/O Lines
- 16-Bit Timer with Capture and Compare Registers
- Serial Peripheral Interface (SPI) System
- Watchdog Timer and Slow Clock Detect
- 10MHz Operating Frequency (5.0MHz Internal Bus Frequency) at 5V
- Built-In-Test Bootstrap Mode with 242 Bytes of ROM
- Two Channel Analog Comparator
- On-Chip Oscillator Amplifier
- 8-Bit CPU Architecture
- Power-Saving STOP, WAIT and Data Retention Modes
- Full -40°C to +125°C Operating Range
- Single 3.0V to 6.0V Supply
- 28 Lead Dual-In-Line and Small Outline Plastic Packages

Software Features

- Standard 68HC05 Instruction Set
- True Bit Manipulation
- Addressing Modes Include Indexed Addressing
- Memory Mapped I/O

Description

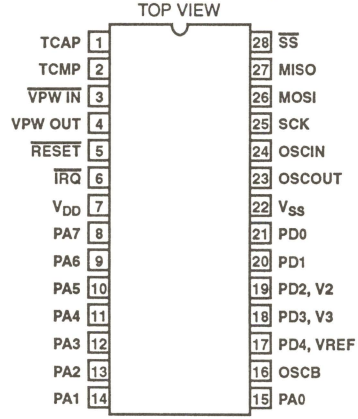
The HIP7030A2 HCMOS Microcomputer is a member of the CDP68HC05 family of low-cost single-chip microcomputers. The integrated hardware functions provide the system designer with a complete set of building blocks for implementing a "Class B" multiplexed communications network interface, which fully conforms to the VPW Multiplexed Wiring protocol specified in SAE Recommended Practice J1850. This 8-bit microcomputer unit (MCU) contains an on-chip oscillator, CPU, 176 bytes of RAM, 2110 bytes of user ROM, 13 I/O lines, a J1850 Variable Pulse Width Symbol Encoder/Decoder (VPW SENDEC) system, a Serial Peripheral Interface (SPI) system, a two channel analog Comparator, a Watchdog Timer, a Slow Clock Detect, and a 16-bit Timer. The static HCMOS design allows operation at input frequencies up to 10MHz (5MHz internal clock).

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP7030A2P	-40°C to +125°C	28 Lead Plastic DIP
HIP7030A2M	-40°C to +125°C	28 Lead Plastic SOIC (W)

Pinout

HIP7030A2 (PDIP, SOIC)
TOP VIEW

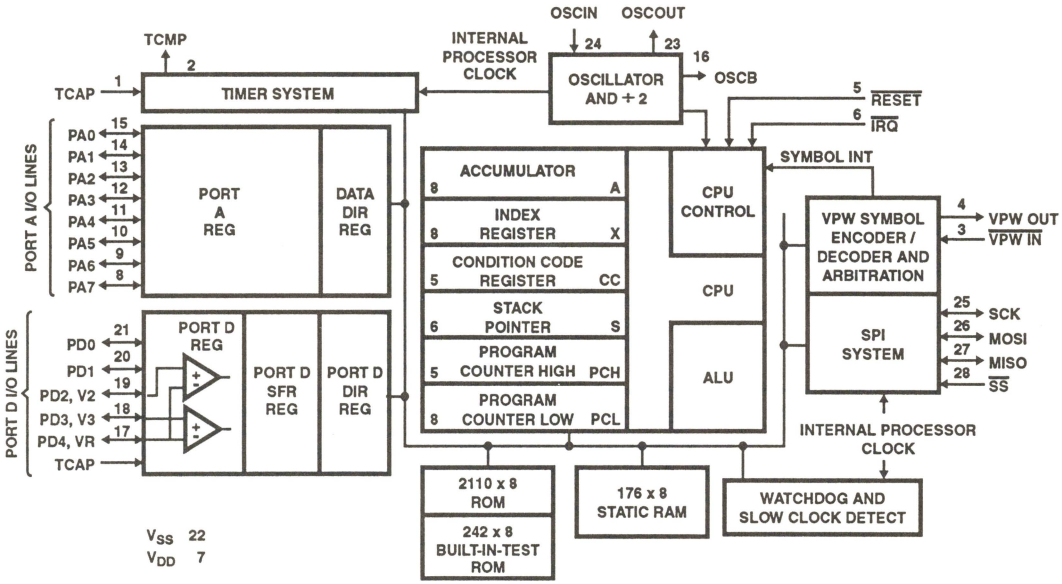


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3646.1**

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... -0.3V to +7.0V
Input or Output Voltage
  Pins with V_{DD} Diode ..... -0.3V to V_{DD}+0.3V
  Pins without V_{DD} Diode ..... -0.3V to +10V
Current Drain Per Pin, I (Excluding V_{DD} and V_{SS}) 25mA
Lead Temperature (Soldering 10s) ..... +265°C
ESD Classification ..... Class 2
Gate Count ..... 9000 Gates

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	60°C/W
Plastic SOIC Package	75°C/W

Maximum Package Power Dissipation at +125°C
  DIP Package 415mW
  SOIC Package 325mW
Operating Temperature Range (T_A) ..... -40°C to +125°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +3.0V to +5.5V
Operating Temperature Range ..... -40°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... .(0.8•V_{DD}) to V_{DD}
Input Rise and Fall Time
  CMOS Inputs ..... 100ns Max.
  CMOS Schmitt Inputs ..... Unlimited

DC Electrical Specifications

V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} < ±10µA	-	-	0.1	V
	V_{OH}		V_{DD} -0.1	-	-	V
Output High Voltage: PA0-7, PD0-4, VPWOUT, TCMP	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} -0.8	V_{DD} -0.4	-	V
Output High Voltage: OSCOUT	V_{OH}	I_{LOAD} = TBD	TBD	TBD	-	V
Output High Voltage: MISO, MOSI, SCK, OSCB	V_{OH}	I_{LOAD} = -1.6mA	V_{DD} -0.8	V_{DD} -0.4	-	V
Output Low Voltage	V_{OL}	I_{LOAD} = 1.6mA	-	0.2	0.4	V
Input High Voltage: PA0-7, PD0-4, $\overline{VPWIN}$, MISO, MOSI, $\overline{SS}$, SCK	V_{IH}		-	0.5•V_{DD}	0.7•V_{DD}	V
Input High Voltage: $\overline{RESET}$, $\overline{IRQ}$,TCAP, OSCIN	V_{IH}		0.45•V_{DD}	0.6•V_{DD}	0.8•V_{DD}	V
Input Low Voltage: PA0-7, PD0-4, $\overline{VPWIN}$, MISO, MOSI, $\overline{SS}$, SCK	V_{IL}		0.3•V_{DD}	0.5•V_{DD}	-	V
Input Low Voltage: $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSCIN	V_{IL}		0.2•V_{DD}	0.4•V_{DD}	0.55•V_{DD}	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSCIN	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V
Supply Current						
RUN	I_{RUN}		-	8	TBD	mA
WAIT	I_{WAIT}		-	3.2	TBD	mA
STOP	I_{STOP}	T_A = 25°C	-	2	TBD	µA
		T_A = -40°C to +125°C	-	10	TBD	µA
I/O Ports Hi-Z Leakage Current: PA0-7, PD0-4, MISO, MOSI, SCK	I_{IL}		-10	±0.01	+10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSCIN, $\overline{VPWIN}$	I_{IN}		-1	.001	+1	µA
Capacitance: (Note 2)	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Powerdown Input Voltage: $\overline{RESET}$, $\overline{IRQ}$, $\overline{VPWIN}$, OSCIN	V_{INPD}	V_{DD} = 0	-0.3	-	7	V

DC Electrical Specifications V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator:						
Input Voltage: V_2, V_3, V_{REF}	V_{IN}		V_{SS}-0.2	-	V_{DD} + 0.02	V
Input Current: V_2, V_3, V_{REF}	I_{IN}		-1	-	+1	µA
Offset Voltage	V_{OFF}		-	20	-	mV
Response	t_R		-	2	-	µs

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS}<(V_{IN} or V_{OUT})<V_{DD}. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}),
2. Includes Ports used as Input/Output Pins, Ports used as Input only Pins; Ports used as Output only Pins.

Control Timing V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Of Operation						
Crystal Option	f_{OSC}		1	-	10	MHz
External Clock Option	f_{OSC}		1	-	10	MHz
Internal Operating Frequency						
Crystal (f_{OSC} ÷ 2)	f_{OP}		0.5	-	5	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}		0.5	-	5	MHz
Cycle Time	t_{CYC}		200	-		ns
Crystal Oscillator Start-up Time for AT-cut Crystal	t_{OXOV}		-	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator)	t_{ILCH}		-	-	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}		1.5	-	-	t_{CYC}
Timer						
Resolution (Note 1)	t_{RES}		4	-	-	t_{CYC}
Input Capture Pulse Width	t_{TH}, t_{TL}		50	-	-	ns
Input Capture Pulse Period	t_{TL}, t_{TL}		(Note 2)			t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}		50			ns
Interrupt Pulse Period	t_{ILIH}		(Note 3)			t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}		35			ns

NOTES:

1. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

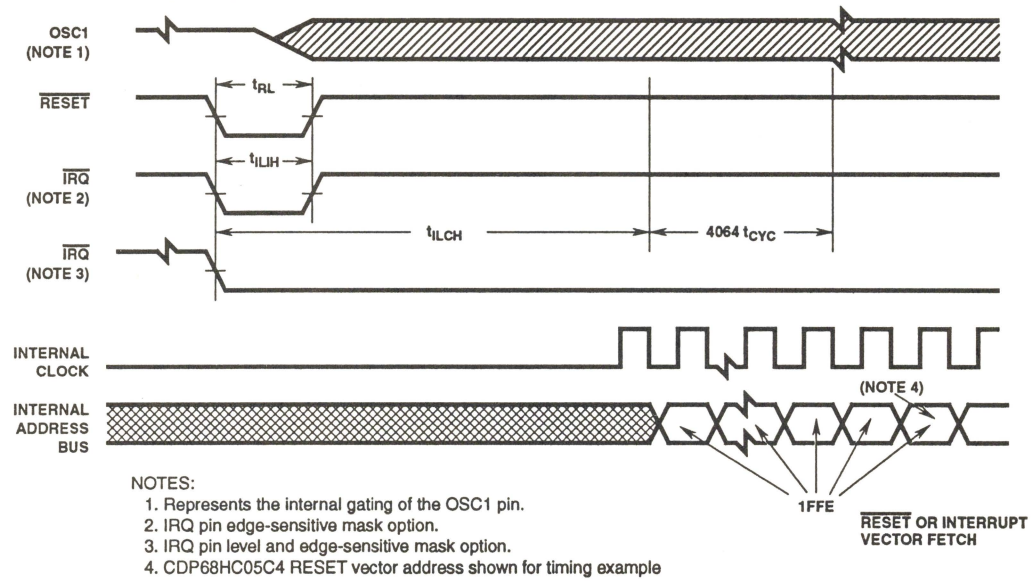
Serial Peripheral Interface (SPI) Timing (See Figure 3) $V_{DD} = 5V_{DC} \pm 10\%$, $V_{SS} = 0V_{DC}$, $T_A = -40°C$ to $+125°C$ Unless Otherwise Specified.

NUMBER	PARAMETER	SYMBOL	MIN	MAX	UNITS
	Operating Frequency				
	Master	$f_{OP(M)}$	0.03	0.5	f_{OP} (Note 3)
	Slave	$f_{OP(S)}$	DC	5	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2	-	t_{CYC}
	Slave	$t_{CYC(S)}$	200	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 1)	-	-
	Slave	$t_{LEAD(S)}$	TBD	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 1)	-	-
	Slave	$t_{LAG(S)}$	TBD	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	TBD	-	ns
	Slave	$t_{W(SCKH)S}$	TBD	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	TBD	-	ns
	Slave	$t_{W(SCKL)S}$	TBD	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	TBD	-	ns
	Slave	$t_{SU(S)}$	TBD	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	TBD	-	ns
	Slave	$t_{H(S)}$	TBD	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	TBD	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	TBD	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	TBD	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 2)	$t_{V(S)}$	-	TBD	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	TBD	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	t_{RSI}	-	TBD	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{R(S)}$	-	TBD	ns
13	Fall Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{F(M)}$	-	TBD	ns
	SPI Inputs (SCK, MOSI,MISO, $\overline{SS}$)	$t_{F(S)}$	-	TBD	ns

NOTES:

1. Signal Production depends on software.
2. Assumes 200pF load on all SPI pins.
3. Note that the units this specification uses is f_{OP} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the devices's internal operating frequency, therefore 2.5MHz maximum.

Control Timing Diagrams



NOTES:
1. Represents the internal gating of the OSC1 pin.
2. IRQ pin edge-sensitive mask option.
3. IRQ pin level and edge-sensitive mask option.
4. CDP68HC05C4 RESET vector address shown for timing example

FIGURE 1. STOP RECOVERY TIMING DIAGRAM

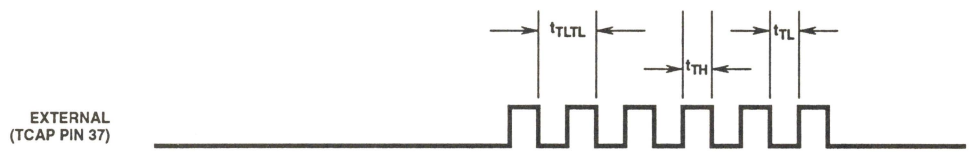


FIGURE 2. TIMER RELATIONSHIPS

Serial Peripheral Interface (SPI) Timing Diagrams

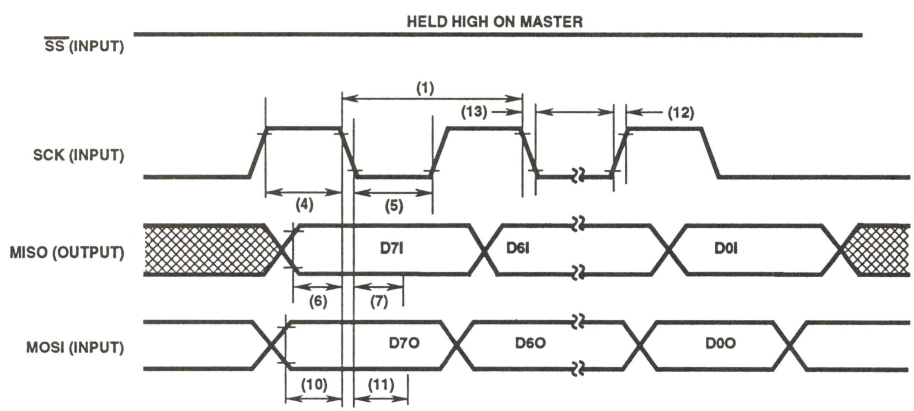
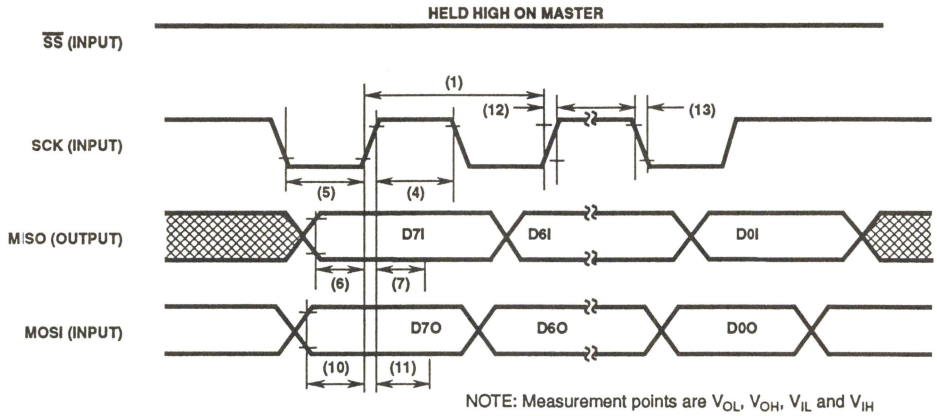


FIGURE 3A. SPI MASTER TIMING CPOL = 0, CPHA =1



NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}

FIGURE 3B. SPI MASTER TIMING CPOL = 1, CPHA = 1

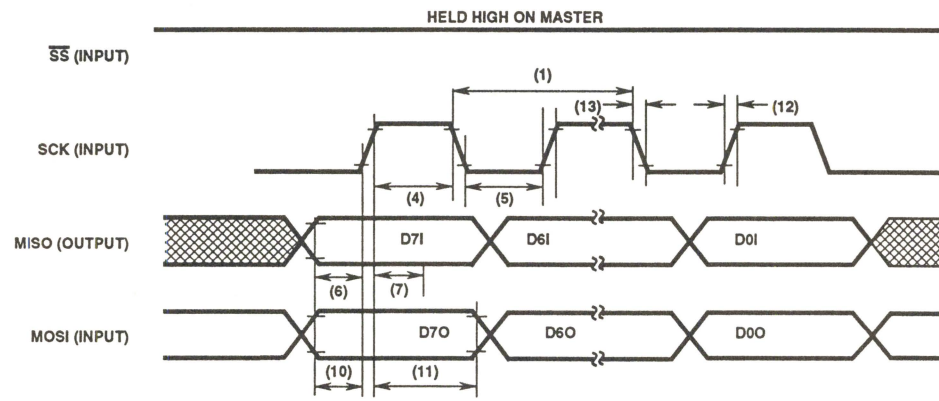
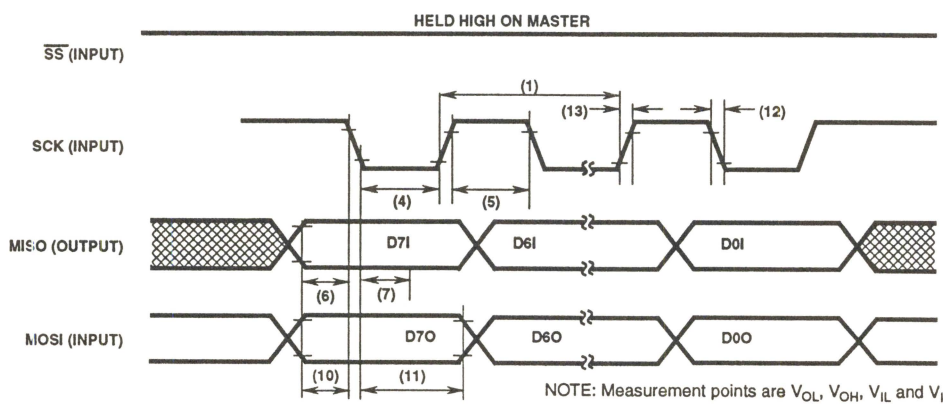


FIGURE 3C. SPI MASTER TIMING CPOL = 0, CPHA = 0



NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}

FIGURE 3D. SPI MASTER TIMING CPOL = 1, CPHA = 0

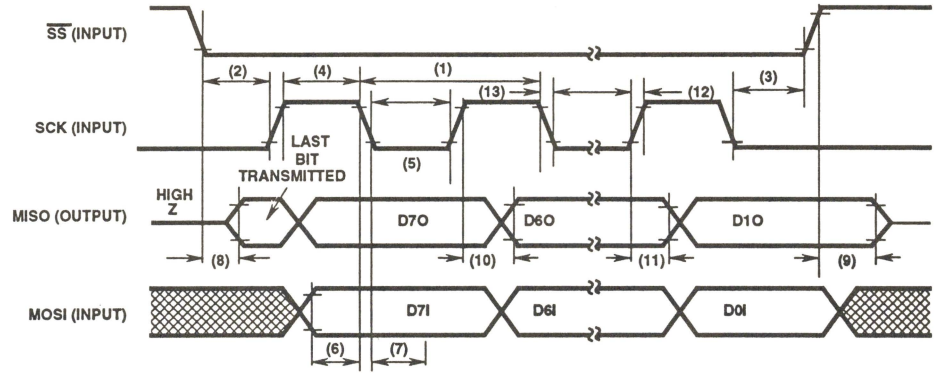
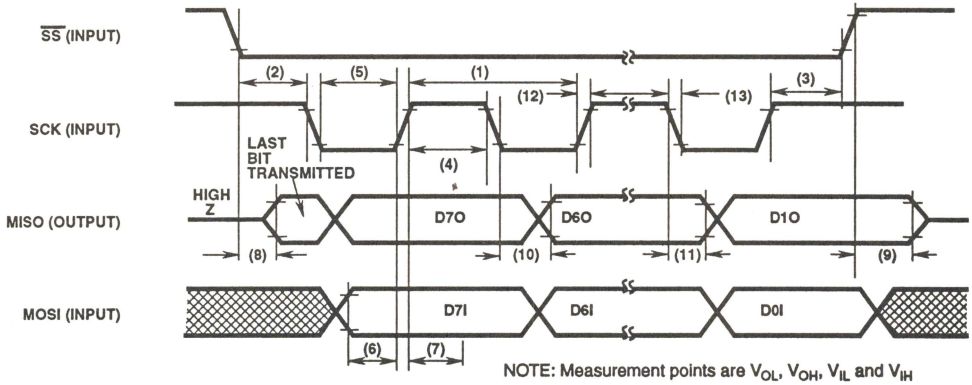


FIGURE 3E. SPI SLAVE TIMING CPOL = 0, CPHA = 1



NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}

FIGURE 3F. SPI SLAVE TIMING CPOL = 1, CPHA = 1

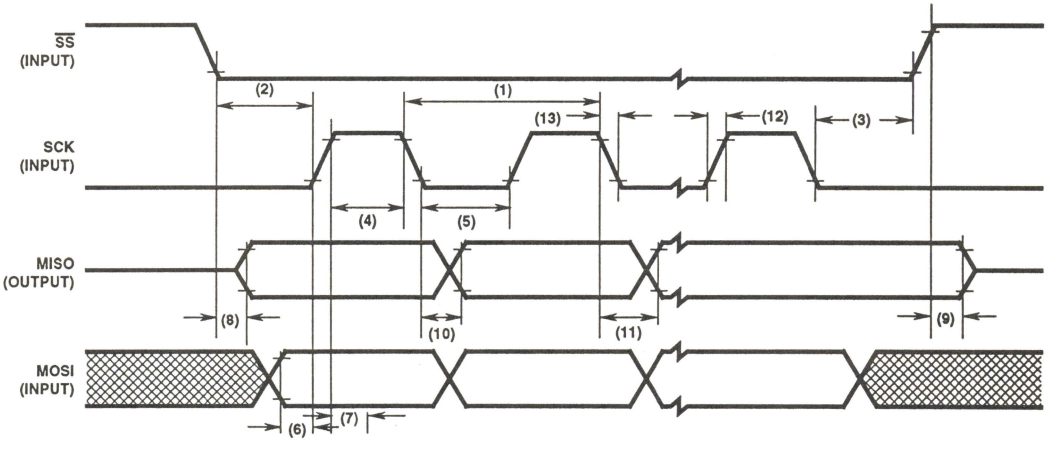
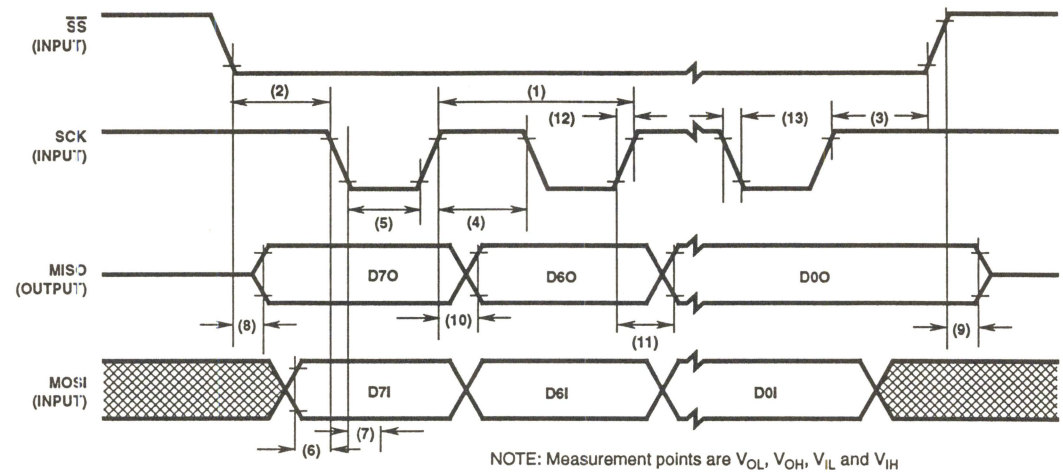


FIGURE 3G. SPI SLAVE TIMING CPOL = 0, CPHA = 0



NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL} and V_{IH}

FIGURE 3H. SPI SLAVE TIMING CPOL = 1, CPHA = 0

FIGURE 3.

Functional Pin Description

This section provides a description of each of the 28 pins of the HIP7030A2 MCU.

V_{DD} and V_{SS} (Power)

Power is supplied to the MCU using these two pins. V_{DD} is connected to the positive supply and V_{SS} is connected to the negative supply.

$\overline{IRQ}$ (Maskable Interrupt Request - Input)

The $\overline{IRQ}$ pin is negative edge-sensitive triggering. A high to low transition on the $\overline{IRQ}$ pin will produce an interrupt.

In the event of an interrupt request, the MCU always completes the current instruction before it responds to the request. An internal mask can be used to inhibit the MCU from responding to IRQ interrupts.

An IRQ interrupt is generated if the $\overline{IRQ}$ pin is pulled low for at least one t_{ILIH}. The occurrence of the low going pulse is registered in a flip-flop and the IRQ interrupt will be recognized even if the $\overline{IRQ}$ pin has returned to a high state before the interrupt can be serviced.

Once the edge-sensitive flip-flop is cleared (it is automatically cleared at the start of the interrupt service routine) the interrupt request is removed until the $\overline{IRQ}$ pin returns to a high level and once again goes low.

See *INTERRUPTS* for more details concerning IRQ interrupts.

$\overline{RESET}$ (Master Reset - Input)

The HIP7030A2 contains an integrated Power-On Reset (POR) circuit and the $\overline{RESET}$ input is therefore not required for start-up. It can be used to reset the MCU internal state and provides for an orderly re-start of the software after initial power-up. Refer to *RESETS* for a detailed description of POR and $\overline{RESET}$.

TCAP (Timer Capture - Input)

The TCAP input controls the input capture feature for the on-chip programmable timer system. The TCAP input is also used as the strobe signal to the Port D strobed outputs. Refer to *Input Capture Register* and *PD0, PD1 Strobed Output Mode* for additional information.

TCMP (Timer Compare - Output)

The TCMP pin provides an output for the output compare feature of the on-chip timer system. Refer to *Output Compare Register* for additional information.

OSCIN (Oscillator Input - Input),
OSCOUT (Oscillator Output - Output),
OSCB (Oscillator Buffered Output - Output)

OSCIN is the input and OSCOUT is the output of an inverter/amplifier which can be used to build either a quartz crystal or ceramic resonator based clock oscillator. Alternatively the OSCIN input can be driven from any external clock source which satisfies the CMOS schmitt trigger input level requirements of the OSCIN pin. See *Electrical Specifications* for input level specification.

OSCB is a squared, buffered version of the OSCIN signal, available for driving one external CMOS load.

The fundamental internal clock is derived by a divide-by-two of the external oscillator frequency (f_{OSC}). All other internal clocks are also derived from the external frequency. These clocks include the input to the 16-bit Timer, the Serial Clock (SCK), and the VPW Symbol Encoder/Decoder (SENDEC).

Quartz Crystal

The circuit shown in Figure 4A is recommended when using a quartz crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal in the frequency range specified for f_{OSC} in *Electrical Specifications*. Figure 4B lists the recommended capacitance and feedback resistance values. Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the OSCIN and OSCOUT pins to minimize output distortion and start-up stabilization time.

Ceramic Resonator

A ceramic resonator may be used in place of the crystal in cost sensitive applications. The circuit in Figure 4A is recommended when using a ceramic resonator. Figure 4C lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

External Clock

If an external clock is used, it should be applied to the OSCIN input with the OSCOUT output not connected, as shown in Figure 4E. The t_{OXOV} or t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV} or t_{ILCH}.

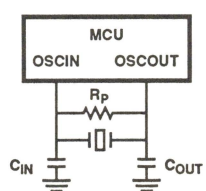


FIGURE 4A. CRYSTAL/RESONATOR CIRCUIT CONNECTIONS

	2MHz	4MHz	8MHz	10MHz	UNITS
R_S (Max)	400	75	TBD	TBD	Ω
C_0	5	7	TBD	TBD	pF
C_1	0.008	0.012	TBD	TBD	µF
C_{IN}	15-40	15-30	12-30	12-30	pF
C_{OUT}	15-30	15-25	12-25	12-25	pF
R_P	1-10	1-10	1-10	1-10	MΩ
Q	30	30	TBD	TBD	K

FIGURE 4B. QUARTZ CRYSTAL PARAMETERS

	2MHz	UNITS
R_S (Typical)	10	Ω
C_0	40	pF
C_1	4	pF
C_{IN}	30	pF
C_{OUT}	30	pF
R_P	2-10	MΩ
Q	1200	

NOTES:

1. When no power is applied to the HIP7030A2, the OSCIN, $\overline{IRQ}$, $\overline{RESET}$, and $\overline{VPWIN}$ pins can have up to 9VDC applied with no side effects.
2. When power is applied to the HIP7030A2, it is recommended that all unused inputs, except Port A and Port D I/O lines configured as outputs, be tied to an appropriate logic level (i.e. - either V_{DD} or V_{SS}).

FIGURE 4C. CERAMIC RESONATOR PARAMETERS

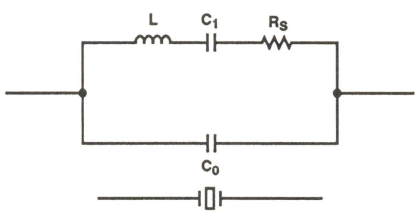


FIGURE 4D. CRYSTAL/RESONATOR EQUIVALENT CIRCUIT

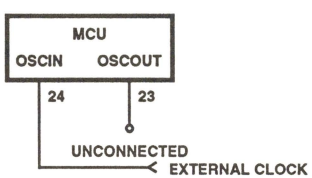


FIGURE 4E. EXTERNAL CLOCK SOURCE CONNECTIONS

FIGURE 4.

PA0-PA7 (Port A - Input/Output)

These eight I/O lines comprise Port A. The mode (i.e. - input or output) of each pin is software programmable. All Port A I/Os are configured as inputs during a POR, COP, or external reset. Refer to *Port A* under *Port A and D I/O Lines* for a detailed description of programming the Port A I/O lines.

PD0-PD4 (Port D - Input/Output)

These five I/O lines comprise Port D. As with PA0-PA7, the mode (i.e. - input or output) of each pin is software programmable. In addition a Special Function Register (SFRD) allows configuring PD0 and PD1 as "strobed" outputs, and/or PD2,PD3, and PD4 as inputs to an on-chip analog comparator.

All Port D I/Os are configured as inputs during a POR, COP, or external reset. Refer to *PD0-PD4 Special Function I/O Lines* under *Port A and D I/O Lines* for a detailed description of programming the Port D I/O lines.

VPWOUT (Variable Pulse Width Out - Output),
$\overline{\text{VPWIN}}$ (Variable Pulse Width In - Input)

These two lines are used to interface to the J1850 bus transceiver.

VPWOUT is the pulse width modulated output of the SENDEC encoder block.

$\overline{\text{VPWIN}}$ is the inverted input to the SENDEC decoder block.

See *VPW Symbol Encoder/Decoder (SENDEC)* for a detailed description of the J1850 interface pins.

MISO (Master-In/Slave-out - Input/Output),
MOSI (Master-out/Slave-In - Input/Output),
SCK (Serial Clock - Input/Output),
$\overline{\text{SS}}$ (Slave Select - Input)

These four lines constitute the Serial Peripheral Interface (SPI) communications port. The MCU can be configured as a SPI "master" or as a SPI "slave". In master mode MOSI and SCK function as outputs and MISO functions as an input. In slave mode MOSI and SCK are inputs and MISO is an output. $\overline{\text{SS}}$ is always an input.

Serial data words are transmitted and received over the MISO/MOSI lines synchronously with the SCK clock stream. The word size is fixed at 8-bits. Single buffering is used which results in an inherent inter-byte delay. The master device always provides the synchronizing clock.

A low on the $\overline{\text{SS}}$ line causes the MCU to immediately assume the role of slave, regardless of it's current mode. This allows multi-master systems to be constructed with appropriate arbitration protocols.

See the detailed discussion of the SPI interface under *Serial Peripheral Interface (SPI).*

Integrated Hardware I/O Functions

PORT A

Each of the Parallel Port pins of Port A may be individually programmed as an input or an output under software control. The direction of each pin is determined by the state of the corresponding bit in the Port A Data Direction Register (DDRA, location $04).

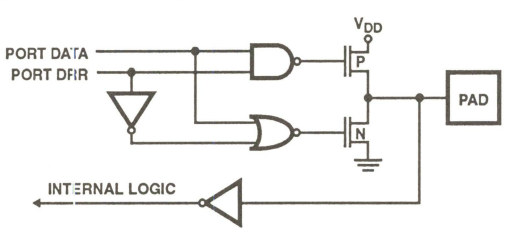


FIGURE 5A. PORT A I/O PAD CIRCUITRY

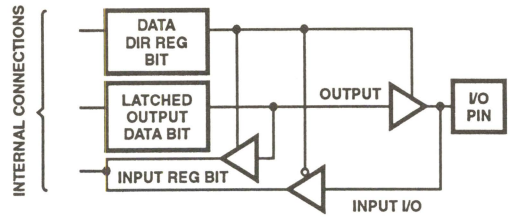


FIGURE 5B. PORT A FUNCTIONAL BLOCK DIAGRAM
FIGURE 5.

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

PORT A DATA DIRECTION REGISTER (DDRA, LOCATION $04)

Any Port A pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. Any reset will clear all DDR bits, which configures all Port A and D pins as inputs. The data direction register is capable of being written to or read by the processor. Refer to Figure 5 and Table 1.

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORT A DATA REGISTER (PORTA, LOCATION $00)

PortA is an 8-bit wide read-write data register. Regardless of the state of the DDRA bits, all Port A data latches are modified with each write to PortA. When PortA is read, the value read for bits programmed as outputs, is the contents of the data latch not the pin. The value read for bits programmed as inputs is the value on the pin.

TABLE 1. PORT A TRUTH TABLE

R/W (NOTE 1)	DDR	I/O PIN FUNCTION
W	0	The I/O pin is in input mode. Data is written into the output data latch
W	1	Data is written into the output data latch and simultaneously output to the I/O pin.
R	0	The state of the I/O pin is read.
R	1	The I/O pin is in output mode. The output data latch is read.

NOTE:

1. R/W is an internal signal which equals R when reading the Port Data Register and equals W when writing the Port Data Register

PD0-PD4 SPECIAL FUNCTION I/O LINES

These five lines comprise Port D. The five lines can be individually programmed to provide input or output capabilities similar to the eight Port A lines. Additionally, each of the lines can be programmed to provide special capabilities, beyond the standard digital input and output functions. The PD0-PD4 I/O lines are controlled via three read/write registers.

7	6	5	4	3	2	1	0
0	0	0	DD4	DD3	DD2	DD1	DD0

PORT D DATA DIRECTION REGISTER (DDRD, LOCATION $07)

DDRD contains five data direction bits, DD0-DD4, which control whether the associated I/O line behaves as an Input or as an Output. Setting a data direction bit causes the related I/O line to be configured as an output, while clearing the bit causes the line to be configured as an input. When configured as an output, the I/O line is actively driven by the HIP7030A2. When configured as an input, the I/O line appears as a high impedance input and should be driven by external circuitry.

DDRD bits D0-D4 are cleared by RESET.

7	6	5	4	3	2	1	0
CMP3	CMP2	0	D4	D3	D2	D1	D0

PORT D DATA REGISTER (PORTD, LOCATION $03)

PortD is an 8-bit wide register with 5 read/write data bits and 2 read-only bits. When writing to PortD, bits 5-7 are ignored. All other bits (D0-D4) are stored in latches until they are explicitly modified with a subsequent write (or read-modify-write) instruction. The utilization of bits D0-D4 is dependent on the value in the associated DDRD bit. If a line is programmed as an input, the value read in PortD (D0-D4) is the logic level present on the external I/O line. If a line is programmed as an output, the value read in PortD (D0-D4) is the value last written to the same bit in PortD and that value is forced onto the corresponding I/O line. The PortD CMP2 and CMP3 read-only input bits indicate the results of the last analog comparisons (see *PD2, PD3, PD4 Analog Comparator Inputs* for details on CMP2 and CMP3). PortD bit 5 is always read as a 0.

PortD is not affected by RESET.

7	6	5	4	3	2	1	0
0	0	CMPE	0	0	0	STE1	STE0

PORT D SPECIAL FUNCTION REGISTER (SFRD, LOCATION $08)

SFRD is an 8 bit wide register with 3 read/write control bits. The Strobe Enable 0 and 1 bits (STE0 and STE1) and used to configure PD0 and PD1 as strobed outputs. STE0 and STE1 only affect PD0 and PD1 when they are programmed as outputs by setting the corresponding bits in DDRD. See *PD0, PD1 Strobed Outputs* for a detailed explanation. The Comparator Enable bit (CMPE) controls the HIP7030A2's auto-zeroing, analog comparator (see *PD2, PD3, PD4 Analog Comparator Inputs* for details on CMPE). SFRD bits 2, 3, 4, 6 and 7 are always read as a 0.

SFRD bit CMPE, is cleared by RESET. All other SFRD bits are unaffected by RESET.

PD0, PD1 Strobed Output Mode

(DD0/DD1) is set, setting the STE0/1 bit configures the PD0/1 output in strobed mode. Clearing the STE0/1 bit causes the PD0/1 output to function identically to a PortA line in output mode. If the DDRD direction bit is clear, the associated line functions as an input and the state of the STE bit has no effect. When programmed as strobed outputs, data written to Port D Data Register bits 0 and 1 will appear on the external PD0 and PD1 pins synchronously with a low to high transition on the TCAP pin. This same transition on TCAP can be programmed to generate an interrupt to the processor. See *Programmable Timer* for details on using the interrupt capabilities of the TCAP pin. The strobed output mode of PD0 and PD1, coupled with the interrupt capability of TCAP, provides a mechanism for synchronously passing two bits of data between the HIP7030A2 and an external, asynchronous device.

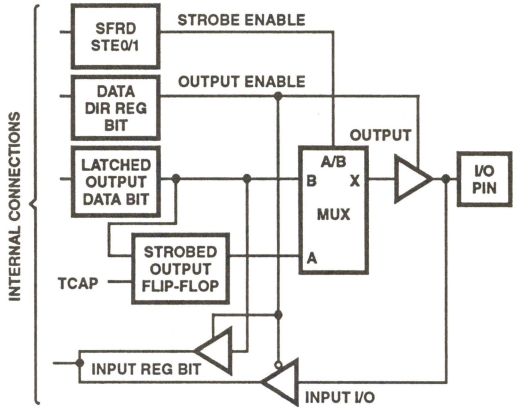


FIGURE 6. STROBED OUTPUT BLOCK DIAGRAM (PD0, PD

STE0 and STE1 are not affected by RESET.

TABLE 2. PORT D STROBED OUTPUTS TRUTH TABLE

R/W (NOTE 1)	DDR	STE	I/O PIN FUNCTION
W	0	X	The I/O pin is in input mode. Data is written into the output data latch.
W	1	0	Data is written into the output data latch and simultaneously output to the I/O pin.
W	1	1	Data is written into the output data latch and transferred to the I/O pin on the next TCAP low to high transition.
R	0	X	The state of the I/O pin is read.
R	1	0	The I/O pin is in standard output mode. The output data latch is read.
R	1	1	The I/O pin is in strobed output mode. The output data latch is read.

NOTE:

1. R/W is an internal signal which equals R when reading the Port Data Register and equals W when writing the Port Data Register

PD2, PD3, PD4 Analog Comparator Input Mode

When the CMPE bit is low in SFRD PD2, PD3, and PD4 behave as standard bidirectional I/O pins. Each of these three pins can be programmed as an input pin by setting the associated DDR bit low. Setting the DDR bit high configures the pin as an output. When CMPE is set high the three pins are connected to the appropriate comparator inputs and the contents of the DDRD doesn't affect comparator operation. While it is possible to perform comparisons of the pins when they are in the output mode (DDR bits are set high) the com-

parator result of comparing two equal digital values is not predictable. The comparator is intended for comparing analog input values, in which case the DDR bits must be set low to configure the pins as inputs. When CMPE is high, all of the associated PortD digital inputs (bits D4, D3, and D2 of PortD) are forced to 0, to conserve power.

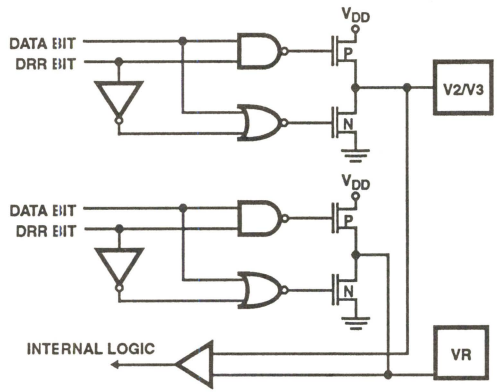


FIGURE 7. ANALOG INPUT I/O PINS

The circuitry of the clocked comparator consists of a differential amplifier with requisite current sources, auto-zero storage elements, and multiplexing switches. It is convenient to view it as a conventional differential comparator to which PD4 is connected as a "reference" at the negative input and PD2 and PD3 are connected via a multiplexer at the positive input. The comparator is enabled be setting the CMPE bit (bit 5) of SFRD and disabled by clearing CMPE. To conserve power the comparator should be disabled when not in use. RESET clears the CMPE bit. The three analog inputs function properly with inputs from -0.3V to V_{DD} +0.3V.

In order to use the comparator, PD4 and either (or both) PD2 or(and) PD3 should be selected as inputs via the DD2, DD3, and DD4 bits in DDRD. The results of the last comparison are available each time the PortD register is read. The CMP2 bit of PortD is set if PD2 was greater than PD4 during the last comparison and cleared otherwise. Similarly, the CMP3 bit of PortD is set if PD3 was greater than PD4 during the last comparison and cleared otherwise. CMP2 and CMP3 are not affected by RESET.

The HIP7030A2 includes a hardware sequencer to control the auto-zero function and input multiplexer of the comparator. Each complete compare cycle consists of a series of:

1. Auto Zero
2. Compare V2, write results to CMP2
3. Auto Zero
4. Compare V3, write results to CMP3

The hardware sequencer is enabled via the CMPE bit. Once enabled the compare cycling is performed continuously at a 1MHz step rate until CMPE is set low. A complete cycle takes 4µs. It follows that, at any given time, the results read in CMP2 or CMP3 of the PortD Data Register can be, at most,4µs old.

The auto-zero operation involves charging a pair of bias capacitors. The charging time depends on the source impedance of the analog inputs, the relative voltages of V2 and V3, and the slew rate of all three input voltages. Incomplete charging of the capacitors will affect the accuracy of the comparator. The comparator is intended to perform favorably with input impedances up to 10kΩ and moderate slew rates.

J1850 BUS INTERFACE

The VPW Symbol Encoder/Decoder (SENDEC) block provides the designed with all the features needed to send and received properly timed messages on a J1850 Class B Multiplexed Bus. Refer to *VPW Symbol Encoder/Decoder (SENDEC)* for detailed documentation on the use of the SENDEC.

16-BIT TIMER

The integrated 16-bit Timer includes both capture and compare features. External events can be timed, pulses generated, and periodic interrupts programmed. A sophisticated set of control and status registers allows interrupt or polled operation. For a detailed guide to the operation of the Timer refer to *Programmable Timer.*

SERIAL PERIPHERAL INTERFACE(SPI)

The serial peripheral interface (SPI) is a synchronous serial interface with separate input, output, and clock lines. The SPI uses the MISO (serial data input/output), MOSI (serial data output/input), SCK (serial clock), and $\overline{SS}$ (slave select) pins. Refer to *Serial Peripheral Interface* for a detailed discussion of the SPI system.

Memory Organization

The HIP7030A2 MCU is capable of addressing 8192 bytes of memory and I/O registers with its program counter. The MCU has implemented 2520 bytes of these locations as shown in Figure 8. The first 256 bytes of memory (page zero) include: 24 bytes of I/O features such as data ports, the port DDRs, Timer, serial peripheral interface (SPI), and J1850 VPW Registers; 48 bytes of user ROM, and 176 bytes of RAM. The next 2048 bytes complete the user ROM. The Built-In-Test ROM (228 bytes) and Built-In-Test vectors (14 bytes) are contained in memory locations $1F00 through $1FF1. The 14 highest address bytes contain the user defined reset and the interrupt vectors. Eight bytes of the lowest 32 memory locations are unused and the 176 bytes of user RAM include up to 64 bytes for the stack. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage.

CPU Registers

The CPU contains five registers, as shown in the programming model of Figure 9. The interrupt stacking order is shown in Figure 10.

ACCUMULATOR (A)

The accumulator is an 8-Bit general purpose register used to hold operands, results of the arithmetic calculations, and data manipulations.

INDEX REGISTER (X)

The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit value which is used to create an effective address. The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations.

PROGRAM COUNTER (PC)

The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor.

STACK POINTER (SP)

The stack pointer is a 13-bit register containing the address of the next free locations on the pushdown/popup stack. When accessing memory, the most significant bits are permanently configured to 0000011. These bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a reset stack pointer (RSP) instruction, the stack pointer is set to its upper limit ($00FF). Nested interrupt and/or subroutines may use up to 64 (decimal) locations. When the 64 locations are exceeded, the stack pointer wraps around and points to its upper limit ($00FF), thus, losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five RAM bytes.

Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. Each bit is explained in the following paragraphs.

Half Carry Bit (H)

The H bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in binary coded decimal subroutines.

Interrupt Mask Bit (I)

When the I bit is set, all interrupts are disabled. Clearing this bit enables the interrupts. If an external interrupt occurs while the I bit is set, the interrupt is latched and processed after the I bit is next cleared; therefore, no interrupts are lost because of the I bit being set. An internal interrupt can be lost if it is cleared while the I bit is set (refer to Programmable Timer, Serial Communications Interface, and Serial Peripheral Interface Sections for more information).

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logic one).

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is zero.

Carry/Borrow (C)

Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

Built-In-Test (BIT)

The Built-In-Test (BIT) capability of the HIP7030A2 MCU provides a simple, efficient means to test the device functionality. The BIT mode is entered by applying a $9V_{DC}$ input (through a 4.7KΩ resistor) to the $\overline{IRQ}$ pin and $5V_{DC}$ input (through a 4.7KΩ resistor) to the TCAP pin and then depressing the reset switch to execute a RESET. After RESET, the MCU will begin executing the BIT code stored at locations $1F00-$1FF1. The COP system remains active during BIT.

The BIT routines utilizes the SPI capability of the HIP7030A2. When the BIT is initially accessed the SPI is configured in slave mode and the routine waits for a command to be received via the SPI. There are five defined commands:

Download and Execute - Command 1($01)

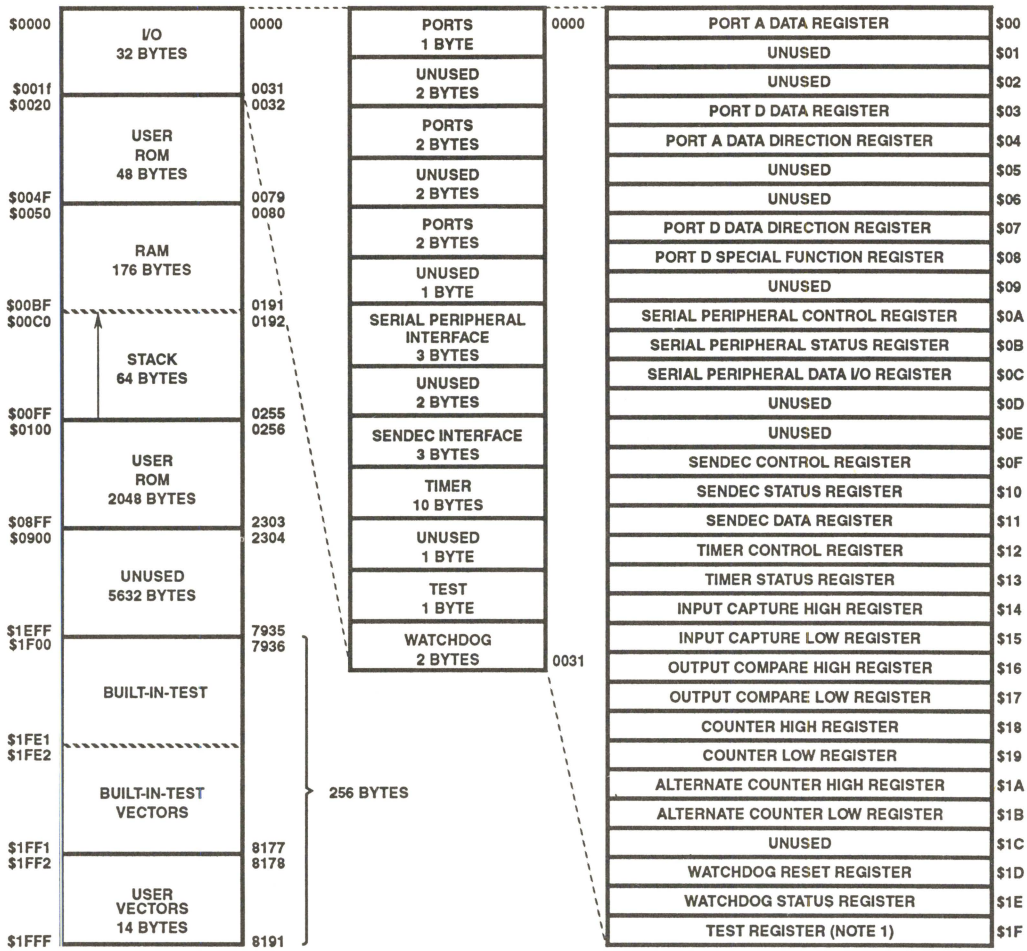
Fill RAM with data and begin execution at location $62. After receiving a $01 command, the BIT routines read the next 176 bytes of data received via the SPI and place each byte in successive RAM locations beginning at location $50. The SPI master is responsible for pacing the transmission to allow the HIP7030A2 to process each received byte. XXX clocks are required between transfers. Once all 176 bytes are received the HIP7030A2 jumps to location $62 and begins execution. SP is cleared before jumping to $62. Returning to the BIT routine can be accomplished by branching to location $1F00.

Dump ROM - Command 2($02)

After receiving a $02 command, the BIT software "dumps" the contents of ROM. Beginning with locations $0020 through $003F, followed by locations $0100 through $08FF, and ending with locations $1F00 through $1FFF the ROM contents are transferred byte by byte on the SPI bus. The HIP7030A2 remains in slave mode, and the master is responsible for pacing the transmission to allow the HIP7030A2 to retrieve each ROM byte. XXX clocks are required between transfers. After all bytes have been transferred the BIT software once again waits for a command.

Read Page 0 - Command 3($03)

After receiving a $03 command, the BIT software waits for an address byte to be received. The address points to a location on page 0, the contents of which are read and placed in the SPI data register for transfer to the master. After receiving the command and address bytes and placing the value read in the SPI register, the BIT routines wait for



NOTE:
1. Accessible In Test Mode Only

FIGURE 8. MEMORY MAP OF THE HIP7030A2

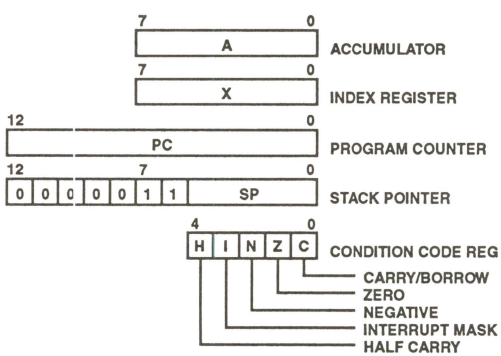


FIGURE 9. CPU REGISTER SET

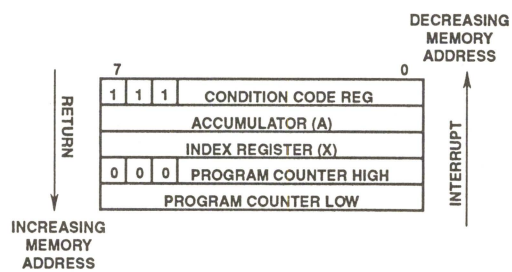


FIGURE 10. STACKING ORDER DURING INTERRUPTS

the data to be transferred and then resume looking for a command. The master is responsible for pacing the transmission to allow the HIP7030A2 time to read the data byte. XXX clocks are required between transfers.

Read/Write Page 0 - Command 4($04)

After receiving a $04 command, the BIT software waits for an address byte to be received. The address points to a location on page 0, the contents of which are read and placed in the SPI data register for transfer to the master. After receiving the command and address bytes and placing the value read in the SPI register, the BIT routines wait for the master to send a data byte (and to simultaneously unload the data which was placed in the SPDR). Upon receiving the new data byte, the BIT program writes the new data to the selected page 0 location. After completing the write, the BIT routines resume looking for a command. The master is responsible for pacing the transmission to allow the HIP7030A2 to properly process the address and data bytes. XXX clocks are required between transfers. Writing to the upper 20 bytes of RAM (subroutine stack) or to the SPI registers can cause the BIT routine to malfunction.

Checksum - Command 5($05)

After receiving a $05 command, the BIT software calculates the checksum of all bytes in ROM space and places the result in the SPI data register for reading. The master is responsible for pacing the transmissions to allow the HIP7030A2 to properly calculate the checksum byte. XXX clocks are required between issuing the command and reading the result.

Resets

The MCU has three reset modes: an active low external reset pin ($\overline{\text{RESET}}$), a power-on reset function, and a Computer Operating Properly (COP) reset function.

$\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one and one half t_{CYC}. The $\overline{\text{RESET}}$ pin contains an internal Schmitt Trigger as part of its input to improve noise immunity.

Power-On Reset

The power-on reset occurs when a positive transition is detected on VDD. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides for a 4064 t_{CYC} delay from the time that the oscillator becomes active to allow for stabilization (see Figure 11). If the external $\overline{\text{RESET}}$ pin is low at the end of the 4064 t_{CYC} time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high. Table 3 shows the actions of the two resets on internal circuits, but not necessarily in order of occurrence (X indicates that the condition occurs for the particular reset).

COP Reset

The COP reset is generated by either of two events: 1) the Watchdog Timer reaches its maximum value prior to being cleared, or 2) the Slow Clock Detect circuitry doesn't detect a transition on the OSCIN pin during a period of approximately 2µs. The COP reset is identical to an external $\overline{\text{RESET}}$ pin reset, except the Program Counter is loaded with the address at $1FFA-$1FFB instead of the address at $1FFE-$1FFF and the Watchdog Flag (bit 0) is set in the Watchdog Status Register (WSR, location $1E). COP Resets are discussed under Interrupts.

Interrupts

Systems often require that normal processing be interrupted so that some external event may be serviced. The HIP7030A2 may be interrupted by one of six different methods: either one of four maskable hardware interrupts ($\overline{\text{IRQ}}$, SPI, SENDEC, or Timer), one non-maskable Watchdog/Slow Clock Detect interrupt, and one non-maskable software interrupt (SWI). Interrupts such as Timer, SPI, and SENDEC have several flags which will cause the interrupt. Generally, interrupt flags are located in read-only status register, whereas their equivalent enable bits are located in associated control registers. The interrupt flags and enable bits are never contained in the same register. If the enable bit is a logic zero it blocks the interrupt from occurring but does not inhibit the flag from being set. Reset clears all enable bits to preclude interrupts during the reset procedure. The general sequence for clearing an interrupt is a software sequence of first accessing the status register while the interrupt flag is set, followed by a read or write of an associated register. When any of these interrupts occur, and if the enable bit is a logic one, normal processing is suspended at the end of the current instruction execution. Interrupts cause the processor registers to be saved on the stack (see Figure 12) and the interrupt mask (I bit) set to prevent additional interrupts. The appropriate interrupt vector then points to the starting address of the interrupt service routine (refer to Table 4 for vector location). Upon completion of the interrupt service routine, the RTI instruction (which is normally a part of the service routine) causes the register contents to be recovered from the stack followed by a return to normal processing. The stack order is shown in Figure 12.

NOTE: The interrupt mask bit (I bit) will be cleared if and only if the corresponding bit stored in the stack is zero. A discussion of interrupts, plus a table listing vector addresses for all interrupts including RESET, in the MCU is provided in Table 4.

Hardware Controlled Interrupt Sequence

The following three functions (RESET, STOP, and WAIT) are not in the strictest sense an interrupt; however, they are acted upon in a similar manner. Flowcharts for hardware interrupts are shown in Figure 13, and for STOP and WAIT are provided in Figure 14. A discussion is provided below.

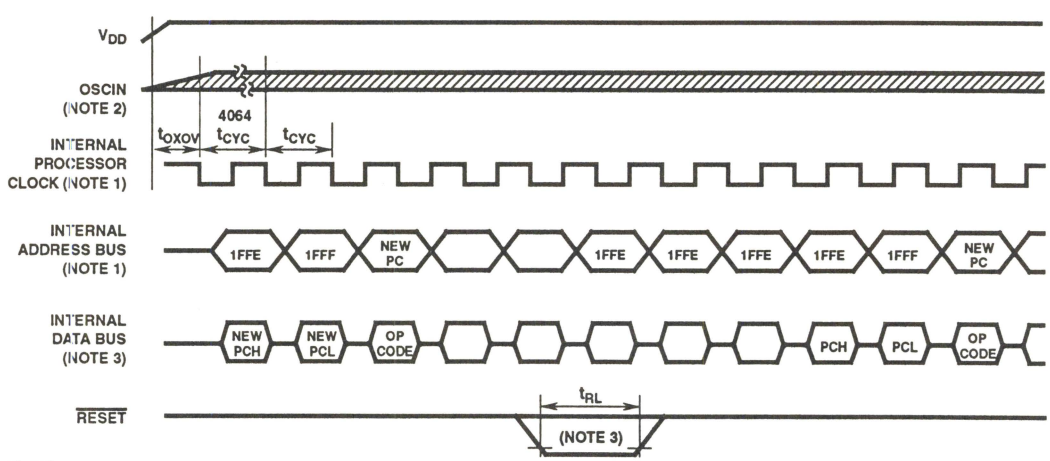
(a) **RESET** - A low input on the $\overline{\text{RESET}}$ input pin causes the program to vector to its starting address which is specified by the contents of memory locations $1FFE and $1FFF. The I bit in the condition code register is also set. Much of the

TABLE 3. $\overline{\text{RESET}}$ PIN, COP, AND POR ACTIONS ON INTERNAL CIRCUITRY

CONDITION	$\overline{\text{RESET}}$ PIN/ COP RESET	POWER-ON RESET
Timer Prescaler Reset to Zero State	X	X
Timer Counter Configure to $FFFC	X	X
Timer Output Compare (TCMP) Bit Reset to Zero	X	X
All Timer Interrupt Enable Bits Cleared (ICIE, OCIE, and TOIE) to Disable Timer Interrupts	X	X
Timer Output Level (OLVL) Bit is Cleared	X	X
Port A and Port D Data Direction Registers (DDRA and DDRD) Cleared to Zero, Placing all Port Pins in Input Mode	X	X
Port D Special Function Register Bit CMPE is Cleared Disabling Comparator	X	X
Set Stack Pointer (SP) to $00FF	X	X
Force Internal Address to RESET Vector ($1FFE)	X	X
Set I Bit in Condition Code Register (CC) to 1; Disabling all Maskable Interrupts	X	X
Clear STOP Latch	X	X
Clear WAIT Latch	X	X
Reset Oscillator Stabilization Delay To 4064	(Note 1)	X
Clear External Interrupt (Irq) Flip-flop	X	X
VPWOUT Set Low (passive state)	X	X
Slow Clock Detect Circuitry Reset	(Note 1)	X
Watchdog Timer Reset to Zero State	X	X
Watchdog Flag (WDF) Cleared/Set in Watchdog Status Register (WSR)	(Note 2)	(Note 2)
Watchdog Timer Interrupt Latch Cleared	X	X
Serial Peripheral Interface (SPI) Control Bits SPIE, MSTR, SPIF, WCOL, and MODF Cleared; Disabling SPI Interrupts and Setting to Slave Mode	X	X

NOTES:

1. Only if MCU is in STOP state; if NDEL is set in the SENDEC Control Register a delay of 128 is used for $\overline{\text{RESET}}$/COP.
2. WDF is cleared by POR and $\overline{\text{RESET}}$ and is set by a Watchdog Reset.



NOTES:

1. Internal signal and bus information is not available externally.
2. OSCIN is not mean to represent frequency. It is only mean to represent time.
3. The next rising edge of the internal processor clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

FIGURE 11. POWER-ON RESET AND $\overline{\text{RESET}}$

TABLE 4. VECTOR ADDRESSES FOR INTERRUPTS AND RESETS

REGISTER	FLAG NAME	INTERRUPTS SOURCE	INTERRUPT NAME	VECTOR ADDRESS
N/A	N/A	RESET	RESET	$1FFE-$1FFF
N/A	N/A	Software	SWI	$1FFC-$1FFD
N/A	N/A	Watchdog Timeout	COP	$1FFA-$1FFB
		Slow Clock Detect		
SENDEC Status (SEDSR)	TX	Transition Detected	SENDEC	$1FF8-$1FF9
	BRK	Break Detected		
	NEW	IFS or SOF		
	NECHO	Echo Failure		
N/A	N/A	External Interrupt	IRQ	$1FF6-$1FF7
TIMER Status (TSR)	ICF	Input Capture	TIMER	$1FF4-$1FF5
	OCF	Output Compare		
	TOF	Timer Overflow		
SPI Status (SPSR)	SPIF	Transfer Complete	SPI	$1FF2-$1FF3
	MODF	Mode Fault		

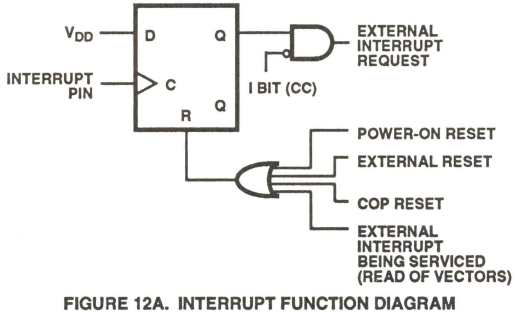


FIGURE 12A. INTERRUPT FUNCTION DIAGRAM

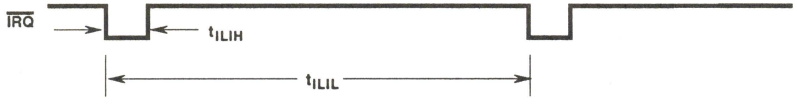


FIGURE 12B. INTERRUPT TIMING DIAGRAM

FIGURE 12. EXTERNAL INTERRUPT

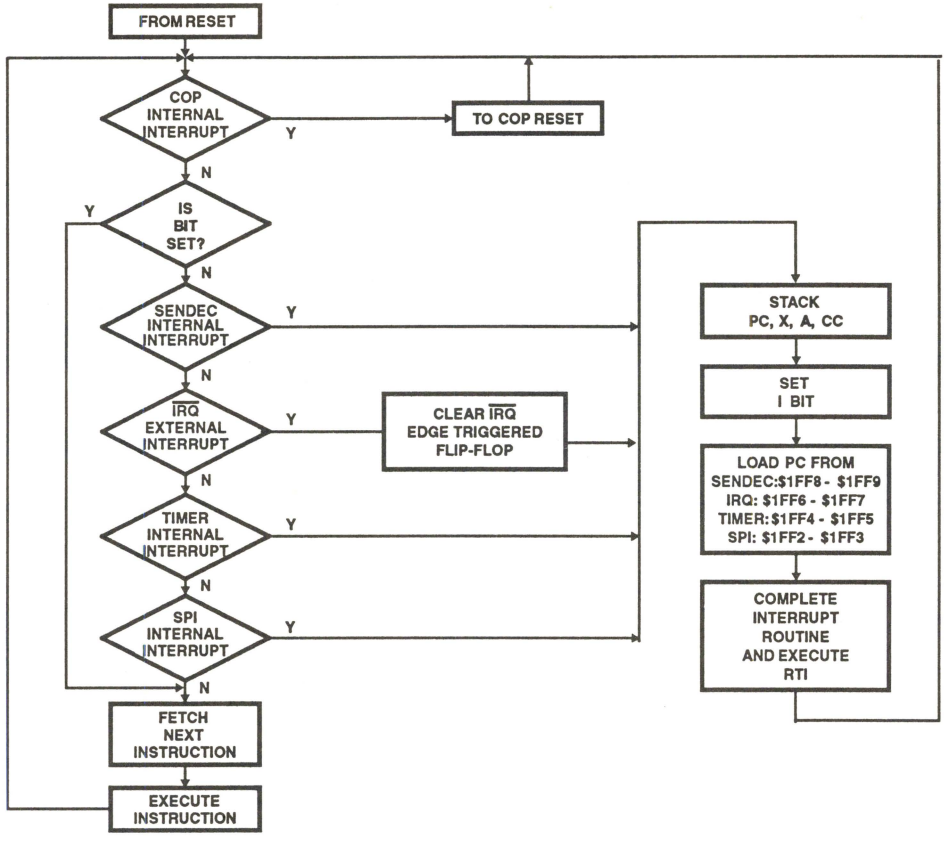


FIGURE 13. HARDWARE INTERRUPT FLOW DIAGRAM

MCU is configured to a known state during this type of reset as previously described in RESETS paragraph.

(b) **STOP** - The STOP instruction causes the oscillator to be turned off and the processor to "sleep" until an external interrupt (IRQ) or reset occurs. The VPWOUT pin is forced to a low level, the SPI is set to slave mode, and all other pins remain at their previously set levels.

(c) **WAIT** - The WAIT instruction causes all processor clocks to stop, but leaves the Timer, the Watchdog, SENDEC, and SPI clocks running. This "rest" state of the processor can be cleared by RESET, Slow Clock Detect, an external interrupt (IRQ), Timer interrupt, SPI interrupt, or SENDEC interrupt. There are no special "wait mode" vectors for these interrupts.

Software Interrupt (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask (I bit) in the condition code register. The interrupt service routine address is specified by the contents of memory location $1FFC and $1FFD.

COP Interrupt/Reset

The Computer Operating Properly (COP) system consists of two functions: 1) the Watchdog Timer, and 2) the Slow Clock Detect Circuit. These interrupts cause a complete system restart and the effect is identical in every respect to an externally generated $\overline{\text{RESET}}$ pin reset, except the restart address is taken from locations $1FFA and $1FFB and the Watchdog Flag (bit 0) is set in the Watchdog Status Register (WSR, location $1E) if the reset was the result of a Watchdog Timer overflow. Starting the PC with an address different than the standard RESET address allows the system to provide an appropriate response to the situation.

Because the CPU is reset during a COP Interrupt, the COP service routine must not exit with an RTI. Instead the routine should branch to subsequent code.

Since the most likely cause of a Slow Clock Detect is a malfunctioning oscillator, a COP Interrupt caused by a Slow Clock Detect will generally reset the MCU per Table 3 and remain in the RESET state.

SENDEC Interrupt

The VPW Symbol Encoder/Decoder (SENDEC) system has four different interrupt flags that will cause a SENDEC interrupt whenever they are set and enabled. These four interrupt flags are found in the SENDEC status register (SEDSR, location $10) and all will vector to the same interrupt service routine ($1FF8 - $1FF9). One of the interrupt flags (TX - transition) has a corresponding enable bit in the SENDEC control register (SEDCR, location $0F). RESET clears the enable bit, thus preventing a TX interrupt from occurring during the reset time period. The other three interrupts (BRK - break, NECHO - no echo, and NEW - new frame) are nonmaskable at the SENDEC level. The processor responds to all SENDEC interrupts only if the I bit in the condition code register is also cleared. When the interrupt is recognized, the current machine state is pushed onto the stack and I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $1FF8 and $1FF9. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to VPW Symbol Encoder/Decoder (SENDEC) for additional information about the SENDEC interrupts.

External Interrupt

If the interrupt mask (I bit) of the condition code register has been cleared and the external interrupt pin ($\overline{IRQ}$) has gone low, then an external interrupt is recognized. When the interrupt is recognized, the current state of the CPU is pushed onto the stack and the I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $1FF6 and $1FF7. Figure 12 shows both a functional and mode timing diagram for the interrupt line. The timing diagram shows treatment of the interrupt line ($\overline{IRQ}$) for generating periodic interrupts to the processor. The figure shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles (for interrupt call and return delays). Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs).

The internal interrupt latch is cleared in the first part of the service routine; therefore, one (and only one) external interrupt pulse can be latched during t_{ILIL} and will be serviced as soon as the I bit is cleared.

Timer Interrupt

There are three different timer interrupt flags that will cause a timer interrupt whenever they are set and enabled. These three interrupt flags are found in the three most significant bits of the timer status register (TSR, location $13) and all three will vector to the same interrupt service routine ($1FF4 - $1FF5). All interrupt flags have corresponding enable bits (ICIE, OCIE, and TOIE) in the timer control register (TCR, location $12). Reset clears all enable bits, thus preventing an interrupt from occurring during the reset time period. The actual processor interrupt is generated only if the I bit in the condition code register is also cleared. When the interrupt is recognized, the current machine state is pushed onto the stack and I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $1FF4 and $1FF5. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to Programmable Timer for additional information about the timer circuitry.

Serial Peripheral Interface (SPI) Interrupts

An interrupt in the serial peripheral interface (SPI) occurs when one of the interrupt flag bits in the serial peripheral status register (location $0B) is set, provided the I bit in the condition code register is clear and the enable bit in the serial peripheral control register (location $0A) is enabled. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I bit in the condition code register is set. This masks further interrupts until the present one is serviced. The SPI interrupt causes the program counter to vector to memory location $1FF2 and $1FF3 which contain the starting address of the interrupt service routine. Software in the serial peripheral interrupt service routine must determine the priority and cause of the SPI interrupt by examining the interrupt flag bits located in the SPI status register. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to Serial Peripheral Interface for a description of the SPI system and its interrupts.

Low Power Modes

STOP Instruction

The STOP instruction places the MCU in its lowest power consumption mode. In the STOP mode the internal oscillator is turned off, causing all internal processing to be halted; refer to Figure 14. During the STOP mode, the I bit in the condition code register is automatically cleared to enable external and SENDEC interrupts. All other registers and memory remain unaltered and all input/output lines remain unchanged, except the VPWOUT line which is forced to a passive (low) state and the SPI Master bit (MSTR) in the SPI Control Register (SPCR) which is cleared placing the SPI pins into Slave mode. This mode persists until an external interrupt (IRQ), a low on the VPWIN pin, or a low on $\overline{RESET}$ is sensed at which time the internal oscillator is turned on. The interrupt or reset causes the program counter to vector to the starting address of the interrupt or reset service routine respectively.

WAIT Instruction

The WAIT instruction places the MCU in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock remains active, and all CPU processing is stopped; however, the programmable timer, serial peripheral interface, Watchdog Timer, and SENDEC systems remain active. Refer to Figure 14. During the WAIT mode, the I bit in the condition code register is cleared to enable all interrupts. All other registers and memory remain unaltered and all parallel input/output lines remain unchanged. This continues until any interrupt or reset is sensed. At this time the pro-

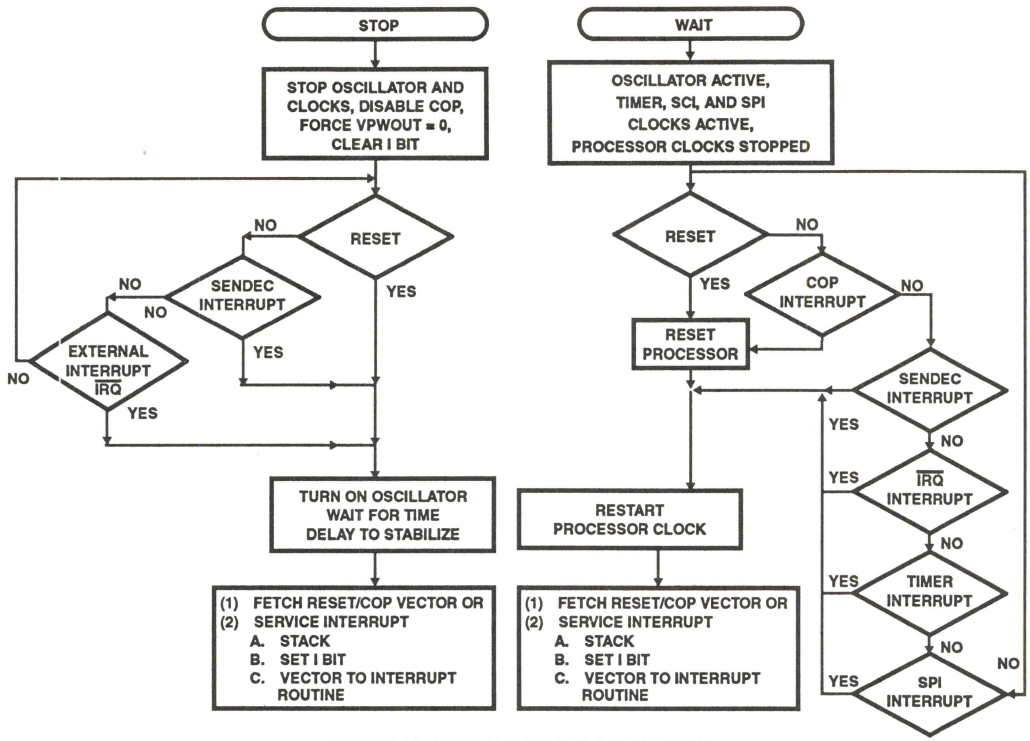


FIGURE 14. STOP AND WAIT FLOW DIAGRAM

gram counter vectors to the memory location ($1FF2 through $1FFF) which contains the starting address of the interrupt or reset service routine.

Data Retention Mode

The contents of RAM and CPU registers are retained at supply voltages as low as $2V_{DC}$. This is referred to as the DATA RETENTION mode, where the data is held, but the device is not guaranteed to operate.

Programmable Timer

INTRODUCTION

The programmable timer, which is preceded by a fixed divide-by-four prescaler, can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. A block diagram of the timer is shown in Figure 15 and timing diagrams are shown in Figure 16 through 19. Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

The I bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur. This prevents interrupts from occurring between the time that the high and low bytes are accessed.

The programmable timer capabilities are provided by using the following ten addressable 8-bit registers (note the high and low represent the significance of the byte). A description of each register is provided below.

Timer Control Register (TCR) locations $12, Timer Status Register (TSR) location $13, Input Capture High Register location $14, Input Capture Low Register location $15, Output Compare High Register location $16, Output Compare Low Register location $17, Counter High Register location $18, Counter Low Register location $19, Alternate Counter High Register location $1A, and Alternate Counter Low Register location $1B.

COUNTER

The key element in the programmable timer is a 16-bit free running counter, or counter register, preceded by a prescaler which divides the internal processor clock by four. The prescaler gives the timer a resolution of 800ns if the internal processor clock is 5.0MHz. the counter is clocked to increasing values during the low portion of the internal processor clock. Software can read the counter at any time without affecting its value.

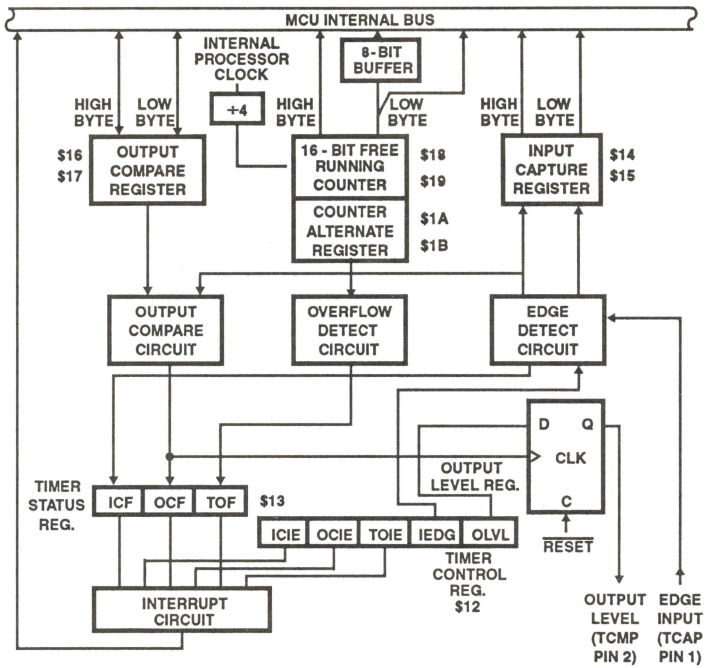
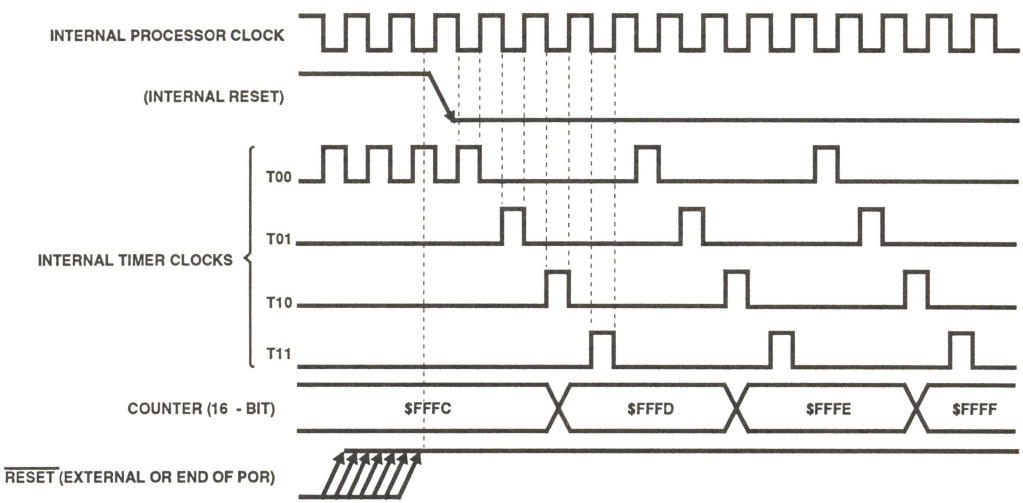


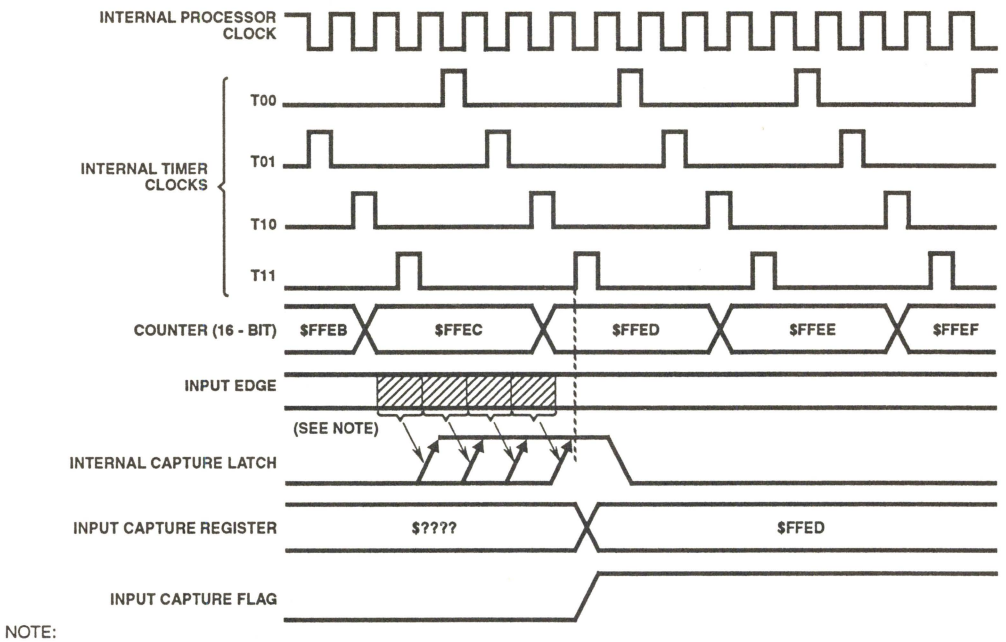
FIGURE 15. PROGRAMMABLE TIMER BLOCK DIAGRAM



NOTE:

1. The Counter Register and the Timer Control Register are the only ones affected by reset.

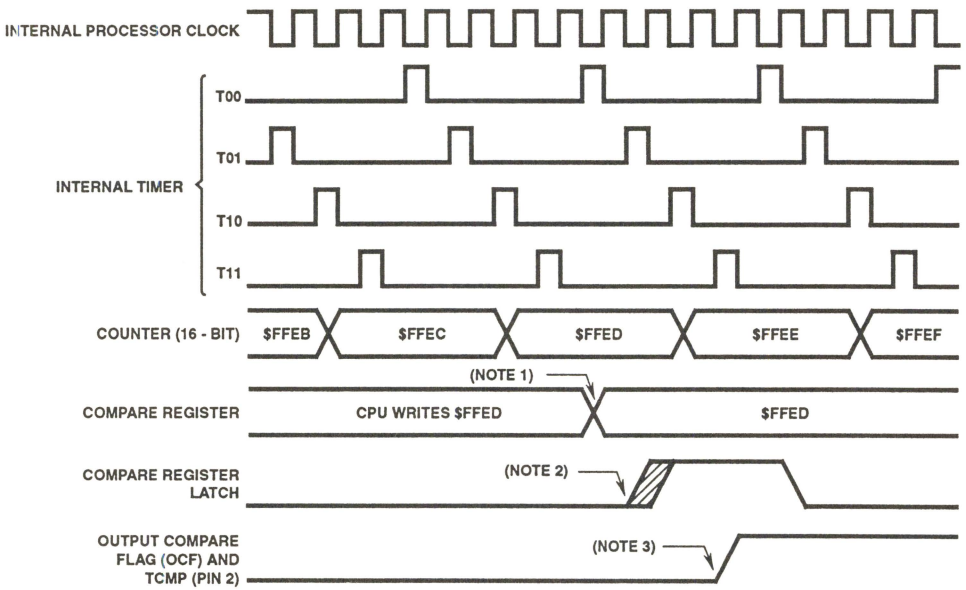
FIGURE 16. TIMER STATE DIAGRAM FOR RESET



NOTE:

1. If the input edge occurs in the shaded area from one timer state T10 to the next, the input capture flag is set during the next T11.

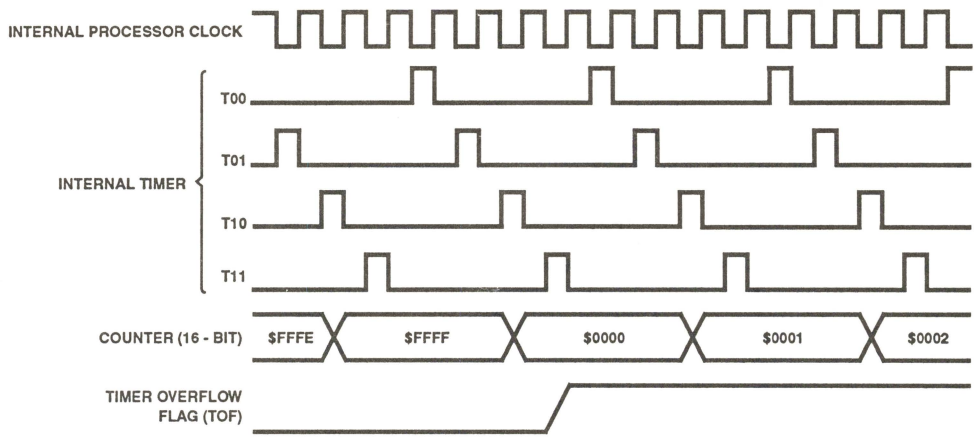
FIGURE 17. TIMER STATE DIAGRAM FOR INPUT CAPTURE



NOTES:

1. The CPU write to the Compare Register may take place at any time, but a compare only occurs at timer state T01. Thus a 4 cycle difference may exist between the write to the Compare Register and the actual compare.
2. Internal compare takes place during timer state T01.
3. OCF is set at the timer state T11 which follows the comparison match ($FFED in this example).

FIGURE 18. TIMER STATE DIAGRAM FOR OUTPUT COMPARE



NOTE:

1. The TOF bit is set at timer state T11 (transition of the counter from $FFFF to $0000). It is cleared by a read of the Timer Status Register during the internal processor clock high time followed by a read of the Counter Low Register.

FIGURE 19. TIMER STATE DIAGRAM FOR TIMER OVERFLOW

The double byte free running counter can be read from either of two locations $18 - $19 (called counter register at this location), or $1A - $1B (counter alternate register at this location). A read of only the least significant byte (LSB) of the free running counter ($19, $1B) retrieves the current count value. If a read of the free running counter first addresses the most significant byte ($18, $1A) the least significant byte is transferred to a buffer. This buffer value remains fixed after the first most significant byte "read" even if the user reads the most significant byte several times. This buffer is accessed when reading the LSB of the free running counter or counter alternate register ($19, $1B), if the most significant byte is read, the least significant byte must also be read in order to complete the sequence.

The free running counter is configured to $FFFC during reset and is always a read-only register. During a power-on-reset (POR), the counter is also configured to $FFFC and begins running after the oscillator start-up delay. Because the free running counter is 16 bits preceded by a fixed divide-by-four prescaler, the value in the free running counter repeats every 262,144 MPU internal processor clock cycles. When the counter rolls over from $FFFF to $0000, the timer overflow flag (TOF) bit is set. An interrupt can also be enabled when counter rollover occurs by setting its interrupt enable bit (TOIE).

OUTPUT COMPARE REGISTER

The output compare register is a 16-bit register, which is made up of two 8-bit registers at locations $16 (most significant byte) and $17 (least significant byte). The output compare register can be used for several purposes such as, controlling an output waveform or indicating when a period of time has elapsed. The output compare register is unique in that all bits are readable and writable and are not altered by the timer hardware. Reset does not affect the contents of this register and if the compare function is not utilized, the two bytes of the output compare register can be used as storage locations.

The contents of the output compare register are compared with the contents of the free running counter once during every four internal processor clocks. If a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked (by the output compare circuit pulse) to an output level register. The values in the output compare register and the output level bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit, OCIE, is set.

After a processor write cycle to the output compare register containing the most significant byte ($16), the output compare function is inhibited until the least significant byte ($17) is also written. The user must write both bytes (locations) if the most significant byte is written first. A write made only to the least significant byte ($17) will not inhibit the compare function. The free running counter is updated every four internal processor clock cycles due to the internal prescaler. The minimum time required to update the output compare register is a function of the software program rather than the internal hardware.

A processor write may be made to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

Because neither the output compare flag (OCF bit) nor the output compare register is affected by RESET, care must be exercised when initializing the output compare function with software. The following procedure is recommended:

1. Write the high byte of the output compare register to inhibit further compares until the low byte is written.
2. Read the timer status register to arm the OCF if it is already set.
3. Write the output compare register low byte to enable the output compare function with the flag clear.

The advantage of this procedure is to prevent the OCF bit from being set between the time it is read and the write to the output compare register. A software example is shown below.

```
B716  STA OCMPHI;   INHIBIT OUTPUT COMPARE
B613  LDA TSTAT;    ARM OCF BIT IF SET
BF17  STX OCMPLO;   READY FOR NEXT COMPARE
```

INPUT CAPTURE REGISTER

The two 8-bit registers which make up the 16-bit input capture register are read-only and are used to latch the value of the free running counter after a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). The selected edge is also fed to the Port D strobed output pins (see Port D Strobed Output Mode). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free running counter on the rising edge of the internal processor clock preceding the external transition (refer to timing diagram shown in Figure 17). This delay is required for internal synchronization. Resolution is affected by the prescaler allowing the timer to only increment every four internal processor clock cycles.

After a read of the most significant byte of the input capture register ($14), counter transfer is inhibited until the least significant byte ($15) of the input capture register is also read. This characteristic forces the minimum pulse period attainable to be determined by the time used in the capture software routine and its interaction with the main program. The free running counter increments every four internal processor clock cycles due to the prescaler.

A read of the least significant byte ($15) of the input capture register does not inhibit the free running counter transfer. Again, minimum pulse periods are ones which allow software to read the least significant byte ($15) and perform needed operations. There is no conflict between the read of the input capture register and the free running counter transfer since they occur on opposite edges of the internal processor clock.

TIMER CONTROL REGISTER (TCR)

The timer control register (TCR, location $12) is an 8-bit read/write register which contains five control bits. Three of these bits control interrupts associated with each of the three flag bits found in the timer status register (discussed below). The other two bits control: 1) which edge is significant to the capture edge detector (i.e., negative or positive), and 2) the next value to be clocked to the output level register in response to a successful output compare. The timer control register and the free running counter are the only sections of the timer affected by RESET. The TCMP pin is forced low during external reset and stays low until a valid compare changes it to a high. The timer control register is illustrated below followed by a definition of each bit.

7	6	5	4	3	2	1	0
ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL

TCR (LOCATION $12)

B7, ICIE — If the input capture interrupt enable (ICIE) bit is set, a timer interrupt is enabled when the ICF status flag (in the timer status register) is set. If the ICIE bit is clear, the interrupt is inhibited. The ICIE bit is cleared by RESET.

B6, OCIE — If the output compare interrupt enable (OCIE) bit is set, a timer interrupt is enabled whenever the OCF status flag is set. If the OCIE bit is clear, the interrupt is inhibited. The OCIE bit is cleared by RESET.

B5, TOIE — If the timer overflow interrupt enable (TOIE) bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set. If the TOIE bit is clear, the interrupt is inhibited. The TOIE bit is cleared by RESET.

B1, IEDG — The value of the input edge (IEDG) bit determines which level transition on pin 1 will trigger a free running counter transfer to the input capture register. Reset does not affect the IEDG bit.

0 = negative edge

1 = positive edge

B0, OLVL — The value of the output level (OLVL) bit is clocked into the output level register by the next successful output compare and will appear at pin 2. This bit and the output level register are cleared by RESET.

0 = low output

1 = high output

TIMER STATUS REGISTER (TSR)

The timer status register (TSR) is an 8-bit register of which the three most significant bits contain read-only status information. These three bits indicate the following:

1. A proper transition has taken place at the TCAP pin with an accompanying transfer of the free running counter contents to the input capture register,
2. A match has been found between the free running counter and the output compare register, and
3. A free running counter transition from $FFFF to $0000 has been sensed (timer overflow).

The timer status register is illustrated below followed by a definition of each bit. Refer to timing diagrams shown in Figures 13, 14, and 15 for timing relationship to the timer status register bits.

7	6	5	4	3	2	1	0
ICF	OCF	TOF	0	0	0	0	0

TSR (LOCATION $13)

B7, ICF — The input capture flag (ICF) is set when a proper edge has been sensed by the input capture edge detector. It is cleared by a processor access of the timer status register (with ICF set) followed by accessing the low byte ($15) of the input capture register. Reset does not affect the input compare flag.

B6, OCF The output compare flag (OCF) is set when the output compare register contents match the contents of the free running counter. The OCF is cleared by accessing the timer status register (with OCF set) and then accessing the low byte ($17) of the output compare register. Reset does not affect the output compare flag.

B5, TOF The timer overflow flag (TOF) bit is set by a transition of the free running counter from $FFFF to $0000. It is cleared by accessing the timer status register (with TOF set) followed by an access of the free running counter least significant byte ($19). Reset does not affect the TOF bit.

Accessing the timer status register satisfies the first condition required to clear any status bits which happen to be set during the access. The only remaining step is to provide an access of the register which is associated with the status bit. Typically, this presents no problem for the input capture and output compare functions.

A problem can occur when using the timer overflow function and reading the free running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if: 1) the timer status register is read or written when TOF is set, and 2) the least significant byte of the free running counter is read but not for the purpose of servicing the flag. The counter alternate register at address $1A and $1B contains the same value as the free running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

During STOP and WAIT instructions, the programmable timer functions as follows: during the wait mode, the timer continues to operate normally and may generate an interrupt to trigger the CPU out of the wait state; during the stop mode, the timer holds at its current state, retaining all data, and resumes operation from this point when an external interrupt is received.

Serial Peripherial Interface (SPI)

INTRODUCTION

The serial peripheral interface (SPI) is an interface built into the MCU which allows several MCUs, or one MCU plus peripheral devices, to be interconnected within a single "black box" or on the same printed circuit board. In a serial peripheral interface (SPI), separate wires (signals) are required for data and clock. In the SPI format, the clock is not included in the data stream and must be furnished as a separate signal. An SPI system may be configured as one containing one master MCU and several slave MCUs, or in a system in which an MCU is capable of being either a master or a slave.

Figure 20 illustrates a typical multi-computer system configuration. Figure 20 represents a system of five different MCUs in which there are one master and four slave (0, 1, 2, 3). In this system four basic line (signals) are required for the MOSI (master out slave in), MISO (master in slave out), SCK serial clock, and $\overline{SS}$ (slave select) lines.

FEATURES

- Full Duplex, Three-wire Synchronous Transfers
- Master or Slave Operation
- Master Bit Frequency - 2.5MHz Maximum
- Slave Bit Frequency - 5.0MHz Maximum
- Four Programmable Master Bit Rates
- Programmable Clock Polarity And Phase
- End Of Transmission Interrupt Flag
- Write Collision Flag Protection
- Master-master Mode Fault Protection Capability

SIGNAL DESCRIPTION

The four basic signals (MOSI, MISO, SCK, $\overline{SS}$) discussed above are described in the following paragraphs. Each signal function is described for both the master and slave mode.

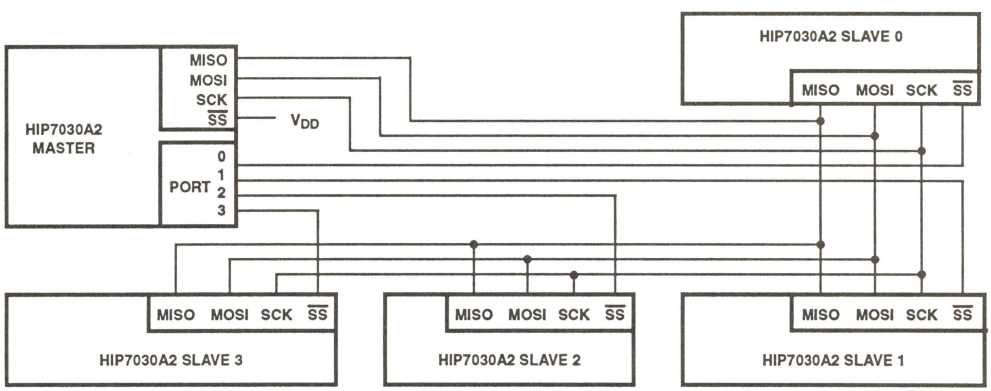


FIGURE 20. MASTER-SLAVE SYSTEM CONFIGURATION (SINGLE MASTER, FOUR SLAVES)

Master Out Slave In (MOSI)

The MOSI pin is configured as a data output in a master (mode) device and as a data input in a slave (mode) device. In this manner data is transferred serially from a master to a slave on this line; most significant bit first, least significant bit last. The timing diagrams of Figure 21 summarize the SPI timing and show the relationship between data and clock (SCK). As shown in Figure 21, four possible timing relationships may be chosen by using control bits CPOL and CPHA. The master device always allows data to be applied on the MOSI line a half-cycle before the clock edge (SCK) in order for the slave device to latch the data.

NOTE: Both the slave device(s) and a master device must be programmed to similar timing modes for proper data transfer.

When the master device transmits data to a second (slave) device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) is used to signify that the I/O operation is complete. Configuration of the MOSI pin is a function of the MSTR bit in the serial peripheral control register (SPCR, location $0A). When a device is operating as a master, the MOSI pin is an output because the program in firmware sets the MSTR bit to a logic one.

Master In Slave Out (MISO)

The MISO pin is configured as an input in a master (mode) device and as an output in a slave (mode) device. In this manner data is transferred serially from a slave to a master on this line; most significant bit first, least significant bit last. The MISO pin of a slave device is placed in the high-impedance state if it is not selected by the master; i.e., its $\overline{SS}$ pin is a logic one. The timing diagram of Figure 21 shows the relationship between data and clock (SCK). As shown in Figure 21, four possible timing relationships may be chosen by using control bits CPOL and CPHA. The master device always allows data to be applied on the MOSI line a half-cycle before the clock edge (SCK) in order for the slave device to latch the data.

NOTE: The slave device(s) and a master device must be programmed to similar timing modes for proper data transfer.

When the master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) in the serial peripheral status register (SPSR, location $0B) is used to signify that the I/O operation is complete.

In the master device, the MSTR control bit in the serial peripheral control register (SPCR, location $0A) is set to a logic one (by the program) to allow the master device to receive data on its MISO pin. In the slave device, its MISO pin is enable by the logic level of the $\overline{SS}$ pin; i.e., if $\overline{SS}$ = 1 then the MISO pin is placed in the high-impedance state, whereas, if $\overline{SS}$ = 0 the MISO pin is an output for the slave device.

Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) pin is a fixed input, which receives an active low signal that is generated by the master device to enable slave device(s) to accept data. To ensure that data will be accepted by a slave device, the $\overline{SS}$ signal line must be a logic low prior to occurrence of SCK (system clock) and must remain low until after the last (eighth) SCK cycle. Figure 21 illustrates the relationship between SCK and the data for two different level combinations of CPHA, when $\overline{SS}$ is pulled low. These are: 1) with CPHA = 1, the first bit of data is applied to the MISO line for transfer ($\overline{SS}$ must go high between successive characters), and 2) when CPHA = 0 the slave device is prevented from writing to its data register ($\overline{SS}$ can remain low between characters). Refer to the WCOL

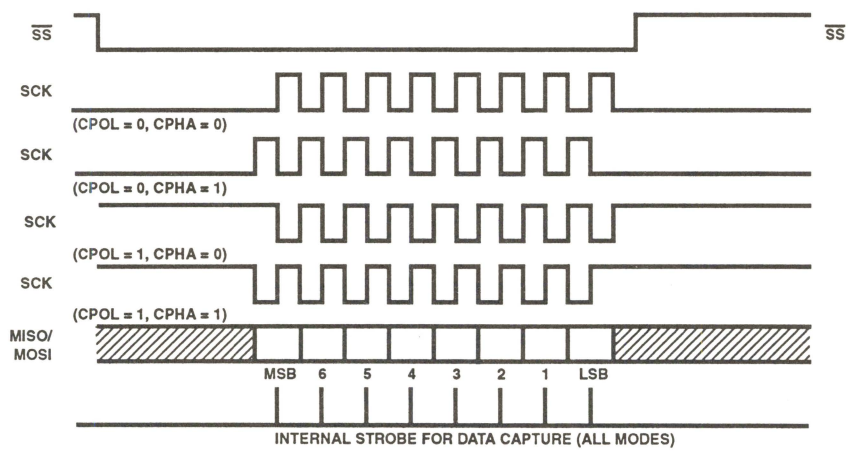


FIGURE 21. DATA CLOCK TIMING DIAGRAM

status flag in the serial peripheral status register (location $0B) description for further information on the effects that the $\overline{SS}$ input and CPHA control bit have on the I/O data register. A high level $\overline{SS}$ signal forces the MISO (master in slave out) line to the high-impedance state. Also, SCK and the MOSI (master out slave in) line are ignored by a slave device when its $\overline{SS}$ signal is high.

When a device is a master, it constantly monitors its $\overline{SS}$ signal input for a logic low. The master device will become a slave device any time its $\overline{SS}$ signal input is detected low. This ensures that there is only one master controlling the $\overline{SS}$ line for a particular system. When the $\overline{SS}$ line is detected low, it clears the MSTR control bit (serial peripheral control register, location $0A). Also, control bit SPE in the serial peripheral control register is cleared which causes the serial peripheral interface (SPI) to be disabled (port D SPI pins become inputs). The MODF flag bit in the serial peripheral status register (location $0B) is also set to indicate to the master device that another device is attempting to become a master. Two devices attempting to be outputs are normally the result of a software error; however, a system could be configured which would contain a default master which would automatically "take-over" and restart the system.

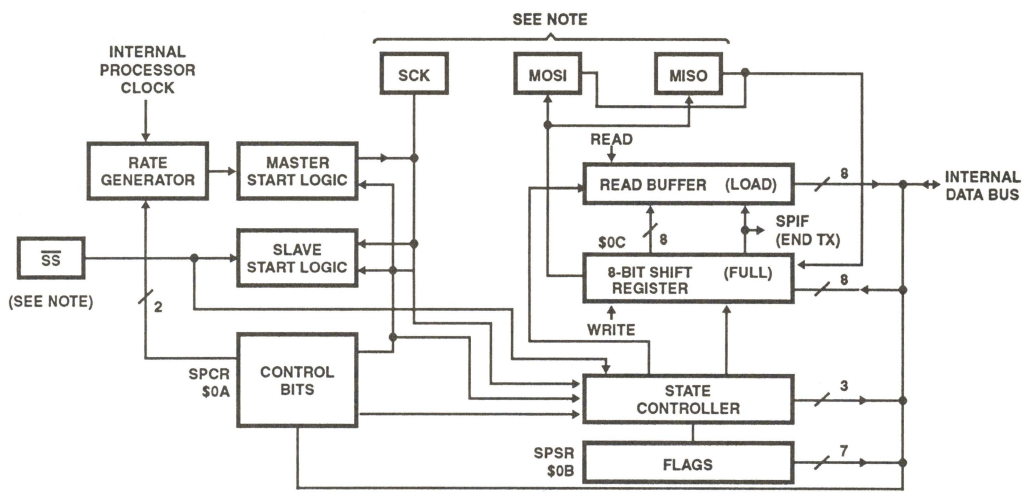
Serial Clock (SCK)

The serial clock is used to synchronize the movement of data both in and out of the device through its MOSI and MISO pins. The master and slave devices are capable of exchanging a data byte of information during a sequence of eight clock pulses. Since the SCK is generated by the master device, the SCK line becomes an input on all slave devices and synchronizes slave data transfer. The type of clock and it relationship to data are controlled by the CPOL and CPHA bits in the serial peripheral control register (location $0A) discussed below. Refer to Figure 21 for timing.

The master device generates the SCK through a circuit driven by the internal processor clock. Two bits (SPR0 and SPR1) in the serial peripheral control register (location $0A) of the master device select the clock rate. The master device uses the SCK to latch incoming slave device data on the MISO line and shifts out data to the slave device on the MOSI line. Both master and slave devices must be operated in the same timing mode as controlled by the CPOL and CPHA bit in the serial peripheral control register. In the slave device, SPR0, SPR1 have no effect on the operation of the serial peripheral interface. Timing is shown in Figure 21.

Functional Description

A block diagram of the serial peripheral interface (SPI) is shown in Figure 22. In a master configuration, the master start logic receives an input from the CPU (in the form of a write to the SPI rate generator) and originates the system clock (SCK) based on the internal processor clock. This clock is also used internally to control the state controller as well as the 8-bit shift register. As a master device, data is parallel loaded into the 8-bit shift register (from the internal bus) during a write cycle, data is applied serially from a slave device via the MISO pin to the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to



NOTES: The $\overline{SS}$, SCK, MOSI, and MISO are external pins which provide the following functions:

1. MOSI - Provides serial output to slave unit(s) when device is configured as a master. Receives serial input from master unit when device is configured as a slave unit.
2. MISO - Provides serial input from slave unit(s) when device is configured as a master. Receives serial output to master unit when device is configured as a slave unit.
3. SCK - Provides system clock when device is configured as a master. Receives system clock when device is configured as a slave unit.
4. $\overline{SS}$ - Provides a logic low to select device for a transfer with the master.

FIGURE 22. SERIAL PERIPHERAL INTERFACE (SPI) BLOCK DIAGRAM

the read buffer and then is made available to the internal data bus during a CPU read cycle.

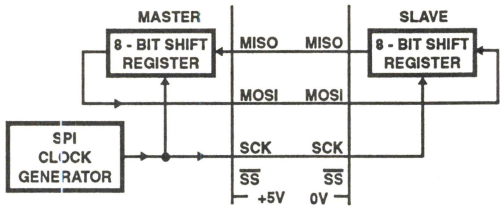


FIGURE 23. SERIAL PERIPHERAL INTERFACE (SPI) MASTER-SLAVE INTERCONNECTION

In a slave configuration, the slave start logic receives a logic low (from a master device) at the $\overline{SS}$ pin and a system clock input (from the same master device) at the SCK pin. Thus, the slave is synchronized with the master. Data from the master is received serially at the slave MOSI pin and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer and then is made available to the internal data bus during a CPU read cycle. During a write cycle, data is parallel loaded into the 8-bit shift register from the internal data bus and then shifted out serially to the MISO pin for application to the master device.

Figure 23 illustrates the MOSI, MISO, and SCK master-slave interconnections. Note that in Figure 23 the master $\overline{SS}$ pin is tied to a logic high and the slave $\overline{SS}$ pin is a logic low. Figure 20 provides a larger system connection for these same pins. Note that in Figure 20, all $\overline{SS}$ pins are connected to a port pin of a master/slave device. In this case any of the devices can be a slave.

Registers

There are three register in the serial parallel interface which provide control, status, and data storage functions. These registers which include the serial peripheral control register (SPCR, location $0A), serial peripheral status register (SPSR, location $0B), and serial peripheral data I/O register (SPDR, location $0C) are described below.

Serial Peripheral Control Register (SPCR)

The serial peripheral control register bits are defined as follows:

7	6	5	4	3	2	1	0
SPIE	SPE	-	MSTR	CPOL	CPHA	SPR1	SPR0

SPCR (LOCATION $0A)

B7, SPIE — When the serial peripheral interrupt enable is high, it allows the occurrence of a processor interrupt, and forces the proper vector to be loaded into the program counter if the serial peripheral status register flag bit (SPIF and/or MODE) is set to a logic one. It does not inhibit the setting of a status bit. The SPIE bit is cleared by RESET.

B6, SPE — When the serial peripheral output enable control bit is set, all output drive is applied to the external pins and the system is enabled. When the SPE bit is set, it enables the SPI system by connecting it to the external pins thus allowing it to interface with the external SPI bus. The pins that are defined as output depend on which mode (master or slave) the device is in. When SPE is low all pins appear as inputs to the external system. Because the SPE bit is cleared by RESET, the SPI system is not connected to the external pins upon RESET.

B4, MSTR — The master bit determines whether the device is a master or a slave. If the MSTR bit is a logic zero it indicates a slave device and a logic one denotes a master device. If the master mode is selected, the function of the SCK pin changes from an input to an output and the function of the MISO and MOSI pins are reversed. This allows the user to wire device pins MISO to MISO, and MOSI to MOSI, and SCK to SCK without incident. The MSTR bit is cleared by RESET; therefore, the device is always placed in the slave mode during RESET.

B3, CPOL — The clock polarity bit controls the normal or steady state value of the clock when data is not being transferred. The CPOL bit affects both the master and slave modes. It must be used in conjunction with the clock phase control bit (CPHA) to produce the wanted clock-data relationship between a master and a slave device. When the CPOL bit is a logic zero, it produces a steady state low value at the SCK pin of the master device. If the CPOL bit is a logic one, a high value is produced at the SCK pin of the master device when data is not being transferred. The CPOL bit is not affected by RESET. Refer to Figure 21.

B2, CPHA — The clock phase bit controls the relationship between the data on the MISO and MOSI pins and the clock produced or received at the SCK pin. This control has effect in both the master and slave modes. It must be used in conjunction with the clock polarity control bit (CPOL) to produce the wanted clock-data relation. The CPHA bit in general selects the clock edge which captures data and allows it to change states. It has its greatest impact on the first bit transmitted (MSB) in that it does or does not allow a clock transition before the first data capture edge. The CPHA bit is not affected by RESET. Refer to Figure 21.

B1, SPR1
B0, SPR0 — These two serial peripheral rate bits select one of four baud rates to used as SCK if the device is a master; however they have no effect in the slave mode. The slave device is capable of shifting data in and out at a maximum rate which is equal to the CPU clock. A rate table is given below for the generation of the SCK from the master. The SPR1 and SPR0 bits are not affected by RESET.

SPR1	SPR0	INTERNAL PROCESSOR CLOCK DIVIDE BY
0	0	2
0	1	4
1	0	16
1	1	32

Serial Peripheral Status Register (SPSR)

The status flags which generate a serial peripheral interface (SPI) interrupt may be blocked by the SPIE control bit in the serial peripheral control register. The WCOL bit does not cause an interrupt. The serial peripheral status register bits are defined as follows:

7	6	5	4	3	2	1	0
SPIF	WCOL	0	MODF	0	0	0	0

SPSR (LOCATION $0B)

B7, SPIF The serial peripheral data transfer flag bit notifies the user that a data transfer between the device and an external device has been completed. With the completion of the data transfer, SPIF is set, and if SPIE is set, a serial peripheral interrupt (SPI) is generated. During the clock cycle that SPIF is being set, a copy of the received data byte in the shift register is moved to a buffer. When the data register is read, it is the buffer that is read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not responded to the first SPIF, only the first byte sent is contained in the receiver buffer and all other bytes are lost.

The transfer of data is initiated by the master device writing its serial peripheral data register.

Clearing the SPIF bit is accomplished by a software sequence of accessing the serial peripheral status register while SPIF is set and followed by a write to or a read of the serial peripheral data register. While SPIF is set, all writes to the serial peripheral data register are inhibited until the serial peripheral status register is read. This occurs in the master device. In the slave device, SPIF can be cleared (using a similar sequence) during a second transmission; however, it must be cleared before the second SPIF in order to prevent an overrun condition. The SPIF bit is cleared by RESET.

B 6 , WCOL The function of the write collision status bit is to notify the user that an attempt was made to write the serial peripheral data register while a data transfer was taking place with an external device. The transfer continues uninterrupted; therefore, a write will be unsuccessful. A "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation. If a "write collision" occurs, WCOL is set but no SPI interrupt is generated. The WCOL bit is a status flag only.

Clearing the WCOL bit is accomplished by a software sequence of accessing the serial peripheral status register while WCOL is set, followed by 1) a read of the serial peripheral data register prior to the SPIF bit being set, or 2) a read or write of the serial peripheral data register after the SPIF bit is set. A write to the serial peripheral data register (SPDR) prior to the SPIF bit being set, will result in generation of another WCOL status flag. Both the SPIF and WCOL bits will be cleared in the same sequence. If a second transfer has started while trying to clear (the previously set) SPIF and WCOL bits with a clearing sequence containing a write to the serial peripheral data register, only the SPIF bit will be cleared.

A collision of a write to the serial peripheral data register while an external data transfer is taking place can occur in both the master mode and the slave mode, although with proper programming the master device should have sufficient information to preclude this collision.

Collision in the master device is defined as a write of the serial peripheral data register while the internal rate clock (SCK) is in the process of transfer. The signal on the $\overline{SS}$ pin is always high on the master device.

A collision in a slave device is defined in two separate modes. One problem arises in a slave device when the CPHA control bit is a logic zero. When CPHA is a logic zero, data is latched with the occurrence of the first clock transition. The slave device does not have any way of knowing when that transition will occur; therefore, the slave device collision occurs when it attempts to write the serial peripheral data register after its SS pin has been pulled low. The $\overline{SS}$ pin of the slave device freezes the data in its serial peripheral data register and does not allow it to be altered if the CPHA bit is a logic zero. The master device must raise the $\overline{SS}$ pin of the slave device high between each byte it transfers to the slave device.

The second collision mode is defined for the state of the CPHA control bit being a logic one. With the CPHA bit set, the slave device will be receiving a clock (SCK) edge prior to the latch of the first data transfer. This first clock edge will freeze the data in the slave device I/O register and allow the MSB onto the external MISO pin of the slave device. The $\overline{SS}$ pin low state enables the slave device but the drive onto the MISO pin does not take place until the first data transfer clock edge. The WCOL bit will only be set if the I/O register is accessed while a transfer is taking place. By definition of the second collision mode, a master device might hold a slave device $\overline{SS}$ pin low during a transfer of several bytes of data without a problem.

A special case of WCOL occurs in the slave device. This happens when the master device starts a transfer sequence (an edge on SCK for CPHA = 1; or an active $\overline{SS}$ transition for CPHA = 0) at the same time the slave device CPU is writing to its serial peripheral interface data register. In this case it is assumed that the data byte written (in the slave device serial peripheral interface) is lost and the contents of the slave device read buffer becomes the byte that is transferred. Because the master device receives back the last byte transmitted, the master device can detect that a fatal WCOL occurred.

Since the slave device is operating asynchronously with the master device, the WCOL bit may be used as an indicator of a collision occurrence. This helps alleviate the user from a strict real-time programming effort. The WCOL bit is cleared by RESET.

B4, MODF The function of the mode fault flag is defined for the master mode (device). If the device is a slave device the MODF bit will be prevented from toggling from a logic zero to a logic one; however, this does not prevent the device from being in the slave mode with the MODF bit set. The MODF bit is normally a logic zero and is set only when the master device has its $\overline{SS}$ pin pulled low. Toggling the MODF bit to a logic one affects the internal serial peripheral interface (SPI) system in the following ways:

1. MODF is set and SPI interrupt is generated if SPIE = 1.
2. The SPE bit is forced to a logic zero. This blocks all output drive from the device, disables the SPI system.
3. The MSTR bit is forced to a logic zero, thus forcing the device into the slave mode.

Clearing the MODF is accomplished by a software sequence of accessing the serial peripheral status register while MODF is set followed by a write to the serial peripheral control register. Control bit SPE and MSTR may be restored to their original set state during this cleared sequence or after the MODF bit has been cleared. Hardware does not allow the user to set the SPE and MSTR bit while MODF is a logic one unless it is during the proper clearing sequence. The MODF flag bit indicates that there might have been a multi-master conflict for system control and allows a proper exit from system operation to a RESET or default system state. The MODF bit is cleared by RESET.

Serial Peripheral Data I/O Register (SPDR)

7	6	5	4	3	2	1	0
Serial Peripheral Data I/O Register							

SPDR (LOCATION $0C)

The serial peripheral data I/O register is used to transmit and receive data on the serial bus. Only a write to this register will initiate transmission/reception of another byte and this will only occur in the master device. A slave device writing to its data I/O register will not initiate a transmission. At the completion of transmitting a byte of data, the SPIF status bit is set in both the master and slave devices. A write or read of the serial peripheral data I/O register, after accessing the serial peripheral status register with SPIF set, will clear SPIF.

During the clock cycle that the SPIF bit is being set, a copy of the received data byte in the shift register is being moved to a buffer. When the user reads the serial peripheral data I/O register, the buffer is actually being read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not internally responded to clear the first SPIF, only the first byte is contained in the receive buffer of the slave device; all others are lost. The user may read the buffer at any time. The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated or an overrun condition will exist.

A write to the serial peripheral data I/O register is not buffered and places data directly into the shift register for transmission.

The ability to access the serial peripheral data I/O register is limited when a transmission is taking place. It is important to read the discussion defining the WCOL and SPIF status bit to understand the limits on using the serial peripheral data I/O register.

Serial Peripheral Interface (SPI) System Considerations

There are two types of SPI systems; single master system and multi-master systems. Figure 20 illustrates a single master system and a discussion of both is provided below.

Figure 20 illustrates how a typical single master system may be configured, using a CDP68HC05 family device as the master and four CDP68HC05 family devices as slaves. As shown, the MOSI, MISO, and SCK pins are all wired to equivalent pins on each of the five devices. The master device generates the SCK clock, the slave device all receive it. Since the CDP68HC05 master device is the bus master, it internally controls the function of its MOSI and MISO lines, thus writing data to the slave devices on the MOSI and reading data from the slave devices on the MISO lines. The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices. A slave device is selected when the master device pulls its $\overline{SS}$ pin low. The $\overline{SS}$ pins are pulled high during



FIGURE 24. TYPICAL J1850 VPW MESSAGE FRAME

RESET since the master device ports will be forced to be inputs at that time, thus disabling the slave devices. Note that the slave devices do not have to be enabled in a mutually exclusive fashion except to prevent bus contention on the MISO line. For example, three slave devices, enabled for a transfer, are permissible if only one has the capability of being read by the master. An example of this is a write to several display drivers to clear a display with a single I/O operation. To ensure that proper data transmission is occurring between the master device and a slave device, the master device may have the slave device respond with a previously received data byte (this data byte could be inverted or at least be a byte that is different from the last one sent by the master device). The master device will always receive the previous byte back from the slave device if all MISO and MOSI lines are connected and the slave has not written its data I/O register. Other transmission security methods might be defined using ports for handshake lines or data bytes with command fields.

A multi-master system may also be configured by the user. An exchange of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system. The major device control that plays a part in this system is the MSTR bit in the serial peripheral control register and the MODF bit in the serial peripheral status register.

J1850 VPW Messaging

This section provides an introduction to J1850 multiplexed communications. It is assumed that the user is or will become familiar with the appropriate documents published by the Society of Automotive Engineering (SAE). The following discussion is not comprehensive.

Overview

The **SAE Recommended Practice J1850** (Note 1) (J1850) establishes the requirements for communications on a Class B multiplexed wiring network for automotive applications. The J1850 document details the requirements in a three layer description which separately specifies the characteristics of the *physical layer*, the *data link layer*, and the *application layer*. There are several options within each layer which allows vehicle manufacturers to customize the network while still maintaining a level of universality.

NOTE:

1. **SAE Recommended Practice J1850, Class B Data Communication Network Interface,** September 1, 1993, Society of Automotive Engineers Inc.

The hardware of the Harris HIP7030A2 provides features which facilitate implementation of the 10.4Kbps Variable Pulse Width Modulated (VPW) physical layer option of J1850. In combination with a bus transceiver, such as the Harris J1850 Bus Transceiver HIP7020, and appropriate software algorithms the HIP7030A2 circuitry enables the designer to completely implement a 10.4Kbps VPW Class B Communications Network Interface per J1850. Features of such an implementation include:

- Single Wire 10.4Kbps Communications
- Message Buffering and Message Filtering
- Bit-by-Bit Bus Arbitration
- Industry Standard Protocol
- Message Acknowledgment ("In-Frame Response") Capabilities
- Exceptionally Tolerant of Clock Skew, System Noise, and Ground Offsets
- Meets CARB and EPA Diagnostic Requirements
- Supports up to 32 Nodes
- Low Error Rates
- Excellent EMC Levels (when interfaced via Harris J1850 Bus Transceiver HIP7020)

In addition to the standard J1850 features, the HIP7030A2 hardware provides a high speed mode, (intended for receive only use) which can significantly enhance vehicle maintenance capabilities. The high speed mode provides a 41.6Kbps communications path to any node built with the HIP7030A2.

Anatomy of a J1850 VPW Message

All messages in a J1850 VPW system are sent along a single wire, shared bus. At any given moment the bus can be in either of two states: *active* (high) or *passive* (low). Multiple nodes are connected to the bus as a "wired-OR" network in which the bus is high if *any* one (or more) node is generating an active output. The bus is only low when *no* nodes are generating active outputs. It follows that, when no communications are taking place the bus will rest in the passive state. A message begins when the bus is first driven to the high state. Each succeeding state transition (i.e. - a change from active to passive or passive to active) transfers one bit of information (*symbol*) until the message is complete and the bus once again rests at the passive state. The interpretation of each symbol in the message is dependent on its duration (and state), hence the descriptor Variable Pulse Width (VPW).

Each message has a beginning and an end, the span of which encompasses the entire *message* or *frame* (refer to Figure 24). A frame consists of an active *start of frame* (SOF) symbol and a passive *end of frame* (EOF) symbol sandwiched around a series of byte sized (8-bit) groups of symbols. The first byte of the frame contents is always a *header* byte, followed by possibly additional header bytes,

followed by one or more *data* bytes, followed by an integrity check byte (*CRC* byte), followed by a passive *end of data* (EOD) symbol, followed by possibly one or more *in-frame-response* (IFR) bytes. To keep waiting times low, messages are limited to 12 bytes total (including header, data, check, and IFR bytes). All message bytes are transmitted most significant bit (MSB) first.

VPW Symbol Definitions

Within the J1850 scheme, symbols are defined in terms of both duration and state (passive or active). The duration is measured as the time between successive transitions. There is one transition per symbol and one symbol per transition. The end of one symbol marks the beginning of the next. Since the bus is passive when a message begins and must return to that same state when the message completes, all frames have an even number of transitions and hence an even number of symbols.

There are unique definitions for data bit symbols (all the symbols which occur within the header, data, and check bytes) and protocol symbols (including SOF, EOD, and EOF). The duration of each symbol is expressed in terms of VPW Timing Pulses (TV values). Table 5 summarizes the TV definitions. Each TV is specified in terms of a *nominal* (or ideal) duration and a *minimum* and *maximum* duration. The span between the minimum and maximum limits accommodates system noise sources such as node to node clock skew, ground offsets, clock jitter, and electromechanical noise. There are no dead zones between the maximum of one TV and the minimum of the next.

The terms *short* and *long* are often used to refer to pulses of duration TV1 and TV2 respectively.

TABLE 5. J1850 TV DEFINITIONS

TV ID	DURATION (ALL TIMES IN MICROSECONDS)		
	MINIMUM	NOMINAL	MAXIMUM
Illegal	0	NA	≤34
TV1	>34	64	≤96
TV2	>96	128	≤163
TV3	>163	200	≤239
TV4	>239	280	NA
TV5	>239	300	NA
TV6	>280	300	NA

VPW is a non-return-to-zero (NRZ) protocol in which each transition represents a complete bit of information. Accordingly, a *0* data bit will sometimes be transmitted as a passive pulse and sometimes as an active pulse. Similarly, a *1* data bit will sometimes be transmitted as a passive pulse and sometimes as an active pulse. In order to accommodate arbitration (see **Bus Arbitration**) a *long active* pulse represents a 0 data bit and a *short active* pulse represents a 1 data bit. Complementing this fact, a *short passive* pulse represents a 0 and a *long passive* pulse represents a 1. Starting from a transition to the active state, a 0 data bit will maintain the active level longer than a 1. Similarly, starting from a transition to the passive state, a 0 data bit will return to the active level quicker than a 1. These facts give rise to the dominance of 0's over 1's on the J1850 bus as depicted in Figure 25. See **Bus Arbitration** for additional details.

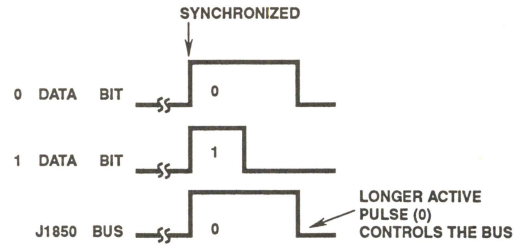


FIGURE 25A. DOMINANCE OF ACTIVE 0 DATA BIT

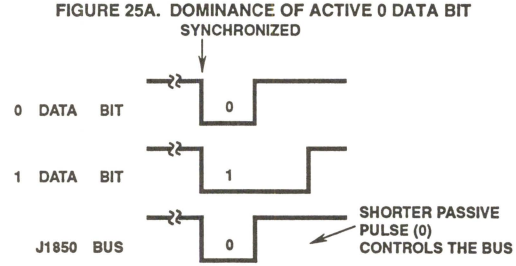


FIGURE 25B. DOMINANCE OF PASSIVE 0 DATA BIT

FIGURE 25.

Table 6 summarizes the complete set of symbol definitions based on duration and state.

TABLE 6. J1850 SYMBOL DEFINITIONS

SYMBOL	DEFINITION
0 Data	Passive TV1 or Active TV2
1 Data	Active TV1 or Passive TV2
SOF (Start of Frame)	Active TV3
EOD (End of Data)	Passive TV3
EOF (End of Frame)	Passive TV4
IFS (Inter-Frame Separation)	Passive TV6
IDLE (Idle Bus)	Passive >TV6 nom
NB (Normalization Bit)	Active TV1 or Active TV2
BRK (Break)	Active TV5

In Frame Response (IFR)

The distinction between two of the passive symbols, EOD and EOF, is subtle but important (refer to Figure 26). The EOD (TV3) interval signifies that the originator of the message is done broadcasting and any nodes which have been requested to respond (i.e. - to acknowledge receipt of the message) can now do so. The EOD interval begins when the transmitting node has completed sending the eighth bit of the check byte. The transmitter simply releases the bus and allows it to revert to a passive state. In the course of normal messaging, no node can seize the bus until an EOD time has been detected. Once an EOD has elapsed, any nodes which are scheduled to produce an IFR will arbitrate for con-



FIGURE 26. J1850 MESSAGE WITH IN-FRAME-RESPONSE

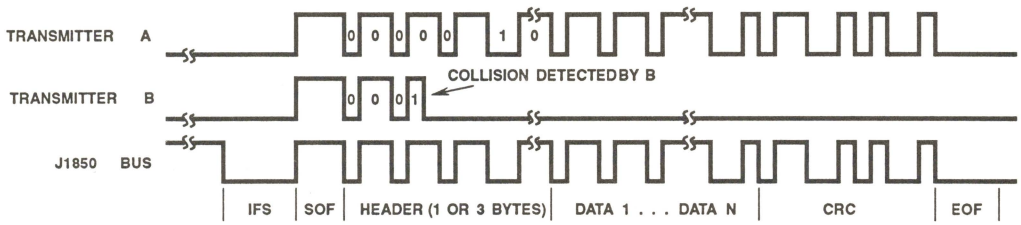


FIGURE 27. TWO NODES ARBITRATING FOR CONTROL OF J1850 BUS

trol of the bus (see **Bus Arbitration**) and respond appropriately. If no responses are forthcoming the bus remains in the passive state until an EOF (TV4) interval has elapsed. After the EOF has been generated, the frame is considered closed and the next communications on the bus will represent a totally new message.

IFRs can consist of multiple bytes from a single respondent, one byte from a single respondent, or one byte from multiple respondents. In all cases the first response byte must be preceded by a *normalization bit (NB)* which serves as a *start of response* symbol and places the bus in an active state so that following the IFR byte(s) the bus will be left in the passive state.

The NB symbol is by definition active, but can be either TV1 or TV2 in duration. The long variety (TV2) signifies the IFR contains a CRC byte. The short variety (TV1) precedes an IFR without CRC.

Message Types

Messages are classified into one of four *Types* according to whether the message has an IFR and what kind of IFR it is. The definitions are:

- Type 0 - No IFR
- Type 1 - One byte IFR from a single respondent (no CRC byte)
- Type 2 - One byte IFRs from multiple respondents (no CRC byte)
- Type 3 - Multiple byte IFR from a single respondent (CRC appended)

Bus Arbitration

The nature of multiplexed communications leads to contention issues when two or more nodes attempt to transmit on the bus simultaneously. Within J1850 VPW systems, messages are assigned varying levels of priority which allows implementation of an arbitration scheme to resolve potential contentions. The specified arbitration is performed on a symbol by symbol basis throughout the duration of every message.

Arbitration begins with the rising edge of the SOF pulse. No node should attempt to issue an SOF until an Idle bus has been detected (i.e. - an *Inter-Frame Separation (IFS)* symbol with a period of TV6 has been received). If multiple nodes are ready to access the bus and are all waiting for an IFS to elapse, invariable skews in timing components will cause one arbitrary node to detect the Idle condition before all others and start transmission first. For this reason, all nodes waiting for an IFS will consider an IFS to have occurred if either:

- An IFS nominal period has elapsed
  or
- An EOF minimum period has elapsed and a rising edge has been detected

Arbitrating devices will all be synchronized during the SOF. Beginning with the first data bit and continuing to the EOF, every transmitting device is responsible for verifying that the symbol it sent was the symbol which appeared on the bus. Each transition, every transmitting node must decode the symbol, verify the received symbol matches the one sent, and begin timing of the next symbol. Since timing of the next symbol begins with the last transition detected on the bus, all transmitters are re-synchronized each symbol. When the received symbol doesn't match the symbol sent, a conflict (*bit collision*) occurs. Any device detecting a collision will assume it has lost arbitration and immediately relinquish the bus. Typically, after losing arbitration, a device will attempt re-transmission of the message when the bus once again becomes Idle.

The definition of 1 and 0 data bits (see Table 6 and discussion under **VPW Symbol Definitions**) leads to 0's having priority over 1's in this arbitration scheme. Header bytes are generally assigned such that arbitration is completed before the first data byte is transmitted. Because of the dominance of 0-bits and the MSB first bit order, a header with the hexadecimal value $00 will have highest priority, then $01, $02, $03, etc. An example of two nodes arbitrating for control of the bus is shown in Figure 27.

Arbitration also takes place during the IFR portion of a message, if more than one node is attempting to generate a response. Arbitration begins with the NB symbol, which follows the EOD and precedes the first IFR byte.

For Type 1 and Type 3 messages only the respondent which successfully arbitrates for control of the bus produces an IFR. All other respondents abort their IFRs.

For Type 2 messages, all respondents which lose arbitration must count symbols and re-attempt transmission at the end of each byte. Each node, which successfully responds, eliminates itself from the subsequent arbitration until all nodes have responded. This arbitration scheme limits each respondent to a single byte during a Type 2 IFR.

Break

To force a message to be aborted before EOF is reached, a break (BRK) symbol can be transmitted by any node. The BRK symbol is an active pulse of duration TV5. Reception of a break causes all nodes to reset to a *ready-to-receive* state and to re-arbitrate for control following an IFS.

Variable Pulse Width Symbol Encoder Decoder (SENDEC)

OVERVIEW OF SENDEC OPERATION

The SENDEC hardware integrated in the HIP7030A2 facilitates generation and reception of J1850 messages on a symbol by symbol basis. Symbols are output from the SENDEC, as a digital signal, on the VPWOUT pin and input, as a digital signal, on the $\overline{\text{VPWIN}}$ pin. These two lines must be connected through a bus transceiver (such as the Harris J1850 Bus Transceiver HIP7020) to the single wire J1850 bus. The transceiver is responsible for generating and receiving waveforms consistent with the physical layer specifications of J1850. In addition, the transceiver is responsible for providing isolation from bus transients.

Every symbol sent out on the VPWOUT is in effect inverted and echoed back on the $\overline{\text{VPWIN}}$ pin after some finite delay through the transceiver. In actuality, only long active symbols are guaranteed to be echoed unchanged. If the transmitted symbol is passive and another node is simultaneously sending an active symbol, the active symbol will dominate and pull the bus to a high level.

The SENDEC circuitry includes a 3-bit digital filter which effectively filters out noise pulses less than 7µs in duration.

Communications between the CPU and the SENDEC are via three registers mapped into Page 0 of the MCUs memory space.

When transmitting symbols, the desired symbol is specified by writing an appropriate code to the SENDEC Data Register (SEDDR). Timing of each symbol is calculated from the last transition on the $\overline{\text{VPWIN}}$ line. Each write to the SEDDR, which occurs within 34µs of the last received transition, will enable the VPWOUT pin and the SENDEC automatically produces a transition on the VPWOUT pin after the proper delay (the seven microseconds added by the digital filter and a 17 microsecond delay through the bus transceiver are compensated for). The VPWOUT pin remains active until 34 microseconds after the last received transition. Failure to write a new symbol during the 34 microsecond window causes the VPWOUT pin to go low until the next valid write or until the Force Start of Frame (FSOF) bit is set in the SENDEC Data Register (SEDDR).

Decoding of received symbols is automatically performed by the SENDEC. The decoded symbol is valid until the next transition occurs. The value can be read via the SEDDR.

Generally the SENDEC is programmed to interrupt the MCU with each transition on the $\overline{\text{VPWIN}}$ pin. When the SENDEC is receiving a message, the interrupt signals that a new symbol has been received and appropriate actions must be taken to read and process the symbol. When the SENDEC is transmitting, the transition interrupt signifies that the reflected symbol has been received, and it is time to start timing the next symbol. The reflected symbol should be read and compared to the previously sent one. If the reflected symbol doesn't match the symbol sent, a collision has occurred and the software must cease transmissions until the next idle period. If there was no collision, the new symbol must be immediately (within one TV1 minimum time) written to the SEDDR (the SEDDR is not buffered).

In addition to features already discussed, the SENDEC includes, noise detection, idle bus detection, a clock prescaler, an echo fail detector, a wake-up facility, and a high speed receive mode. Symbol timing is based on the main MCU oscillator. The programmable prescaler allows proper SENDEC operation with 10MHz, 8MHz, or 4MHz oscillators. The high speed receive mode is a J1850 extension which allows maintenance equipment to transmit messages at 4X the normal 10.4Kbps rate.

Software algorithms can be employed to implement message buffering and filtering, CRC generation and detection, IFR handling, and other needed features to create a complete J1850 VPW node. See the *Applications* section for typical algorithms.

SENDEC REGISTERS

The SENDEC register set consists of the read-write SENDEC Data Register (SEDDR), the read-write SENDEC Control Register (SEDCR), and the read-only SENDEC Status Register (SEDSR). A detailed description of the operation of each follows:

SENDEC Control Register (SEDCR)

The SENDEC Control Register (SEDCR, location $0F) is an 8-bit read/write register which contains five control bits. One of the bits controls interrupts which are associated with a flag bit in the SENDEC Status Register (discussed following). Three bits control the clock prescaler and the high speed 4X mode of the SENDEC. The final bit doesn't directly control the SENDEC, rather it controls the start-up delay following exit from the STOP mode of the processor. The bit assignments are illustrated below, followed by a detailed description of each bit.

7	6	5	4	3	2	1	0
TXIE	-	-	NDEL	-	4X	PRE1	PRE0

SEDCR (LOCATION $0F)

B7, TXIE — If the transition interrupt enable (TXIE) bit is set, the MCU will receive a SENDEC interrupt on the occurrence of each transition on the $\overline{\text{VPWIN}}$ line.

If TXIE is low the TX interrupts are inhibited but the associated flags in the SENDEC Status Register (SEDSR) are still set (see discussion following).

TXIE is cleared by RESET.

B4, NDEL — When set, the No Delay (NDEL) bit suppresses the 4064 t_{CYC} delay which is normally introduced when exiting from the STOP mode via an interrupt. Instead of the 4064 t_{CYC} delay a 128 t_{CYC} delay is introduced. NDEL is intended for applications where the clock source to the HIP7030A2 continues to run when the device enters STOP mode or when a ceramic resonator based oscillator is used. NDEL should not be used when the HIP7030A2 is driven by a quartz crystal based oscillator.

NDEL is cleared by RESET and POR.

B2, 4X — When set, the 4X bit causes the SENDEC symbol timing to be accelerated by a factor of four. Due to fixed delays in the loop back from VPWOUT to $\overline{\text{VPWIN}}$, the 4X mode is only useful for receiving symbols. 4X mode is intended for high speed data linking between the HIP7030A2 and maintenance or test equipment which has capability to send at the accelerated rate.

Writing to the 4X bit is inhibited except when the NEW bit in the SENDEC Status Register (SEDSR) is set.

Once modified, the new value of 4X doesn't take effect until the next transition on the $\overline{\text{VPWIN}}$ pin.

Receipt of a Break symbol on the $\overline{\text{VPWIN}}$ line will automatically clear 4X.

RESET and POR clear the 4X bit.

B1, PRE1
B2, PRE0 — PRE1 and PRE0 control the SENDEC clock prescaler. The SENDEC circuit requires a fundamental clock of 1MHz. To generate the 1MHz frequency, while allowing a choice of MCU oscillator frequencies, the PRE1 and PRE0 bits must be set to match the OSCIN frequency.

TABLE 7. SENDEC PRESCALER BIT SELECTION

PRE1	PRE0	OSCIN FREQUENCY (MHz)
0	0	4
0	1	8
1	0	10
1	1	12

Following RESET a window of 4 instructions is allowed for setting the PRE1 and PRE0 bits. Writes to these bits after the fourth instruction have no effect on their values.

Table 7 gives the proper settings of PRE1 and PRE0 for various frequencies.

RESET and POR force PRE1 to a 1 and PRE0 to a 0, selecting the 10MHz mode.

SENDEC Status Register (SEDSR)

The SENDEC Status Register (SEDSR, location $10) is an 8-bit read-only register which contains seven status bits. One of the bits is a flag bit which correspond to the interrupt control bit in the SENDEC Control Register (discussed earlier). Three other bits provide error status information. Another two bits provide an indication of special symbols (Break, IFS) occurring on the bus. The final bit indicates the transmit status of the SENDEC. The bit assignments are illustrated below, followed by a detailed description of each bit.

7	6	5	4	3	2	1	0
TX	BRK	NEW	NOIZ	OVR	TALK	NECHO	-

SEDSR (LOCATION $10)

B7, TX — The transition (TX) flag bit indicates that a transition has occurred on the VPWIN line. The line is first filtered through the SENDECs 3-bit digital filter to reject noise.

Once set the TX flag will interrupt the MCU if the TXIE bit in the SEDCR is set and the I bit in the condition code register is clear. TX is cleared by a sequence of first reading the SEDSR followed by reading or writing the SENDEC Data Register (SEDDR).

Note that both TX and NEW will be set on the leading edge of an SOF. See description of the NEW flag below.

TX is cleared by RESET.

B6, BRK — The break (BRK) bit indicates that a break symbol has been detected on the $\overline{\text{VPWIN}}$ line. BRK is set at the end of the break symbol, on the active to passive transition.

Once set the BRK flag will interrupt the MCU if the I bit is cleared in the condition code register. BRK is cleared by a sequence of first reading the SEDSR followed by a read or write of the SEDCR.

BRK is cleared by RESET.

B5, NEW — The new frame (NEW) flag indicates that one of two possible events has been detected on the J1850 bus:

The bus has been passive for at least an IFS nominal symbol time (i.e. - the bus is Idle)

or

A transition has occurred on the bus following an EOF minimum (i.e. - another node has started a new message).

NEW is set when either of these events is detected. In the case of a transition following an EOF, the TX bit is also set.

When NEW goes from a 0 to a 1, a SENDEC interrupt will be generated if the I bit is cleared in the CC register. The NEW interrupt can be cleared under software control by reading the SEDSR followed by writing the SEDCR. This only removes the source of the interrupt and does not clear the NEW bit.

The NEW flag cannot be cleared by software. It is automatically cleared 128 (nominal) microseconds into the next (or current - if NEW was set by a transition following EOF) symbol. This is normally during the SOF of a new message. If the symbol is less than 128µs in duration (an illegal SOF symbol), the NEW flag is cleared on the active to passive transition.

Polling NEW provides a convenient means for software to determine that transmission of a new message can be commenced.

NEW is cleared by all resets.

B4, NOIZ — The noise (NOIZ) flag indicates that a symbol shorter than a legal TV1 has been received. NOIZ is cleared by a sequence of first reading the SEDSR followed by reading or writing the SEDCR.

NOIZ is cleared by RESET.

B3, OVR — The overrun (OVR) flag is set if TALK is set in the SEDSR and a minimum short symbol time (34µs) has elapsed since the last transition and no write to the SEDDR has taken place. An overrun condition is a serious error and the user should treat it as such. When OVR is set it automatically forces the VPWOUT pin to a low level. OVR is cleared by a sequence of first reading the SEDSR followed by reading or writing the SEDCR.

Setting of OVR is inhibited while NEW is true in the SEDSR.

OVR is cleared by RESET.

B2, TALK — The transmit (TALK) flag is set if the HIP7030A2 is actively transmitting symbols via the SENDEC. TALK is set by writing a non-zero to the SEDDR (see *SENDEC Data Register* for details).

The TALK bit is cleared by writing a $00 to the SEDDR, when NECHO is set, or when OVR is set.

TALK is cleared by RESET.

B1, NECHO — The No Echo Received (NECHO) flag is set if, during the process of transmitting a symbol, the expected echo of the symbol is not received. This event will cause the VPWOUT pin to be forced to a 0 level. Setting of NECHO automatically clears the TALK bit.

The time required to detect an echo failure is dependent on many factors. The minimum time to detect a failure is 105µs (26µs in 4X mode) and the maximum time to detect a failure is 512µs.

When NECHO goes from a low to a high level, a SENDEC interrupt will be generated if the I bit is cleared in the CC register. NECHO must go low then high again to generate another interrupt.

NECHO is cleared by a sequence of first reading the SEDSR followed by reading or writing the SENDEC Data Register (SEDDR).

NECHO is cleared by all resets.

SENDEC Data Register

The SENDEC Data Register (SEDDR, location $11) is an 8-bit read/write register which contains one write-only bit, three read/write bits, and four read-only bits. The write only bit triggers SOF symbols required to initiate new transmissions, the three read/write bits are used to specify transmitted symbol durations, and the four read only bits uniquely identify the received J1850 symbol. Reading the SEDDR at anytime provides the received symbol which resulted from the last transition of $\overline{\text{VPWIn}}$. When writing data to the SEDDR, the value represents the duration of the symbol currently being transmitted. The bit assignments are illustrated below, followed by a detailed description.

7	6	5	4	3	2	1	0
FSOF	S2	S1	S0	LEV	R2	R1	R0

SEDDR (LOCATION $11)

B7, FSOF — Writing a 1 to the Force Start of Frame (FSOF) bit while simultaneously writing a non-zero value to S2-0, causes the VPWOUT to immediately go active (high level). The low to high transition will eventually be reflected on the $\overline{\text{VPWIN}}$ line causing a TX interrupt. Upon receipt of the TX interrupt an SOF symbol (S2-0 = 3) must be written to the SEDDR to time the high SOF.

Setting the FSOF bit can only be done when the NEW flag is set in the SENDEC Status Register (NEW is set when the J1850 bus is idle or during the first portion of an SOF symbol).

FSOF is a write only bit. Reading FSOF always returns a 0.

B6, S2
B5, S1
B4, S0 — When writing to the SEDDR, the three bits (S2-0) determine the transmitted symbol as shown in Table 8. During a write to the SEDDR the S2-0-bits are ignored except in three specific situations:

The NEW flag is high in the SEDSR)

or

A transition has been received on the $\overline{\text{VPWIN}}$ pin, from the bus, within the past 34µs

or

S2-0-bits = 0

In the first two cases, each write to the SEDDR will produce one properly timed symbol on the VPWOUT pin. The completion of the symbol is reported to the controller, *not* at the end of the transmitted symbol, but at the end of the symbol echoed back via the $\overline{\text{VPWIN}}$ input. Writing the FSOF bit, in conjunction with S2-0 = 3, produces the initial transition for the SOF symbol. All timing for a message begins with the receipt of that transition.

Writing a $00, at anytime, immediately disables transmissions (forcing the VPWOUT pin low) and clears the TALK bit in the SEDSR. This is the preferred method to end transmissions.

RESET doesn't affect S2-S0

TABLE 8. S2-S1 SYMBOL ENCODING

S2	S1	S0	TRANS9MIT SYMBOL
0	0	0	Disable Transmit
0	0	1	TV1
0	1	0	TV2
0	1	1	TV3
1	0	0	TV1
1	0	1	TV1
1	1	0	TV1
1	1	1	TV1

B3, LEV
B2, R2
B1, R1
B0, R0

These four bits uniquely identify all symbols received via the $\overline{\text{VPWIN}}$ pin. The symbol decoding map is shown in Table 9. R2-0 represent the duration of the symbol and LEV represents the level of the symbol (active or passive)

These bits are only updated upon detection of a bus transition and therefore reflect the last symbol received. An exception to this is for an Idle bus. When an Idle has been detected the values in R2-R0 and LEV are immediately updated - no bus transition is necessary.

R2-R0 = 101 with LEV = 0 indicates that the bus is currently Idle.

Note that R2-0 combinations of 110 and 111 will not be produced by the SENDEC. A value of 101 represents all durations equal to and beyond an IFS/IDLE (for the passive case) and a BREAK (for the active case).

RESET does not affect LEV or R2-R0.

When a transition is detected on $\overline{\text{VPWIN}}$, the received symbol is decoded and made available for reading via the SEDDR. The TX bit is set in the SEDSR and, if TXIE is high in the SEDCR, an interrupt will be generated. Once the transition is detected the next symbol begins timing out. A new symbol must be written to the SEDDR, before the minimum transmit time for a short symbol has elapsed (34µs). Failure to write to the SEDDR in time will result in the OVR bit being set and transmission aborted. This is a safety precaution to prevent "streaming" messages.

The control routines should verify that the symbol sent matches the symbol received. A mismatch indicates the device has lost control of the bus. It is up to the user code to handle the collision, in terms of disabling the SENDEC, requeueing of the message, filtering the incoming message, etc.

TABLE 9. R2-R0 AND LEV SYMBOL DECODING

R2	R1	R0	LEV	Receive Symbol
0	0	0	0	Passive Noise
0	0	0	1	Active Noise
0	0	1	0	TV1 Passive
0	0	1	1	TV1 Active
0	1	0	0	TV2 Passive
0	1	0	1	TV2 Active
0	1	1	0	EOD
0	1	1	1	SOF
1	0	0	0	EOF
1	0	0	1	BREAK
1	0	1	0	IFS/IDLE
1	0	1	1	BREAK
1	1	0	0	-
1	1	0	1	-
1	1	1	0	-
1	1	1	1	

In the receive mode (i.e. - no writes to the SEDDR) the controller typically responds to the TX interrupts and reads the incoming symbols as they become available, performing necessary real-time operations such as filtering messages, computing and verifying CRCs, and issuing IFRs.

Computer Operating Properly (COP) System

INTRODUCTION

The Computer Operating Properly (COP) system is comprised of two basic circuit components. One is a free running watchdog timer which, left unattended, generates a periodic MCU reset. The second is a Slow Clock Detect circuit which constantly monitors the OSCIN line for activity. A lack of activity on OSCIN will generate a reset.

Both circuits are capable of generating a COP interrupt which forces an MCU reset and restarts operation at the vector specified by the contents of location $1FFA,$1FFB. Because the COP interrupt behaves as a reset, the stack pointer is cleared and exiting the COP interrupt software handler must be done via a jump instruction as opposed to an RTI or RTS.

The Watchdog Status Register (WSR, location $1E) contains a flag (Watchdog Flag, bit 0) which is set whenever a Watchdog Timer overflow interrupt occurs. The flag is cleared by RESET, POR, and Slow Clock Detect and can therefore be used to distinguish the type of COP reset (Watchdog timeout vs. Slow Clock Detect) which has occurred.

Operation of each of the two circuits is detailed in the following discussion.

SLOW CLOCK DETECT CIRCUIT

The Slow Clock Detect Circuit consists of a reset-able timer element. The timer is constructed with integrated resistive and capacitive components. Each positive transition on the OSCIN line reinitializes the timer. In the absence of frequent enough transitions on the input, the timer will eventually reach a preset limit at which point the MCU will be reset via a COP interrupt.

When the frequency has dropped below the preset threshold a COP reset will take place. A COP reset is identical to a POR or RESET pin reset, except the restart vector is the COP Vector. Following the COP reset the HIP7030A2 is held reset until the start-up timeout of 4064 clocks has been reached. During the 4064 clocks the Slow Clock Detect circuit is inhibited. If at the end of the 4064 clocks the frequency remains below the threshold, a COP reset will immediately take place again.

The primary purpose of this circuit is to force the HIP7030A2 off of the J1850 and SPI busses should the oscillator circuit fail. Due to variability of integrated resistors and capacitors there is a non-critical spread in the timeout specification of approximately 5:1. Maximum frequency threshold is 500kHz. Refer to *Electrical Specifications* for details.

There is no means to disable the Slow Clock Detect. RESET resets the Slow Clock Detect circuit and holds it reset until the start-up timeout of 4064 clocks has been reached and the RESET pin has gone high.

WATCHDOG TIMER

The Watchdog Timer is a free-running 21 stage counter which divides the OSCIN input by 2,097,152. The Timer is software reset-able, and must be constantly reset before the terminal count is reached. Failure to reset the Watchdog Timer, in due time, results in a forced MCU RESET via a COP interrupt.

7	6	5	4	3	2	1	0
Watchdog Reset Register							

WRR (LOCATION $1D)

Resetting the Watchdog Timer requires two distinct operations. A write of the value $55 to the Watchdog Reset Register (WRR, location $1D) must be followed by a write of the value $AA to the WRR. There is no limit on the time between the writes, other than both must take place before the Watchdog Timer has reached its limit. Typically the two writes are placed in distinct sections of code, which can only be reached by proper flow through the software.

Each time that the Watchdog Timer is successfully cleared the Watchdog Flag in the WSR is also cleared. The Watchdog flag is also cleared by POR, RESET, and Slow Clock Detect. It is set by a Watchdog Timer overflow and can be used to distinguish a Slow Clock Detect reset from the Watchdog reset, both of which share the COP reset vector ($1FFA,$1FFB).

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	WDF

WSR (LOCATION $1E)

Watchdog timeout periods for various OSCIN frequencies are given in Table 10.

There is no mechanism to disable the Watchdog Timer. RESET clears the Watchdog Timer to its initial value.

TABLE 10. WATCHDOG TIMEOUTS FOR COMMON OSCIN FREQUENCIES

WATCHDOG TIMEOUT	OSCIN FREQUENCY (MHz)
175ms	12
210ms	10
262ms	8
524ms	4

Effects of Stop and Wait Modes on the Timer, COP, and Serial Systems

INTRODUCTION

The STOP and WAIT instructions have different effects on the programmable timer, VPW Symbol Encoder/Decoder (SENDEC), and serial peripheral interface (SPI) systems. These effects are discussed separately below.

STOP MODE

When the processor executes the STOP instruction, the internal oscillator is turned off. This halts all internal CPU processing including the operation of the programmable timer, serial communications interface, and serial peripheral interface. The only way for the MCU to "wake up" from the STOP mode is by receipt of an external interrupt (logic low on IRQ pin), a negative edge on the VPWIN pin, or by the detection of a RESET (logic low on RESET pin or a power-on reset). Execution will resume at the instruction immediately following the STOP instruction that caused the HIP7030A2 to enter the STOP mode.

Normally a start-up delay of 4064 t_{CYC} is inserted after exiting from STOP before fetching the first instruction. This delay is intended to guarantee stability of a crystal clock source. If it is known that the clock source will be stable prior to exiting STOP, then the NDEL bit in the SEDCR can be set prior to executing the STOP instruction. Setting NDEL has the effect of shortening the start-up delay to 128 tCYC.

The effects of the STOP mode on each of the MCU systems (COP, Timer, SENDEC, and SPI) are described separately in the following sections.

COP During STOP Mode

When the MCU enters the STOP mode, the Watchdog Timer and the Slow Clock Detect circuits are both inhibited.

Timer During STOP Mode

When the MCU enters the STOP mode, the timer counter stops counting (the internal processor is stopped) and remains at that particular count value until the STOP mode is exited by an interrupt (if exited by RESET the counter is forced to $FFFC). If the STOP mode is exited by an external low on the $\overline{IRQ}$ pin, then the counter resumes from its stopped value as if nothing had happened. Another feature of the programmable timer, in the STOP mode, is that if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuitry is armed. This action does not set any timer flags or "wake up" the MCU, but when the MCU does "wake up" there will be an active input capture flag (and data) from that first valid edge which occurred during the STOP mode. If the STOP mode is exited by an external reset (logic low on $\overline{RESET}$ pin), then no such input capture flag or data action takes place even if there was a valid input capture edge (at the TCAP pin) during the MCU STOP mode.

SENDEC During STOP Mode

When the MCU enters the STOP mode, the absence of any internal clocks causes all SENDEC functions, except Wake Up to cease. If the SENDEC was currently being used to transmit a symbol, that symbol is truncated and the VPWOUT is forced to a low (passive) state. For proper operation, a STOP instruction should not be executed except when the bus is Idle.

Normally all transitions are first filtered through the SENDECs three bit digital filter. When in STOP mode the 3-bit filter is bypassed and any passive to active transition (high to low) on $\overline{VPWIN}$ will cause a SENDEC interrupt which will, in turn, cause the processor to exit the STOP mode.

Upon exiting the STOP mode the processor will execute a SENDEC interrupt. The setting of the TX bit in the SEDSR does *not* bypass the 7µs filter and as such the TX bit will *not* be set when first awakening from STOP. If the NDEL bit has been set prior to entering STOP, software should delay 8µs and check TX. If at that time TX has not been set, the assumption can be made that a noise pulse caused the wakeup and the STOP mode can be reentered. When NDEL is not employed monitoring of TX must continue for several hundred microseconds, as a complete message could have transpired during the oscillator start-up time.

During handling of a SENDEC interrupt following STOP, the SEDSR must be read at least one time to remove the source of the interrupt.

SPI During STOP Mode

When the MCU enters the STOP mode, the baud rate generator which drives the SPI shuts down. This essentially stops all master mode SPI operation. To ensure the SPI bus remains free for transfers, the MSTR bit in the SPCR is cleared, configuring the SPI pins in slave mode. If the STOP instruction is executed during an SPI transfer, in which the HIP7030A2 was the master, that transfer is aborted. If the STOP mode is exited by a RESET, then the appropriate control/status bits are cleared and the SPI is disabled. If the device is in the slave mode when the STOP instruction is executed, the slave SPI will still operate. It can still accept data and clock information in addition to transmitting its own data back to a master device.

At the end of a possible transmission with a slave SPI in the STOP mode, no flags are set until an $\overline{IRQ}$ or SENDEC interrupt results in an MCU "wake up". Caution should be observed when operating the SPI (as a slave) during the STOP mode because none of the protection circuitry (write collision, mode fault, etc.) is active.

WAIT MODE

When the MCU enters the WAIT mode, the CPU clock is halted. All CPU action is suspended; however, the timer, SENDEC, and SPI systems remain active. In fact an interrupt from the timer, SENDEC, or SPI (in addition to a logic low on the $\overline{IRQ}$ or $\overline{RESET}$ pins) causes the processor to exit the WAIT mode. Since the three systems mentioned above operate as they do in the normal mode, only a general discussion of the WAIT mode is provided below.

Note that the Slow Clock Detect and Watchdog Timer circuitry continues to function during WAIT. It is requisite upon the designed to ensure that the CPU is removed from WAIT (via an external or TIMER or SENDEC interrupt) frequently enough to prevent a Watchdog Timer overflow.

The WAIT mode power consumption depends on how many systems are active. The power consumption will be highest when all the systems (timer, TCMP, SENDEC, and SPI) are active. The power consumption will be the least when the SENDEC and SPI systems are disabled (timer operation cannot be disabled in the WAIT mode). If a non-RESET exit from the WAIT mode is performed (i.e., timer overflow interrupt exit), the state of the remaining systems will be unchanged. If a RESET exit from the WAIT mode is performed all the systems revert to the disabled reset state.

Instruction Set

The MCU has a set of 62 basic instructions. They can be divided into five different types: register/memory, read- modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

Register/Memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The operand for the jump unconditional (JMP) and jump to subroutine (JSR) instructions is the program counter. Refer to Table 11.

Read-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value. Refer to Table 12.

TABLE 11. REGISTER/MEMORY INSTRUCTIONS

FUNCTION	MNEM	ADDRESSING MODES																	
		IMMEDIATE			DIRECT			EXTENDED			INDEXED (NO OFFSET)			INDEXED (8-BIT OFFSET)			INDEXED (16-BIT OFFSET)		
		OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	-	-	-	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	-	-	-	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory From A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	-	-	-	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	-	-	-	BD	2	2	CD	3	3	FD	1	5	ED	2	6	DD	3	7

TABLE 12. READ-MODIFY-WRITE INSTRUCTIONS

FUNCTION	MNEM	ADDRESSING MODES														
		INHERENT (A)			INHERENT (X)			DIRECT			INDEXED (NO OFFSET)			INDEXED 8-BIT OFFSET)		
		OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES	OP CODE	NO. BYTES	NO. CYCLES
Increment	INC	4C	3	3C	2	5	7C	1	5	6C	2	6	-	-	-	-
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11	-	-	-	-	-	-	-	-	-	-	-	-

Branch Instructions

Most branch instructions test the state of the condition code register and if certain criteria are met, a branch is executed. This adds an offset between -127 and +128 to the current program counter. Refer to Table 13.

TABLE 13. BRANCH INSTRUCTIONS

FUNCTION	MNEM	RELATIVE ADDRESSING MODE		
		OP CODE	NO. BYTES	NO. CYCLES
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

Bit Manipulation Instructions

The MCU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space except for ROM, port D data location ($03), serial peripheral status register ($0B), serial communications status register (10), timer status register ($13), and timer input capture register ($14 - $15). All port registers, port DDRs, timer, two serial systems, on-chip RAM, and 48 bytes of ROM reside in the first 256 bytes (page zero). An additional feature allows the software to test and branch on the state of any bit within the first 256 locations. The bit set, bit clear, and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions, the value of the bit tested is automatically placed in the carry bit of the condition code register. Refer to Table 14.

TABLE 14A. BIT MANIPULATION INSTRUCTIONS

FUNCTION	MNEM	BIT SET/CLEAR		
		OP CODE	NO. BYTES	NO. CYCLES
Set Bit n	BSET n (n = 0 . . .7)	10 + 2•n	2	5
Clear Bit n	BCLR n (n = 0 . . .7)	11 + 2•n	2	5

TABLE 14A. BIT MANIPULATION INSTRUCTIONS

FUNCTION	MNEM	BIT TEST AND BRANCH		
		OP CODE	NO. BYTES	NO. CYCLES
Branch IFF Bit n is Set	BRSET n (n = 0 . . . 7)	2•n	3	5
Branch IFF Bit n is Clear	BRCLR n (n = 0 . . . 7)	01 + 2•n	3	5

Control Instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 15.

TABLE 15. CONTROL INSTRUCTIONS

FUNCTION	MNEM	INHERENT		
		OP CODE	NO. BYTES	NO. CYCLES
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

Alphabetical Listing

The complete instruction set is given in alphabetical order in Table 16.

Opcode Map

Table 17 is an opcode map for the instructions used on the MCU.

Addressing Modes

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit accessing tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One and two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory. Table 17 shows the addressing modes for each instruction, with the effects each instruction has on the condition code register.

The term "effective address" (EA) is used in describing the various addressing modes, and is defined as the byte address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of" the location or register referred to; e.g., (PC) indicates the contents of the location pointed to by the PC. An arrow indicates "is replaced by", and a colon indicates concatenation of two bytes.

Inherent

In inherent instructions, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

Immediate

In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

EA = PC + 1; PC ← PC + 2

Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes most on-chip RAM and all I/O registers. Direct addressing is efficient in both memory and time.

EA = (PC +1); PC ← PC + 2

Address Bus High 0; Address Bus Low ← (PC + 1)

Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three-byte instruction.

EA = (PC + 1) : (PC + 2); PC ← PC + 3

Address Bus High ← (PC + 1); Address Bus Low ← (PC + 2)

Indexed, No Offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

EA = X; PC ← PC + 1

Address Bus High ← 0; Address Bus Low ← X

Indexed, 8-Bit Offset

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register; therefore, the operand is located anywhere within the lowest 511 mem-

ory locations. For example, this mode of addressing is useful for selecting the mth element in a n element table. All instructions are two bytes. The content of the index register (S) is not changed. The content of (PC + 1) is an unsigned 8-bit integer. One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

EA = X + (PC + 1); PC ← PC + 2

Address Bus High ← K; Address Bus Low ← X + (PC + 1)

where: K = the carry from the addition of x + (PC + 1).

Indexed, 16-Bit Offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). The content of the index register is not changed.

EA = X + [(PC + 1) : (PC + 2)]; PC ← PC + 3

Address Bus High ← (PC + 1) + K

Address Bus Low ← X + (PC + 2)

where: K = The carry from the addition of X + (PC + 2).

Relative

Relative addressing is only used in branch instructions. In relative addressing, the content of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to the range of -126 to +129 bytes from the branch instruction opcode location.

EA = PC + 2 + (PC + 1); PC ← EA if branch taken;

otherwise, EA = PC ← PC + 2.

Bit Set/Clear

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 256 addressable locations are thus accessed. The bit to be modified within that byte is specified in the first three bits of the opcode. The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the other to address the byte which contains the bit of interest.

EA = (PC + 1); PC ← PC + 2

Address Bus High ← 0; Address Bus Low ← (PC + 1).

Bit Test and Branch

Bit test and branch is a combination of direct addressing, bit set/clear addressing, and relative addressing. The actual bit to be tested, within the byte, is specified within the low order nibble of the opcode. The address of the data byte to be tested is located via a direct address in the location following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or cleared in the specified memory location. This single three byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

EA1 = (PC +1)

Address Bus High Q 0; Address Bus Low ← (PC + 1)

EA2 = PC + 3 + (PC + 2); PC ← EA2 if branch taken;

otherwise, PC ← PC + 3.

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (PD \bullet \theta_{JA}) \quad \text{(EQ. 1)}$$

Where: T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \bullet V_{CC}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

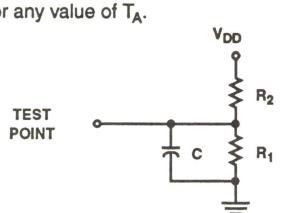
An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K / (T_J + 273°C) \quad \text{(EQ. 2)}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad \text{(EQ. 3)}$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a know T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.



EQUIVALENT TEST LOAD (SEE TABLE FOR VALUES OF R_1 AND R_2)

PINS	R_1	R_2	C
V_{DD} = 4.5V PA0 - PA7, PD0 - PD4	3.26kΩ	2.38kΩ	50pF
MISO, MOSI, SCK	1.9kΩ	2.2kΩ	200pF

TABLE 16. INSTRUCTION SET

MNEM	ADDRESSING MODES										CONDITION CODES				
	INHERENT	IMMEDIATE	DIRECT	EXTENDED	RELATIVE	INDEXED (NO OFFSET)	INDEXED (8 BITS)	INDEXED (16 BITS)	BIT SET/ CLEAR	BIT TEST AND BRANCH	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	•	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	•	Λ	Λ	Λ
AND		X	X	X		X	X	X			•	•	Λ	•	Λ
ASL	X		X			X	X				•	•	Λ	Λ	Λ
ASR	X		X			X	X				•	•	Λ	Λ	Λ
BCC					X						•	•	•	•	•
BCLR									X		•	•	•	•	•
BCS					X						•	•	•	•	•
BEQ					X						•	•	•	•	•
BHCC					X						•	•	•	•	•
BHCS					X						•	•	•	•	•
BHI					X						•	•	•	•	•
BHS					X						•	•	•	•	•
BIH					X						•	•	•	•	•
BIL					X						•	•	•	•	•
BIT		X	X	X		X	X	X			•	•	Λ	Λ	•
BLO					X						•	•	•	•	•
BLS					X						•	•	•	•	•
BMC					X						•	•	•	•	•
BMI					X						•	•	•	•	•
BMS					X						•	•	•	•	•
BNE					X						•	•	•	•	•
BPL					X						•	•	•	•	•
BRA					X						•	•	•	•	•
BRN					X						•	•	•	•	•
BRCLR										X	•	•	•	•	Λ
BRSET										X	•	•	•	•	Λ
BSET									X		•	•	•	•	•
BSR					X						•	•	•	•	•
CLC	X										•	•	•	•	0
CLI	X										•	0	•	•	•
CLR	X		X			X	X				•	•	0	1	•
CMP		X	X	X		X	X	X			•	•	Λ	Λ	Λ
COM	X		X			X	X				•	•	Λ	Λ	1
CPX		X	X	X		X	X	X			•	•	Λ	Λ	
DEC	X		X			X	X				•	•	Λ	Λ	•
EOR		X	X	X		X	X	X			•	•	Λ	Λ	•
INC	X		X								•	•	Λ	Λ	•

TABLE 16. INSTRUCTION SET (Continued)

	ADDRESSING MODES										CONDITION CODES				
MNEM	INHERENT	IMMEDIATE	DIRECT	EXTENDED	RELATIVE	INDEXED (NO OFFSET)	INDEXED (8 BITS)	INDEXED (16 BITS)	BIT SET/ CLEAR	BIT TEST AND BRANCH	H	I	N	Z	C
JMP			X	X		X	X	X			•	•	•	•	•
JSR			X	X		X	X	X			•	•	•	•	•
LDA		X	X	X		X	X	X			•	•	Λ	Λ	•
LDX		X	X	X		X	X	X			•	•	Λ	Λ	•
LSL	X		X			X	X				•	•	Λ	Λ	Λ
LSR	X		X			X	X				•	•	0	Λ	Λ
MUL	X										0	•	•	•	0
NEG	X		X			X	X				•	•	Λ	Λ	Λ
NOP	X										•	•	•	•	•
ORA		X	X	X		X	X	X			•	•	Λ	Λ	•
ROL	X		X			X	X				•	•	Λ	Λ	Λ
ROR	X		X			X	X				•	•	Λ	Λ	Λ
RSP	X										•	•	•	•	•
RTI	X										?	?	?	?	?
RTS	X										•	•	•	•	•
SBC		X	X	X		X	X	X			•	•	Λ	Λ	Λ
SEC	X										•	•	•	•	1
SEI	X										•	1	•	•	•
STA			X	X		X	X	X			•	•	Λ	Λ	•
STOP	X										•	0	•	•	•
STX			X	X		X	X	X			•	•	Λ	Λ	•
SUB		X	X	X		X	X	X			•	•	Λ	Λ	Λ
SWI	X										•	1	•	•	•
TAX	X										•	•	•	•	•
TST	X		X			X	X				•	•	Λ	Λ	•
TXA	X										•	•	•	•	•
WAIT	X										•	0	•	•	•

Condition Code Symbols:

H = Half Carry (from Bit 3)

I = Interrupt Mask

N = Negate (Sign Bit)

Z = Zero 0 = Cleared

Λ = Test and Set if True Cleared Otherwise

• = Not Affected

? = Load CC Register From Stack

C = Carry/Borrow 1 = Set

TABLE 17. HCMOS INSTRUCTION SET OPCODE MAP

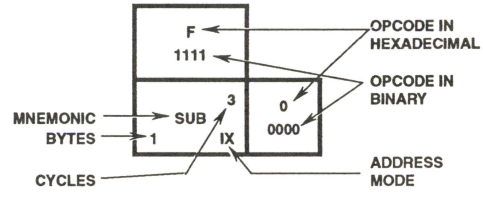
	BIT MANIPULATION		BRANCH	READ/MODIFY/WRITE					CONTROL		REGISTER/MEMORY						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
HI / LOW	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	HI / LOW
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 NH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0010	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0010
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DTR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0100	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0100
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INHY	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010

TABLE 17. HCMOS INSTRUCTION SET OPCODE MAP (Continued)

	BIT MANIPULATION		BRANCH	READ/MODIFY/WRITE					CONTROL		REGISTER/MEMORY						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
HI / LOW	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	HI / LOW
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes:
- INH = Inherent
- A = Accumulator
- X = Index Register
- IMM = Immediate
- DIR = Direct
- EXT = Extended
- REL = Relative
- BSC = Bit Set/Clear
- BTB = Bit Test and Branch

LEGEND



HARRIS SEMICONDUCTOR

HIP7038A8

PRELIMINARY

April 1994

J1850 8-Bit 68HC05 Microcontroller 8K EEPROM Version

Features

- Direct Replacement for HIP7030A2/A8 Microcontrollers
  - All Hardware and Software Features
  - Equivalent Timing and Performance
- Memory
  - 176 Bytes of RAM
  - 7744 Bytes of Programmable EEPROM
  - 242 Bytes of Bootstrap Program
- Single 5V Supply
- 10MHz Operating Frequency (5.0MHz Internal Bus Frequency) at 5V.
- 28 Lead Small Outline Ceramic Package
  - Same Terminal Assignment as HIP7030A2 and HIP7030A8

Description

The HIP7038A8 HCMOS Microcomputer is an EEPROM version of the HIP7030A family of low-cost single-chip J1850 microcontrollers. These microcontrollers provide the system designer with a complete set of building blocks for implementing a "Class B" VPW multiplexed communications network interface, which fully complies with SAE Recommended Practice J1850. The HIP7038A8 contains all hardware and software features of the HIP7030A2/A8 microcontrollers with equivalent timing, performance characteristics, and an identical footprint.

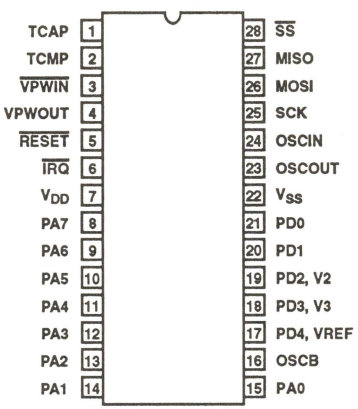
The device can be programmed using the HIP7038A8 EEPROM Programmer available from Harris. In-circuit Emulation Tools are also provided for system development.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP7038A8F	-40°C to +85°C	28 Lead Ceramic SOIC

Pinout

HIP7038A8 (SOIC FLATPACK)
TOP VIEW



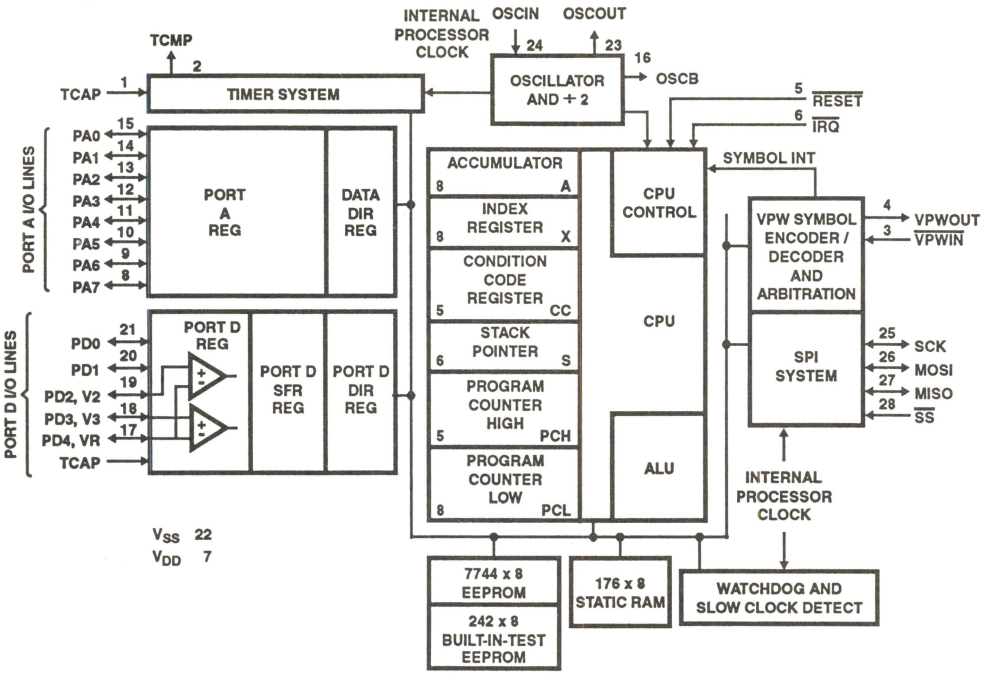
9 MULTIPLEX COMM. CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3647.1

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... -0.3V to +6.0V
Input or Output Voltage
Pins with V_{DD} Diode ..... -0.3V to V_{DD} +0.3V
Pins without V_{DD} Diode ..... -0.3V to +10.0V
Current Drain Per Pin, I (Excluding V_{DD} and V_{SS}) 25mA
ESD Classification ..... Class 2
Gate Count ..... 21000 Gates

Thermal Information

Operating Temperature Range (T_A) ..... -40°C to +125°C
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (During Soldering) ..... +265°C
1/16in. ± 1/32in. (1.59 ± 0.79mm) from case for 10s Max.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -40°C to +85°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... .(0.8•V_{DD}) to V_{DD}
Input Rise and Fall Time
CMOS Inputs ..... 100ns Max.
CMOS Schmitt Inputs ..... Unlimited

DC Electrical Specifications

V_{DD} = 5V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +85°C Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
RUN	I_{RUN}		-	50	-	mA
WAIT	I_{WAIT}		-	4	-	mA
STOP	I_{STOP}	T_A = +25°C	-	100	-	µA
		T_A = -40°C to +85°C	-	100	-	µA
Powerdown Input Voltage: $\overline{RESET}$, $\overline{IRQ}$, $\overline{VPWIN}$, OSCIN	V_{INPD}	V_{DD} = 0	-0.3	-	9	V

NOTE:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS}<(V_{IN} or V_{OUT})<V_{DD}. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Functional Description

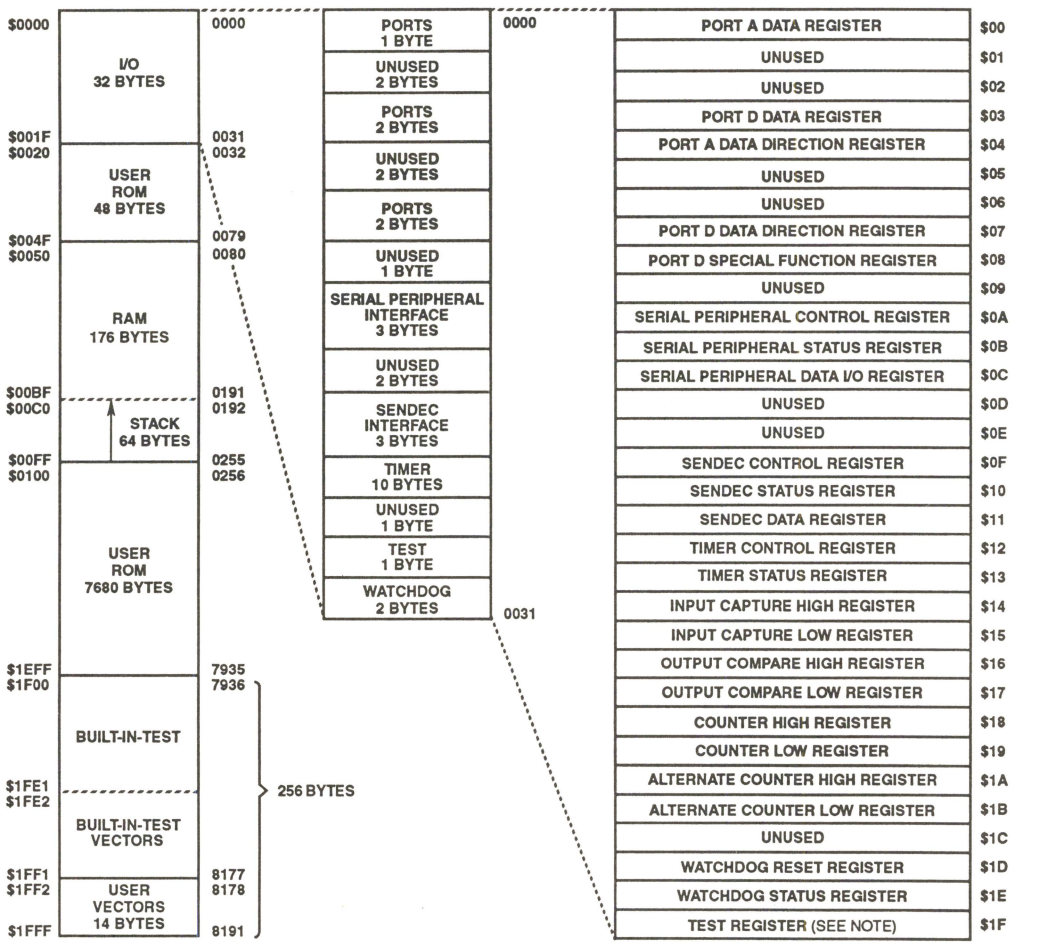
The HIP7038A8 MCU is functionally identical to the HIP7030A2 and HIP7030A8 microcontrollers. The device differs only in that the on-board masked ROM has been replaced with EEPROM, which allows the device to be rapidly programmed by the user. For detailed information about the functions included on the HIP7038A8 refer to File Number 3646, the technical specification of the HIP7030A2 Microcontroller. Only differences are presented here.

The availability of the HIP7038A8 dramatically reduces the time-to-market of new products by providing the development engineer rapid feedback during the design phase of a HIP7030A2/8 project.

The EEPROM is reusable and can be reprogrammed up to 10^4 times.

Memory Organization

The HIP7038A8 MCU addresses 8192 bytes of memory and I/O registers with its program counter. Of these locations, 8184 have been implemented as shown in Figure 1. The first 256 bytes of memory (page zero) include: 24 bytes of I/O features such as data ports, the port DDRs, Timer, serial peripheral interface (SPI), and J1850 VPW Registers; 48 bytes of user ROM, and 176 bytes of RAM. The next 7680 bytes complete the user ROM. The Built-In-Test ROM (242 bytes) is contained in memory locations $1F00 through $1FF1. The 14 highest address bytes contain the user defined reset and the interrupt vectors. Eight bytes of the lowest 32 memory locations are unused and the 176 bytes of user RAM include up to 64 bytes for the stack. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage.



NOTE: Accessable in test mode only.

FIGURE 1. MEMORY MAP OF THE HIP7038A8

INTELLIGENT POWER ICs 10

SPECIAL FUNCTIONS

		PAGE
SPECIAL FUNCTION IC SELECTION GUIDE		10-2
SPECIAL FUNCTION DATA SHEETS		
CA3020	Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz	10-3
CA3094	Programmable Power Switch/Amplifier for Control and General Purpose Applications	10-11
CA3165	Electronic Switching Circuit	10-25
CA3228	Speed Control System with Memory	10-31
CA3274	Current Limiting Power Switch with Current Limiter Sense Flag	10-40
HIP9010	Engine Knock Signal Processor	10-44
HIP9020	Programmable Quad Buffer with Pre and Post Scaler Dividers	10-54

Special Function IC Selection Guide

PART NUMBER	DESCRIPTION	MAX SUPPLY VOLTAGE	MAX SUPPLY CURRENT	SENSOR/INPUT RANGE	I_{OUT} MAX	V_{OUT} MAX
CA3165E CA3165E1	Electronic Switching Circuits for Ignition and Proximity Sensing in General Purpose Control Circuits Using Q-Loaded Inductive Sensor (Multiple Outputs).	24V	18.4mA	Q-Loaded Self-Osc. Coil Pickup (~100µH)	120mA (Sink)	24V
CA3228	Speed Control System for Cruise Control and General Purpose Rate or Motion Control Feedback Applications. Self-Contained Controller with 9 bit D/A Memory (Multiple Inputs and Outputs).	9V	30mA	Inductive Pickup with 3.5V to 15V Range (Ext. RC Filter, 8.2kΩ/ 0.05µF Interface)	8mA (Sink)	9V
CA3274	Power Switch with Current Limiting Feedback Control and Current Limiter Sense Flag. Used for Ignition and Current Controlled Switching Applications.	16V	25mA	0.4V to 2V Input Switching Thresholds (w/hysteresis)	200mA (Sink/ Source)	16V
HIP9010AB	Analog signal processing IC suitable for engine "Knock" detection. Extensive signal processing is achieved in the frequency and time domain within the IC via microprocessor control through a "SPI" interface bus.	Intended to operate from same power supply as a microcontroller with a maximum V_{DD} of 7V and has a maximum supply current of 12mA at 5V.		5mV to 8 V_{RMS} Input (from piezoelectric type sensors). In the application, the useful dynamic signal range is less.	Output signal, pin 4 INOUT, is an analog voltage that ranges from approximately V_{DD} to 0.5V.	
HIP9020AP HIP9020AB	Vehicle Speed Sensor (VSS) Buffer ICs with Pre and Post Scaler Dividers for processing Sinusoidal Waveforms from Magnetic Pickup Sensors with divide by 1, 6-11 Prescaling and 1, 2 Post Scaling Options (Multiple Ouputs).	Shunt Regulator ~5.6V with Series Forward Diode/Resistor to Power Supply (V_{BATT}); or Use Ext. 5 ±0.3V Power Supply (Max I_{CC} = 12mA)		±(0.25 to 100)V with 40kΩ Ext. Series Current Limiting Resistor to Input	15mA (Sink)	24V
CA3020 CA3020A	Multipurpose Differential Power Amplifier and Switch Control Circuit.	3V to 12V	35mA	±100mV	240mA	18V/25V
CA3094 CA3094A CA3094B	Multipurpose Differential Programmable Power Switch and Power Amplifier with 30MHz Unity Gain-BW.	To 44V	300mA	±100mV, (100dB Gain, Adj. with Operational Transconductance Amplifier Input)	To 300mA	To 44V

HARRIS SEMICONDUCTOR

CA3020

Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz

April 1994

Features

- High Power Output Class B Amplifier
  - CA3020 ..... 0.5W Typ. at V_{CC} = +9V
  - CA3020A ..... 1.0W Typ. at V_{CC} +12V
- Wide Frequency Range .. Up to 8MHz with Resistive Loads
- High Power Gain..... 75dB Typ.
- Single Power Supply For Class B Operation With Transformer
  - CA3020 ..... 3V to 9V
  - CA3020A ..... 3V to 12V
- Built-In Temperature-Tracking Voltage Regulator Provides Stable Operation Over -55°C to +125°C Temperature Range

Applications

- AF Power Amplifiers For Portable and Fixed Sound and Communications Systems
- Servo-Control Amplifiers
- Wide-Band Linear Mixers
- Video Power Amplifiers
- Transmission-Line Driver Amplifiers (Balanced and Unbalanced)
- Fan-In and Fan-Out Amplifiers For Computer Logic Circuits
- Lamp-Control Amplifiers
- Motor-Control Amplifiers
- Power Multivibrators
- Power Switches

Description

The CA3020 and CA3020A are integrated-circuit, multistage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1W from a 12VDC supply with a typical power gain of 75dB. The CA3020 provides 0.5W power output from a 9V supply with the same power gain.

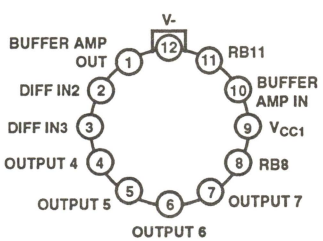
These types are supplied in hermetically sealed TO-101 style 12 lead metal cans. Refer to AN5766 for application information.

Ordering Information

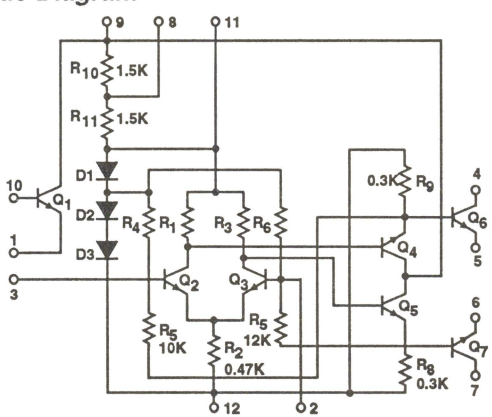
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3020	-55°C to +125°C	12 Pin Metal Can
CA3020A	-55°C to +125°C	12 Pin Metal Can

Pinout

CA3020 (CAN)
TOP VIEW



Schematic Diagram



The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as 30%.

Harris reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 339.3

Absolute Maximum Ratings

Maximum Pin 9 Supply Voltage, V_{CC1} (Note 1)
- CA3020 ..... +10V
- CA3020A ..... +12V

Maximum Pin 9 Supply Current, I_{CC1} 20mA
Maximum Pin 11 Sink Current, I_{11} 20mA
Output Voltage, V_4 and V_7 (Note 1)
- CA3020 ..... +25V
- CA3020A ..... +18V

Output Current, I_O 300mA
Input Voltage Range, V_2, V_3 ..... -2V to +2V
Maximum Input Voltage, V_{10} (Ref to Pin 1) ..... -3V
Maximum Source Current, V_1 ..... 1mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Metal Can Package	135°C/W	60°C/W

Power Dissipation Without Heat Sink
- At T_A = +25°C 1W
- Above T_A = +25°C ..... Derate Linearly 7.4mW/°C

Power Dissipation With Heat Sink
- At T_C = +25°C 2W
- At T_C = +25°C to T_C = +55°C 2W
- Above T_C = +55°C ..... Derate Linearly 16.7 mW/°C

Maximum Junction Temperature ..... +150°C
Operating Temperature Range ..... -55°C to +125°C
Storage Operating Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS: CIRCUIT AND PROCEDURE FIGURE	TEST CONDITIONS: DC SUPPLY VOLTAGE V_{CC1}	TEST CONDITIONS: DC SUPPLY VOLTAGE V_{CC2}	CA3020 MIN	CA3020 TYP	CA3020 MAX	CA3020A MIN	CA3020A TYP	CA3020A MAX	UNITS
Collector-to-Emitter Breakdown Voltage, Q_6 and Q_7 at 10mA	$V_{(BR)CER}$	1A	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 and Q_7	I_4 IDLE I_7 IDLE	7	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 and Q_7	I_4PK I_7PK	7	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 and Q_7	I_4 CUTOFF I_7 CUTOFF	7	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differential Amplifier Current Drain	I_{CC1}	7	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	7	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	7	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	7	9.0	2.0	-	2.35	-	-	2.35	-	V
Q_1 Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	µA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	µA
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	µA
Forward Current Transfer Ratio, Q_1 at 3mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3dB Point	BW	8	6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output for R_{CC} = 130Ω	$P_{O(MAX)}$	9	6.0	6.0	200	300	-	200	300	-	mW
		9	9.0	9.0	400	550	-	400	550	-	mW
Maximum Power Output for R_{CC} = 200Ω		9	9.0	12.0	-	-	-	800	1000	-	mW
Sensitivity for P_{OUT} = 400mW, R_{CC} = 130Ω	e_{IN}	9	9.0	9.0	-	35	55	-	-	-	mV
Sensitivity for P_{OUT} = 800mW, R_{CC} = 200Ω	e_{IN}	9	9.0	12.0	-	-	-	-	50	100	mV
Input Resistance - Terminal 3 to Ground	R_{IN3}	10	6.0	6.0	-	1000	-	-	1000	-	Ω

NOTE:
1. The voltage ratings for Pin 9, Pin 4 and Pin 7 are referenced to the V- (Pin 12). A normal bias configuration for Pin 8 and Pin 11 is shown in Figure 1B. Refer to Application Note AN5766 for other options.

Typical Performance Data (Note 1) A heat sink is recommended for high ambient temperature operation.

PARAMETERS		SYMBOL	CA3020	CA3020A	UNITS
Power Supply Voltage		V_{CC1}	9.0	9.0	V
		V_{CC2}	9.0	12.0	V
Zero Signal Current	Differential Amplifier	I_{CC1}	15	15	mA
	Output Amplifier	I_{CC2}	24	24	mA
Maximum Signal Current	Differential Amplifier	I_{CC1}	16	16.6	mA
	Output Amplifier	I_{CC2}	125	140	mA
Maximum Power Output at THD = 10%		PO	550	1000	mW
Sensitivity		e_{IN}	35	45	mV
Power Gain		G_P	75	75	dB
Input Resistance		R_{IN}	55	55	kΩ
Efficiency		η	45	55	%
Signal-to-Noise Ratio		S/N	70	66	dB
THD at 150mW Level			3.1	3.3	%
Test Signal Frequency from 600Ω Generator			1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance		R_{CC}	130	200	Ω

NOTE:

1. Refer to Figures 7 through 11 for measurement and symbol information.

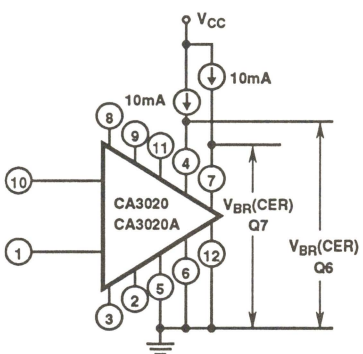


FIGURE 1A. COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE (Q6 AND Q7) CIRCUIT

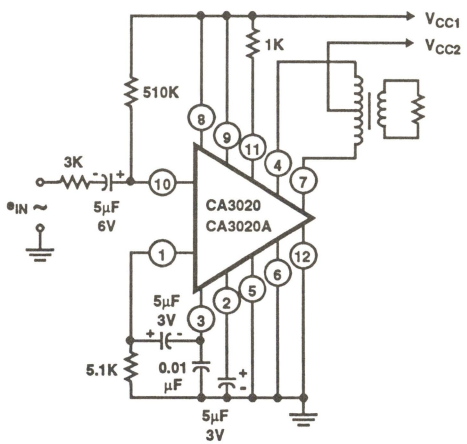


FIGURE 1B. TYPICAL AUDIO AMPLIFIER CIRCUIT UTILIZING THE CA3020 OR CA3020A AS AN AUDIO PREAMPLIFIER AND CLASS B POWER AMPLIFIER

FIGURE 1.

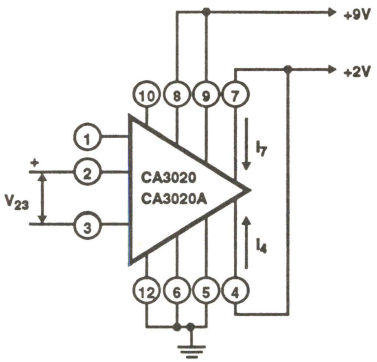


FIGURE 2A. TEST SETUP

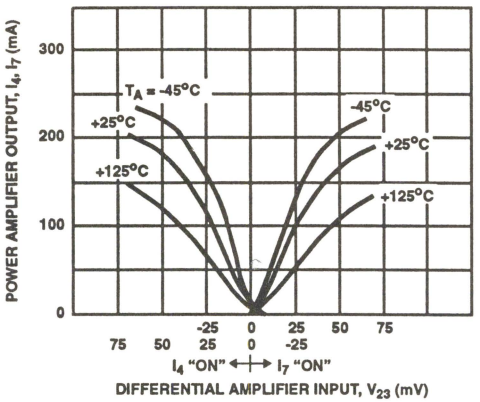


FIGURE 2B. CHARACTERISTICS WITH R_{10} SHORTED OUT

FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

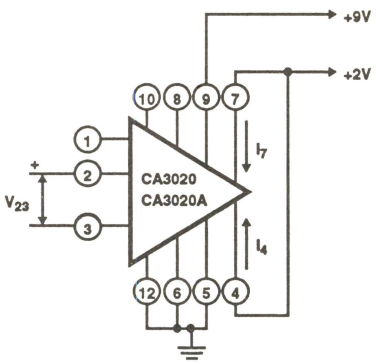


FIGURE 3A. TEST SETUP

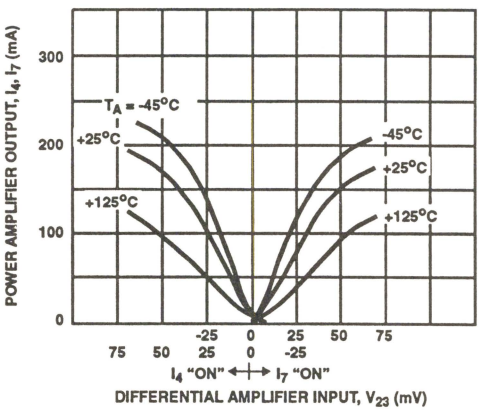


FIGURE 3B. CHARACTERISTIC WITH R_{10} IN CIRCUIT

FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS

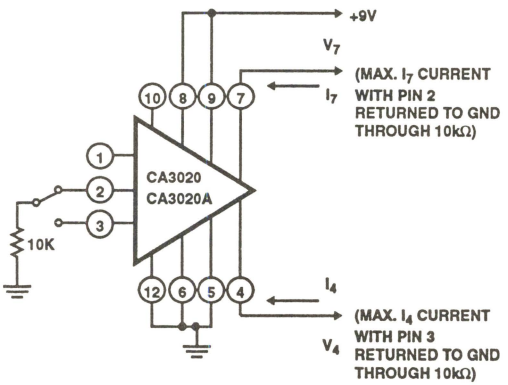


FIGURE 4A. TEST SETUP

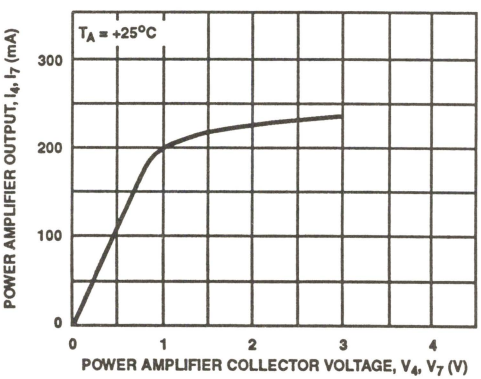


FIGURE 4B. CHARACTERISTIC

FIGURE 4. "MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE

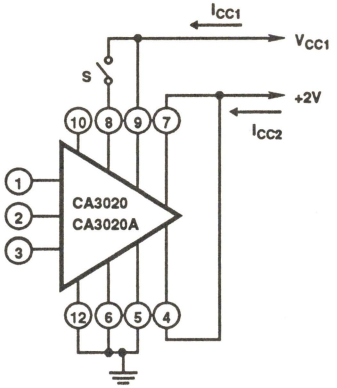


FIGURE 5A. TEST SETUP

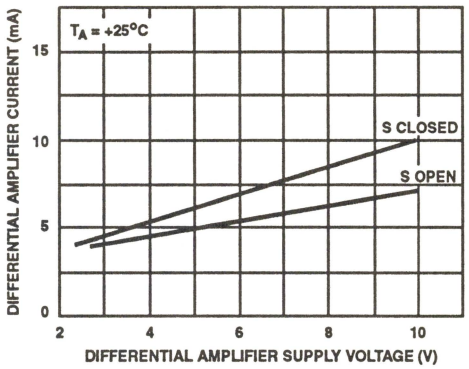


FIGURE 5B. DIFFERENTIAL AMPLIFIER CHARACTERISTICS OF I_{CC1} CURRENT vs V_{CC1} VOLTAGE

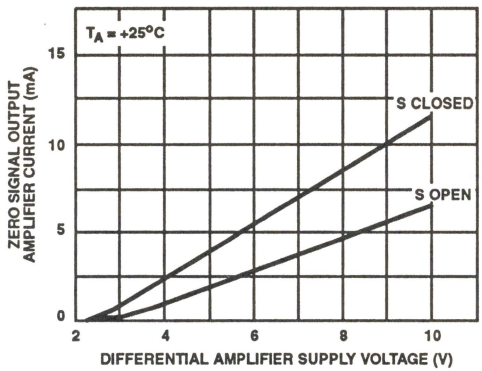


FIGURE 5C. OUTPUT AMPLIFIER CHARACTERISTICS OF I_{CC2} CURRENT vs V_{CC1} VOLTAGE

FIGURE 5. ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE

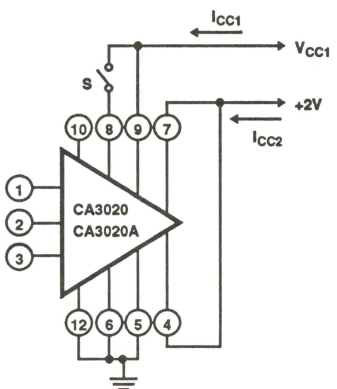


FIGURE 6A. TEST SETUP

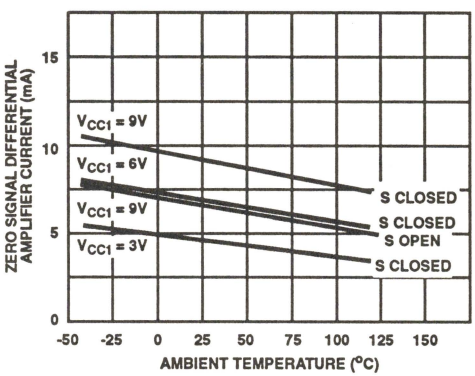


FIGURE 6B. DIFFERENTIAL AMPLIFIER CHARACTERISTICS OF I_{CC1} CURRENT vs AMBIENT TEMPERATURE

FIGURE 6. ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE

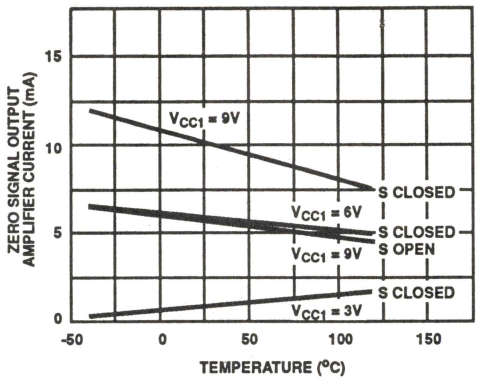
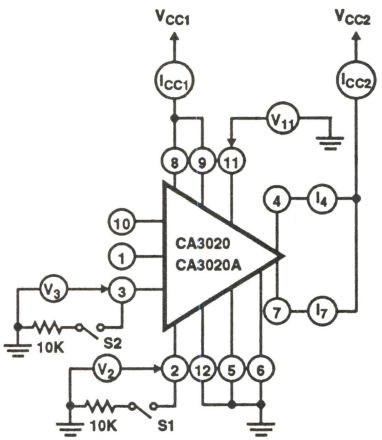


FIGURE 6C. OUTPUT AMPLIFIER CHARACTERISTICS OF I_{CC2} CURRENT vs AMBIENT TEMPERATURE

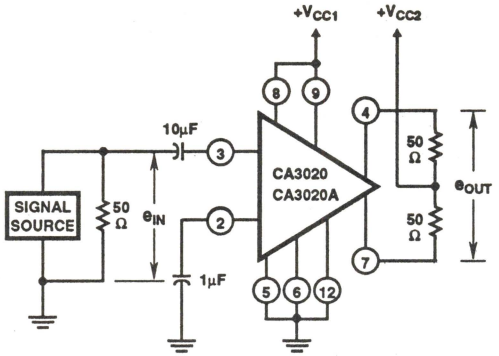
FIGURE 6. ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE (Continued)



CURRENTS OR VOLTAGES	S1	S2
I_4 -IDLE	OPEN	OPEN
I_7 -IDLE	OPEN	OPEN
I_4 -PEAK	OPEN	CLOSE
I_7 -PEAK	CLOSE	OPEN
I_4 -CUTOFF	CLOSE	OPEN
I_7 -CUTOFF	OPEN	CLOSE

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	OPEN	OPEN
I_{CC2}	OPEN	OPEN
V_2	OPEN	OPEN
V_3	OPEN	OPEN
V_{11}	OPEN	OPEN

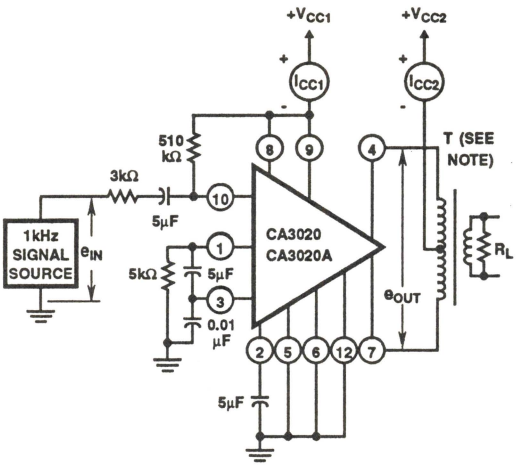
FIGURE 7. STATIC CURRENT AND VOLTAGE TEST CIRCUIT



PROCEDURES:

1. Apply desired value of V_{CC1} and V_{CC2}.
2. Apply 1kHz input signal and adjust for e_{IN} = 5mV (RMS).
3. Record the resulting value of e_{OUT} in dB (reference value).
4. Vary input-signal frequency, keeping e_{IN} constant at 5mV, and record frequencies above and below 1kHz at which e_{OUT} decreases 3dB below reference value.
5. Record bandwidth as frequency range between -3dB points.

FIGURE 8. MEASUREMENT OF BANDWIDTH AT -3dB POINTS



NOTE: Push-pull output transformer; load resistance (R_L) should be selected to provide indicated collector-to-collector load impedance (R_{CC}).

PROCEDURES:

1. Apply desired value of V_{CC1} and V_{CC2} and reduce e_{IN} to 0V.
2. Record resulting values of I_{CC1} and I_{CC2} in mA as Zero-Signal DC Current Drain.
3. Apply desired value of V_{CC1} and V_{CC2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%.
4. Record resulting value of I_{CC1} and I_{CC2} in mA as Maximum Signal DC Current Drain.
5. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT}).
6. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100\frac{P_{OUT}}{V_{CC1}I_{CC1} + V_{CC2}I_{CC2}}$$

where P_{OUT} is in watts, V_{CC1} and V_{CC2} are in volts, and I_{CC1} and I_{CC2} are in amperes.

7. Record value of e_{IN} in mV (rms) required in Step 3 as Sensitivity (e_{IN}).
8. Calculate Transducer Power Gain (G_p) in dB as follows:

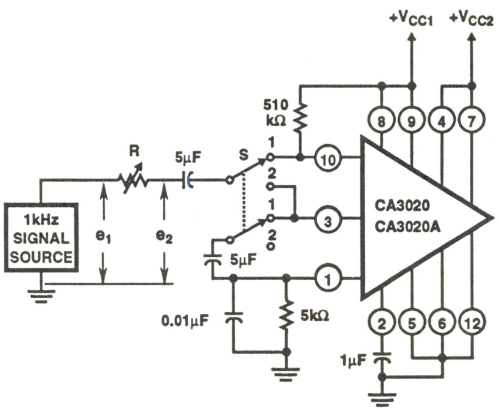
$$G_p = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

$$\text{where } P_{IN}\,(\text{in mW}) = \frac{e_{IN}^2}{3000 + R_{IN\,(10)\,(\text{Note 1})}}$$

NOTE:

1. See Figure 10 for definition of $R_{IN(10)}$.

FIGURE 9. MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



PROCEDURES:

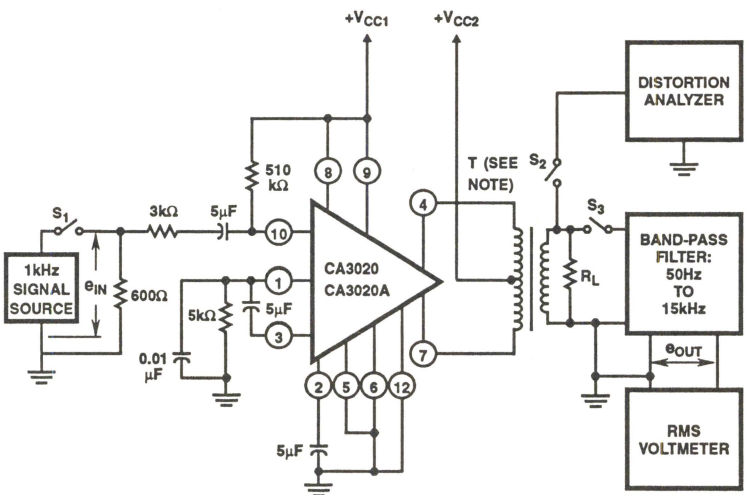
Input Resistance Terminal 10 to Ground (R_{IN10}).

1. Apply desired value of V_{CC1} and V_{CC2} and set S in Position 1.
2. Adjust 1kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$.
4. Record resulting value of R as R_{IN10}.

Input Resistance Terminal 3 to Ground (R_{IN3}).

1. Apply desired value of V_{CC1} and V_{CC2} and set S in Position 2.
2. Adjust 1kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$.
4. Record resulting value of R as R_{IN3}.

FIGURE 10. MEASUREMENT OF INPUT RESISTANCE



NOTE: Push-pull output transformer; load resistance (R_L) should be selected to provide indicated collector-to-collector load impedance (R_{CC}).

PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2.
2. Apply desired values of V_{CC1} and V_{CC2}.
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT1} (reference value).
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT2}
5. Signal-to-Noise Ratio $(S/N) = 20\log_{10}\frac{e_{OUT1}}{e_{OUT2}}$.

Total Harmonic Distortion

1. Close S1 and S2; open S3.
2. Apply desired values of V_{CC1} and V_{CC2}.
3. Adjust e_{IN} for desired level amplifier output power.
4. Record Total Harmonic Distortion (THD) in %.

FIGURE 11. MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION

HARRIS SEMICONDUCTOR

CA3094

Programmable Power Switch/Amplifier for Control and General Purpose Applications

April 1994

Features

- CA3094T, E, M for Operation Up to 24V
- CA3094AT, E, M for Operation Up to 36V
- CA3094BT, M for Operation Up to 44V
- Designed for Single or Dual Power Supply
- Programmable: Strobing, Gating, Squelching, AGC Capabilities
- Can Deliver 3W (Average) or 10W (Peak) to External Load (in Switching Mode)
- High Power, Single Ended Class A Amplifier will Deliver Power Output of 0.6W (1.6W Device Dissipation)
- Total Harmonic Distortion (THD) at 0.6W in Class A Operation 1.4% (Typ.)

Applications

- Error Signal Detector: Temperature Control with Thermistor Sensor; Speed Control for Shunt Wound DC Motor
- Over Current, Over Voltage, Over Temperature Protectors
- Dual Tracking Power Supply with CA3085
- Wide Frequency Range Oscillator
- Analog Timer
- Level Detector
- Alarm Systems
- Voltage Follower
- Ramp Voltage Generator
- High Power Comparator
- Ground Fault Interrupter (GFI) Circuits

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3094T, AT, BT	-55°C to +125°C	8 Lead Metal Can
CA3094E, AE, BE	-55°C to +125°C	8 Lead Plastic DIP
CA3094M, AM, BA	-55°C to +125°C	8 Lead Plastic SOIC (N)

Description

The CA3094 is a differential input power control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional control output signal up to 100mA. This signal is sufficient to directly drive high current thyristors, relays, DC loads, or power transistors. The CA3094 has the generic characteristics of the CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100mA.

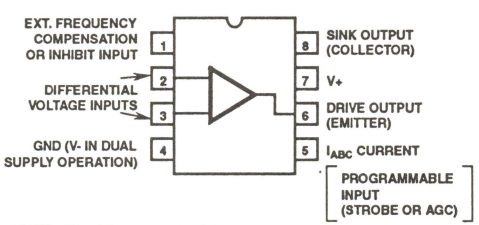
The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100μA, a 1mV change at the input will change the output from 0 to 100μA (typical).

The CA3094 is intended for operation up to 24V and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24V is a primary design requirement (see Figures 28, 29 and 30 in Typical Applications text). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36V and 44V, respectively (single or dual supply).

These types are available in 8 lead TO-99 Metal Cans ("T" suffix). Type CA3094 is also available in an 8 lead dual-in-line plastic DIP package ("E" suffix) and Small Outline Package ("M" suffix).

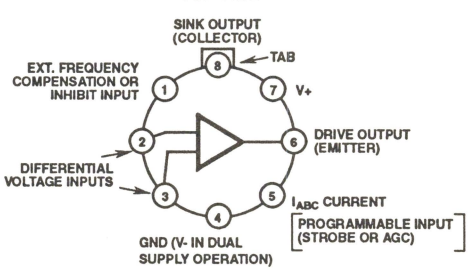
Pinouts

CA3094 (PDIP, SOIC)
TOP VIEW



NOTE: Pin 4 is connected to case

CA3094 (CAN)
TOP VIEW



10 SPECIAL FUNCTIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 598.3

Absolute Maximum Ratings

Dual Supply Voltage
- CA3094 ..... ±12V
- CA3094A ..... ±18V
- CA3094B ..... ±22V

Single Supply Voltage
- CA3094 ..... 24V
- CA3094A 36V
- CA3094B 44V

Differential Input Voltage (Term. 2 and 3) Note 1 ..... 5V
DC Input Voltage ..... V+ to V-
Input Current (Term. 2 and 3) ..... ±1mA
Amplifier Bias Current (Term. 5) 2mA
Average Output Current 100mA
Peak Output Current 300mA

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	150°C/W	-
Plastic SOIC Package	170°C/W	-
Metal Can	156°C/W	68°C/W

Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10s) ..... +300°C
(SOIC - Lead Tips Only)
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C for Equipment Design. Single Supply V+ = 30V, Dual Supply V+ = 15V, V- = -15V, I_{ABC} = 100µA Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT PARAMETERS						
Input Offset Voltage	V_{IO}	T_A = +25°C	-	0.4	5.0	mV
		T_A = 0°C to +70°C	-	-	7.0	mV
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	Change in V_{IO} between I_{ABC} = 100µA and I_{ABC} = 5µA	-	1	8.0	mV
Input Offset Current	I_{IO}	T_A = +25°C	-	0.02	0.2	µA
		T_A = 0°C to +70°C	-	-	0.3	µA
Input Bias Current	I_I	T_A = +25°C	-	0.2	0.50	µA
		T_A = 0°C to +70°C	-	-	0.70	µA
Device Dissipation	P_D	I_{OUT} = 0mA	8	10	12	mW
Common Mode Rejection Ratio	CMRR		70	110	-	dB
Common Mode Input Voltage Range	V_{ICR}	V+ = 30V (High)	27	28.8	-	V
		V- = 0V (Low)	1.0	0.5	-	V
		V+ = 15V	12	13.8	-	V
		V- = -15V	-14	-14.5	-	V
Unity Gain Bandwidth	f_T	I_C = 7.5mA, V_{CE} = 15V, I_{ABC} = 500µA	-	30	-	MHz
Open Loop Bandwidth at -3dB Point	BW_{OL}	I_C = 7.5mA, V_{CE} = 15V, I_{ABC} = 500µA	-	4	-	kHz
Total Harmonic Distortion (Class A Operation)	THD	P_D = 220mW	-	0.4	-	%
		P_D = 600mW	-	1.4	-	%
Amplifier Bias Voltage (Terminal 5 to Terminal 4)	V_{ABC}		-	0.68	-	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$		-	4	-	µV/°C
Power Supply Rejection	$\Delta V_{IO}/\Delta V$		-	15	150	µV/V
1/F Noise Voltage	E_N	f = 10Hz, I_{ABC} = 50µA	-	18	-	$nV/\sqrt{Hz}$
1/F Noise Current	I_N	f = 10Hz, I_{ABC} = 50µA	-	1.8	-	$pA/\sqrt{Hz}$
Differential Input Resistance	R_I	I_{ABC} = 20µA	0.50	1.0	-	MΩ
Differential Input Capacitance	C_I	f = 1MHz, V+ = 30V	-	2.6	-	pF
OUTPUT PARAMETERS (Differential Input Voltage = 1V)						

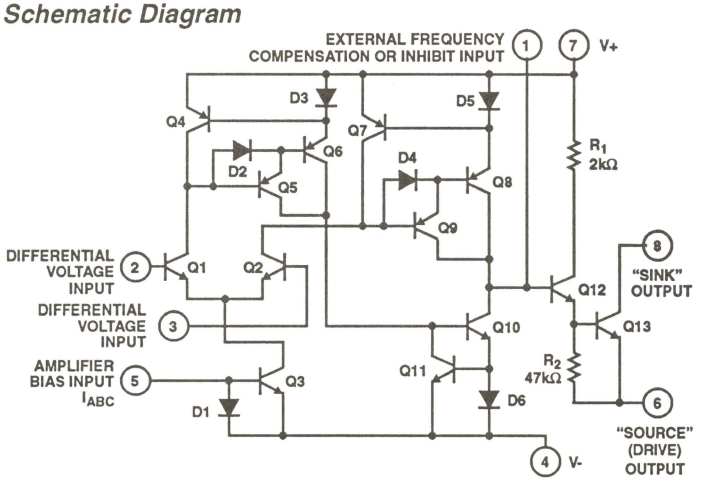
Electrical Specifications T_A = +25°C for Equipment Design. Single Supply V+ = 30V, Dual Supply V+ = 15V, V- = -15V, I_{ABC} = 100µA Unless Otherwise Specified **(Continued)**

PARAMETERS		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak Output Voltage (Terminal 6)	With Q13 "ON"	V+OM	V+ = 30V, R_L = 2kΩ to GND	26	27	-	V
	With Q13 "OFF"	V-OM		-	0.01	0.05	V
Peak Output Voltage (Terminal 6)	Positive	V+OM	V+ = 15V, V- = -15V, R_L = 2kΩ to -15V	11	12	-	V
	Negative	V-OM		-	-14.99	-14.95	V
Peak Output Voltage (Terminal 8)	With Q13 "OFF"	V+OM	V+ = 30V, R_L = 2kΩ to 30V	29.95	29.99	-	V
	With Q13 "ON"	V-OM		-	0.040	-	V
Peak Output Voltage (Terminal 8)	Positive	V+OM	V+ = 15V, V- = -15V, R_L = 2kΩ to 15V	14.95	14.99	-	V
	Negative	V-OM		-	-14.96	-	V
Collector-to-Emitter Saturation Voltage (Terminal 8)		$V_{CE(SAT)}$	V+ = 30V, I_C = 50mA, Terminal 6 Grounded	-	0.17	0.80	V
Output Leakage Current (Terminal 6 to Terminal 4)			V+ = 30V	-	2	10	µA
Composite Small Signal Current Transfer Ratio (Beta) (Q12 and Q13)		h_{FE}	V+ = 30V, V_{CE} = 5V, I_C = 50mA	16,000	100,000	-	
Output Capacitance	Terminal 6	C_O	f = 1MHz, All remaining Terminals Tied to Terminal 4	-	5.5	-	pF
	Terminal 8			-	17	-	pF
TRANSFER PARAMETERS							
Voltage Gain		A	V+ = 30V, I_{ABC} = 100µA, ΔV_{OUT} = 20V, R_L = 2kΩ	20,000	100,000	-	V/V
				86	100	-	dB
Forward Transconductance to Terminal 1		g_M		1650	2200	2750	µmhos
Slew Rate (Open Loop)	Positive Slope	SR	I_{ABC} = 500µA, R_L = 2kΩ	-	500	-	V/µs
	Negative Slope			-	50	-	V/µs
Unity Gain (Non-Inverting Compensated)			I_{ABC} = 500µA, R_L = 2kΩ	-	0.70	-	V/µs

NOTE:

1. Exceeding this voltage rating will not damage the device unless the peak input signal current (1mA) is also exceeded.

Schematic Diagram



OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"Source"	6	2	3
"Sink"	8	3	2

10 SPECIAL FUNCTIONS

Typical Performance Curves

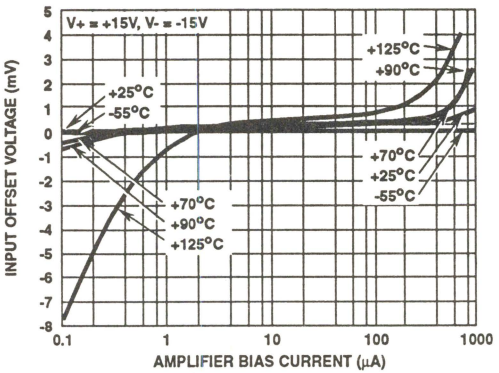


FIGURE 1. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

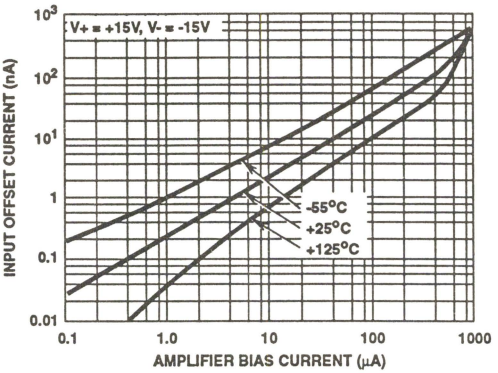


FIGURE 2. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

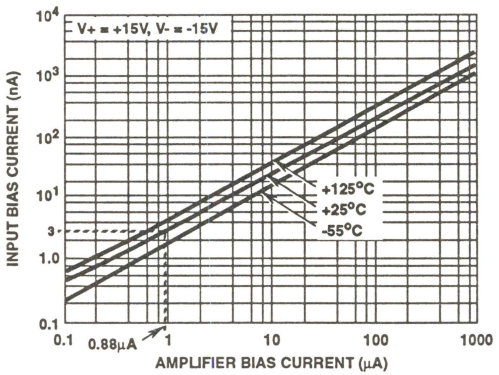


FIGURE 3. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

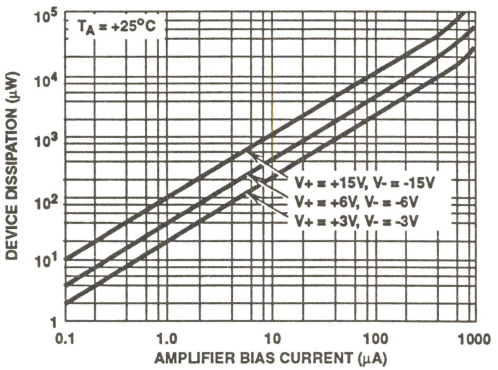


FIGURE 4. DEVICE DISSIPATION vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

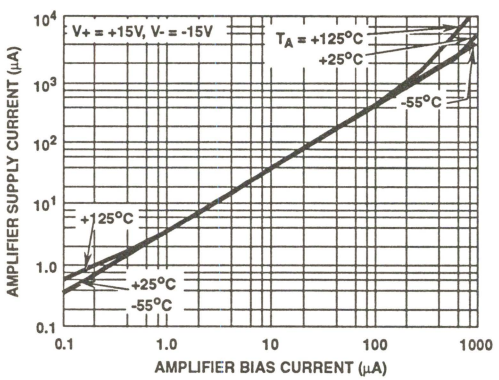


FIGURE 5. AMPLIFIER SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

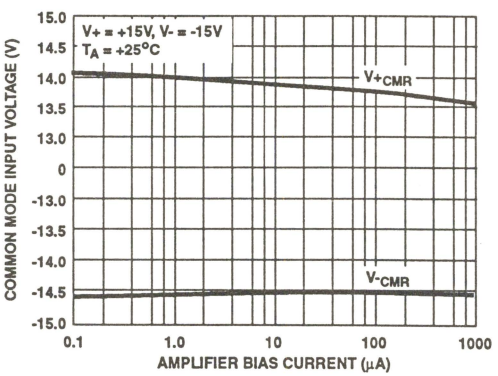


FIGURE 6. COMMON MODE INPUT VOLTAGE vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

Typical Performance Curves (Continued)

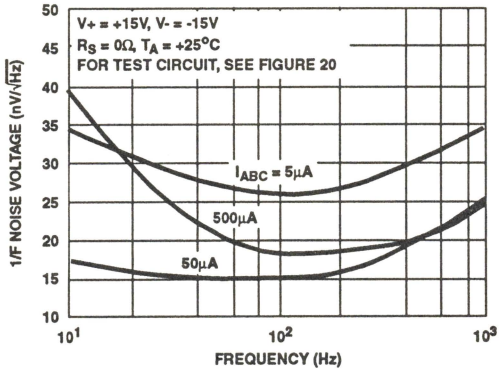


FIGURE 7. 1/F NOISE VOLTAGE vs FREQUENCY

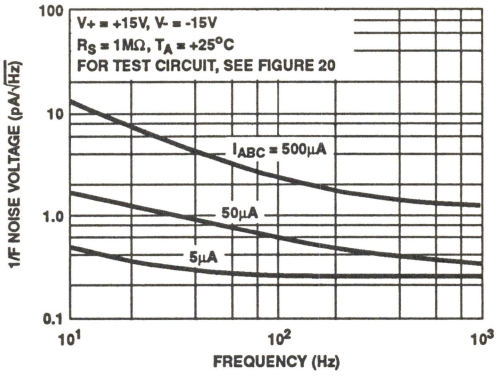


FIGURE 8. 1/F NOISE CURRENT vs FREQUENCY

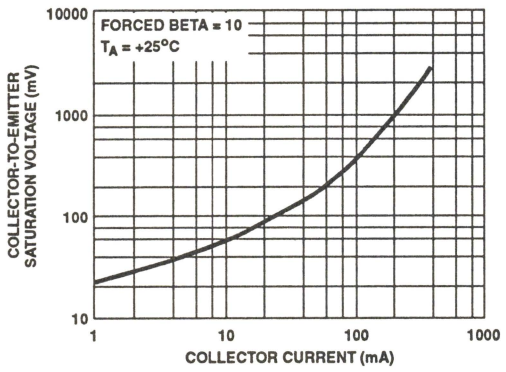


FIGURE 9. COLLECTOR EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT OF OUTPUT TRANSISTOR (Q13)

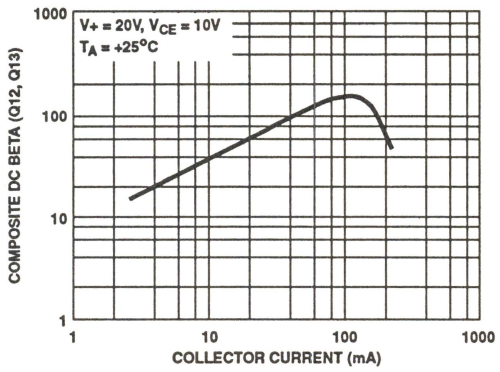


FIGURE 10. COMPOSITE DC BETA vs COLLECTOR CURRENT OF DARLINGTON CONNECTED OUTPUT TRANSISTORS (Q12, Q13)

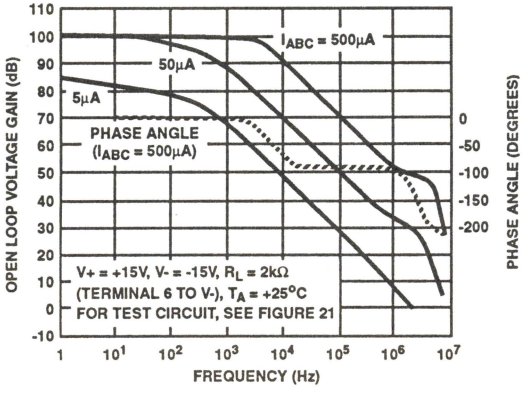


FIGURE 11. OPEN LOOP VOLTAGE GAIN vs FREQUENCY

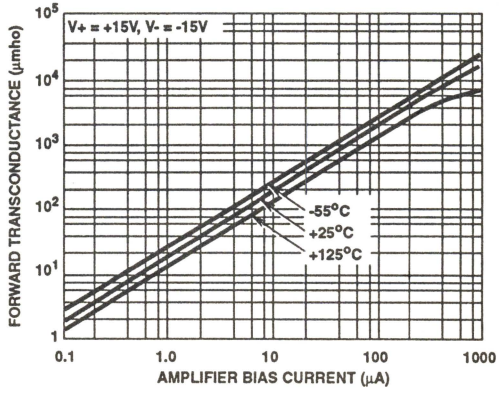


FIGURE 12. FORWARD TRANSCONDUCTANCE vs AMPLIFIER BIAS CURRENT

10 SPECIAL FUNCTIONS

Typical Performance Curves (Continued)

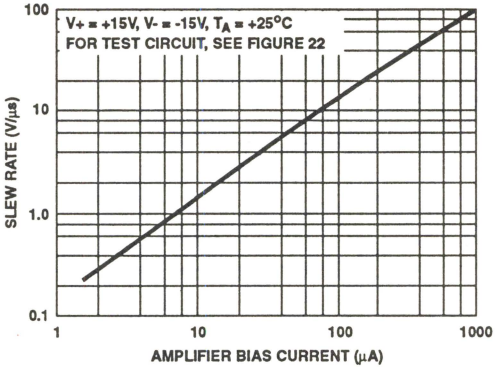


FIGURE 13. SLEW RATE vs AMPLIFIER BIAS CURRENT

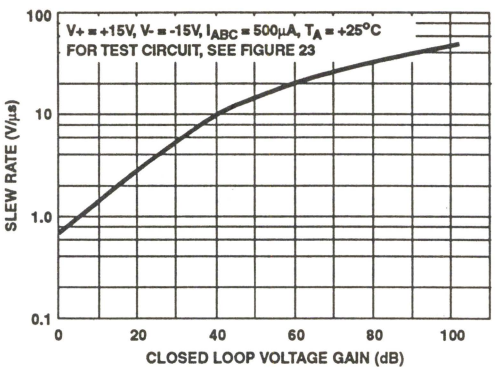


FIGURE 14. SLEW RATE vs CLOSED LOOP VOLTAGE GAIN

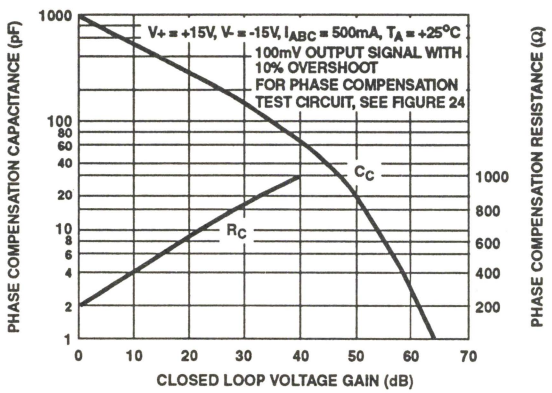


FIGURE 15. PHASE COMPENSATION CAPACITANCE AND RESISTANCE vs CLOSED LOOP VOLTAGE GAIN

Operating Considerations

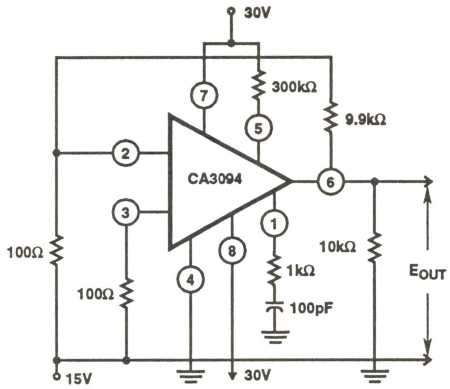
The "Sink" Output (Terminal 8) and the "Drive" Output (Terminal 6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between Terminal 6 and Terminal 4 (V- or Ground), it is important to connect a current limiting resistor between Terminal 8 and Terminal 7 (V+) to protect transistor Q13 under shorted load conditions. Similarly, if a load is connected between Terminal 8 and Terminal 7 (V+), the current limiting resistor should be connected between Terminal 6 and Terminal 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100Ω current limiting resistor be inserted between Terminal 7 and the V+ supply.

Test Circuits

1/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Figure 20. This circuit is a 30dB, non-inverting amplifier with emitter follower output and phase compensation from Terminal 2 to ground. Source resistors (R_S) are set to 0Ω or 1MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10Hz, 100Hz and 1kHz with a 1Hz measurement bandwidth. Typical values for 1/f noise at 10Hz and 50μA I_{ABC} are $E_N = 18nV/\sqrt{Hz}$ and $I_N = 1.8pA/\sqrt{Hz}$.

Test Circuits



NOTES:

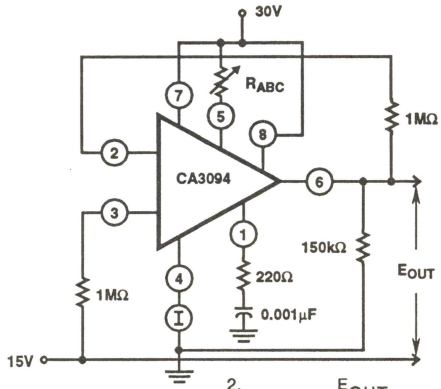
1. Input Offset Voltage: $V_{IO} = \frac{E_{OUT}}{100}$.
2. For Power Supply Rejection Test: (1) vary V+ by -2V; then (2) vary V- by +2V.
3. Equations:

   (1) V+ Rejection $= \frac{E_0OUT - E_1OUT}{200}$

   (2) V- Rejection $= \frac{E_0OUT - E_2OUT}{200}$
4. Power Supply Rejection: dB) $= 20\log \frac{1}{V_{REJECTION}}$.

† Maximum Reading of Step 1 or Step 2

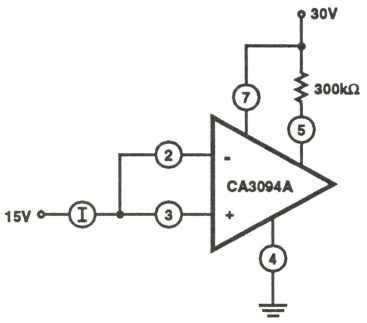
FIGURE 16. INPUT OFFSET VOLTAGE AND POWER SUPPLY REJECTION TEST CIRCUIT



NOTES:

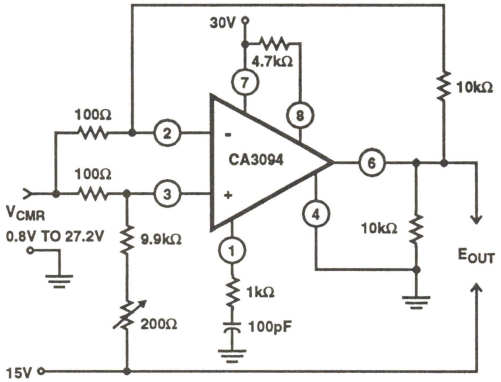
1. $P_{DISSIPATION} = (V+)(I)$
2. $I_{OS} = \frac{E_{OUT}}{10^6 \frac{VOLTS}{AMPS}}$

FIGURE 17. INPUT OFFSET CURRENT TEST CIRCUIT



NOTE: $I_I = \frac{I}{2}$

FIGURE 18. INPUT BIAS CURRENT TEST CIRCUIT

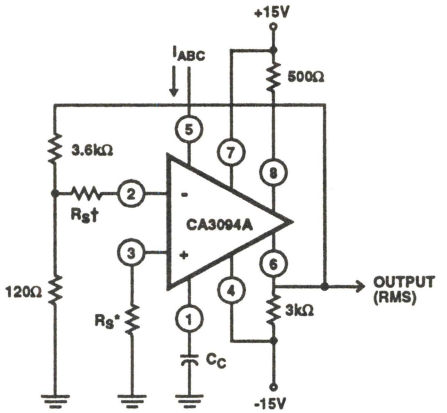


NOTES:

1. CMRR $= \left| \frac{100 \times 26V}{E_{2OUT} - E_{1OUT}} \right|$.
2. Input Voltage Range for CMRR = 1V to 27V.
3. CMRR (dB) $= 20\log \left| \frac{100 \times 26V}{E_{2OUT} - E_{1OUT}} \right|$.

FIGURE 19. COMMON MODE RANGE AND REJECTION RATIO TEST CIRCUIT

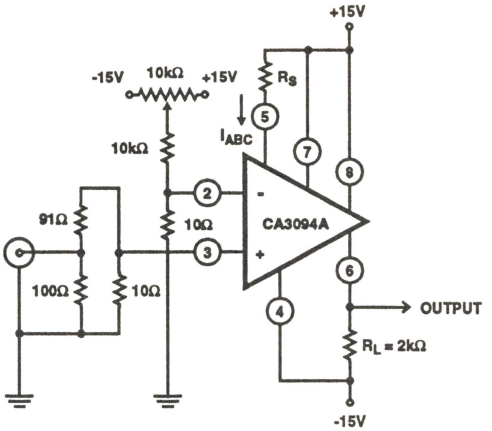
Test Circuits (Continued)



I_{ABC} (μA)	C_{COMP} (pF)
5	0
50	50
500	500

NOTES:
1. R_S† = 1MΩ (1/F Noise Current Test)
2. R_S = 0Ω (1/F Noise Voltage Test)

FIGURE 20. 1/F NOISE TEST CIRCUIT



R_S (Ω)	I_{ABC} (μA)
56K	500
560K	50
56M	5

FIGURE 21. OPEN LOOP GAIN vs FREQUENCY TEST CIRCUIT

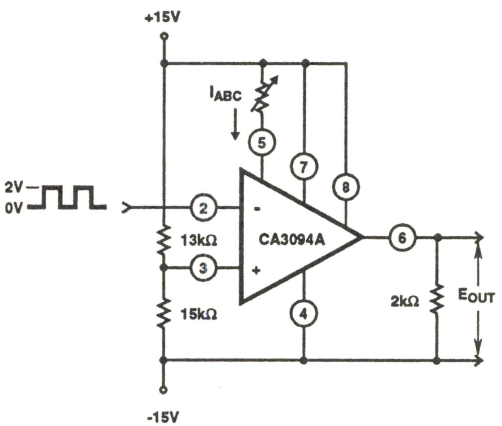


FIGURE 22. OPEN LOOP SLEW RATE vs I_{ABC} TEST CIRCUIT

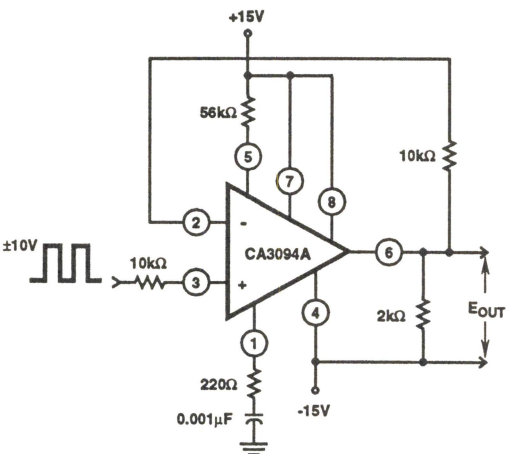
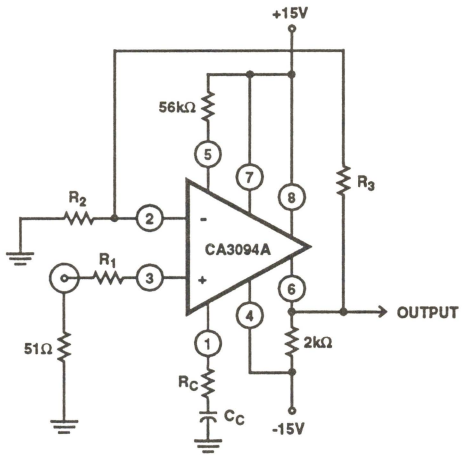


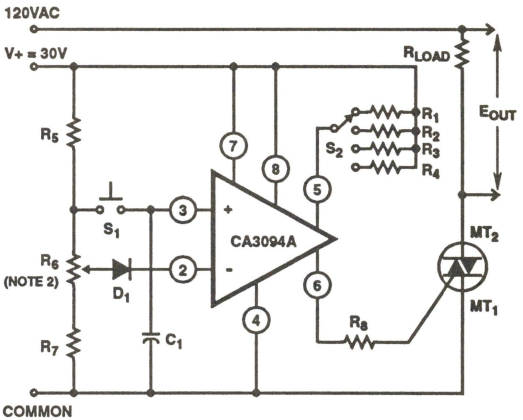
FIGURE 23. SLEW RATE vs NON-INVERTING UNITY GAIN TEST CIRCUIT

Test Circuits (Continued)



CLOSED LOOP GAIN (dB)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)
0	10	∞	10
20	10	1	10
40	1	0.1	10

FIGURE 24. PHASE COMPENSATION TEST CIRCUIT



NOTES:

1. $C_1 = 0.5\mu F$
   $D_1 = 1N914$
   $R_1 = 0.51M\Omega$ = 3 min.
   $R_2 = 5.1M\Omega$ = 30 min.
   $R_3 = 22M\Omega$ = 2 hrs.
   $R_4 = 44M\Omega$ = 4 hrs.
   $R_5 = 1.5k\Omega$
   $R_6 = 50k\Omega$
   $R_7 = 5.1k\Omega$
   $R_8 = 1.5k\Omega$
2. Potentiometer required for initial time set to permit device interconnecting. Time variation with temperature < 0.3%/°C.

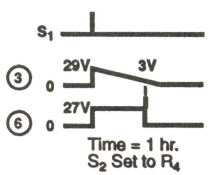


FIGURE 25. PRESETTABLE ANALOG TIMER

Typical Applications

For additional application information, refer to Application Note AN6048, "Some Applications of a Programmable Power/Switch Amplifier IC" and AN6077 "An IC Operational Transconductance Amplifier (OTA) with Power Capability".

Design Considerations

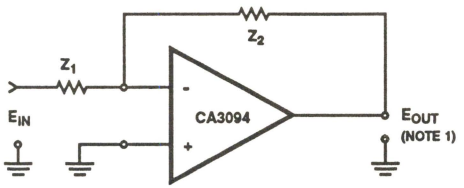
The selection of the optimum amplifier bias current (I_{ABC}) depends on:

1. The Desired Sensitivity - The higher the I_{ABC}, the higher the sensitivity, i.e., a greater drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance - The lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and required input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

Typical Applications



Where $\frac{E_{OUT}}{E_{IN}} = f\left(\frac{Z_2}{Z_1}\right)$ depends on the characteristics of Z1 and Z2

FIGURE 26A.

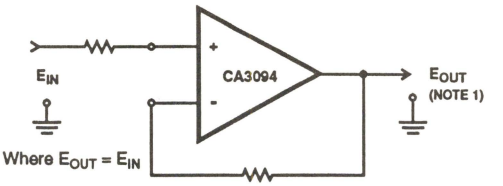
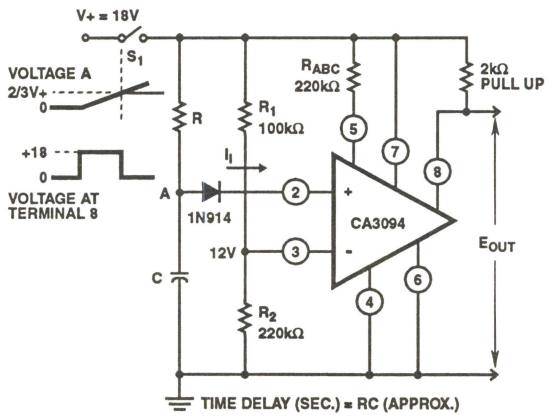


FIGURE 26B.

NOTE: 1. In single-ended output operation, the CA3094 may require a pull up or pull down resistor

FIGURE 26. APPLICATION OF THE CA3094: (a) AS AN INVERTING OP AMP AND (b) IN A NON-INVERTING MODE, AS A FOLLOWER



Problem: To calculate the maximum value of R required to switch a 100mA output current comparator

Given: $I_{ABC} = 5\mu A$, $R_{ABC} = 3.6M\Omega \approx \frac{18V}{5\mu A}$

$I_I = 500nA$ at $I_{ABC} = 100\mu A$ (from Figure 3)

$I_I = 5\mu A$ can be determined by drawing a line on Figure 3 through $I_{ABC} = 100\mu A$ and $I_B = 500nA$ parallel to the typical $T_A = +25°C$ curve.

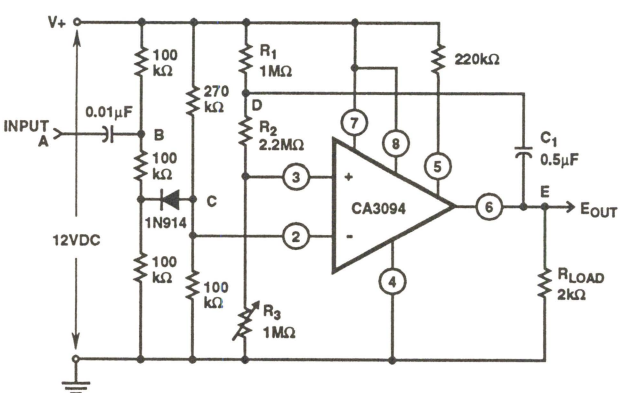
Then: $I_I = 33nA$ at $I_{ABC} = 5\mu A$

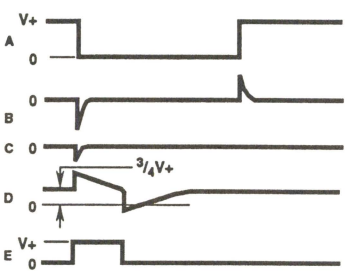
$$R_{MAX} = \frac{18V - 12V}{33nA} = 180M\Omega \text{ at } T_A = +25°C$$

$$R_{MAX} = 180M\Omega \times 2/3\dagger = 120M\Omega \text{ at } T_A = -55°C$$

† Ratio of I_I at $T_A = +25°C$ to I_I at $T_A = -55°C$ for any given value of I_{ABC}

FIGURE 27. RC TIMER





On a negative going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.

At the end of the time constant determined by C1, R1, R2, R3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input (A) returns to a high level.

FIGURE 28. RC TIMER TRIGGERED BY EXTERNAL NEGATIVE PULSE

Typical Applications (Continued)

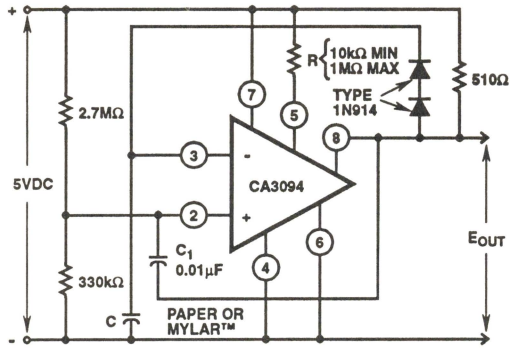


FIGURE 29. FREE RUNNING PULSE GENERATOR

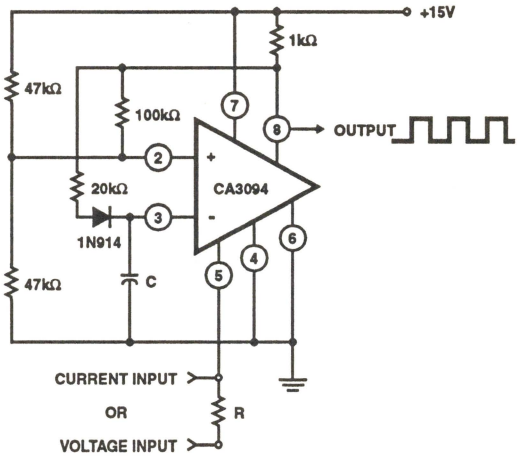


FIGURE 30. CURRENT OR VOLTAGE CONTROLLED OSCILLATOR

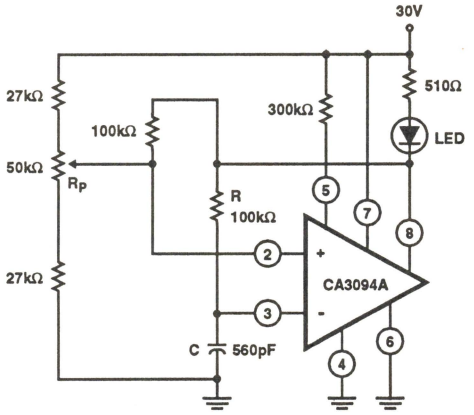
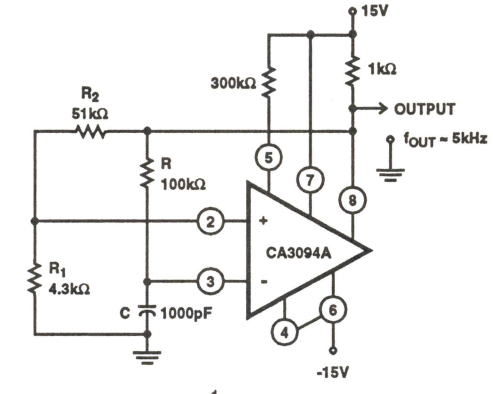


FIGURE 31. SINGLE SUPPLY ASTABLE MULTIVIBRATOR



NOTE: $f_{OUT} = \dfrac{1}{2RC \ln\left(\dfrac{2R_1}{R_2} + 1\right)}$

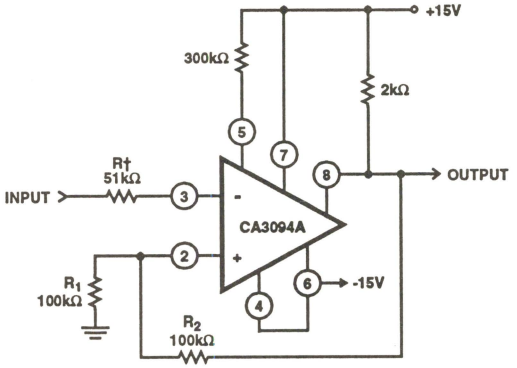
If: $R_2 = 3.08R_1$, $f_{OUT} = \dfrac{1}{RC}$

FIGURE 32. DUAL SUPPLY ASTABLE MULTIVIBRATOR

10 SPECIAL FUNCTIONS

Mylar™ is a trademark of E.I. Dupont de Nemours.

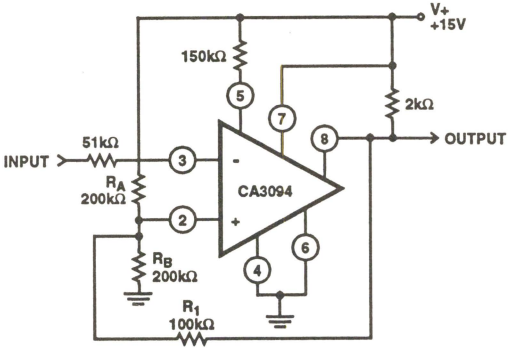
Typical Applications (Continued)



NOTES:

1. $R\dagger = \dfrac{R_1 R_2}{R_1 + R_2}$

2. $\pm\text{Threshold} = [\pm\text{Supply}]\left[\dfrac{R_1}{R_1 + R_2}\right]$



NOTES:

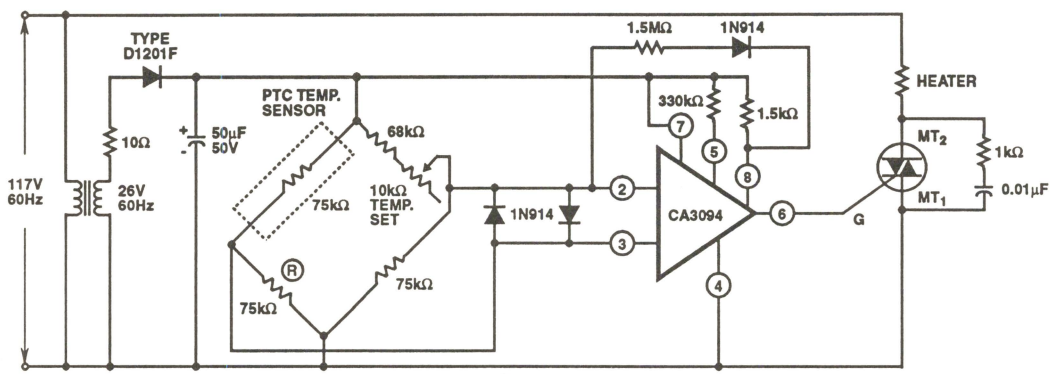
1. Upper Threshold $= [V+]\left[\dfrac{R_B}{\left(\dfrac{R_1 R_A}{R_1 + R_A}\right) + R_B}\right]$

2. Lower Threshold $= [V+]\left[\dfrac{\dfrac{R_1 R_B}{R_1 + R_B}}{\left(\dfrac{R_1 R_B}{R_1 + R_B}\right) + R_A}\right]$

FIGURE 33A. DUAL SUPPLY

FIGURE 33B. SINGLE SUPPLY

FIGURE 33. COMPARATORS (THRESHOLD DETECTORS) DUAL AND SINGLE SUPPLY TYPES

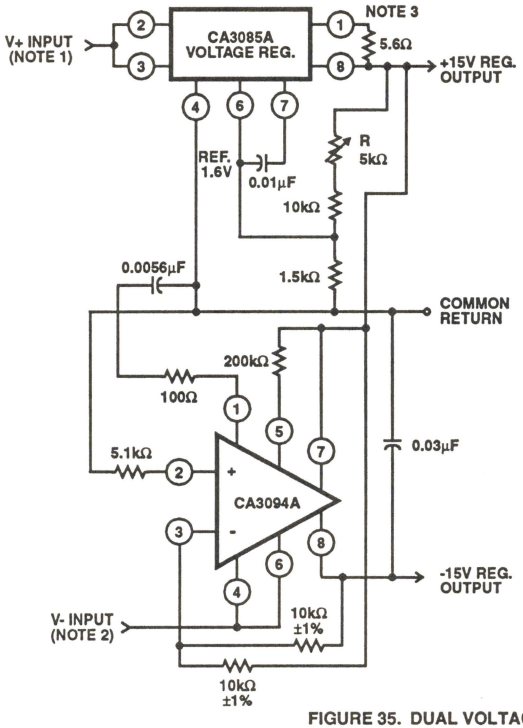


FOR NTC SENSOR, INTERCHANGE POSITION OF SENSOR AND Ⓡ.

NOTE: All Resistors are 1/2W.

FIGURE 34. TEMPERATURE CONTROLLER

Typical Applications (Continued)



NOTES:

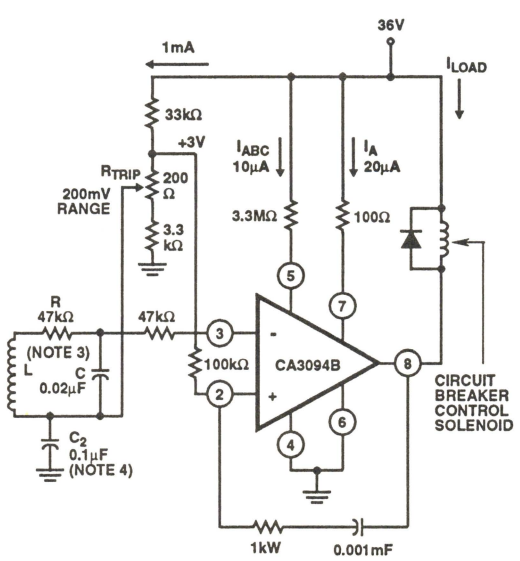
1. V+ Input Range = 19V to 30V for 15V output.
2. V- Input Range = -16V to -30V for -15V output.
3. Max I_{OUT} = ±100mA.
4. Regulation:

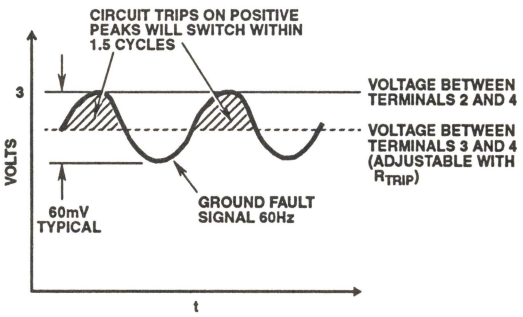
$$\text{Max Line} = \frac{\Delta V_{OUT}}{[V_{OUT}(\text{Initial})]\,\Delta V_{IN}} \times 100 = 0.075\%/V$$

$$\text{Max. Load} = \frac{\Delta V_{OUT}}{V_{OUT}(\text{Initial})} \times 100 = 0.075\%\ V_{OUT}$$

(IL from 1mA to 50mA)

FIGURE 35. DUAL VOLTAGE TRACKING REGULATOR



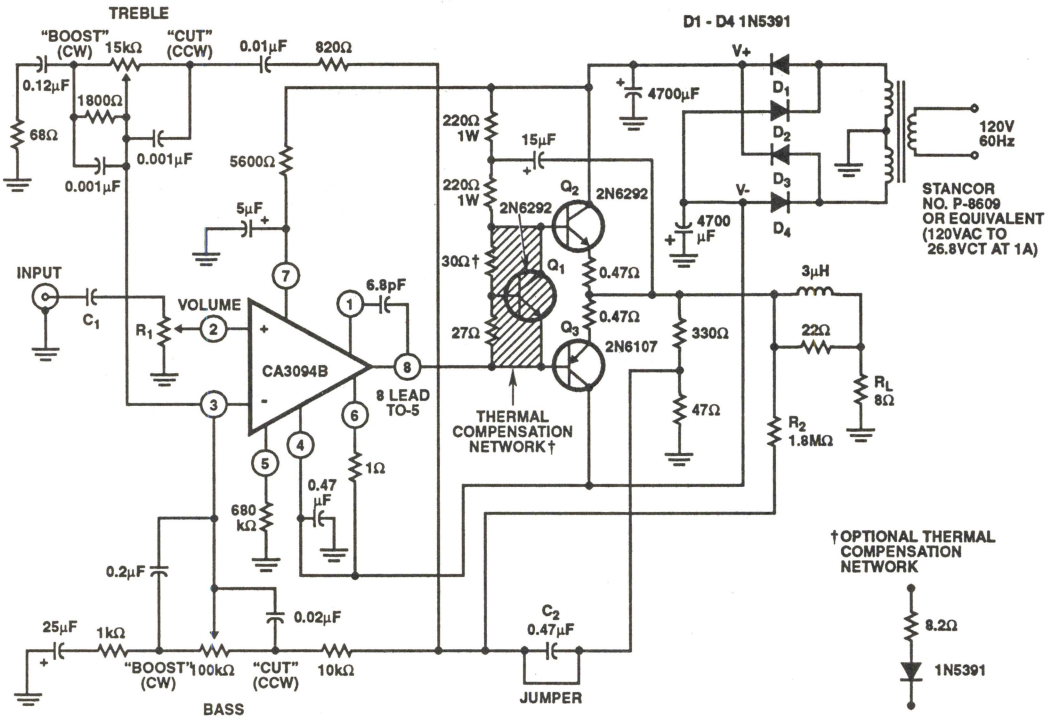


NOTES:

1. Differential current sensor provides 60mV signal ≈ 5mA of unbalance (Trip) current.
2. All Resistors are 1/2 Watt, ±10%.
3. RC selected for 3dB point at 200Hz.
4. C_2 = AC by-pass.
5. Offset adj. included in R_{TRIP}.
6. Input impedance from 2 to 3 = 800kΩ.
7. With no input signal Terminal 8 (output) at 36V.

FIGURE 36. GROUND FAULT INTERRUPTER (GFI) AND WAVEFORMS PERTINENT TO GROUND FAULT DETECTOR

Typical Applications (Continued)



TYPICAL PERFORMANCE DATA FOR 12W AUDIO AMPLIFIER CIRCUIT

Power Output (8Ω load, Tone Control set at "Flat")
- Music (at 5% THD, regulated supply) 15W
- Continuous (at 0.2% IMD, 60Hz and 2kHz mixed in a 4:1 ratio, unregulated supply)
- See Figure 8 in AN6048 . . . . . 12W

Total Harmonic Distortion
- At 1W, unregulated supply 0.05%
- At 12W, unregulated supply 0.57%

Voltage Gain 40dB
Hum and Noise (below continuous power output) 83dB
Input Resistance 250kΩ
Tone Control Range . . . . . See Figure 9 in AN6048

FIGURE 37. 12W AUDIO AMPLIFIER CIRCUIT FEATURING TRUE COMPLEMENTARY SYMMETRY OUTPUT STAGE WITH CA3094 IN DRIVER STAGE

HARRIS SEMICONDUCTOR

CA3165

April 1994

Electronic Switching Circuit

Features

- Switching Initiated by Damping of Internal Oscillator
- Proximity Sensing of Rotational Motion
- Repeatable Timing of Switching States
- Five Outputs - Two Complementary Pairs and One Non-Inverting Output CA3165E1
- Two Outputs - One Complementary Pair CA3165E

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3165E	-40°C to +85°C	8 Lead Plastic DIP
CA3165E1	-40°C to +85°C	14 Lead Plastic DIP

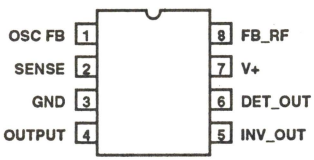
Description

The CA3165 is a single chip electronic switching circuit intended primarily for ignition applications. It includes an oscillator that is amplitude-modulated by the rotor teeth of a distributor, a detector that develops the positive going modulation envelope, a Schmitt trigger that eliminates switching uncertainties. Both types include two complementary high current switched outputs for driving power transistors requiring up to 120mA. The CA3165E also includes two complementary low current outputs that incorporate internal current limiting and a non-inverting output amplifier with uncommitted input capable of switching 27mA.

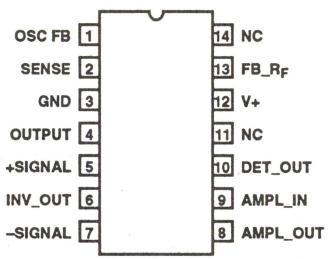
The CA3165 is supplied in the 8 lead dual-in-line plastic package (E suffix) and in the 14 lead dual-in-line plastic package (E1 suffix).

Pinouts

CA3165 (PDIP)
TOP VIEW



CA3165 (PDIP)
TOP VIEW



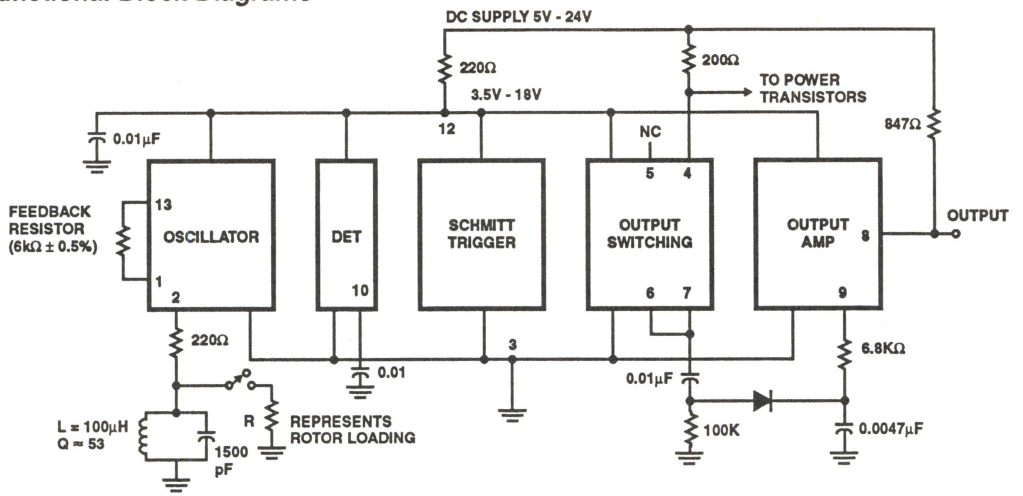
10 SPECIAL FUNCTIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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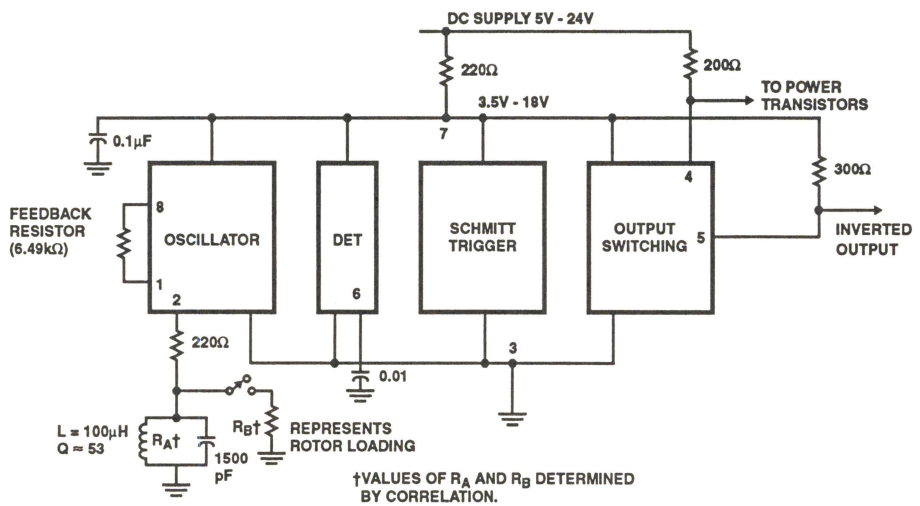
File Number **1278.2**

Functional Block Diagrams



OSCILLATOR CONDITION	TERMINAL 10	TERMINAL 4	TERMINAL 5	TERMINAL 6	TERMINAL 7	TERMINAL 8
Unloaded	Low	High	High	Low	Low	Low
Loaded	High	Low	Low	High	High	High

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM FOR CA3165E1



OSCILLATOR CONDITION	TERMINAL 4	TERMINAL 5	TERMINAL 6
Unloaded	High	High	Low
Loaded	Low	Low	High

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM FOR CA3165E

Absolute Maximum Ratings

DC Voltage (With Reference to Terminal 3)
- CA3165E1
  - Terminals 4, 6, 8 ..... 24V
  - Terminals 5, 7, 12 ..... 18V
  - Terminal 9 ..... 1.5V
- CA3165E
  - Terminals 4, 5 ..... 24V
  - Terminal 7 ..... 18V

Current (At Terminals Indicated)
- CA3165E1
  - Terminals 4, 6 ..... 120mA
  - Terminals 5, 7 ..... -0.1mA to 0.1mA
  - Terminal 8 ..... 30mA
- CA3165E
  - Terminals 4, 5 ..... 120mA

Thermal Information

Thermal Resistance θ_{JA}
- Plastic DIP Package 8 Lead ..... 150°C/W
- Plastic DIP Package 14 Lead ..... 100°C/W

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature ..... +265°C
- At Distance 1/16" ±1/32" (1.59 ±0.79mm) from Case for 10s Maximum

Device Dissipation Plastic DIP Package 8 Lead
- Up to T_A = +55°C 600mW
- Above T_A = +55°C ..... Derate Linearly at 6.67mW/°C

Device Dissipation Plastic DIP Package 14 Lead
- Up to T_A = +55°C 950mW
- Above T_A = +55°C ..... Derate Linearly at 10mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

At T_A = +25°C, V+ = 13V, Measured in the circuit of Figure 5 (CA3165E1) or Figure 6 (CA3165E)

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3165E1			CA3165E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Current at Term. (Note 1)	Δ	Dwell	-	18.4	-	-	18.4	-	mA
		Spark	-	17.5	-	-	17.5	-	mA
Output Voltage at Term. 4	V_4	Dwell	12.8	-	-	12.8	-	-	V
		Spark	-	-	0.5	-	-	0.5	V
Output Volatge at Term. 7	V_7	Dwell	-	-	1	-	-	-	V
Output Voltage at Term. 8	V_8	Dwell	-	-	0.9	-	-	-	V
		Portion of Spark	1.2	-	-	-	-	-	V
Oscillator Voltage at Term. 2	V_2	Dwell	-	4.4	-	-	4.4	-	Vp-p
		Spark	-	0.6	-	-	0.6	-	Vp-p

NOTE:

	Δ
1. CA3165E at Term. 7	I7
CA3165E1 at Term. 12	I12

10 SPECIAL FUNCTIONS

Schematic Diagrams

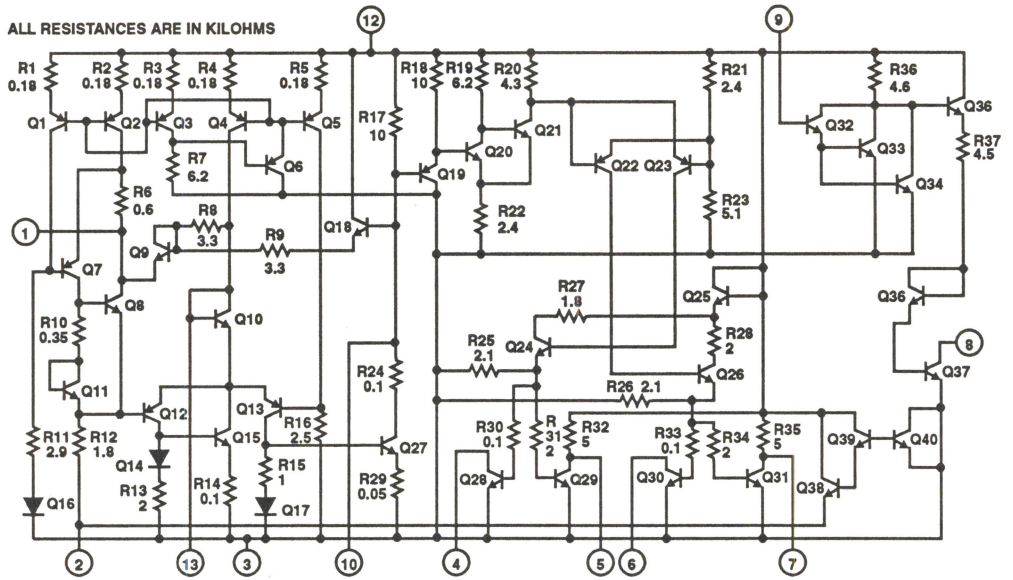


FIGURE 3. SCHEMATIC DIAGRAM FOR CA3165E1

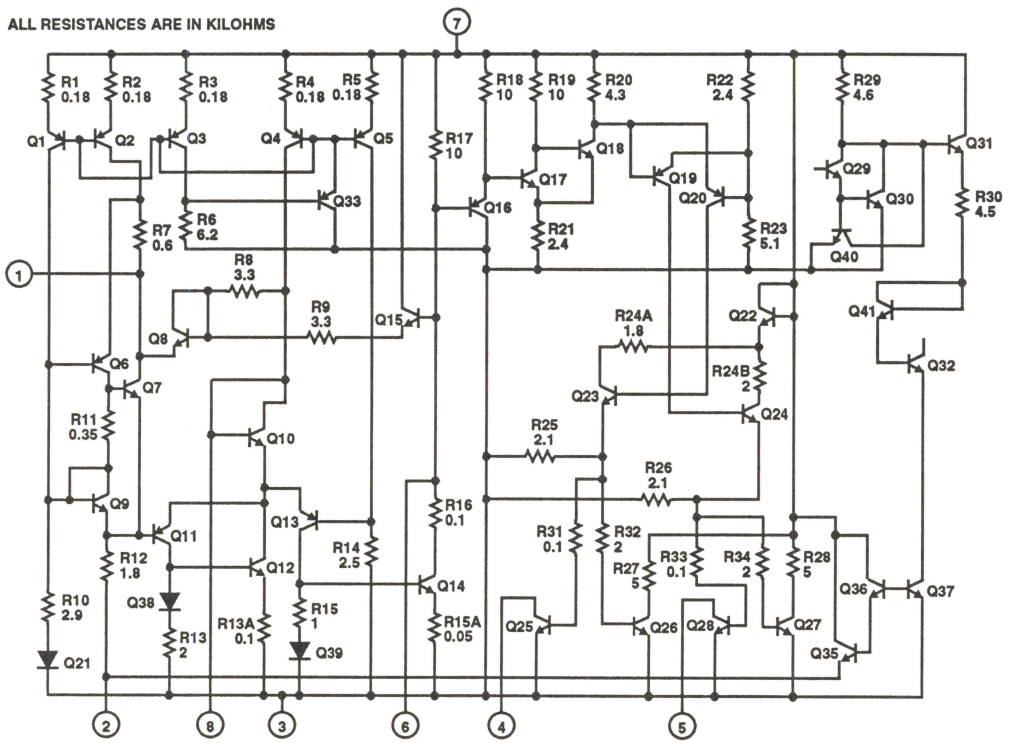


FIGURE 4. SCHEMATIC DIAGRAM FOR CA3165E

Application Information Figure 5 and Figure 6 show the application of the CA3165 in a typical ignition system.

TERMINAL DESCRIPTIONS		
TERMINAL		FUNCTION
CA3165E1	CA3165E	
1	1	Oscillator Feedback Resistor, R_F
2	2	220Ω Protective Resistor To Tank Circuit
3	3	Ground
4	4	Direct Output - R_7 load resistor 200Ω ± 5%, and R_8 to power Darlington 15Ω ± 10%
5	-	Direct Output - Low Current - Not Connected
6	5	Inverted High Current Output
7	-	Inverted Low Current Output Through C_1 (0.01μF) to D_3 and R_3 (100kΩ)
8	-	Output Amplifier Output - Through R_6 and R_5 (27Ω and 820Ω to Supply)
9	-	Output Amplifier Input - through R_4 (6800Ω) to D_3 and C_5 (0.0047μF)
10	6	Detector Output - C_2 to Ground (0.01μF)
11	-	No Connection
12	7	Circuit Supply Voltage Through R_1 (220Ω Protective Resistor) to Automotive Supply
13	8	Oscillator Feedback Resistor R_F to Terminal 1
14	-	No Connection

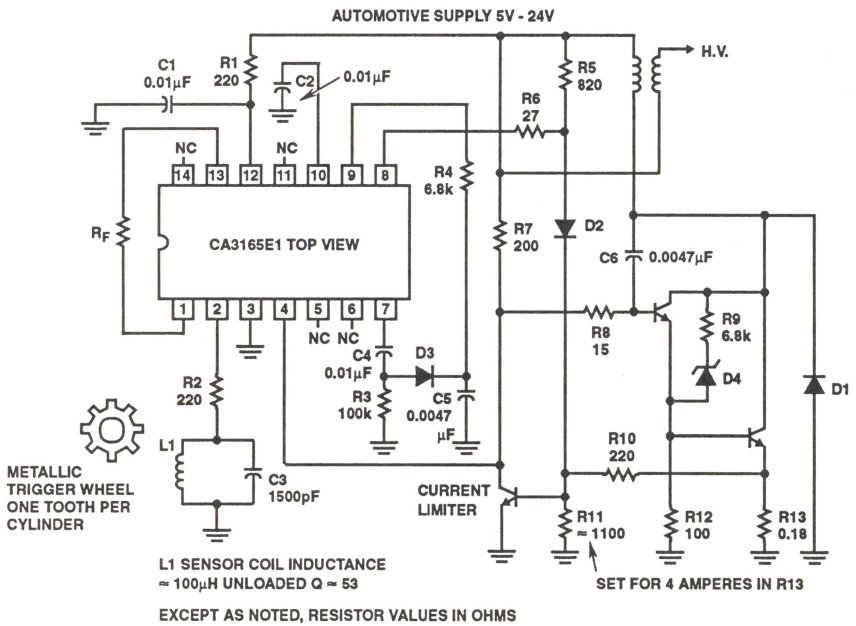


FIGURE 5. TYPICAL IGNITION SYSTEMS USING THE CA3165E1

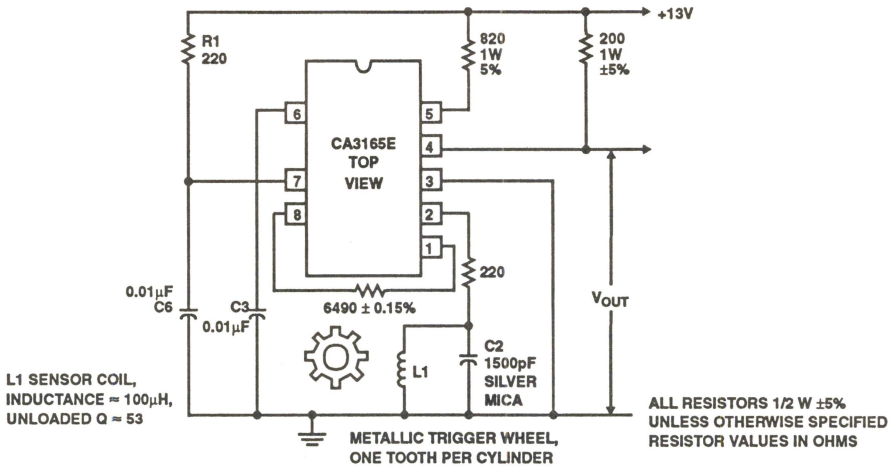


FIGURE 6. TYPICAL IGNITION SYSTEM USING THE CA3165E

Application Information

Figure 5 and Figure 6 show the application of the CA3165 in a typical ignition system. The oscillator on the chip operates at about 400kHz as determined by the tuned circuit L1, C2. The amplitude of the oscillation is detected on the chip and applied to a Schmitt trigger which sets the terminal voltage as shown in the chart in Figure 1 and Figure 2 for the unloaded condition of the oscillator. As a metallic tooth in the rotor passes the coil L1, eddy-current losses occur which reduce the Q of the resonant circuit and decrease the amplitude of the oscillations to a level below that of a reference in the detector circuit. The output terminals are then switched to states as shown in the chart in Figure 1 and Figure 2 for the loaded condition of the oscillator. The oscillation is maintained at this lower amplitude by switching in additional feedback in the oscillator circuit. The fact that the oscillator continues to operate at some minimum level during this dwell period eliminates timing variations which would occur if the oscillator had to be restarted by random noise.

Spark occurs as terminal 4 is switched from high to low. The output amplifier clamps terminal 4 low through the regulator during the duration of the spark.

The Dwell period represents the time that terminal 10 (CA3165E1) or terminal 6 (CA3165E) is high, terminal 4 is low, and the coil is charged.

The value of the oscillator feedback, resistor, R_F, is selected to set the dwell period. With a sintered-iron 8 f-tooth rotor, a typical value of R_F is 6500Ω for 28.5 degrees of dwell out of a 45 degree cycle. For a star-type rotor and a particular coil in a typical distributor, the feedback resistor would be larger (typically 8800Ω) depending on clearances, coil geometry and tooth shape.

For typical F-Tooth Rotor with Rod Sensor and 113μH of coil inductance, the Q and frequency with respect to rotor position was measured for the following positions

CENTER	46 at 377kHz
SLOT	6 at 390kHz
FIRE	15 at 381kHz

(Free air Q = 55.7 at 375kHz.)

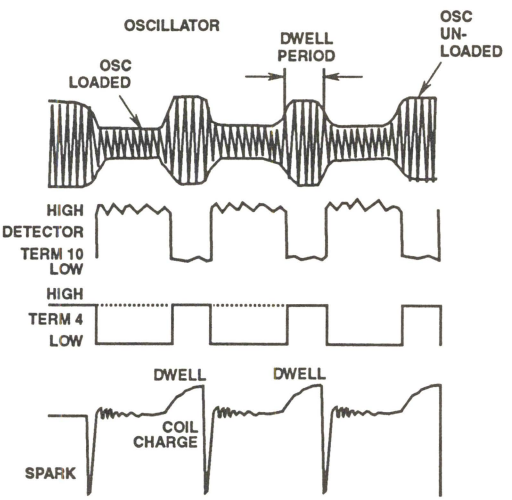


FIGURE 7. TIMING SEQUENCE

HARRIS SEMICONDUCTOR

CA3228

April 1994

Speed Control System with Memory

Features

- Low Power Dissipation
- I^2L Control Logic
- Power-On Reset
- On-Chip Oscillator for System Time Reference
- Single Input Line for Operator Commands
- Amplitude Encoded Control Signals
- Transient Compensated Input Commands
- Controlled Acceleration Mode
- Internal Redundant Brake and Low-Speed Disable
- Braking Disable

Applications

- Automotive Speed Control
- Residential and Industrial Heating and Cooling Controls
- Industrial AC and DC Motor Speed Control
- Applications Requiring Acceleration and Deceleration Control

Description

The CA3228 is a monolithic integrated circuit designed as an automotive speed-control system.

The system monitors vehicle speed and compares it to a stored reference speed. Any deviation in vehicle speed causes a servo mechanism to open or close the engine throttle as required to eliminate the speed error. The reference speed, set by the driver, is stored in a 9-bit counter.

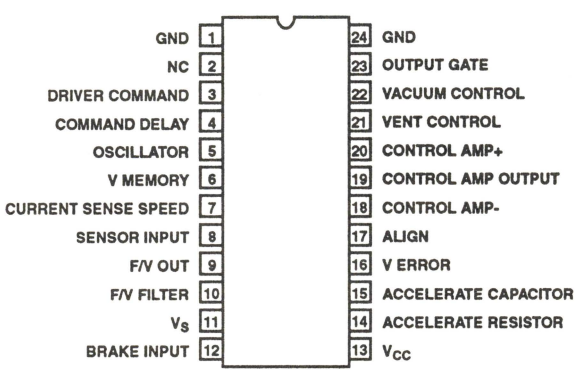
The reference speed can be altered by the ACCEL and COAST driver commands. The ACCEL command causes the vehicle to accelerate at a controlled rate; the COAST command disables the servo, thereby forcing the vehicle to slowdown. Application of the brake disables the servo and places the system in the standby mode while the RESUME command returns the vehicle to the last stored speed.

Vehicle speed and driver commands are inputs to the integrated circuit via external sensors. Actuators are needed to convert the output signals into the mechanical action necessary to control vehicle speed.

The CA3228 is supplied in a 24 lead dual-in-line plastic package (E suffix). Refer to AN7326 for application information.

Pinout

CA3228 (PDIP)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3228E	-40°C to +85°C	24 Lead Plastic DIP

10 SPECIAL FUNCTIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **1436.2**

Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... +9.0V
Supply Current, I_{CC} 30mA
Driver Command Input (I_{CMD}), Pin 3 ..... 2mA
Brake Input (I_{BRAKE}), Pin 12 ..... 2mA
Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package ..... 65°C/W
Power Dissipation Per Package
For T_A = -40°C to +70°C 1.2mW
For T_A Above +70°C ..... Derate Linearly at 15.4mW/°C
Lead Temperature (Soldering 10s) ..... +265°C
Operating Temperature Range ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Typical Switching Characteristics

Driver Command Input Hold Times (Based on 0.68µF on Pin 4):
ACCEL 50ms
COAST 50ms
RESUME 330ms
ON 50ms
OFF 50ms
Internal Oscillator Frequency, F_{OSC} 10kHz
(Based on 0.001µF at Pin 5)

System Performance F_{OSC} = 50kHz, f_S/Speed Ratio = 2.22Hz/mph

Speed Sensor Input Frequency Range, f_S at Pin 8 ..62Hz to 222Hz
Speed Resolution ..... 0.45 mph
Minimum Operating Speed ..... 25 mph
Maximum Stored Speed ..... 100 mph
Redundant Brake Speed ..... 11 mph

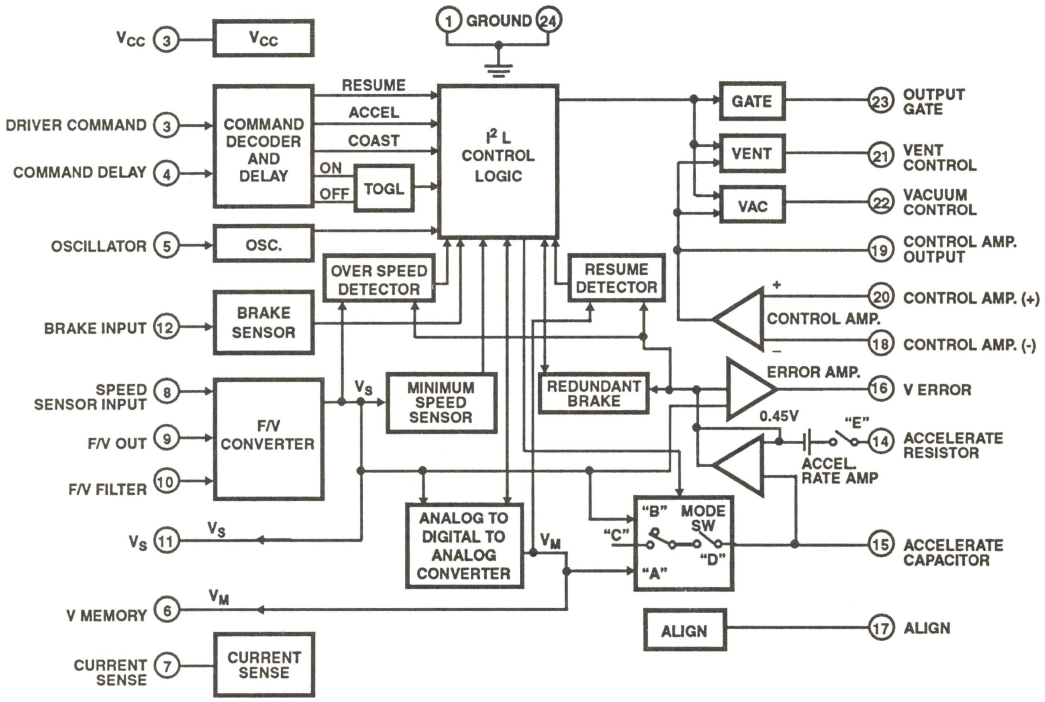
Electrical Specifications T_A = +25°C, V_{CC} = 8.20V, Unless Otherwise Specified (Refer to Figures 2 and 3)

PARAMETERS	SYMBOLS	TEST PIN	TEST CONDITIONS	MIN	MAX	UNITS
Operating Voltage	V_{CC}	13		7.40	9.00	V
Speed Sensor Input Voltage Amplitude		T.P.B.	62Hz ≤ f_S ≤ 222Hz	3.50	15.0	Vpp
V_{CC} Supply Current	I_{CC}	13		7.50	30.0	mA
Current Sense Voltage	V_7	7	43kΩ to Ground	4.85	5.95	V
Align Voltage	V_{17}	17	41kΩ to Ground	4.00	4.20	V
Command Idle Voltage	V_{3IDLE}	3	S1, S2, S3, S4, S5 Open	7.6	7.9	V
RESUME Command Voltage	V_{3RES}	3	S2 Closed	5.95	6.56	V
ACCEL Command Voltage	V_{3ACCEL}	3	S3 Closed	3.95	4.91	V
COAST Command Voltage	V_{3COAST}	3	S4 Closed	1.22	2.23	V
OFF Voltage	V_{3OFF}	3	S5 Closed	0	0.77	V
ON Voltage	V_{3ON}	T.P.A.	S1 Closed	9.2	28	V
Brake Input Voltage	V_{BRAKE}	12	S6 Closed	5.4	28	V
OUTPUT VOTLAGE						
Gate	V_{OL}	23	4.7kΩ to V_{CC}	-	300	mV
	V_{OH}			8	-	V
VAC	V_{OL}	22	1.2kΩ to V_{CC}	-	400	mV
	V_{OH}			8	-	V
VENT	V_{OL}	21	1.2kΩ to V_{CC}	-	400	mV
	V_{OH}			8	-	V

Electrical Specifications T_A = +25°C, V_{CC} = 8.20V, Unless Otherwise Specified (Refer to Figures 2 and 3) **(Continued)**

PARAMETERS	SYMBOLS	TEST PIN	TEST CONDITIONS	MIN	MAX	UNITS
Memory Set Error	$V_6 - V_{10}$	6, 10		-77	67	mV
Deadband Range (VAC and VENT Outputs Off)	V_{DB}	21, 22	Sweep Pin 19, Voltage at 1V/sec	0.96	1.43	V
Control Amplifier Gain	A_{CNTL}	16, 19	A_{CNTL} = V19/V16	74	-	Ratio
D/A Voltage Range	V_M	6	Set Mode	6	7.50	V

Functional Block Diagram



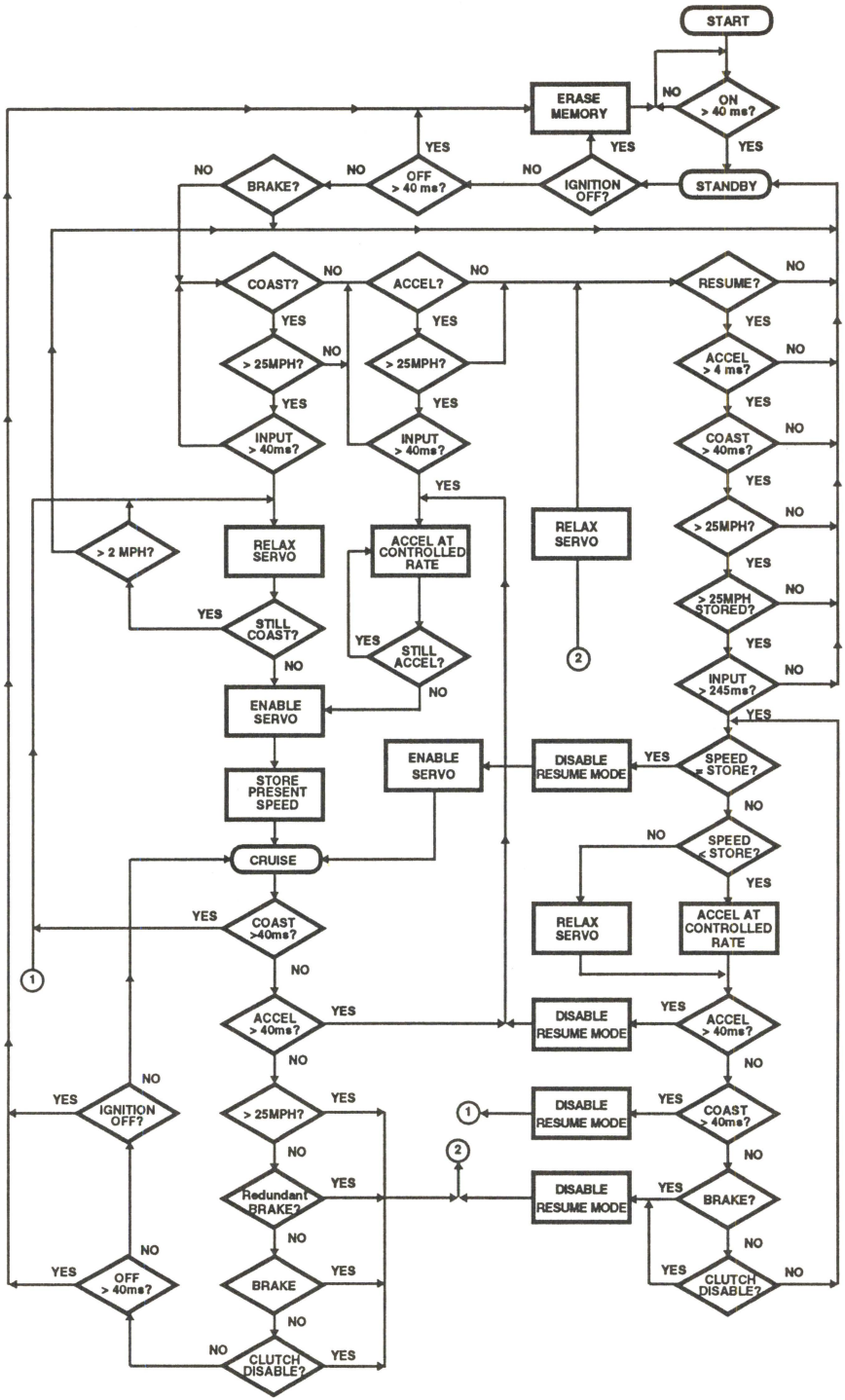
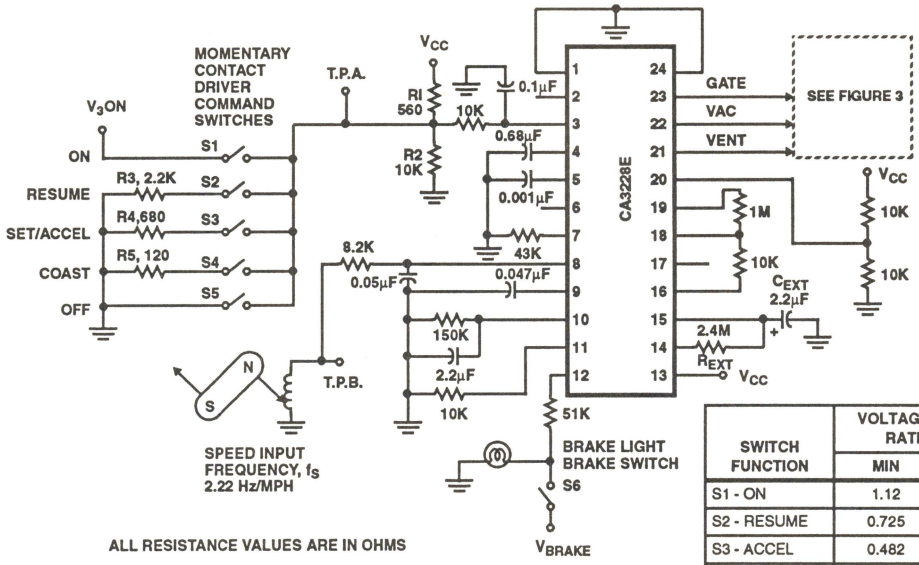


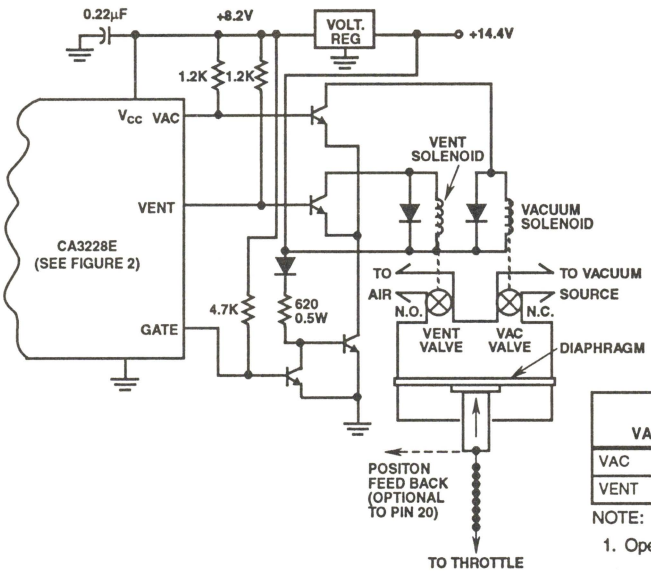
FIGURE 1. SPEED CONTROL FLOW CHART



SWITCH FUNCTION	VOLTAGE AT TERM. 3 RATIO TO V_{CC}	
	MIN	MAX
S1 - ON	1.12	-
S2 - RESUME	0.725	0.8
S3 - ACCEL	0.482	0.599
S4 - COAST	0.148	0.272
S5 - OFF	0	0.094
IDLE (Note 1)	0.93	0.96

NOTE: 1. All Switches Open

FIGURE 2. TYPICAL AUTOMOTIVE SPEED CONTROL APPLICATION



VALVE	SYSTEM MODE		
	ACCEL	CRUISE	COAST
VAC	Open	NC (Note 1)	NC
VENT	Close	Close (Note 1)	NC

NOTE:

1. Open or Closed as Required to Maintain Set Speed Error

	ACCEL	CRUISE	COAST	BRAKE	REDUNDANT BRAKE	HI-SPEED DROPOUT	LO-SPEED DROPOUT
VAC (Pin 22)	H	L	L	L	L	L	L
VENT (Pin 21)	H	H	L	L	L	L	L
GATE (pin 23)	L	L	L	H	H	H	H

FIGURE 3. SOLENOID DRIVERS AND SERVO VACUUM CONTROL MECHANISM TYPICAL APPLICATION

Device Description and Operation

The functional block diagram and Figures 1, 2 show the speed- control flow chart, and a typical automotive speed-control application, respectively.

Command Decoder and Delay Logics (Pins 3,4)

Driver commands are input to pin 3 through the Driver Command Line. These signals are encoded on a single line as voltage levels selected by switches which adjust a resistor divider network.

The voltage level established is compared to a reference level which decodes the command. A command level greater than V_{CC} + 0.8V turns the system On, enabling dynamic control. Once the system is enabled, a voltage level of $0.88V_{CC}$, $0.66V_{CC}$, and $0.38V_{CC}$ decodes the RESUME, ACCEL, and COAST command, respectively. A driver command of $0.12V_{CC}$ or less turns the system Off.

The Driver Command Delay established by the current sources and a capacitor at pin 4 assures that ON, OFF, ACCEL, and COAST commands are considered valid only if longer than 50ms. The time for RESUME is 330ms.

Control Logic

The Control Logic accepts signals from the command decoder and other sensors. It causes the memory to be updated when operating in ACCEL and COAST modes. It will put the system in Standby mode if brakes are applied, if the speed error exceeds 11mph, or if the vehicle speed drops below the minimum Speed Lockout (25mph). It will return the vehicle to the previous set memory speed when a RESUME command is given.

Frequency to Voltage Converter (Pins 8-11)

The speed sensor input f_S at pin 8 is an AC signal whose frequency is directly proportional to the vehicle speed at approximately 2.22Hz/mph The current sources, capacitor and comparators at pin 9 cause equal rise and fall times to occur at pin 9 on the positive- and negative-going slopes of the sensor input. Pulse currents of time duration equal to the rise and fall times are used to charge the parallel resistor capacitor combination at pin 10 to give a voltage (V_S) at pin 10 proportional to frequency at approximately 27mV/Hz. The f_S frequency range may be altered by changing the values of the filter capacitors at pins 8 and 9. However, the maximum-to-minimum frequency ratio will remain fixed.

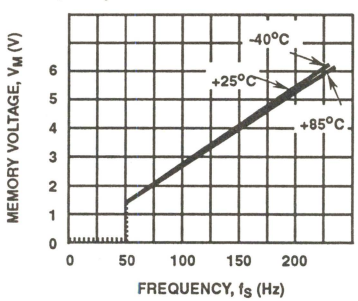


FIGURE 4. TYPICAL D/A MEMORY VOLTAGE, V_M vs FREQUENCY

Memory Voltage, V_M (Pin 6)

Upon release of the ACCEL or COAST switches the voltage, representing vehicle speed V_S determined by the output from the frequency-to-voltage converter, is stored as a binary number in a 9 bit counter. A memory update comparator allows clocking of the counter until memory voltage V_M equals V_S. The output of the counter controls a ladder network which provides memory voltage V_M at pin 6.

Analog Accelerate and Resume Generator (Pins 14,15)

Numerous functions are combined in what is called the Analog Accelerate and Resume Generator. The circuit switches the signal output at pin 15 depending on the mode of operation. In the Accelerate and Resume mode the capacitor at pin 15 is charged at a fixed rate [450mV/(R_{EXT}) (C_{EXT})]. In the Cruise mode pin 15 follows the memory voltage (V_M) and in the On, Off, Brake, Redundant Brake, Minimum Speed Lockout, and Coast modes, pin 15 follows the voltage representing vehicle speed (V_S).

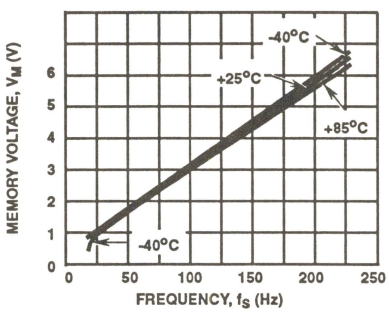


FIGURE 5. TYPICAL CHARACTERISTIC F/V CONVERTER OUTPUT, V_S vs FREQUENCY

Error Amplifier (Pin 16)

In the Cruise mode the Error Amplifier determines the difference between the set memory speed (V_M) and the actual speed (V_S). This error signal is fed to the control amplifier where it defines whether VAC or VENT is required. The error signal represents deviation in vehicle speed from the memory or set speed condition. The Error signal is also used to control the Redundant Brake feature.

Redundant Brake Comparator

When the error output drops below approximately $0.42V_{CC}$, the Redundant Brake output is activated. Redundant Brake causes the chip to go into the Standby mode.

Control Amplifier (Pins 18, 20)

The Control Amplifier is an op amp using external components to set the gain. Inputs to the Control Amplifier are from the Error Amplifier output, servo position sensor and align output. The output of the Control Amplifier controls the VAC and VENT outputs.

VAC, VENT and Gate-Driver Outputs (Pins 21, 22, 23)

The VAC, VENT and Gate Outputs are open collector devices used to control the throttle position. For the system to be able to supply vacuum, the gate output must be low. If

the output from the Control Amplifier exceeds $0.573V_{CC}$, vacuum is supplied to the servo unit. If the output of the Control Amplifier is between $0.573V_{CC}$ and $0.427V_{CC}$ the vacuum is held in the servo unit and vehicle speed is maintained. If the output from the Control Amplifier drops below $0.427V_{CC}$ or if the gate output is high, the servo unit vacuum is vented.

Overspeed Detector Comparator

The Overspeed Detector circuit is used when the following sequence of events occur: A speed is set in memory, the vehicle is manually accelerated (foot pedal) to a higher speed and then the ACCEL switch is activated.

During vehicle acceleration V_S voltage is greater than the V_M voltage into the memory update comparator. When the ACCEL command is given, the capacitor at pin 15 rapidly charges to within 60mV of V_S before switching the comparator output low and starting the fixed acceleration rate from the present vehicle speed. The 60mV of offset is required to insure that the output of the overspeed detector is low under normal operating conditions. Hysteresis is also designed into the comparator to eliminate noise problems which may prevent the chip from going into the Acceleration mode.

End of Resume Comparator

The Resume Comparator is used when the following sequence of events occurs: A speed is set in memory, the brake applied, causing the vehicle to go to a lower speed, and the RESUME switch is activated.

Activation of the RESUME switch causes a fixed acceleration rate from the lower speed until the capacitor voltage at pin 15 is equal to the V_M voltage. A filter circuit contained in the output of the resume comparator insures that noise doesn't reset the comparator until V_{PIN} actually equals V_M.

Align Voltage Source (Pin 17)

The Align Voltage Source is a X1 buffer with an output of $0.5V_{CC}$.

Brake Input Comparator (Pin 12)

When the Brake Input exceeds $0.55V_{CC}$, the chip will go into the Standby mode from Cruise.

Minimum Speed Lockout

Assures that the system remains in a Standby mode if vehicle speed V_S is below $0.183V_{CC}$. It causes the system to revert to the Standby mode if V_S drops below $0.183V_{CC}$ in the Cruise mode.

Digital Filter for Redundant Brake and Minimum Speed Lockout

A 4 bit shift register with an all '1's output decode is used to filter transients and electromagnetic interference. The filter prevents false signals from putting the system into Standby from Cruise.

Ramp Oscillator (Pin 5)

The Ramp Oscillator at pin 5 nominally varies between amplitudes of 4.1V and 6.1V. The discharge rate is approximately 4X the charge rate. With a capacitor of 0.001µF on pin 5, the nominal oscillator frequency is 50kHz.

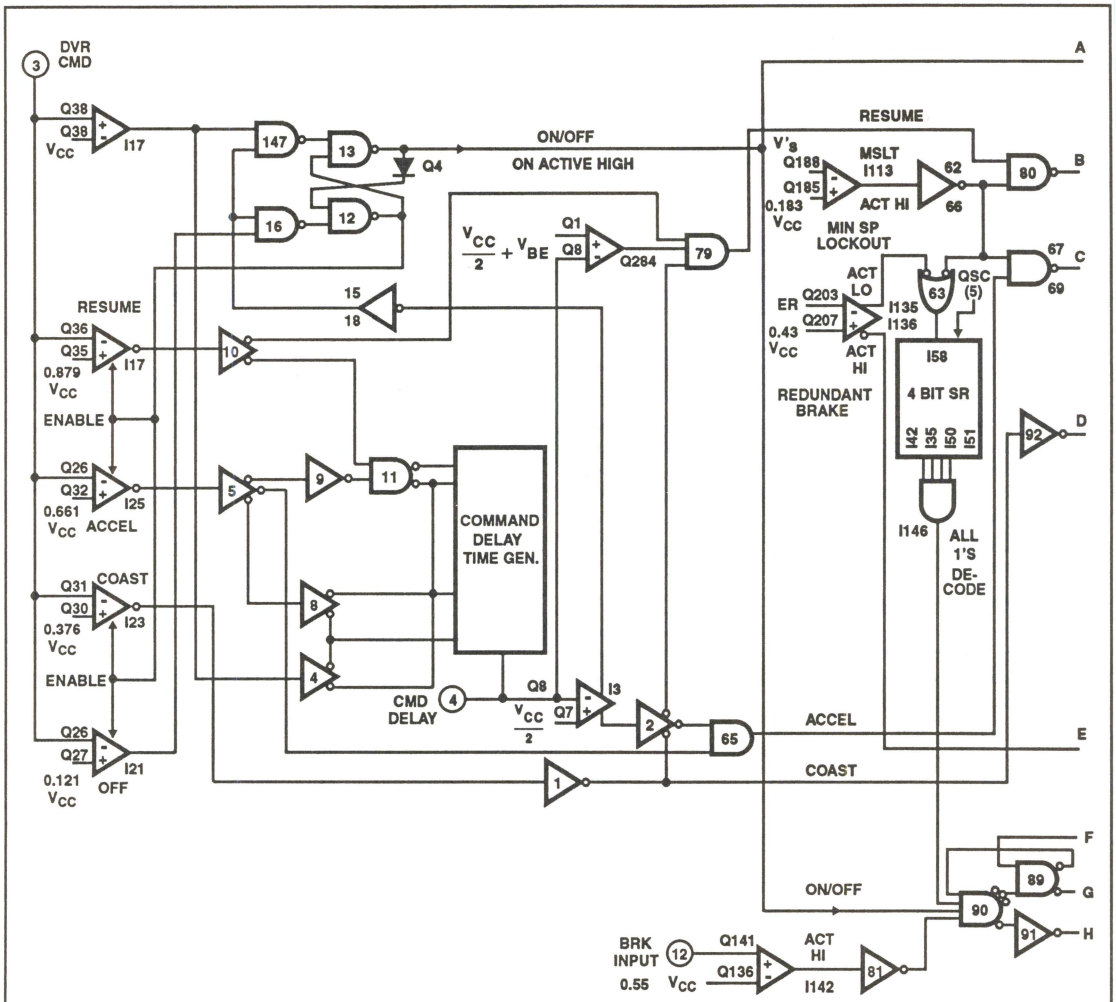


FIGURE 6. FUNCTIONAL BLOCK DIAGRAM FOR SPEED CONTROL (Continued On Next Page)

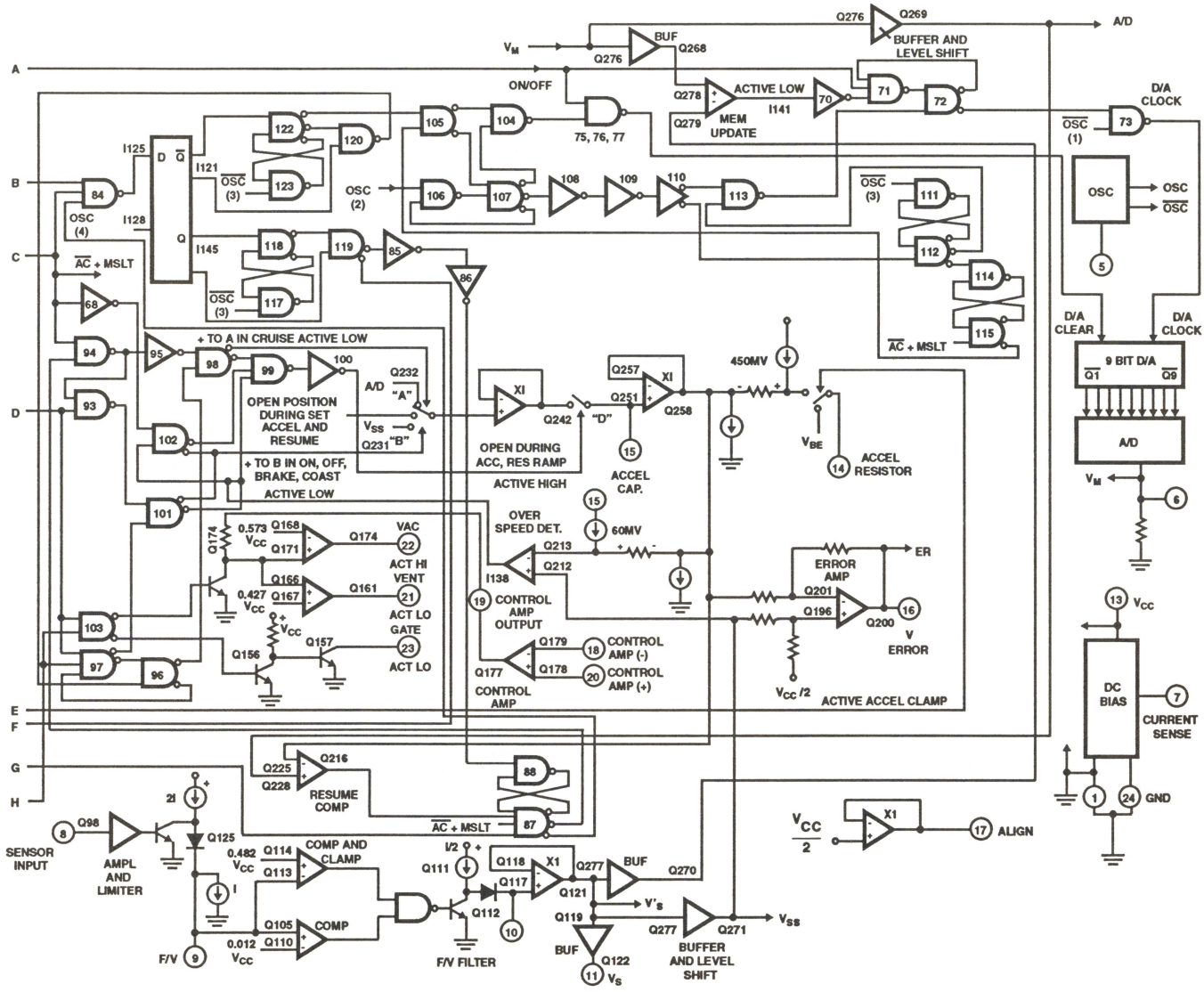


FIGURE 6. FUNCTIONAL BLOCK DIAGRAM FOR SPEED CONTROL (Continued)

HARRIS SEMICONDUCTOR

CA3274

Current Limiting Power Switch with Current Limiter Sense Flag

April 1994

Features

- Drive-Current Limiting at Output
- Current-Sense Buffer and Reference
- 200mA Driver Current Capability
- Logic-Level Control Input
- Current Limiting Flag Output
- 50dB Minimum PSRR
- 5μs Typical Switch Time
- Separate Signal and Power Grounds

Applications

- Solenoid Switch Driver
- Relay Driver
- Lamp Control Switch
- Ignition Coil Pre-Driver
- Constant Current Driver
- Current Limiting Switch
- Fault Output Sense Appliance
- Power Supply Fault Mode Control

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3274E	-40°C to +85°C	8 Lead Plastic DIP

Description

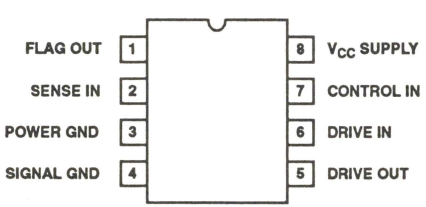
The CA3274 is a controlled current switch and may be used in general purpose switching applications that require specified maximum levels of current. The functional block diagram of the CA3274 is shown and a typical application circuit is shown in Figure 1. An internal emitter follower has 200mA of source drive output capability. The Control Input is a Schmitt trigger buffer amplifier for noise immunity in the environments typical of industrial and automotive control systems.

Current sensing in the emitter circuit of a power-darlington output stage is fed back from a sampling resistor to the sense input of the CA3274 which has a 335mV typical offset. For the example shown in Figure 1, a sampling resistor of 0.056Ω permits 6.0A (0.335/0.056) of current in the emitter of the output driver. When the current limiter is activated, the flag output changes state conditionally. If the control input is the "0" state, the flag output will remain in a "1" state. If the control input is in the "1" state and the sense input is less than the voltage reference level of 335mV, the flag output will remain in the "1" state. If the control input is the "1" state and the sense input is equal to or greater than the 335mV reference level, the flag output goes to the "0" state. The output flag switch may be used to accurately establish dwell timing in automotive applications. When the control input goes to "0", the flag is reset to "1". Noise-immunity hold-off is used to prevent pre-triggering of the flag output and is noted as t_D in the timing diagram of Figure 2.

The flag output may be used for diagnostic feedback via the current sense input to detect a fault mode. In this case the sampled drive current is either from the emitter of the CA3274 internal power transistor or an external output amplifier, such as a darlington power transistor or power-FET output stage. The CA3274 has separate power and signal grounds to minimize transient-loop feedback to the input ground and thus prevent false triggering of the output. Optionally, the output from the CA3274 may be taken from the open collector (DRIVE IN) at pin 6. An external resistor at pin 6 may be used to set the level at which Q2 will saturate, providing additional limiting protection for the maximum forward-drive from the CA3274.

Pinout

CA3274 (PDIP)
TOP VIEW

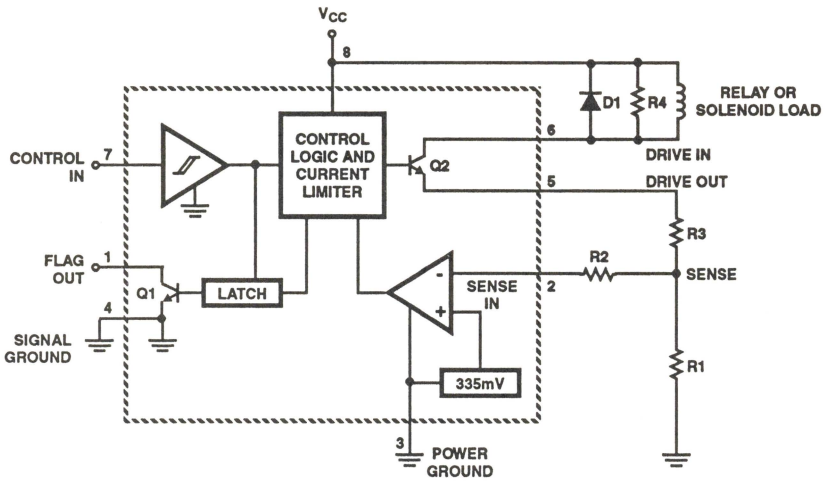


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2222.2**

Block Diagram



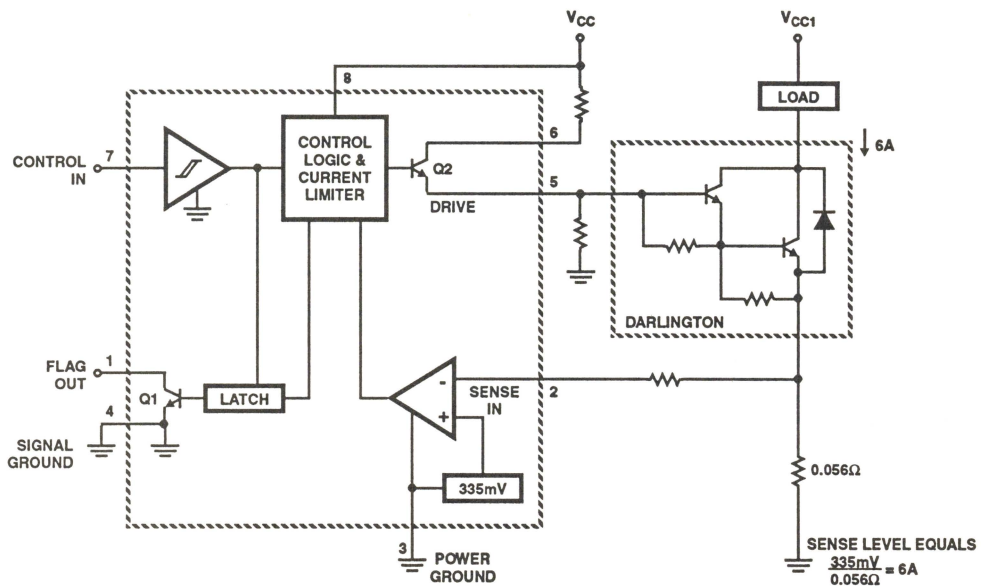


FIGURE 1. TYPICAL APPLICATION AS A POWER SWITCH PRE-DRIVER SWITCH

Absolute Maximum Ratings

Operating Drive Supply, V_{CC} 16V
Maximum Output Current, I_O 200mA
Control, Sense Input..... Gnd - 0.5V, V_{CC} + 0.5V
Signal, Power Differential Ground Voltage..... ±1V

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package 8 Lead ..... 130°C/W
Power Dissipation, P_D
Up to 70°C..... 630mW
Above 70°C..... Derate linearly at 7.7mW/°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16in. (1.59mm ± 0.79mm) from
case for 10s Max. ..... +265°C

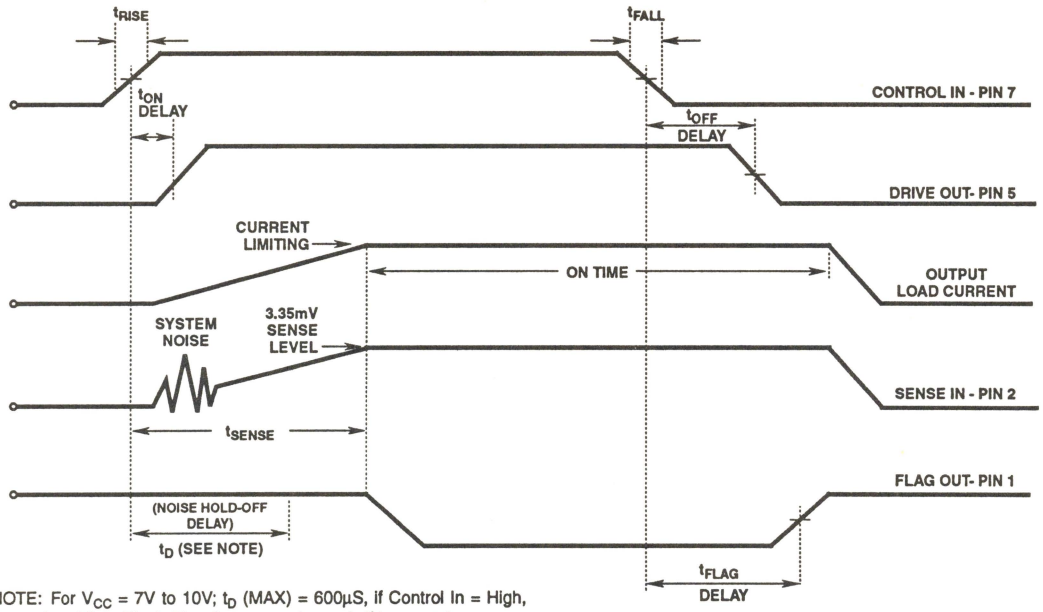
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = -40°C to +85°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current: S1 = 2	I_{CCH}	Control = High (Output On)	-	-	25	mA
	I_{CCL}	Control = Low (Output Off)	-	-	5	mA
Control Input: S1 = 3	V_{THDH}	Thd. Voltage, High	-	-	3.5	V
	V_{THDL}	Thd. Voltage, Low	0.9	-	-	V
	V_{THDH}-V_{THDL}	Hysteresis	0.4	0.65	2.0	V
	I_{IL}	Leakage, 0.0 to 5.5V	-20	-	+20	µA
Driver In, Out (Pin 6, 5): S1 = 3	V_{SAT}	Output Saturation Voltage, I_{CC1} = 200mA, $V_{CONTROL}$ = High	-	-	0.5	V
	I_{LEAK}	Collector Output Leakage, $V_{CONTROL}$ = Low	-	-	100	µA
Flag Output Low: S1 = 2	V_{FSAT}	V_{SENSE} = High, I_{FLAG} = 3mA	-	-	0.8	V
Flag Output High: S1 = 3	V_{FLEAK}	Output Leakage, V_{CC} = V_{FLAG} = 10V	-	-	10	µA
Prop. Delay: S1 = 1	t_{ON}, t_{OFF}	Control In to Drive Out	-	5	-	µs
	t_{FLAG}	Drive Off to Flag Off	-	10	-	µs
	t_D	Flag Delay from Control In	150	-	600	µs
Sense Input Thd. Level: S1 = 1	V_{SENTHD}		310	335	360	mV
Power Supply Rejection Ratio	PSSR		50	-	-	dB

NOTES:

1. Refer to Figure 3 Test Diagram for electrical test connections.
2. Refer to Figure 2 Timing Diagram for logic switching and prop delay.
3. Unless otherwise specified: V_{CC} = V_{CC1} = V_{CC2} = 7V to 10V;
V_{SENSE} = "Low"; $V_{CONTROL}$ = "Low";
Control in levels are defined as "Low" equals 0.0V and "High" equals 5.0V.



NOTE: For V_{CC} = 7V to 10V; t_D (MAX) = 600µS, if Control In = High, Sense In = High; Pin 1, Flag Out can go low only if $t_{SENSE} \geq t_D$

FIGURE 2. CA3274 TIMING DIAGRAM

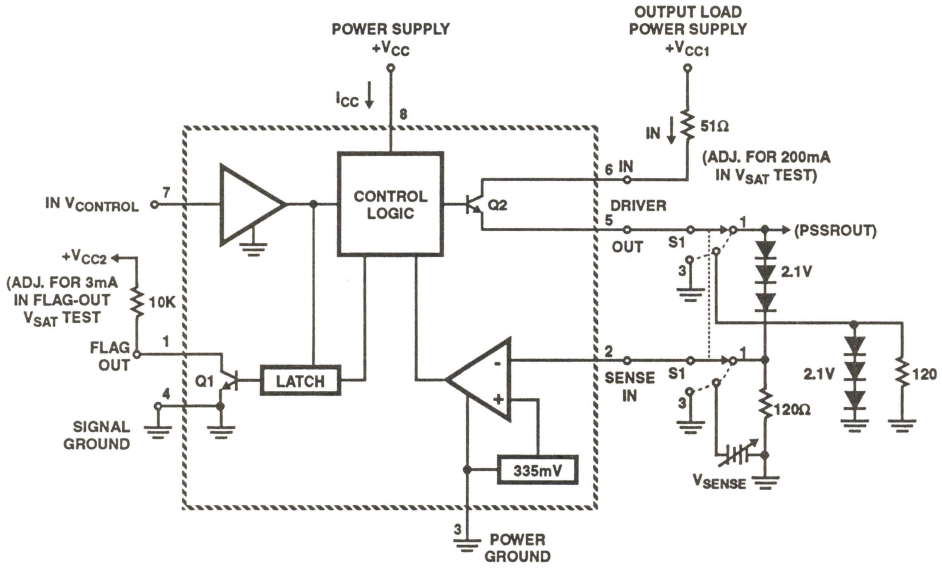


FIGURE 3. CA3274 TEST CIRCUIT

HARRIS SEMICONDUCTOR

HIP9010

April 1994

Engine Knock Signal Processor

Features

- Two Sensor Inputs
- Microprocessor Programmable
- Accurate Filter Elements
- Digitally Programmable Gain
- Digitally Programmable Time Constants
- Stable Analog Filter Characteristics
- On-Chip Clock
- Operating Temperature Range -40°C to +125°C

Applications

- Engine Knock Detector Processor
- Analog Signal Processing where Controllable Filter Characteristics are Required

Description

The HIP9010 is used to provide a method of detecting premature detonation or "Knock" in automotive engines.

A block diagram of this IC is shown in Figure 1. The chip alternately selects one of the two sensors mounted on the engine block. Two programmable bandpass filters process the signal from both sensors, and divides the signal into two channels. When the engine is not knocking, programmable gain adjust stages are set to ensure that both the reference channel and the knock channel contain similar energies. This technique ensures that the detection system is comparatively immune to changes in the engine background noise level. When the engine is knocking, the energy in the knock channel increases.

An active, full wave rectifier detects energy in each channel. During integration, the energy from the reference channel is subtracted from the energy in the knock channel. The result is an analog voltage, whose output level is proportional to the engine knock.

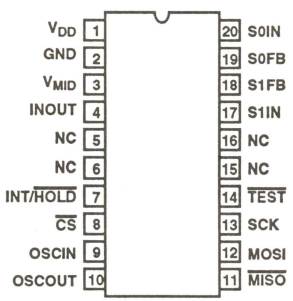
The chip is under microprocessor control via an SPI interface bus.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP9010AB	-40°C to +125°C	20 Lead Plastic SOIC (W)

Pinout

HIP9010 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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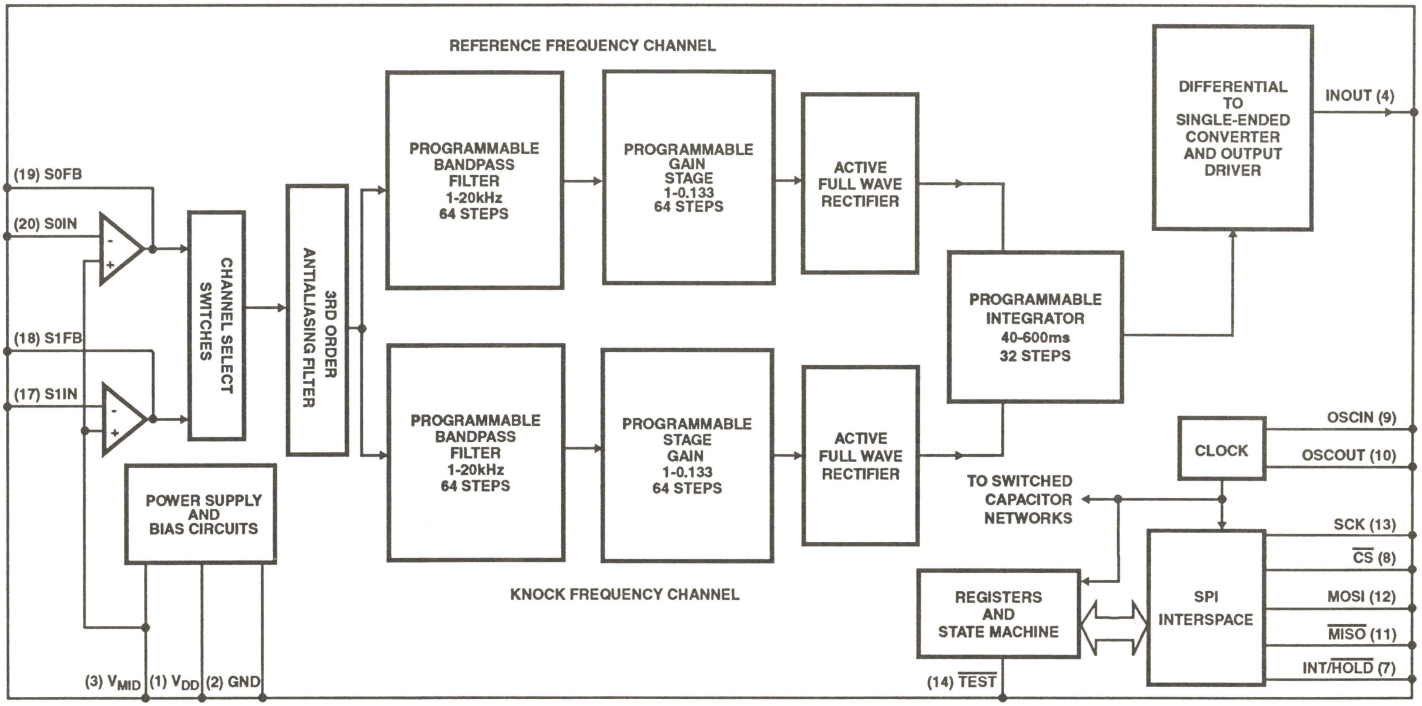


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF THIE HIP9010

Absolute Maximum Ratings

DC Logic Supply, V_{DD} ..... -0.5V to +7.0V
Output Voltage, V_O ..... -0.5V to +7.0V
Input Voltage, V_{IN} ..... +7V Max.

Thermal Information

Thermal Resistance θ_{JA}
Plastic SOIC Package ..... 120°C/W
Power Dissipation, P_D
For T_A = -40°C to +70°C ..... 450mW Max.
For T_A = +70°C to +125°C ..... Derate Linearly at 8.3mW/°C
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range, TSTG ..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5V, ±5%, GND = 0V, Clock Frequency 4MHz, ±0.5%, T_A = -40°C to +125°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Quiescent Supply Current	I_{DD}	V_{DD} = 5.25V, GND = 0V	3	7.5	12	mA
Midpoint Voltage, Pin 3	V_{MID}	V_{DD} = 5.0V, I_L = 2mA Source	2.3	2.45	2.55	V
Midpoint Voltage, Pin 3	V_{MID}	V_{DD} = 5.0V, I_L = 0mA	2.4	2.5	2.6	V
Input Leakage, Pin 14	$IL_{\overline{TEST}}$	V_{DD} = 5.0V	-	-	3	µA
Internal Pull-Up Resistor, Pin 14	$R_{\overline{TEST}}$		30	100	200	KΩ
Leakage of Pins 7, 8,12 and 13	I_L	Measured at GND and V_{DD} = 5V	-	-	±3	µA
Low Input Voltage, Pins 7, 8,12 and 13	V_{IL}		-	-	30	% of V_{DD}
High Input Voltage, Pins 7, 8,12 and 13	V_{IH}		70	-	-	% of V_{DD}
Low Level Output, Pin11	V_{OL}	I_{SOURCE} = 4mA	0.01	-	0.30	V
High Level Output, Pin11	V_{OH}	100µA	5.4	5.5	6.0	V
Leakage Pin 11	I_L	Measured at GND and V_{DD} = 5V	-	-	10	µA
Low Level Output, Pin 10	V_{OL}	I_{SOURCE} = 500µA	-	-	1.5	V
High Level Output, Pin 10	V_{OH}	I_{SINK} = -800µA	4.4	-	-	V
INPUT AMPLIFIERS						
S0FB and S1FB High Output Voltage	V_{OUT}HI	100µA I_{SINK}	4.7	4.9	-	V
S0FB and S1FB Low Output Voltage	V_{OUT}LO	100µA I_{SINK}	-	15	200	mV
S0FB and S1FB Closed Loop Gain -26dB	A_{CL}	Input Resistor = 1MΩ, Feedback Resistor = 50KΩ, -26dB	-25	-26	-27	dB
S0FB and S1FB Closed Loop Gain 20dB	A_{CL}	Input Resistor = 47.5MΩ, Feedback Resistor = 475KΩ, 20dB	18	20	21	dB
ANTIALIASING FILTER						
Response 1kHz to 20kHz, Referenced to 1kHz	BW	Test Mode, 70mV_{RMS} Input to S0FB or S1FB, Output Pin 4	-	-2	-	dB
Attenuation at 180kHz Referenced to 1kHz	ATEN	Test Mode, 70mV_{RMS} Input to S0FB or S1FB, Output Pin 4	-10	-15	-	dB

Electrical Specifications V_{DD} = 5V, ±5%, GND = 0V, Clock Frequency 4MHz, ±0.5%, T_A = -40°C to +125°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PROGRAMMABLE FILTERS						
Peak to Peak Voltage Output	V_{OUTP-P}	Test Mode, 330mV_{RMS}, 1.22kHz Input S0FB or S1FB, Output Pin 4	3.0	3.5	-	V_{P-P}
Filters Q at 20% of Center Frequency (Note 1)	Q	Test Mode, 70mV_{RMS}, 1.22kHz to 19.98kHz, Input S0FB or S1FB Output Pin 4	-	2.5	-	Q
Output Noise, Clock ON	V_{NOISE}	Test Mode, RMS Metering BW 50Hz to 200kHz, Open Input to S0FB or S1FB, Output Pin 4	-	0.4	1	mV_{RMS}
PROGRAMMABLE GAIN AMPLIFIERS						
Percent Amplifier Gain Deviation Per Table 1	%G	Test Mode, 1V_{P-P} Input S0FB or S1FB, Output Pin 4	-	±5	-	%
INTEGRATOR						
Integrator Offset Voltage	$INTGV_{IO}$	Test Mode, 25mV_{RMS}, TC = 600µs Gain = 0.5,1.22kHz to 19.98kHz	-	-	±30	mV
Integrator Reset Voltage	V_{RESET}	Pin 4 Voltage at Initiation of Integration Cycle	520	590	660	mV
Integrator Droop after 500µs	V_{DROOP}	Test Mode	-	±1	±3	mV
DIFFERENTIAL CONVERTER						
Differential to Single Ended Converter Offset Voltage	$DIFV_{IO}$	Pin 3 to 4, S0FB and S1FB Pins Open	-5	5	15	mV
Change in Converter Output	DIFOUT	Test Mode, 500mA, Sinking Load to No Load	-	±1	±3	mV

NOTE:

1. Q = fo/bBW, Where: fo = Center Frequency, BW = 3dB bandwidth.

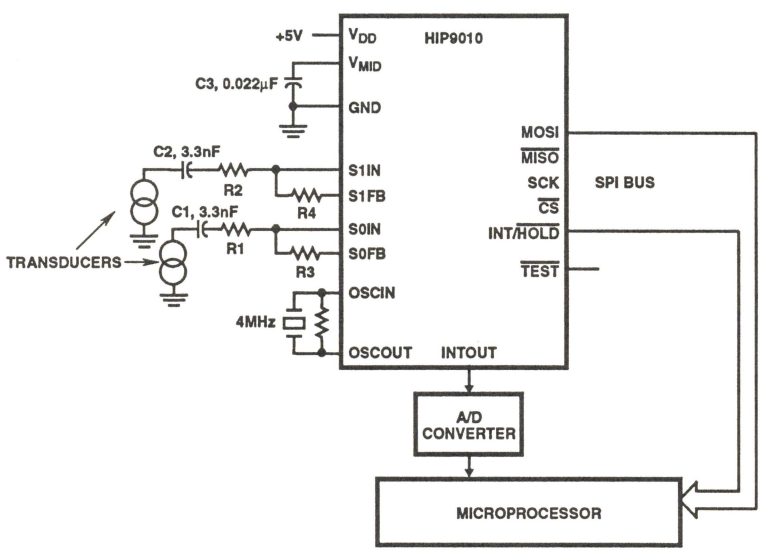


FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE HIP9010 IN AN AUTOMOTIVE APPLICATION

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{DD}	Five volt power input.
2	GND	This terminal is tied to ground.
3	V_{MID}	This terminal is tied to the internal mid-supply generator and is brought out for supply bypassing by a 0.022µF capacitor.
4	INTOUT	Buffered output of the integrator.
5 and 6	NC	These terminals are not internally connected. DO NOT USE.
7	INT/$\overline{HOLD}$	Selects whether the chip is in the Integrate Mode (Input High) or in the Hold Mode (Input Low).
8	$\overline{CS}$	A low input on this pin enables the chip to communicate over the SPI bus.
9	OSCIN	Input to inverter used for the oscillator circuit. A 4MHz crystal or ceramic resonator is connected between this pin and pin 10. To bias the inverter, a 10MΩ resistor is usually connected between this pin and pin 10.
10	OSCOUT	Output of the inverter used for the oscillator. See pin 9 above.
11	$\overline{MISO}$	Output of the chip SPI data bus. It is the inversion of the chip DATAIN line. This is an open drain output. The output must be disabled by placing the $\overline{CS}$ High when the chip is not selected.
12	MOSI	Input of the chip SPI data bus. Data length is eight bits.
13	SCK	Input from the SPI clock. Normally high, the data is clocked to the chip internal circuitry on the rising clock edge.
14	$\overline{TEST}$	A low on this pin places the chip in the test mode. For normal operation this terminal is tied high or left open.
15 and 16	NC	These terminals are not internally connected. DO NOT USE.
17	S1IN	Inverting input to sensor one amplifier. A resistor is tied from this summing input to the transducer. A second resistor is tied between this terminal and terminal 18, S1FB to establish the gain of the amplifier.
18	S1FB	Output of the sensor one amplifier. This terminal is used to apply feedback.
19	S0FB	Output of the sensor zero amplifier. This terminal is used to apply feedback.
20	S0IN	Inverting input to sensor zero amplifier. A resistor is tied from this summing input to the transducer. A second resistor is tied between this terminal and terminal 19, S0FB to establish the gain of the amplifier.

Description of the HIP9010 Operation

This IC is designed to be a universal digitally controlled, analog interface between engine acoustical sensors or accelerometers and internal combustion engine fuel management systems. Two wideband input amplifiers are provided that allow the use of two sensors that may be of the piezoelectric type that can be mounted in optimum locations on either in-line or V type engine configurations.

Output from these amplifiers is directed from a channel select switch into both digitally controlled filter and amplifier channels. Both filter bandpass and gain settings are programmable from a microprocessor. Output from the two channels is combined in a digitally programmable integrator. Integrator output is applied to a line driver for further processing by the engine fuel management system.

Broadband piezoelectric ceramic transducers used for the engine signal pickup have device capacitances in the order of 1100pF and output voltages that range from 5mV to $8V_{RMS}$. During normal engine operation a single input channel is selected and applied to the filters. One filter channel processes a signal that is used to establish the background reference level. The second channel is used to observe the engine during the time interval that preignition may be expected. This information is compared with the "background" signal via the ICs integrator and will tend to cancel the background noise and accentuate noise due to engine pre-detonation. Moreover, the bandpass of filter channels can be optimized to further discriminate between engine background and combustion noise and pre-detonation noise.

A basic approach to engine pre-detonation systems is to only observe engine background during the time interval that noise is expected and if detected, retard timing. This approach does not require the sensitivity and selectivity that is needed for a continuously adjustable solution. Enhanced fuel economy and performance is obtainable when this IC is coupled with a microprocessor controlled fuel management system.

Circuit Block Description

Input Amplifiers

Two amplifiers are used to interface to the two engine sensors. These amplifiers have a typical open loop gain of 100dB, with a typical bandwidth of 2.6MHz. The common mode input voltage range extends to within 0.5V of either supply rail. The amplifier output has a similar output range.

Sufficient gain, bandwidth and output swing capability was provided to ensure that the amplifiers can handle attenuation gain settings of 20 to 1 or -26dB. This would be needed when high peak output signals, in the range of $8V_{RMS}$, are obtained from the transducer. Gain settings of 10 times can also be needed when the transducers have output levels of $5mV_{RMS}$.

In a typical application the input signal frequency may vary from DC to 20kHz. External capacitors are used to decouple the IC from the sensor (C1 and C2). A typical value of the capacitors is 3.3nF. Series input resistors, R1 and R2, are used to connect the inverting inputs of the amplifiers, (pins 20 and 17). Feedback resistors, R3 and R4, in conjunction with R1 and R2 are used to set the gain of the amplifiers.

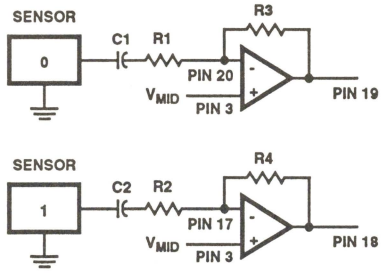


FIGURE 3. INPUT AMPLIFIER CONNECTIONS

A mid-voltage level is generated by the IC. This level is set to be half way between V_{DD} and ground. Throughout the IC this level is used as a quiet, DC reference for the circuits within the IC. This point is brought out for several reasons: it can be used as a reference voltage, and it must be bypassed to ensure that it is a quiet reference for the internal circuitry.

The input amplifiers are designed with power down capability, which, when activated disables their bias circuit and their output goes into a tri-state condition. This is very important during the test mode, in which the output terminals of the amplifiers are driven by the outside world with test signals.

Antialiasing Filter

The IC has a 3rd order Butterworth filter with a -3dB point at 70kHz. Double poly-silicon capacitors and implanted resistors are used to set poles in the filter. This filter is required to have no more than 1dB attenuation at 20kHz (highest frequency off interest) and a minimum attenuation of 10dB at 180kHz. This filter precedes the switch capacitor filters which run at 200kHz.

Programmable Band Pass Switched Capacitor Filters

Two identical programmable filters are used to detect the two frequencies of interest. The Knock Frequency Filter is programmed to pass the frequency component of the engine knock. The Reference Frequency Filter is used to detect background noise at a second programmed frequency. The filter frequency is established by the characteristics of the particular engine and transducer. By subtracting the energy component of these two filters, we can detect if a knock has occurred.

The filters have a nominal differential gain of 4. Their frequency is set by program words (discussed in the Communications Protocol section). Center frequencies can be programmed from 1.22kHz to 19.98kHz, in 64 steps. The filter Q's are typically 2.4.

Balance/Gain Adjust Stage

The gains from the Knock Frequency Filter and the Reference Frequency Filter can be adjusted with respect to one another, so that the difference energies in the two bands can be compensated. This balance is achieved by feeding one of

the filters unattenuated (gain = 1) and attenuating the other. This can be adjusted with 64 different gain settings, ranging between 1 and 0.133. The signals can swing between 20 and 80 percent of V_{DD}.

Programming is discussed in the Communications Protocol section. The test/channel attenuate word is used to determine which of the two channels is attenuated and which is set to unity gain.

Active Full Wave Rectifier

The output of the filters are independently full wave rectified using switch capacitor techniques. Each of two rectifier circuits provide both negative and positive values for the knock frequency and reference frequency filter outputs. The output is able to swing from 20 to 80 percent of V_{DD}. Care was taken to minimize the RMS variations from input to output of this section.

Integrator Stage

The signals from the two rectifiers are summed and integrated together. A differential system is used to reduce noise. One system integrates the positive energy of the Knock Frequency Rectifier with respect to the positive energy of the Reference Frequency Rectifier. The second system does the integration of the negative energy value of the two rectifiers. The positive and negative energy signals are opposite phase signals. Using this technique reduces system noise.

The integrator time constant is software programmable by the Integrator Time Constant discussed in the Communications Protocol section. The time constant can be programmed from 40µs to 600µs, with a total of 32 steps. If for example, we program a time constant to 200µs, then with one volt difference between each channel, the output of the integrator will change by 1 volt in 200µs.

When integration is enabled by the rising edge of the INT/$\overline{\text{HOLD}}$ input, the output of the integrator will fall to 0.5V, within 20µs after the integrate line reaches the integrate state. The output of the integrator is an analog voltage.

Test Multiplexer

This circuit receives the positive and negative outputs from the two integrators, together with the outputs from different parts of the IC. The output is controlled by the fifth programming word of the communications protocol. This multiplexes the switch capacitor filter output, the gain control output and the antialiasing filter output.

Differential to Single-Ended Converter

This signal takes the output of the two integrators (through the test-multiplexer circuit) and provides a signal that is the sum of the two signals. This technique is used to improve the noise immunity of the system.

Output Buffer

This output amplifier is the same amplifier circuits as the input amplifier used to interface with the sensors. When the output of the antialiasing filter is tested, this amplifier is in the power down mode.

Communications Protocol

The multiprocessor talks to the knock sensor via an SPI bus (MOSI). A chip select pin ($\overline{\text{CS}}$) is used to enable the chip, which, in conjunction with the SPI clock (SCK), moves in the eight bit programming word. Five different programming words are used to set gains, frequency response, integrator constants, test mode, channel select and test mode conditions.

With chip select ($\overline{\text{CS}}$) going low, on the next rising edge of the SPI clock (SCK), data is latched into the IC. The data is shifted with the most significant bit first and least significant bit last. Each word is divided into two parts: first the address and then the value. Depending on the function being controlled, the address is 2 or 3 bits, and the value is either 5 or 6 bits long. During the hold mode of operation, all five programming words can be entered into the IC, but during the integrate time any single byte may be entered but will not be acted upon until the start of the next hold period. The integration or hold mode of operation is controlled by the INT/$\overline{\text{HOLD}}$ input signal.

Programming Words

1. Reference Filter Frequency: Defines the center frequency of the Reference Filter in the system. The first 2 bits are used for the address and the last 6 bits are used for its value. 01FFFFFF Example: 01001010 would be the reference filter (01 for the first two bits) at a center frequency of 1.78kHz (bit value in Table 2 of 10).

2. Knock Filter Frequency: Defines the center frequency of the Knock Filter in the system. The first 2 bits are used for the address and the last 6 bits are used for its value. 00FFFFFF Example: 00100111 would be the knock filter frequency (00 for the first two bits) at a center frequency of 6.37kHz (bit value in Table 2 of 39).

3. Balance Control: Defines the ratio of the gain of the knock band center frequency to that of the reference band center frequency. This role can be reversed by the value of C_A in the fifth programming bit, as explained in 5, Test/Channel Select/Channel Attenuate Control. The first 2 bits are used for the address and the last 6 bits for its value. 10GGGGGG Example: 10010100 would be the balance control (10 for the first two bits) with an attenuation of 0.514 (bit value in Table 2 of 20.) Depending on the value of C_A in the fifth word this would apply to the reference or the knock gain section.

4. Integrator Time Constant: Defines the Integration Time Constant for the system. The first 3 bits are used for the address and the last 5 bits for the value. 110TTTTT Example: 11000011 would be the integrator time constant (110 on for the first 3 bits) and an integration constant of 55µs (bit value of 3 in Table 2).

5. Test/Channel Select/Channel Attenuate Control: This word serves several purposes. By looking at the structure, $111T_AT_BT_CC_SC_A$, the first 3 bits are used for the address, and the last 5 bits are used for the value. The options are:

- If CS is "0" channel "0" is selected. If CS is "1" channel "1" is selected.
- If C_A is "0" attenuation applies to the knock filter. If C_A is "1" attenuation applies to the reference filter.
- During the test mode ($\overline{TEST}$ input is a low level), if T_A is "0" all sections get their input from the output of the antialiasing filter input. This input can come from either the output of channel "0" amplifier or channel "1" output depending upon the state of the C_S bit. If T_A is "0" the input amplifiers are powered down. If T_A is set to "1" during the test mode the chip is configured in its normal operating state, getting inputs to all sections from previous sections.
- Combinations of T_A, T_B and T_C are used to test the different analog parts of the circuit. Table 1 shows these combinations. All blocks except for the antialiasing filter are sampled via the differential to single ended converter in the test mode.

TABLE 1. SHOWING PROGRAMMING IN THE TEST MODE

$\overline{TEST}$ PIN 14	T_A	T_B	T_C	C_{HS}	ANALOG OUTPUT FROM:
0	0	0	0	0	Knock Rectifier
0	0	0	0	1	Reference
0	0	0	1	0	Knock Filter
0	0	0	1	1	Reference Filter
0	0	1	0	0	Antialias Filter(1)
0	0	1	0	1	Antialias Filter(1)
0	0	1	1	0	Integrator
0	0	1	1	1	Integrator
0	1	0	0	0	Knock Rectifier
0	1	0	0	1	Reference
0	1	0	1	0	Knock Filter
0	1	0	1	1	Reference Filter
0	1	1	0	0	Antialias Filter(1)
0	1	1	0	1	Antialias Filter(1)
0	1	1	1	0	Integrator
0	1	1	1	1	Integrator
1	x	x	x	x	Integrator

NOTE:

1. All Test function blocks have their outputs buffered by the differential to single ended converter. Their outputs are available at the INTOUT pin 4 of the chip. In the case of the antialias filter test function, the output is taken directly to the INTOUT pin 4 of the chip.

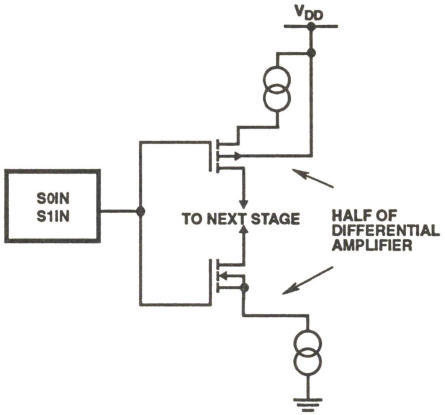


FIGURE 4A. S0IN AND S1IN INPUT CIRCUIT

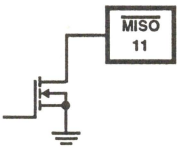


FIGURE 4B. $\overline{MISO}$ OUTPUT OF SPI DATA BUS IS AN OPEN DRAIN TRANSISTOR

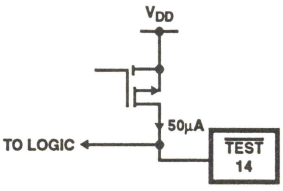


FIGURE 4C. $\overline{TEST}$ PMOS TRANSISTOR HAS EQUIVALENT CURRENT PULLUP CAPABILITY OF A 50k TO 200k RESISTOR

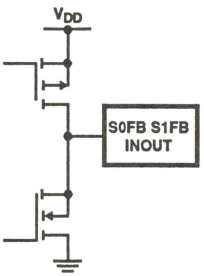


FIGURE 4D. S0FB, S1FB AND INOUT EQUIVALENT OUTPUT CIRCUITS

FIGURE 4. INTERFACE CIRCUITS

TABLE 2. FREQUENCY, BALANCE / GAIN AND INTEGRATOR TIME CONSTANT SETTINGS

BIT VALUE PER FUNCTION	FREQUENCY kHz	OUTPUT LEVEL	TIME CONSTANT µs	BIT VALUE PER FUNCTION	FREQUENCY kHz	OUTPUT LEVEL
0	1.22	1.000	40	32	4.95	0.360
1	1.26	0.960	45	33	5.12	0.346
2	1.31	0.923	50	34	5.29	0.333
3	1.35	0.889	55	35	5.48	0.320
4	1.40	0.857	60	36	5.68	0.309
5	1.45	0.828	65	37	5.90	0.298
6	1.51	0.800	70	38	6.12	0.288
7	1.57	0.774	75	39	6.37	0.279
8	1.63	0.750	80	40	6.64	0.270
9	1.71	0.727	90	41	6.94	0.262
10	1.78	0.706	100	42	7.27	0.254
11	1.87	0.686	110	43	7.63	0.247
12	1.96	0.667	120	44	8.02	0.240
13	2.07	0.649	130	45	8.46	0.234
14	2.18	0.632	140	46	8.95	0.228
15	2.31	0.615	150	47	9.50	0.222
16	2.46	0.600	160	48	10.12	0.217
17	2.54	0.576	180	49	10.46	0.208
18	2.62	0.554	200	50	10.83	0.200
19	2.71	0.533	220	51	11.22	0.193
20	2.81	0.514	240	52	11.65	0.186
21	2.92	0.497	260	53	12.10	0.179
22	3.03	0.480	280	54	12.60	0.173
23	3.15	0.465	300	55	13.14	0.168
24	3.28	0.450	320	56	13.72	0.163
25	3.43	0.436	360	57	14.36	0.158
26	3.59	0.424	400	58	15.07	0.153
27	3.76	0.411	440	59	15.84	0.149
28	3.95	0.400	480	60	16.71	0.144
29	4.16	0.389	520	61	17.67	0.141
30	4.39	0.379	560	62	18.76	0.137
31	4.66	0.369	600	63	19.98	0.133

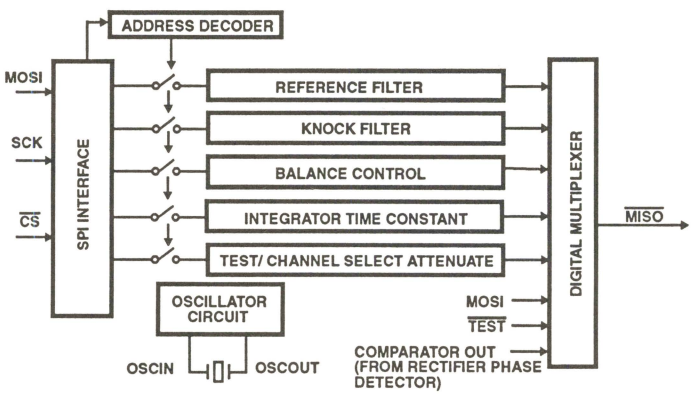


FIGURE 5. DIGITAL BLOCK DIAGRAM

The digital block diagram shows the programming flow of the chip. An eight bit word is received at the $\overline{MISO}$ port. Data is shifted in by the SCK clock when the chip is enabled by the $\overline{CS}$ pin. The word is decoded by the address decoding circuit, and the information is directed to one of 5 registers. These registers control:

1. Reference knock filter frequency.
2. Knock filter frequency.
3. Balance control or attenuation of one channel with respect to the other.
4. Integration time constant of the sum of the two channels.
5. One of 3 functions.
   a) test conditions of the part.
   b) channel select to one of two sensors.
   c) channel to be attenuated.

A crystal oscillator circuit is provided. The chip requires a 4MHz crystal to be connected across OSCIN and OSCOUT pins.

In the test mode, use the digital multiplexer to output one of the following signals:

1. Contents of one of the five registers in the chip.
2. Inverted signal of the MOSI pin.
3. Voltage of an internal comparator used to rectify the analog signal.

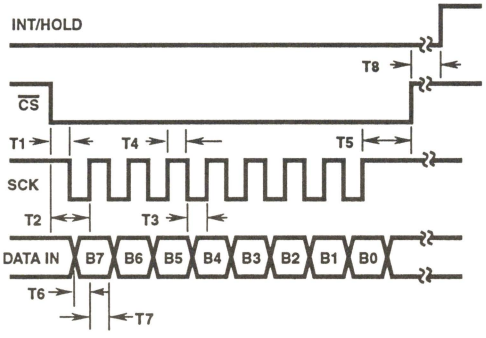


FIGURE 6. SPI TIMING

TABLE 3. SPI TIMING REQUIREMENTS

DESCRIPTION	UNITS
T1 min. time from $\overline{CS}$ falling edge to SCK falling edge.	10ns
T2 min. time from $\overline{CS}$ falling edge to SCK rising edge.	80ns
T3 min. time for the SCK low.	60ns
T4 min. time for the SCK high.	60ns
T5 min. time from SCK rise after 8 bits to $\overline{CS}$ rising edge.	80ns
T6 min. time from data valid to rising edge of SCK.	60ns
T7 min. time for data valid after the rising edge of the SCK.	10ns
T8 min. time after $\overline{CS}$ rises until INT/$\overline{HOLD}$ goes high.	8µs

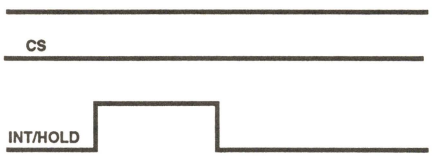


FIGURE 7. POWER UP SEQUENCE

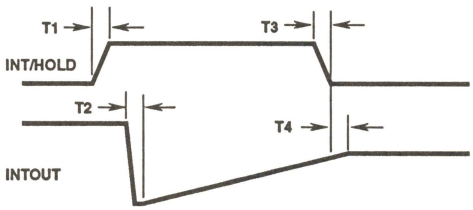


FIGURE 8. INTEGRATOR TIMING

TABLE 4. INTERGRATE/$\overline{HOLD}$ TIMING REQUIREMENTS

DESCRIPTION	UNITS
T1 max. rise time of the INT/$\overline{HOLD}$ signal.	45ns
T2 max. time after INT/$\overline{HOLD}$ rises for the INOUT to begin to intergrate.	20µs
T3 max. fall time of INT/$\overline{HOLD}$ signal.	45ns
T4 typical time after INT/$\overline{HOLD}$ goes high before chip goes into hold state.	20µs

Test Multiplexer

This circuit receives the positive and negative outputs out of the two integrators, together with the outputs from different parts of the chip. The output is controlled by the fifth programming word of the communications protocol. This multiplexes the switch capacitor filter output, the gain control output as well as the antialias output.

Differential to Single-ended Converter

This signal takes the output of the two integrators (through the test multiplexer circuit) and provides a signal that is the sum of the two signals. This technique is used to improve the noise immunity of the system.

Output Buffer

This output amplifier is the same as the input amplifier used to interface to the sensors. For test purposes when we look at the output of the antialias filter, the input amplifiers are in the power down mode.

HARRIS SEMICONDUCTOR

HIP9020

Programmable Quad Buffer with Pre and Post Scaler Dividers

October 1993

Features

- Sine Wave Speedometer Input
- Input Limiting . . . . . ±0.25V to ±100V (with 40kΩ)
- Over Voltage Protection
- Current Limiting
- Programmable Prescaler 1, 6 - 11
- Post Scaler Frequency Divide by 1 or 2
- Drivers with 15mA/24V Capability
- Outputs 4 Separate Square Waves
- Internal Regulator and Bias Source
- 0kHz to 6kHz Input Signal Range
- -40°C to +125°C Operating Temperature Range

Applications

- Prescaler
- Buffer/Limiter
- Signal Interface
- Automotive Speedometer
- Automotive Speed Control
- Automotive Tachometer

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP9020AP	-40°C to +125°C	14 Lead Plastic DIP
HIP9020AB	-40°C to +125°C	20 Lead Plastic SOIC (W)

Description

The HIP9020 is a Vehicle Speed Sensor (V_{SS}) Buffer IC. It receives sinusoidal vehicle speed information from a speedometer signal source. The signal is amplified and squared before frequency processing is done. The circuit provides pin programmable integer prescaler and postscaler dividers to scale the output frequencies. The prescaler divider output of the frequency doubler is mode selected for 1 and 6 through 11. The postscaler mode is selected to the Output 3 with a divide by 1 or 2. The four V_{OX} outputs are open collector drivers.

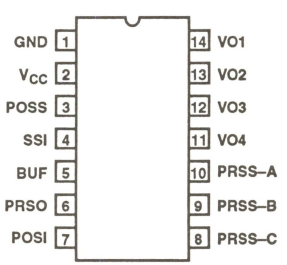
Speed Sensor Input (SSI) - When current limited with a 40kΩ source impedance from the vehicle speed sensor, the SSI input is capable of functioning over a wide range of input signal. The limiter and squaring action is derived from the zero crossing of the input signal. The signal is converted into a square wave with a controlled hysteresis squaring amplifier.

Power Supply - The power supply pin 2 input is intended to operate from a 5.0V ± 0.3V source. The internal reference sources are derived from a temperature stable bandgap; including an optional 5.7V shunt regulator which may be used as shown in Figure 2.

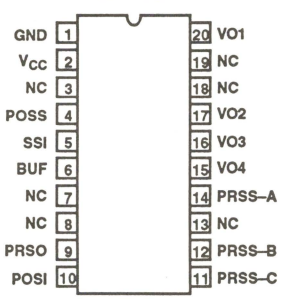
Output Drivers - Each output driver is an open NPN collector with a zener clamp level of typically 35V and short circuit current limiting. Each output is capable of sinking 15mA of current.

Pinouts

HIP9020 (PDIP)
TOP VIEW



HIP9020 (SOIC)
TOP VIEW

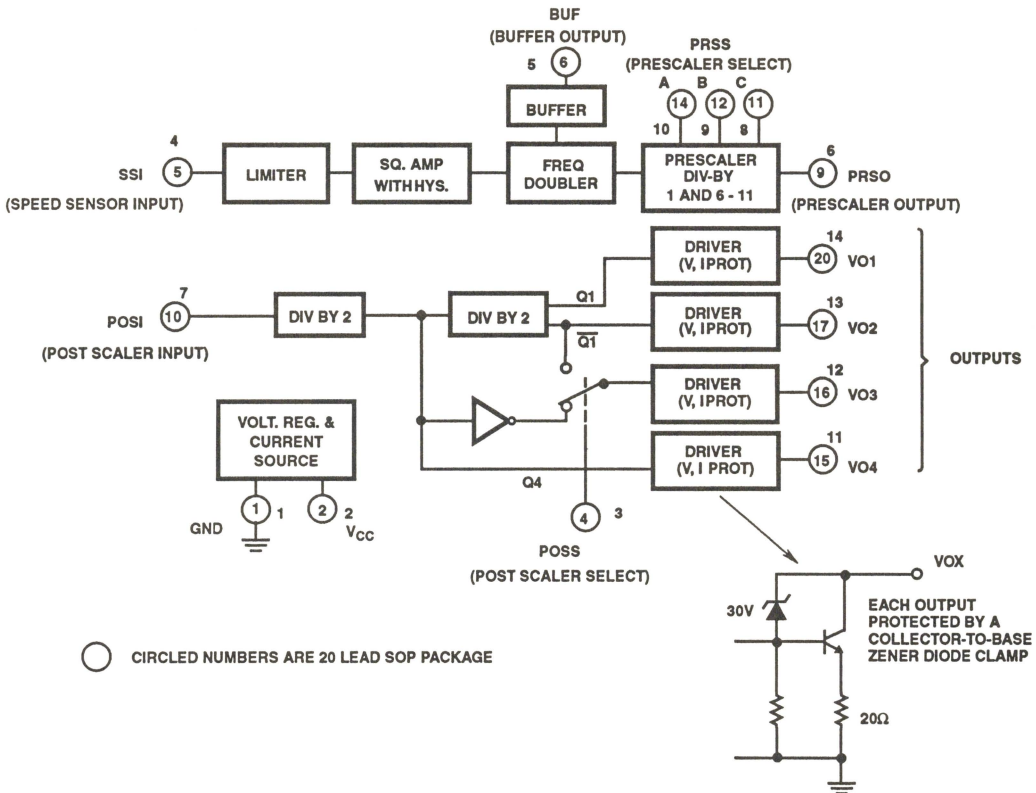


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2790.2**

Programmable Quad Buffer Functional Block Diagram



LOGIC SELECT FOR INPUT (SSI) TO OUTPUT (VOX) DIV-BY NUMBER

PRSS-A	PRSS-B	PRSS-C	VO1, VO2, VO3 (POSS HIGH) DIV-BY	VO4 (POSS HIGH) DIV-BY	VO1, VO2 (POSS LOW) DIV-BY	VO3, VO4 (POSS LOW) DIV-BY
0	0	0	2	1	2	1
0	0	1	12	6	12	6
0	1	0	14	7	14	7
0	1	1	16	8	16	8
1	0	0	18	9	18	9
1	0	1	20	10	20	10
1	1	0	22	11	22	11

Absolute Maximum Ratings

Supply Voltage to Pin 2, V_{CC} (Shunt Regulator) . . . . . +24V_{DC} Max through 300Ω and a Series Diode (1N4005 or Equiv.) or +5.3V Max Direct Voltage Supply Source to V_{CC}
Output Voltage (Sustained) to V01,V02,V03,V04 . . . . . +24V
Output Load Current (Sink) . . . . . +15mA
Input Voltage (Through 40kΩ, See Figure 1) . . . . . ±100V

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP and SOIC Package	90°C/W
Maximum Package Power Dissipation up to +85°C	720mW
Derate above 85°C	11.1mW/°C
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	+150°C
Lead Temperature (Soldering 10s)	+265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +125°C, V_{CC} = 5V ± 0.3V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply (V_{CC})					
Supply Current	I_{CC}		-	12	mA
SSI Input (Test Point - T.P.A., See Figure 1)					
Max. Operating Frequency	$f_{S(MAX)}$	40kΩ Source, 0.01µF Input Shunt	-	6	kHz
Input Signal Range		40kΩ Source, 0.01µF Input Shunt	±0.25	±100	V
Input Hysteresis		40kΩ Source, 0.01µF Input Shunt	0.15	0.45	V
Input Bias Current		40kΩ Source, 0.01µF Input Shunt	-0.5	+0.5	µA
Other Inputs (PRSS, POSS, POSI - See Function Block Diagram)					
Input Low Voltage	V_{IL}		-	1.5	V
Input High Voltage	V_{IH}		3.5	-	V
Input Current High	I_{IH}	V_{CC} = V_{IN} = 4.7V	-	10	µA
Input Current Low	I_{IL}	V_{CC} = 5.3; V_{IN} = 0.4V	-10	-	µA
PRSO Output					
Output Voltage Low	V_{OL}	V_{CC} = 5V	-	0.4	V
Output Voltage High	V_{OH}	V_{CC} = 5V	4.6	-	V
Driver Outputs (V01, V02, V03, V04)					
Output Clamp Voltage		I_{CC} = 1mA	24	45	V
Output Current Limit		I_{SC} Current Pulsed	15	30	mA
Output Leakage		V_{OUT} = 24V	-	30	µA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 15mA	-	1	V
		I_{OUT} = 1mA	-	0.4	V

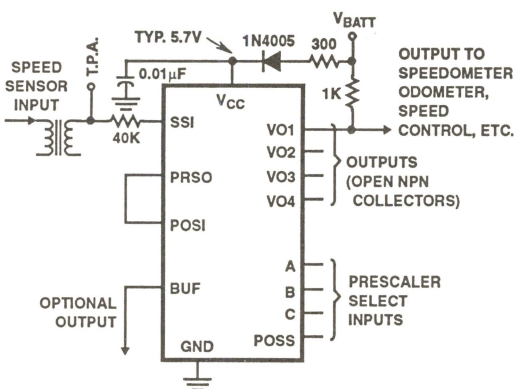


FIGURE 1. TYPICAL AUTOMOTIVE APPLICATION CIRCUIT

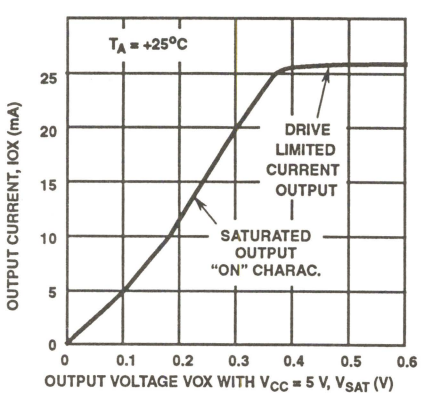


FIGURE 2. TYPICAL OUTPUT DRIVER SATURATED "ON" CHARACTERISTIC

INTELLIGENT POWER ICs 11

APPLICATION NOTES

APPLICATION NOTES		PAGE
AN027.1	Power Supply Design Using the ICL8211 and ICL8212	11-3
AN051.1	Principles and Applications of the ICL7660 CMOS Voltage Converter	11-11
AN5766.1	Application of the CA3020 and CA3020A Multipurpose Wide-Band Power Amplifiers	11-21
AN6048.1	Some Applications of a Programmable Power Switch/Amplifier	11-29
AN6077.1	An IC Operational Transconductance Amplifier (OTA) with Power Capability	11-42
AN6157.1	Applications of the CA3085 Series Monolithic IC Voltage Regulators	11-52
AN6182.1	Features and Applications of Integrated Circuit Zero-Voltage Switches (CA3059 and CA3079)	11-63
AN6915.1	Application of the CA1524 Series Pulse-Width Modulator ICs	11-94
AN7174.1	The CA1524 Pulse-Width Modulator-Driver for an Electronic Scale	11-112
AN7244.2	Understanding Power MOSFETs	11-114
AN7254.2	Switching Waveforms of the L^2FET: A 5 Volt Gate-Drive Power MOSFET	11-118
AN7326.1	Applications of the CA3228E Speed Control System	11-126
AN8614.1	The CA1523 Variable Interval Pulse Regulator (VIPUR) for Switch Mode Power Supplies	11-142
AN8829.2	SP600 and SP601 an HVIC MOSFET/IGT Driver for Half-Bridge Topologies	11-155
AN9010.4	HIP2500 High Voltage ($500V_{DC}$) Half-Bridge Driver IC	11-161
AN9105.1	HVIC/IGBT Half-Bridge Converter Evaluation Circuit	11-169
AN9201.1	Protection Circuits for Quad and Octal Low Side Power Drivers	11-170
AN9208	High Frequency Power Converters	11-178
AN9209.1	A SPICE-2 Subcircuit Representation For Power MOSFETs, Using Empirical Methods	11-187
AN9212.1	HIP5060 Family Of Current Mode Control ICs Enhance 1MHz Regulator Performance	11-191
AN9217.1	High Current Off Line Power Supply	11-198
AN9301	High Current Logic Level MOSFET Driver	11-209
AN9302.1	CA3277 Dual 5V Regulator Circuit Applications	11-212
AN9304.3	ESD and Transient Protection Using the SP720	11-221
AN9323.1	HIP5061 High Efficiency, High Performance, High Power Converter	11-231
AN9324.1	HIP4080, 80V High Frequency H-Bridge Driver	11-241
AN9325	HIP4081, 80V High Frequency H-Bridge Driver	11-253
AN9404	HIP4080A, 80V High Frequency H-Bridge Driver	11-264
AN9405	HIP4081A, 80V High Frequency H-Bridge Driver	11-276

POWER SUPPLY DESIGN USING THE ICL8211 AND ICL8212

Introduction

The ICL8211 and ICL8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the THRESHOLD input is less than 1.15V. Figure 1 shows a simplified functional diagram of the ICL8211.

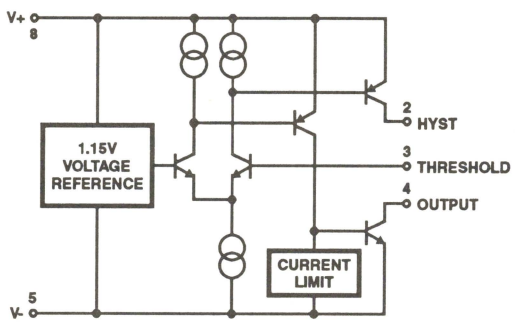


FIGURE 1. ICL8211 FUNCTIONAL DIAGRAM

The ICL8212 provides a saturated transistor output (no current limit) whenever the input THRESHOLD voltage exceeds 1.15V. Both circuits have a low current HYSTERESIS output which is turned on when the THRESHOLD voltage exceeds 1.15V, enabling the user to add controlled hysteresis to his design. Figure 2 shows a simplified functional diagram of the ICL8212.

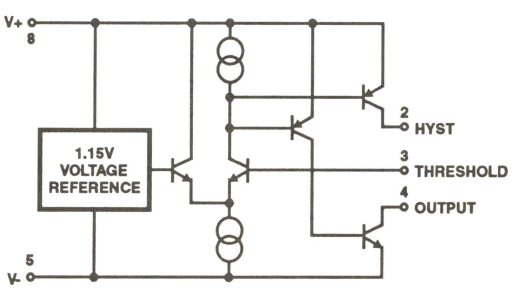


FIGURE 2. ICL8212 FUNCTIONAL DIAGRAM

For a detailed circuit description of the ICL8211/ICL8212 refer to the data sheet. For large volume applications the ICL8211/ICL8212 may be customized by the use of metal mask options to include setting resistors or to vary the output options, or even to adapt the circuit as a temperature sensing element.

Applications for the ICL8211/ICL8212 include a variety of voltage detection circuits, power supply malfunction detectors, regulators, programmable zeners, and constant current sources. In this discussion we will explore the uses of the ICL8211/ICL8212 in power supply circuits of various types. Their attractiveness to the power supply designer lies largely in their ability to operate at low voltage and current levels where standard power supply regulator devices cannot be used. In addition, the unique features of the ICL8211/ICL8212 make them useful in many ancillary circuits such as current sources, overvoltage crowbars, programmable zeners and power failure protection.

Positive Voltage Regulators

Using the ICL8211/ICL8212 it is possible to design a series of power supply regulators having low minimum input voltage and small input/output differential. These are particularly useful for local regulation in electronic systems as their small input/output differential results in low power loss.

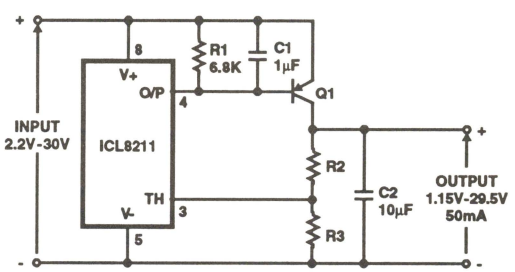


FIGURE 3. POSITIVE REGULATOR - PNP BOOST

The ICL8211 in Figure 3 provides the voltage reference and regulator amplifier while Q1 is the series pass transistor. R1 defines the output current of the ICL8211 while C1 and C2 provide loop stability and also act to suppress feed-through of input transients to the output supply. R2 and R3 determine the output voltage as follows:

$$V_{OUT} = 1.15 \times \frac{R2 + R3}{R3}$$

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In addition, the values of R2 and R3 are chosen to provide a small amount of standing current in Q1, which gives additional stability margin to the circuit. Where accurate setting of the output voltage is required, either R2 or R3 can be made adjustable. If R2 is made adjustable the output voltage will vary linearly with shaft angle; however, if the potentiometer wiper were to open circuit, the output voltage would rise. In general, therefore, it is better to make R3 adjustable as this gives fail-safe operation.

The choice of Q1 depends upon the output requirements. The ICL8211 has a worst case maximum output current of 4mA, so with any reasonable device for Q1 the circuit should be capable of 50mA output current with an input to output drop of 0.5V. If larger output currents are required Q1 could be made into a complementary quasi-darlington, but the input/output differential will then increase.

Note also that Q1 provides an inversion within the loop so the non-inverting ICL8211 must be used to give overall negative feedback.

One limitation of the above circuit is that input voltages must be restricted to 30V due to the voltage rating of the ICL8211. The circuit of Figure 4 avoids this problem.

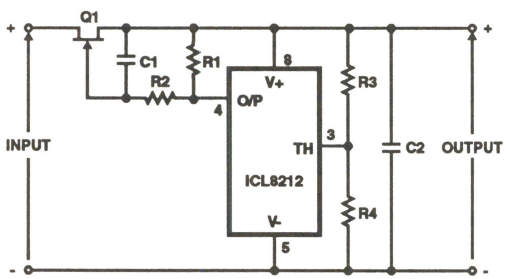


FIGURE 4. POSITIVE REGULATOR - JFET BOOST

In this circuit the input voltage is limited only by the voltage rating of Q1. The input/output differential is now dependent on the $R_{DS(ON)}$ of the JFET boost transistor. For instance, if Q1 were a 2N4391 the maximum output current would be equal to $I_{DSS(MIN)}$ which is 50mA and the input/ output differential would be:

$R_{DS(ON)} \times I_{LOAD} = 30\Omega \times 50mA = 1.5V$

However, at lower load currents the input/output differential will be proportionately lower.

A further consideration when choosing the FET boost transistor is that its pinch-off voltage must be less than the output voltage in order for the ICL8212 to be able to pull the gate down far enough to turn the device off at no load.

The predominant loop time constant is provided by R2 and C1. This time constant should be chosen as small as possible commensurate with loop stability as it also affects load transient response. After an abrupt change in load current C1 must be charged to a new voltage level by R2 to regulate the current in Q1 to the new load level and therefore the smaller the R2 x C1 product the better the load transient response. The value of C2 should be chosen to maintain the output within desired limits during the recovery period of the main loop. Note, however, that because of the wide bandwidth of the ICL8212 and the absence of charge storage effects in the FET, these considerations are not particularly restrictive.

For higher current outputs the system could be further boosted using a bipolar transistor. One attraction of using a FET only output, however, is that the I_{DSS} of the FET gives a measure of output short circuit protection. Should both the low input/output differential of the circuit of Figure 3 plus the extended input voltage capability of Figure 4 be required, the circuit of Figure 5 may be used.

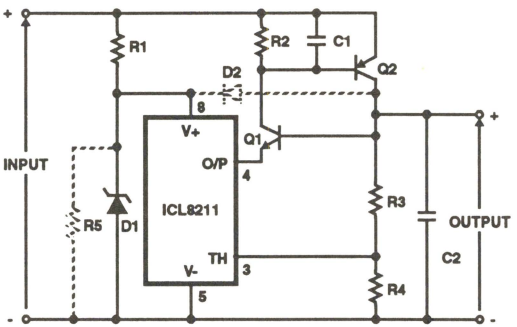


FIGURE 5. POSITIVE REGULATOR - NPN + PNP BOOST

This circuit is similar to that of Figure 3 except that Q1 has been added as a common base stage to buffer the output of the ICL8211 from the input supply and R1 and D1 to protect the input. Unfortunately, the ICL8211 cannot be supplied from the regulated output as this would result in the power supply being non self-starting. The choice of values for R2, R3, R4, C1 and C2 is identical to that of Figure 3, while D1 must be a voltage equal to or larger than the output voltage. R1 must be chosen to provide the relatively low supply current requirement of the ICL8211. An alternative arrangement for starting the circuit is to replace D1 with R5 and add D2. In this case the choice of R1 and R5 is such that once the output supply is established the ICL8211 is supplied through D2.

In the circuit of Figure 5, Q1 and Q2 are connected in the classic S.C.R. or Thyristor configuration. Where higher input voltages or minimum component count are required the circuit of Figure 6 can be used. The thyristor is running in a linear mode with its cathode as the control terminal and its gate as the output terminal. This is known as the remote base configuration.

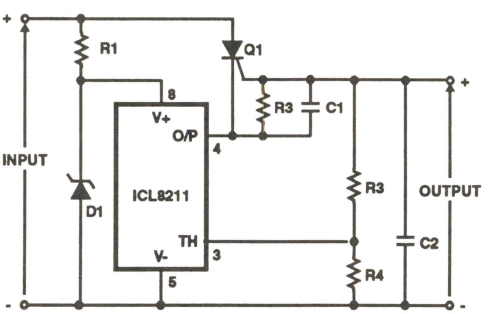


FIGURE 6. POSITIVE REGULATOR - THYRISTOR BOOST

A word of warning, however. Thyristor data sheets do not generally specify individually the gain of the PNP portion of the thyristor, on which the circuit relies. It must therefore either be very conservatively designed or some screening or guarantee of the PNP gain be provided.

Note that, with the exception of the I_{DSS} limit of Figure 4, none of the circuits so far provide output current limiting. In general, they are intended for applications in which the extra voltage drop of a current sensing resistor would be unacceptable. Where the circuits are used as local regulators and the output supplies are only connected to local circuitry the chance of output short circuits is relatively low and overcurrent protection is considered unnecessary. Where protection is required it can be added by any of the standard techniques. Figure 7 shows the simplest possible constant current protection added to the circuit of Figure 3.

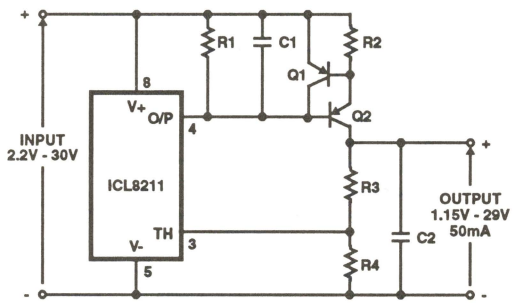


FIGURE 7. POSITIVE REGULATOR - PNP BOOST CURRENT LIMITED

In this circuit the current threshold is set by the base-emitter voltage of Q1 so that when the voltage drop in R2, due to load current, is sufficient to turn on Q1 base drive is removed from Q2 by Q1 collector. Note that this circuit works only because the output current of the ICL8211 is current limited so that there is no danger of Q1 and the ICL8211 blowing each other up with unlimited current.

Negative Voltage Regulators

Because the reference voltage of the ICL8211/ICL8212 is connected to the negative supply rail, and their output consists of the open collector of an NPN transistor, it is not possible to construct a negative equivalent of the circuit of Figure 3. However, a negative equivalent of Figure 4 is easily constructed.

Of course the JFET must now be a P-channel device but otherwise the design considerations are identical to those for Figure 4. Should further boost of the output current level be required, an NPN boost transistor, Q2, (shown dotted) can be added. However, the charge storage effects of the NPN transistor will reduce the loop bandwidth so that R2 or CI should be increased to maintain stability. Note also that in the circuit of Figure 8 an ICL8211 is used instead of an ICL8212 in order to maintain correct feedback polarity.

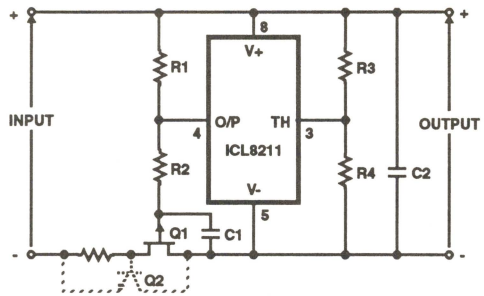


FIGURE 8. NEGATIVE REGULATOR - JFET BOOST

Figure 9 is the closest negative equivalent to the circuits of Figures 5 and 6. In this case R1, R2 and D1 ensure that the circuit is self starting. The divider R1/R2 must be chosen to ensure that sufficient voltage (say -1V) is present at the base of Q1 to start the circuit under minimum output voltage conditions, but once the circuit is running D1 must remain forward biased even at maximum input voltage, otherwise the output of the ICL8212 will be unable to pull the emitter of Q1 low enough to turn it off under no load conditions. Thus for a 3V output supply which runs from a minimum 4V input the ratio of R1 to (R1 + R2) must be one quarter. In order that the base of Q1 is not taken below -3V once the circuit is running the maximum input voltage would therefore be -12V. An alternative arrangement which avoids this restriction is to replace R1 with a zener diode, reduce the value of R2 and delete D1.

In this case the only restriction is that the zener voltage shall be less than or equal to the output voltage of the regulator.

In the circuit of Figure 9, R3 must be chosen to provide sufficient base drive for Q2 via Q1 under maximum load conditions. The maximum value of the current in R3 which may be tolerated is 12mA, the worst case sink current of the ICL8212 output transistor.

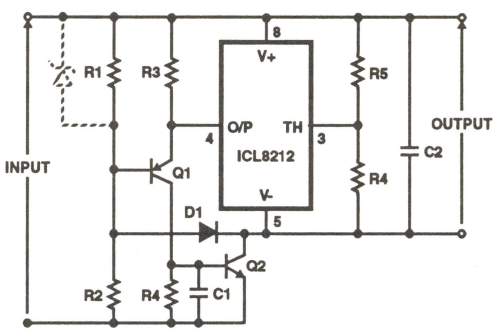


FIGURE 9. NEGATIVE REGULATOR - NPN + PNP BOOST

Current limit can be applied to the circuits of Figure 9 in an analogous manner to Figure 7. In this case R3 is the current source for the base of Q2, ensuring that the current limit transistor Q3 has a defined maximum collector current.

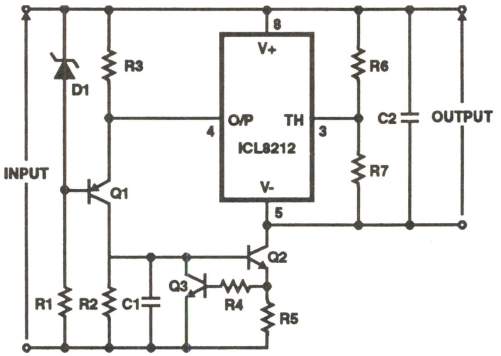


FIGURE 10. CURRENT LIMITED NEGATIVE REGULATOR - NPN + PNP BOOST

Ancillary Power Supply Circuits

Figure 11 shows the ICL8212 connected as a programmable zener diode. Zener voltages from 2V up to 30V may be programmed by suitable selection of R2, the zener voltage being:

$$V_Z = 1.15 \times \frac{R1 + R2}{R1}$$

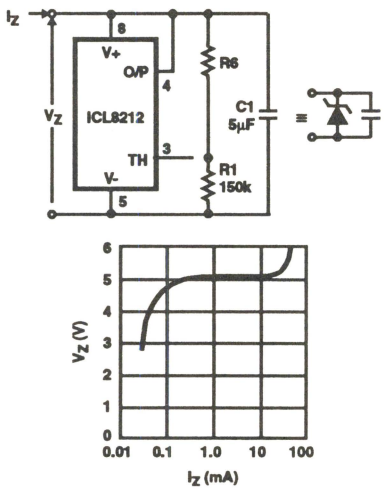


FIGURE 11. PROGRAMMABLE ZENER

Because of the absence of internal compensation in the ICL8212, C1 is necessary to ensure stability. Two points worthy of note are the extremely low knee current (less than 300µA) and the low dynamic impedance (typically 4Ω to 7Ω) over the operating current range of 300µA to 12mA.

The circuit of Figure 12 shows how the ICL8211/ICL8212 may be used as constant current circuits. At the current levels obtained with the ICL8211 or ICL8212 on their own, the principal application will be in providing the "tail" currents of differential amplifiers which may be used in power supply design. A more useful application in power supplies is the programmable current source shown in Figure 13.

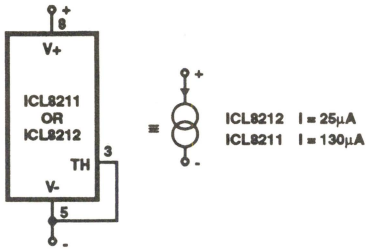


FIGURE 12. CONSTANT CURRENT SOURCES

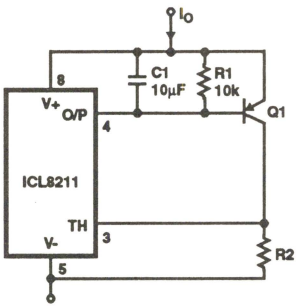


FIGURE 13. PROGRAMMABLE CURRENT SOURCE

In this case the output current is given by:

$$I_O = 25\mu A + \frac{V_{BE}}{R1} + \frac{1.15}{R2}(1 + \beta)$$

Where β is the forward current gain of Q1 and V_{BE} is its emitter-base voltage. The principal cause of departure from a true current source for this circuit will be the variations in β with collector voltage of Q1. With the current settable anywhere in the range of about 300µA to 50mA and an operating voltage range from 2V to 30V, this circuit is particularly suitable as the current source driving the base of an output transistor in conventional series regulator power supplies. Another useful application is as the current source feeding a reference zener in highly stable reference supplies. Again, because of the absence of internal compensation in the ICL8212, C1 is provided to ensure loop stability. It also helps to keep output current constant during voltage changes or transients.

The standard method of overcurrent protection in simple series regulated supplies is shown in Figure 14.

The current limit value is simply:

$$I_{CL} = \frac{V_{BE}(Q3)}{R2}$$

The disadvantages of the circuit is the poor temperature coefficient of the emitter base voltage of Q3, the large variation of V_{BE} between different devices and the badly defined transition between constant voltage and constant current states due to the low gain of the current regulation loop.

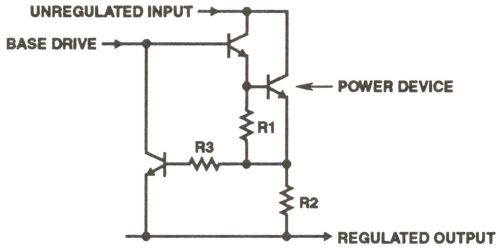


FIGURE 14. STANDARD CURRENT LIMIT

In this case the current limit value is:

$$I_{CL} = \frac{1.15V}{R2}$$

One advantage of the circuit is the much improved temperature coefficient of the limit current. In Figure 14 the typical coefficient is 0.3%/°C, while in Figure 15 the typical coefficient is 0.02%/°C. In addition, the higher gain of the ICL8212 gives a much sharper transition between voltage limit and current limit conditions. The spread of threshold voltages will also be lower in this circuit, but if precise adjustment of the threshold is required R3 and R4 may be added as shown in Figure 15.

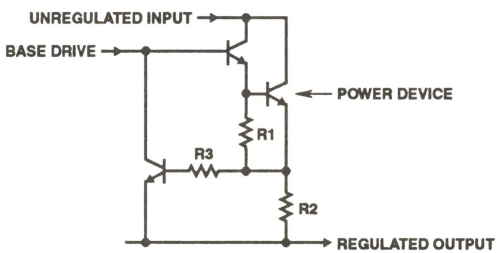


FIGURE 15. IMPROVED CURRENT LIMIT

The major penalty of the system is the extra 500mV which must be dropped in R2 to effect current limiting. Note again that the low operating voltage and power supply current allow the ICL8212 to be powered directly from the base drive voltage of the power supply.

This circuit protects sensitive loads against high voltage transients on the power supply rail. Should the input voltage exceed the threshold set by R2 and R1, the ICL8211 will turn off Q1 and hence protect the load from the transient. R3 provides optional voltage hysteresis if so desired.

The most popular form of overvoltage protection is the Thyristor crowbar, which short circuits the supply in the event of an overvoltage condition. The circuit of Figure 17 triggers a thyristor when the supply voltage reaches a threshold defined by R1 and R2. The very low quiescent current of the ICL8212 means that there is negligible voltage drop in R4 during sensing so that accuracy is unimpaired and there is no danger of triggering the thyristor. The connection from pin 2 provides hysteresis which is necessary in this case because the reference will rise on the top of R4 as soon as the threshold is reached and otherwise would provide negative feedback, which is overcome by the large positive feedback from pin 2. Resistor R3 limits the output current of the ICL8212 to a safe value of, say, 20mA. To operate properly the thyristor should have a gate trigger current not greater than about 10mA. Where higher gate currents are necessary the circuit of Figure 18 may be used.

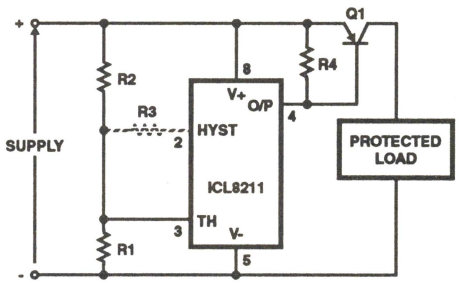


FIGURE 16. HIGH VOLTAGE DUMP CIRCUIT

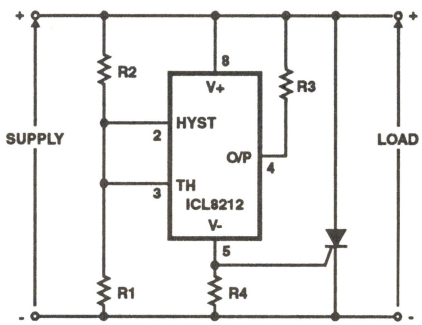


FIGURE 17. OVERVOLTAGE CROWBAR

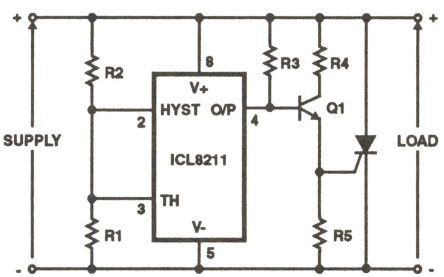


FIGURE 18. OVERVOLTAGE CROWBAR

In this case the ICL8211 holds down the base of Q1 until the circuit is triggered. The current in R3 should not exceed 4mA as this is the worst case current the ICL8211 can sink at its output. With this circuit thyristors requiring gate drives in the 50mA to 100mA region are easily tolerated.

Notice that in both the above circuits no extra supplies are needed to make the crowbars work down to voltages as low as 3V. In particular, this makes the circuits most suitable for use on 5V logic supplies where no other rails may be available to power a crowbar circuit or where, for reasons of safety, one does not wish to rely on auxiliary supplies.

In some systems it is undesirable to allow the supply rail to be partially established. For instance, in a logic system logical malfunctions may occur. Another example is the LM199/299/399 temperature stabilized reference. If the heater supply falls below about 9V the unit tends to "run away" and destroy itself.

Should the power supply voltage fall below the level determined by R1 and R2, Q1 is turned off, disconnecting the load entirely so that it cannot operate at partial voltage. Note that the removal of the load may cause the supply voltage to rise and the possibility of an oscillatory condition exists. Resistor R3 therefore provides a small hysteresis, which should be calculated to exceed the full load regulation drop of the supply.

The circuits of Figures 16 and 19 can be combined so that a load is only connected to the supply when the supply voltage is within a specified range. In this case IC1 senses the overvoltage condition while IC2 senses the undervoltage condition. Again, hysteresis may be added as necessary by the addition of R3 and R5.

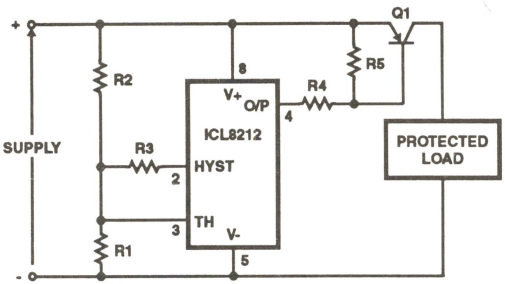


FIGURE 19. LOW VOLTAGE DISCONNECT

In many systems, particularly those using microprocessors, it is necessary to provide a logic signal which gives advance warning of an impeding power failure so that the system can execute a shutdown routine before power is lost. A simple undervoltage detector on the regulated supply is generally insufficient as by the time an undervoltage signal is generated, the supply is already out of regulation and unless it falls very slowly there will not be sufficient time to shut the system down properly.

In the circuit of Figure 21, an incipient power failure is detected at the unregulated input of the regulator. Note that the value of main reservoir capacitor C1 must be large enough so that the shutdown routine can take place before the regulator drops out of regulation. Waveforms for a typical power failure are shown in Figure 22.

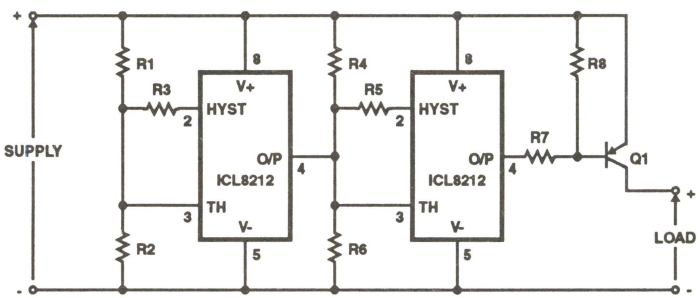


FIGURE 20. POWER SUPPLY WINDOW DETECTOR

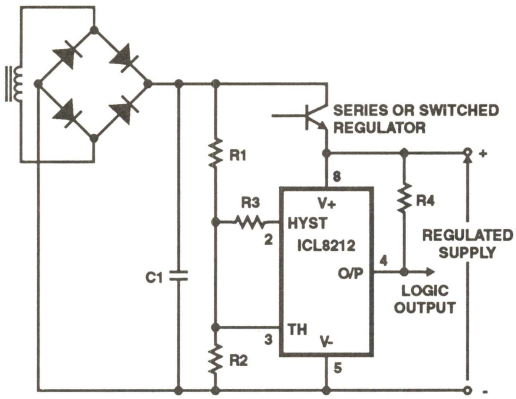


FIGURE 21. SIMPLE POWER FAIL SYSTEM

The threshold detector should be an ICL8212 if a logic '1' is required to initiate shutdown, or an ICL8211 if a logic '0' is required. Note that the ICL8212 will drive 7 TTL loads and the ICL8211 2 TTL loads.

Notice that, because of the ripple always present on the unregulated supply, power failure was not actually detected until some time after the removal of input power. This waste of time means that larger voltage margins must be built into the system, reducing the regulator efficiency under normal operating conditions. In some instances, however, this circuit may be adequate.

In Figure 24, the power is monitored at a point isolated from the main capacitor C1 so that failure can be detected without having to wait for C1 to discharge below the minimum voltage of the normal ripple. Waveforms for this circuit are shown in Figure 24.

In this case R1 tops up C2 to the zener voltage each cycle, while C2 holds the input of the ICL8211 or ICL8212 (depending on the polarity of the required output signal) above its threshold during the zero crossings of the AC waveform. However, in the event of a power failure, C2 discharges through R2 to the threshold voltage of 1.15V, at which point the power fail signal is activated.

In this case, the worst point at which a power failure can occur is just before Ct begins to charge on the rising side of the input AC signal. However, because of the fast warning given by the system, it is still superior than that of Figure 21 in the time allowed for a shutdown routine.

Conclusions

Just a few of the many possible applications of the ICL8211 and ICL8212 in power supply systems have been described. Both in power supply systems and elsewhere, the features of the ICL8211 and ICL8212 make them very useful general purpose circuits. Once aware of the useful features of these low power, low voltage circuits the designer will rapidly discover a large number of applications for himself.

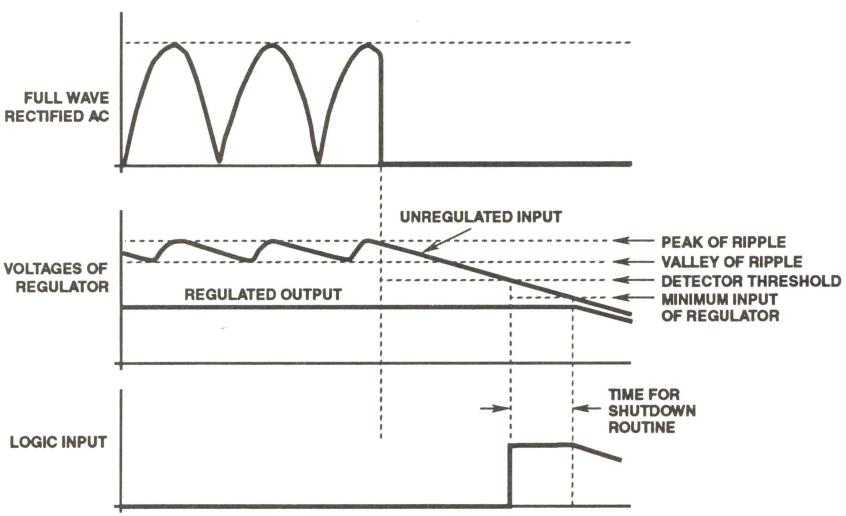


FIGURE 22. SIMPLE POWER FAIL SYSTEM WAVEFORMS

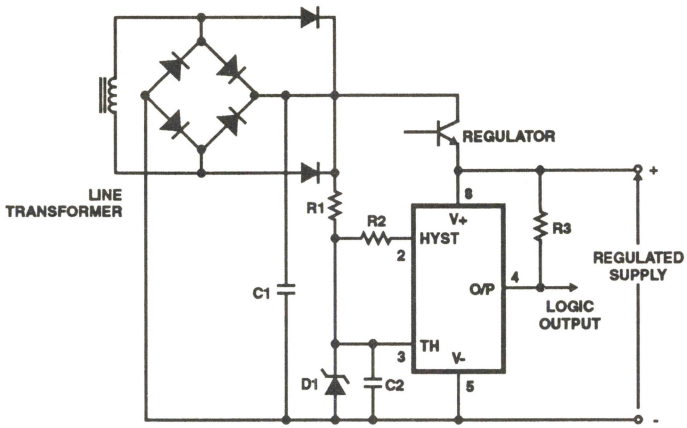


FIGURE 23. IMPROVED POWER FAIL SYSTEM

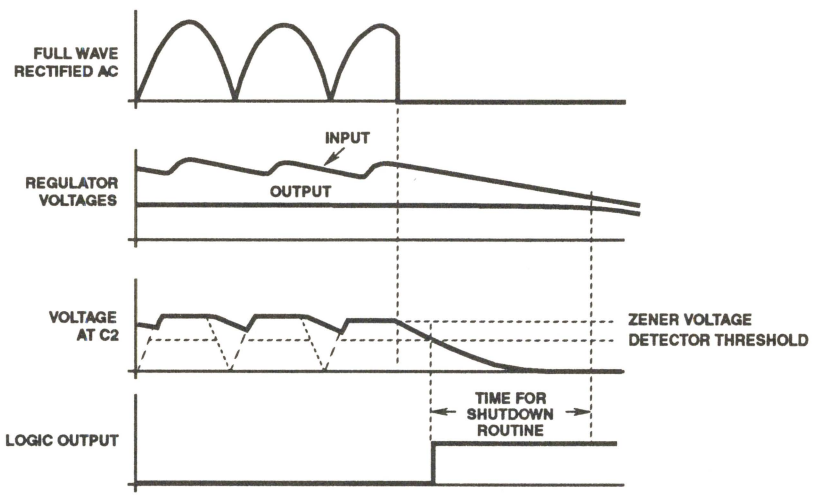


FIGURE 24. IMPROVED POWER FAIL SYSTEM WAVEFORMS

Harris Semiconductor

APPNOTE

No. AN051.1 April 1994

Harris Intelligent Power

PRINCIPLES AND APPLICATIONS OF THE ICL7660 CMOS VOLTAGE CONVERTER

Introduction

This application note describes a device originally designed to solve the specific problem of needing a negative supply when only a positive supply is available. This is very common, and occurs, for example, in systems using dynamic RAMs where the three-supply devices require a low current body bias supply of around -5V. Negative supply voltage is also desired in systems with a lot of digital logic (at +5V) but containing a small analog section using A/O converters, such as the ICL7107 or ICL7109 and/or op amps and comparators, operating on ground referenced signals. In all these cases, the current requirement and regulation are not very demanding, but nevertheless, generating such a -5V supply is usually expensive and inefficient. Typically, a large number of discrete and integrated-circuit components are needed to convert the common +5V line into a negative one, or to add an extra output to the main supply, the backplane wiring, etc.

This problem is solved by the ICL7660, a monolithic CMOS power supply circuit offering unique performance advantages over previously available devices. With the addition of only two noncritical capacitors (for charge pump and storage), it performs the complete supply voltage conversion from positive to negative for any input voltage between +1.5V and +10V, and provides the complementary output voltage of -1.5V to -10V. (An additional diode is needed for voltages above 6.5V.) The device operates by charging a pump capacitor to the input supply voltage and then applying the capacitor across the output supply, transferring the necessary charge to an open-circuit storage capacitor.

The ICL7660 delivers an open-circuit output equal to the negative of the input voltage to within 0.1%. Capable of producing 20mA, the device has a power-conversion efficiency of about 98% for load currents of 2mA to 5mA. The use of two or more ICL7660s extends the device's capability, as will be shown later.

Principles of Operation

Since the ICL7660 multiplies either positive or negative voltages by a factor of two, it can be considered a simple voltage doubler. This basic voltage doubling operation is shown in Figure 1, where S_1 and S_3 are the switches used to charge C_1, and S_2 and S_4 transfer the charge to C_2. It differs from most voltage doublers in that the usual blocking diodes are replaced by on-chip active MOS transistor switches.

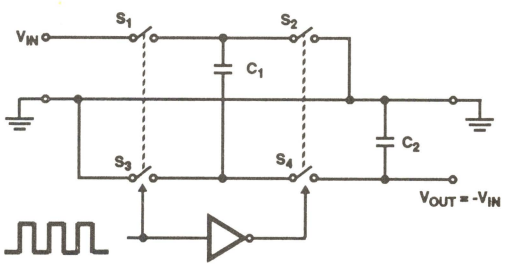


FIGURE 1. IDEALIZED VOLTAGE DOUBLER

For a negligible load, clearly the voltage inversion will be nearly perfect, with only a tiny charge being lost to stray capacitance. With a significant load, the behavior is more complex.

The amount of charge transferred from C_1 to C_2 depends upon the amount lost from C_2 to the load, and this charge must be made up by C_1 from the basic power supply. The switches themselves also have series resistance, leading to further theoretical complications, but the net result is a typical overall output impedance of around 55Ω (100Ω max), provided that the capacitors are sufficiently large. For the natural oscillation frequency of the built-in oscillator (approximately 10kHz) values of 10µF are adequate.

The complete implementation of this function is achieved on a single CMOS chip, as shown in Figure 2.

The ICL7660 contains all the necessary conversion functions on-chip, except for the external pump and output reservoir capacitors and is made with a low-threshold CMOS technology using p- and n-channel transistors that turn on at 0.6V. The low power dissipation, simplicity, and small chip size of CMOS make it a near-ideal technology for this application.

The ICL7660 contains an RC oscillator, a series voltage regulator, a voltage-level translator, and a logic network (Figure 2). The logic network senses the voltage on the sources and drains of the two output n-channel transistors Q3 and Q4 and ensures that their substrates are always correctly biased.

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Power Efficiency

In the case where a capacitor is charged and discharged between two voltages, V_1 and V_2, the energy lost is defined by

$$E = \frac{C(V_1 2 - V_2 2)}{2}$$

where C is value of the capacitor in farads and E is the lost energy. If $V_1 = V_2$ is very small compared with V_1, the percentage energy loss is also small, given as:

$$\frac{100(V_1 2 - V_2 2)}{2(V_1 2)}$$

At the limit, when $V_2 = V_1$, no energy is lost. If the values of C_1 and C_2 in Figure 1 are made very large and their impedances at the switching frequency are very low compared with the load resistance, energy-conversion efficiencies approaching 100% can be obtained. Energy is lost only by a change of voltage during the transfer of charge into and out of a capacitor.

Detailed Description

Oscillator - Divider - Regulator

The ICL7660s oscillator (Figure 3) drives a conventional divide-by-2 counter whose principal function is to supply a 50% duty cycle output (at half the input frequency) to the voltage-level translator circuit. The conventional static counter requires a two-phase clock, and supplies an output signal and its complement.

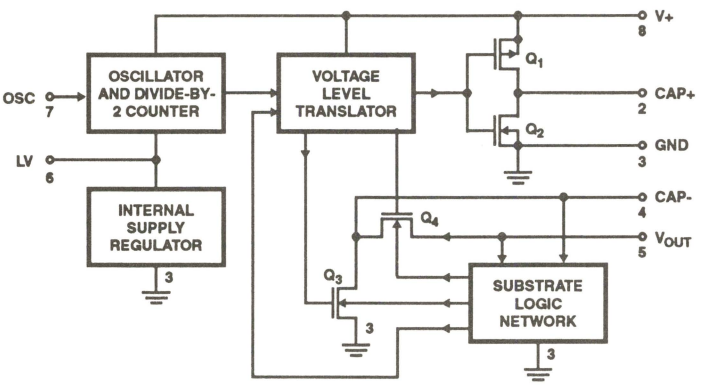


FIGURE 2. FUNCTIONAL DIAGRAM OF COMPLETE CHIP

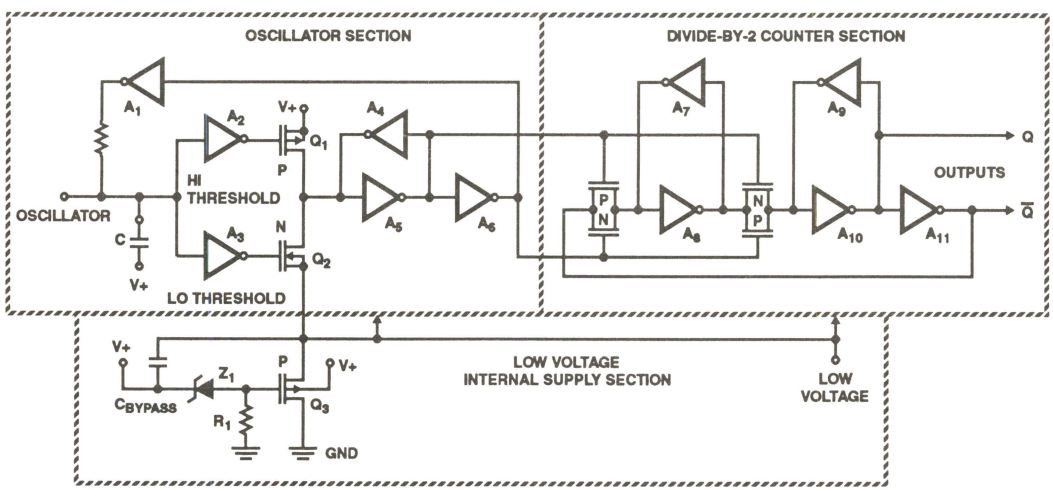


FIGURE 3. THE ICL7660s OSCILLATOR, DIVIDER AND INTERNAL REGULATOR

When the output of inverter A1 is switched high, capacitor C charges positively until inverter A2 (which has a high input-voltage trip point) switches its output low, to turn on transistor Q_1. Q_1 in turn forces the ratioed-inverter latch A4 - A5 to switch its output low. C then discharges negatively until inverter A3 (which has a low input-voltage trip point) switches its output high, turning on transistor Q_2. The output of Q_2 resets A_4 - A_5 and restarts the cycle.

Since the oscillator has a high input impedance of about 1MΩ, it may be driven from an external source such as a TTL gate or equivalent, or its frequency may be lowered by the addition of an external capacitor. At room temperature with a +5V supply and no external capacitor, the oscillator frequency will be 10kHz. The internal capacitance is about 10pF.

A series voltage regulator consisting of zener reference diode Z_1, resistor R_1, and source-follower p-channel transistor Q_3 provides a partially regulated supply for all the low voltage circuitry on the chip. The regulator can supply up to -5V (with respect to the positive power supply) for input supply voltages of about 6V and higher. Because of the modest size of Q3, the voltage regulator not only reduces power consumption at high supply voltages, but also limits the maximum current taken by the oscillator and the divide-by-2 counter.

The LV terminal can be used to short out the on-chip series regulator for better operation at low supply voltages. With the Low-Voltage terminal connected to ground, operation with an input supply voltage as low as 1V is possible. At higher voltages, however, it is mandatory that this terminal be open, in order to allow the internal voltage regulator to stop device latchup and avoid internal damage.

The Level-Translator and Output Switches

The level translators (Figure 4) provide switching signals to the gates of the four output transistors, Q_1 through Q_4, with amplitudes equal to the sum of the output and supply voltages. They also ensure that a break-before-make sequence takes place as switching alternates between charge and pump configurations.

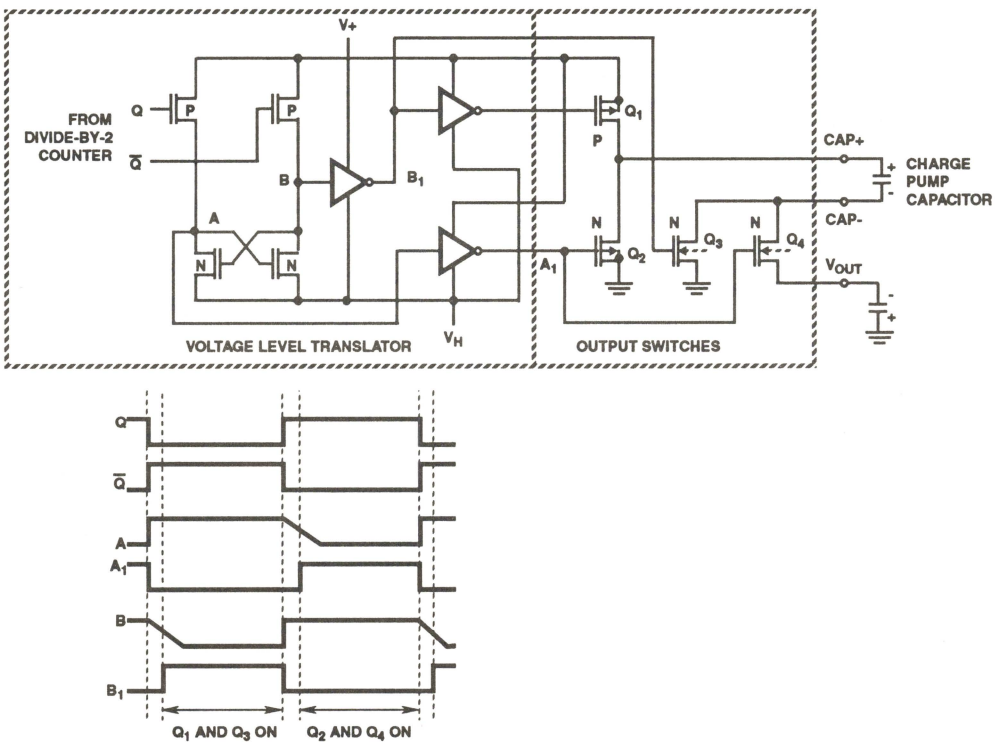


FIGURE 4. THE ICL7660s OUTPUT SWITCHES AND VOLTAGE LEVEL TRANSLATOR CIRCUIT

The Substrate Logic Network

The substrate logic network (Figure 5) is the most critical part of the converter chip. Its two main functions are to make sure that the substrates of Q_2 and Q_4 (Figure 4) are never forward-biased with respect to their sources and drains, and to establish the most negative voltage of any part of the circuit in either the charge or the pump cycles. This internal negative supply, V-, is used to power the level translators. It drives the gate of either Q_3 or Q_4 to a voltage similar to that of the sources to ensure transistor turn off.

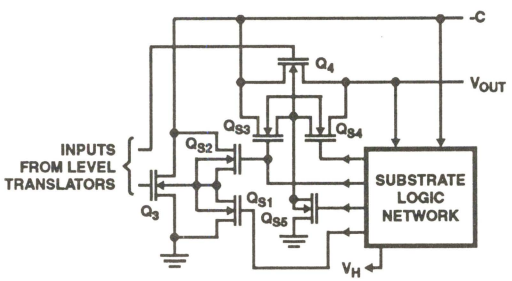


FIGURE 5. THE SUBSTRATE LOGIC NETWORK

Transistors Q_3 and Q_4 require special drive considerations, since the sources and drains are inverted on each device during pump and charge phases. Consider Q_3's operation, for example. During the charge phase, the most positive source/drain terminal is connected to the external charge-pump capacitor. This terminal is then, by definition, the drain, whereas the source which is more negative is connected to ground. To minimize Q_3's resistance, it is also desirable to connect its substrate to ground and not to the output voltage or to V_H, since reverse-biasing the substrate of an MOS transistor with respect to its source increases its threshold voltage, and therefore the ON resistance.

During the pumping phase, the external capacitor's negative terminal is shifted negatively by a voltage approximately equal to the supply voltage. In this case, the most negative source/drain terminal is connected to the negative side of the external capacitor (and thus becomes the source of Q_3), and its drain is connected to ground.

Similar source-drain reversals occur for Q_4 except that here conditions are different for output short-circuit operation than during normal operation. Sensing circuitry monitors the voltages on the external capacitors negative side and V_{OUT}, and compares them with ground. The substrate of Q_4 is then connected to the most negative of them. Figure 5 shows the substrate steering transistors for Q_3 and Q_4. The steering transistors (Q_{S1-5} are relatively small n-channel devices, and share Q_3 and Q_4's substrates).

SCR Latch Up

A CMOS device is inherently a four-layer, or silicon-controlled-rectifier (SCR), structure. This structure can be turned on through the forward biasing of the inherent pn junctions, and unless external current-limiting circuitry is used, latchup and resultant failure can occur.

The n-channel transistor source acts as the cathode of the SCR, and the p+ source of the p-channel transistor acts as the anode. Either n- or p-channel drains can act as the SCR gate. With about 2V or more across the anode and cathode, the SCR can have either a low-impedance (ON) or high impedance (OFF) state. For the ON state to occur, three things must happen: the product of the transistors' current gains, or betas, must be at least unity, a current greater than the holding current must be present, and a trigger pulse must be applied to either gate of the SCR. Trigger signals may be caused by static discharge on the gates or by connecting either gate to the power supplies before connecting Power-supply lines to other terminals of the SCR. Even extremely high rates of voltage change across any two or more SCR pn junctions can produce latchup.

Triggering a CMOS SCR causes it to present an extremely low impedance (1Ω to 100Ω) across the power supply. Unless the power supply is current-limited, the device latches up and is often destroyed, usually by the vaporization of one of the bonding wires.

Although ICL7660 output-section switching transients are mainly capacitive, they inject currents into the substrate. At high input supply voltages, these transients can forward-bias junctions associated with the p- well or the Q_4 substrate. This in turn may trigger the inherent SCR in Q_4 and the adjacent on-chip circuitry. The result is to rapidly discharge the reservoir capacitor.

After the reservoir capacitor is almost totally discharged and the current in the SCR has fallen below the holding value, the device again operates correctly, until the output voltage (reservoir capacitance voltage) reaches the same critical value, and the latchup phenomenon starts again. Since this effect occurs only during the start of the charge cycle, and not during the pump cycle, isolating the reservoir capacitor with an external diode at the V_{OUT} terminal prevents capacitor discharge. This is recommended when using the device at higher voltage and temperatures. Otherwise the substrate logic network prevents SCR triggering, which is therefore not a problem for most operating conditions.

Basic Application

The applications of the ICL7660 are remarkably varied, especially considering the rather narrow nature of the basic device function.

The basic circuit is shown in Figure 6, and the output characteristics for 5V inversion in Figure 7. For light loads, the output voltage follows the input very precisely, while for heavier loads, the output can be viewed as having perfect inversion, plus an output resistance of about 55Ω.

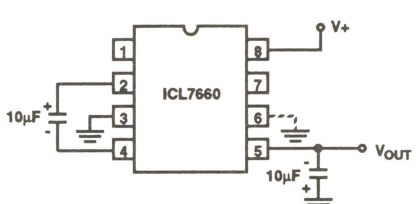


FIGURE 6. SIMPLE NEGATIVE CONVERTER

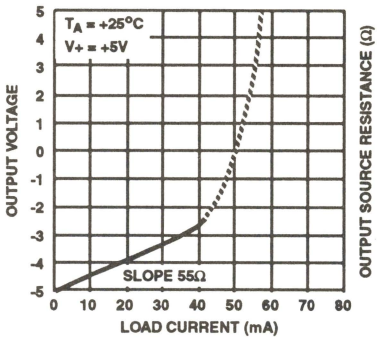


FIGURE 7. OUTPUT CHARACTERISTICS

Thus at 18mA load, the output voltage drops about 1V below the input. Beyond around 40mA, the voltage drop becomes very nonlinear, and the circuit self-limits, thereby protecting itself against excessive power dissipation. The output ripple is dependant primarily upon the output capacitor, since this must hold up the load during half the cycle time (or one oscillator period). In the steady-state case, this ripple is made up during the other half cycle time, and enough pump capacitance should be used to ensure that this is done monotonically. The recommended values ensure this for the internal oscillator frequency.

For operation at low voltages, the output impedance begins to rise rather rapidly, as a result of reduced turn-on voltage on the MOSFET switches (Figure 8). This effect can be reduced by bypassing the internal regulator, tying LV to Ground, as shown in Figure 9. This must not be done, however, if the incoming supply an exceed 8V under any circumstances, a the Internal logic oscillator and divider stages will he damaged. Note also the use of a series diode (Dx) at higher voltage and temperature, to protect the device against SCR action.

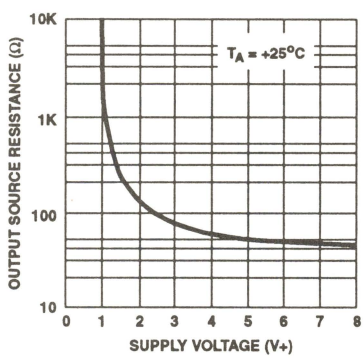


FIGURE 8. OUTPUT RESISTANCE

Figure 9 also shows an external oscillator capacitor. This can be used to reduce the oscillator frequency, giving a slight improvement in efficiency; see Figure 10.

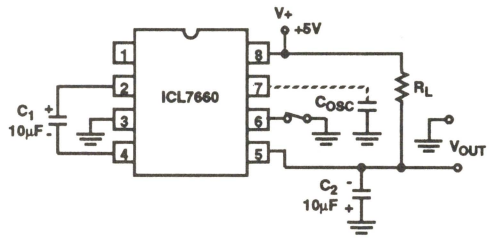


FIGURE 9. VARIATIONS OF BASIC CIRCUIT

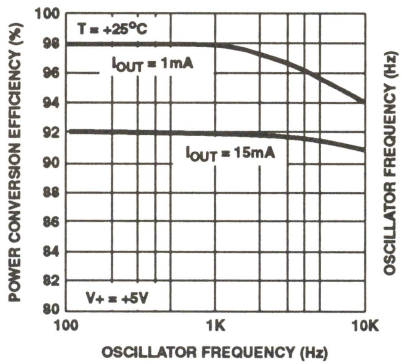


FIGURE 10. EFFICIENCY CHANGE WITH OSCILLATOR FREQUENCY

The dependence of the frequency on this external capacitance is shown in Figure 11. This can also be done to move the frequency away from a band of undue sensitivity to EMI in a system. However the output ripple will be increased, and the output impedance also unless the pump and storage capacitors are correspondingly increased.

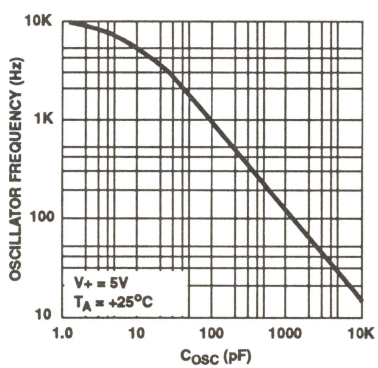


FIGURE 11. FREQUENCY VARIATION WITH OSCILLATOR CAPACITANCE

Synchronization to an external clock can be readily achieved, as shown in Figure 12. A TTL device can be used with the addition of a pull-up resistor (10kΩ to V+ is suitable), as can any input swinging rail-to-rail on the positive supply. The series resistor prevents problems with overdrive on the internal logic. Output transitions occur on the positive edge of the external input.

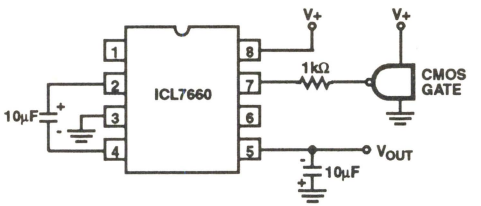


FIGURE 12. EXTERNAL CLOCKING

Wider (Parallel Connections)

For applications where the voltage drop due to load current is excessive, several ICL7660s can be paralleled. Normally this cannot be done efficiently with power supply circuits, since each one has a different idea of where the "ideal" output voltage would be and they usually end up fighting each other. However, here they see equal input voltages, and the virtually perfect inversion assures that each one does have the same idea of where the output should be so load sharing is assured. Each device must have a separate pump capacitor, since the oscillators cannot be synchronized except with an external drive, and even then the -2 will be in a random condition. The connections are shown in Figure 13. Naturally the output capacitor is common to each device. Running independently, the ripple content will include components at the difference frequency as well as the individual pumping frequencies. If this is undesirable, a single exclusive NOR gate can be used to put two ICL7660s into antiphase by comparing the outputs on pin 2, and clocking one to maintain near synchronization with the basic oscillator of the other, as shown in Figure 14.

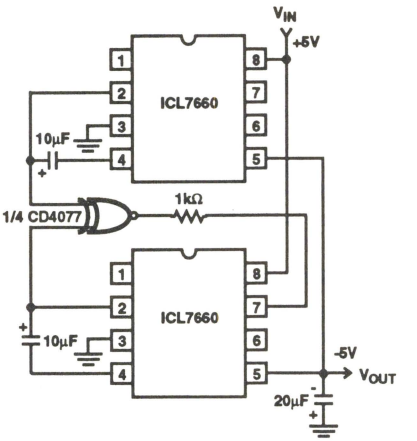


FIGURE 14. SYNCHRONIZING TWO ICL7660s

The concept can be extended to drive four devices in four separate phases, using a single extra logic-gate package, as shown in Figure 15. The duty cycle of the oscillator is reasonably close to 50%, so driving two pairs, each in the configuration of Figure 14, from opposite phases of the oscillator gives four separately-timed pumps per cycle. This circuit will give about 75mA output before the voltage drops by 1V, or an output impedance of under 14Ω. The four phase operation minimizes the ripple, while ensuring very even load sharing. For even more parallel synchronous device, a Johnson counter using Q and Q outputs should be considered.

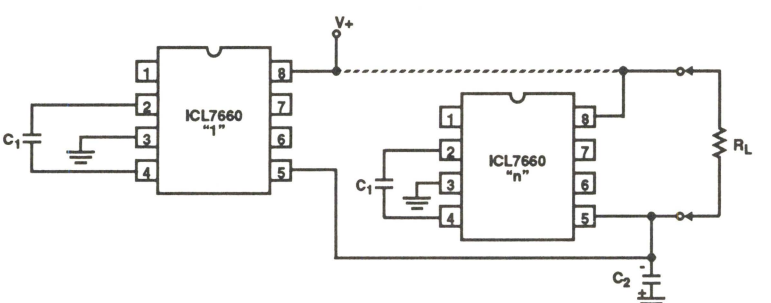


FIGURE 13. PARALLELING DEVICES

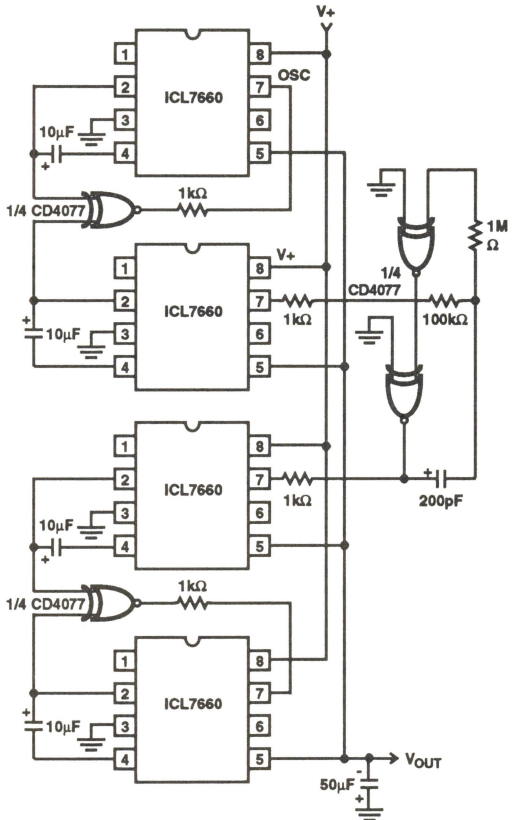


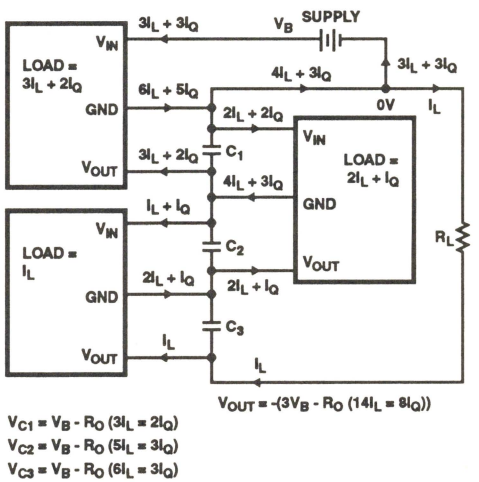
FIGURE 15. SYNCHRONIZING A QUAD

Deeper (Series Connection)

It is also possible to connect ICL7660s in series, cascading them to generate higher negative voltages. The basic connections are shown in Figure 16.

This technique can be extended to several multiplication levels. However, the basic limitations of this technique must be recognized. In line with the Laws of Thermodynamics, the input current required for each stage is twice the load current on that stage, plus the quiescent current required to operate that stage.

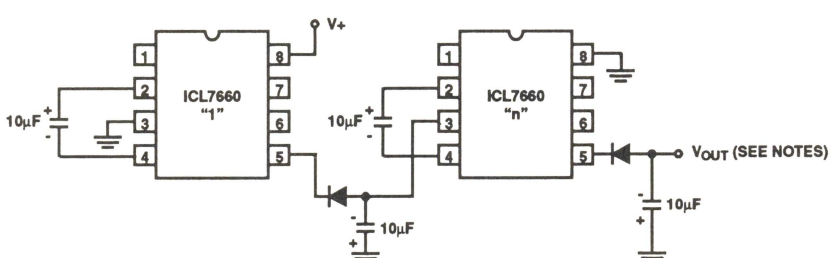
Thus the load current is rapidly multiplied down the chain, as shown in Figure 17. Note also that the quiescent current increases the load current on each stage, though not as fast as the ultimate load itself.



$V_{C1} = V_B - R_O (3I_L = 2I_Q)$
$V_{C2} = V_B - R_O (5I_L = 3I_Q)$
$V_{C3} = V_B - R_O (6I_L = 3I_Q)$

FIGURE 17. CURRENT FLOW FOR CASCADED DEVICES

Furthermore, the loss in voltage in early stages due to series resistance is multiplied through all subsequent stages. Thus the effective output impedance mounts rapidly with the number of stages. (See Table 1) This effect can be reduced by paralleling devices in the lowest stages (see above.) If the weighting corresponds to the square of the position, the effective resistance to load current goes up only linearly with



NOTES:

1. $V_{OUT} = -n+$ for $1.5V \le V+ \le 6.5V$.
2. $V_{OUT} = -n\ (V+ - V_{FOX})$ for $6.5V \le V+ \le 10.0V$.

FIGURE 16. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

the number of stages, but the cost quickly becomes prohibitive. Nevertheless, for light loads and moderate multiplication, useful performance can be achieved.

TABLE 1

# STAGES	RESISTANCE	MULTIPLIERS
n	R_O(L)	R_O(Q)
1	1	0
2	5	2
3	14	8
4	30	20
5	55	40

A variation of this circuit, another form of series circuit, is shown in Figure 18. This circuit can be used effectively to generate -15V from +5V in light load applications using only two devices. The output impedance corresponds roughly to n = 2 in Table 1, much better than if the previous circuit were used with n = 3. In general, geometric increases, as in Figure 18, are better until the voltage limit is reached, at which time arithmetic cascading as in Figure 16 must be utilized.

Upside Down (Positive Multiplication)

The ICL7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 19. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D_1) On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) - ($2V_F$) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 5V and an output current of 10mA it will be approximately 60Ω.

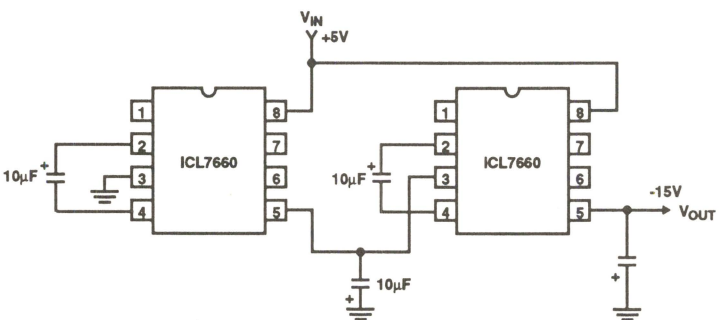


FIGURE 18. GETTING -15V FROM +5V

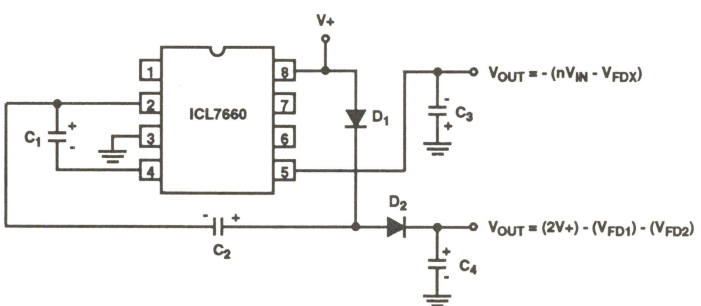


FIGURE 19. COMBINED NEGATIVE CONVERTER AND POSITIVE MULTIPLIER

Divide and Conquer

The ICL7660 can be used to split a supply in half, as shown in Figure 20.

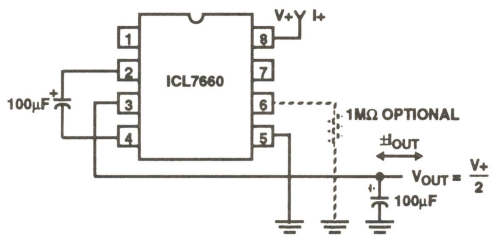


FIGURE 20. EFFICIENT SUPPLY SPLITTING

Here the "basic" output connection and the "basic" negative supply input are exchanged and the output voltage thus becomes the midpoint. Start-up can be a problem, and although careful capacitance and load balancing may frequently be adequate, a simple resistor to LV will always work. The circuit is useful for series-fed line systems, where a heavy local load at low voltage can be converted to a lighter current, at high voltage. Other useful applications are in driving low voltage (e.g. +7.5V) circuits from 15V supplies , or low voltage logic from 9V or 12V batteries. The output impedance is extremely low; all parts of the circuit cooperate in sharing the current, and so act in parallel.

For other division ratios, the series configurations of Figure 16 can be driven backwards, to generate V_{IN}/n, or even $m/n(V_{IN})$, for small values of m and n. Again, care must be taken to ensure start up for each device.

One interesting combination of several preceding circuits is shown in Figure 21, where a +15V supply is converted, via +7.5V and - 7.5V, to -1 5V using three ICL7660s. The output impedance of this circuit is about 250Ω.

For cases where the output impedance of an ICL7660 circuit is too high, obviously some form of output regulation can be used. However in most cases adequate regulation can be achieved at high efficiency by pre-regulating the input. A suitable circuit is shown in Figure 22, using the ICL7611 low power CMOS op amp. Because of the large source-current capability of this op amp, even on its lowest bias current setting, very efficient operation is possible. An ICL8069 bandgap device is used as the reference generator for the regulator. The output impedance can be reduced to 4Ω, while maintaining a current capability of well over 10mA. In designing circuits of this type, it is important to remember that there is a switching delay averaging one oscillator cycle between the output of the op amp and the actual output voltage. This can have substantial repercussions on the transient response if the time-constants in the circuit are not

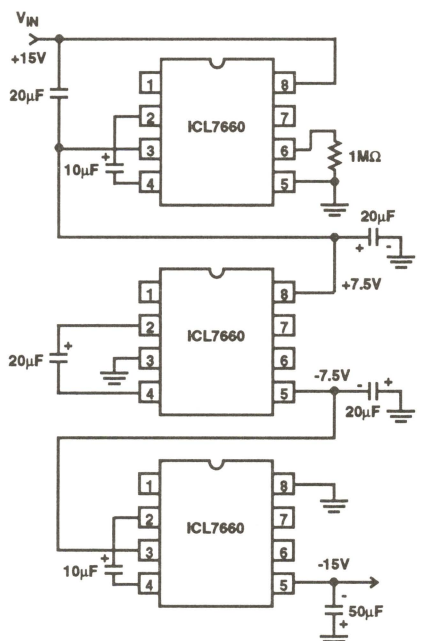


FIGURE 21. +15V TO -15V IN THREE EASY STAGES

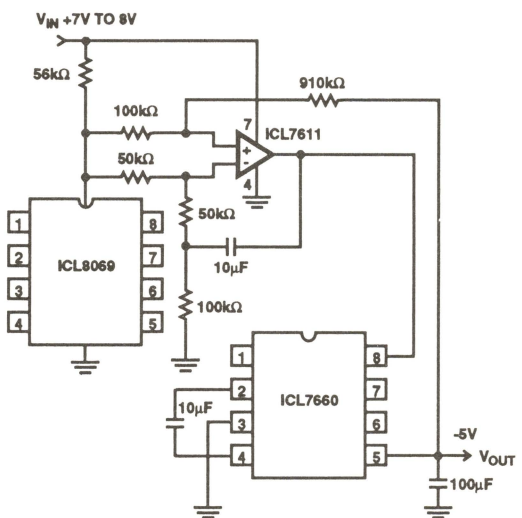


FIGURE 22. REGULATED OUTPUT INVERTER

adequate. If multiple voltage converters are used, synchronization schemes such as those of Figures 14 and 15 are probably advisable.

Messing About

The applications shown so far have corresponded to the use of the ICL7660 as a sort of equivalent of single turns on a power transformer, with paralleled turns to get more current, series turns for more voltage, etc. However, there are some other possibilities. By looking again at the block diagram (Figure 2), it is evident that the device could be used as a 50% duty cycle high power clock driver, using either the internal oscillator or an external signal, as in Figure 23. An antiphase clock can also be derived from the circuit, as shown, but the pull-up on this output, being an N-channel switch only, does not have as good a voltage swing. It is adequate for TIC level operation, but for CMOS clocking may require an external pull-up resistor or transistor.

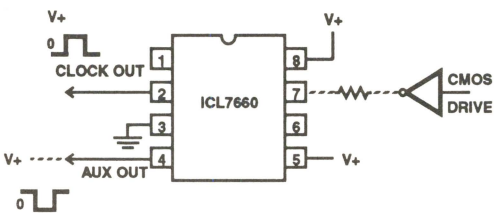


FIGURE 23. HIGH POWER CLOCK DRIVE

Another interesting class of applications comes from the capability to synchronously detect the output of an AC driven transducer, as shown in Figure 24. (This could be viewed as a signal transformer application.) Although the circuit shown utilizes a linear transformer type of transducer, any similar device may be used. The output voltage, which is correctly phased and of either polarity, may be fed into an A/D converter for display or microprocessor interface as desired.

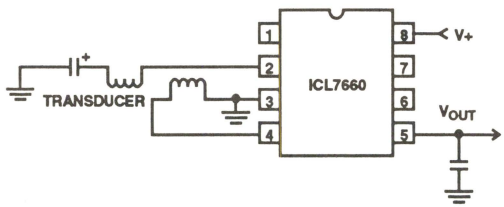


FIGURE 24. TRANSDUCER DRIVER AND DETECTOR

Harris Semiconductor

APPNOTE

No. AN5766.1 April 1994

Harris Intelligent Power

APPLICATION OF THE CA3020 AND CA3020A MULTIPURPOSE WIDE-BAND POWER AMPLIFIERS

Authors: W.M. Austin and H.M. Kleinman

The discussions in this Note are applicable to both integrated circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has a lower voltage rating and must not be used in applications which require voltages on the output transistors greater than 18V. The integrated circuit protects the output transistor by limiting the drive to the output stages. The drive limited current capability of the CA3020 is less than that of the CA3020A, but peak currents in excess of 150mA are an assured characteristic of the CA3020.

The CA3020 and CA3020A integrated circuits are multipurpose, multifunction power amplifiers designed for use as power output amplifiers and driver stages in portable and fixed communications equipment and in AC servo control systems. The flexibility of these circuits and the high frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60dB or more are available with a 3dB bandwidth of 8MHz.

The discussions in this Note are applicable to both integrated circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has more limited voltage and current handling capability and must not be used in applications which require voltage swings on the output transistors greater than 18V or peak currents in excess of 150mA.

The CA3020 and CA3020A are designed to operate from a single supply voltage which may be as low as +3V. The maximum supply voltage is dictated by the type of circuit operation. For transformer loaded class B amplifier service, the maximum supply voltages are +9V and +12V for the CA3020 and the CA3020A, respectively. When operated as a class B amplifier, either circuit can deliver a typical output of 150mW from a +3V supply or 400mW from a +6V supply. At +9V, the idling dissipation can be as low as 190mW, and either circuit can deliver an output of 550mW. An output of slightly more than 1W is available from the CA3020A when a +12V supply is used.

Circuit Description and Operation

Figure 1 shows the schematic diagram of the CA3020 and CA3020A, and indicates the five functional block into which the circuit can be divided for understanding of its operation. Figure 2 shows the relationship of these blocks in block diagram form.

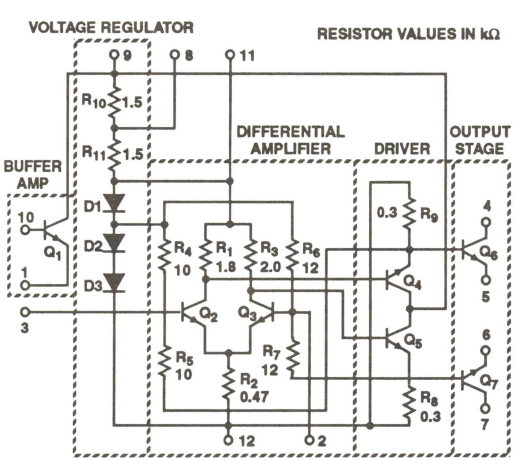


FIGURE 1. SCHEMATIC DIAGRAM OF CA3020 AND CA3020A INTEGRATED CIRCUIT AMPLIFIERS

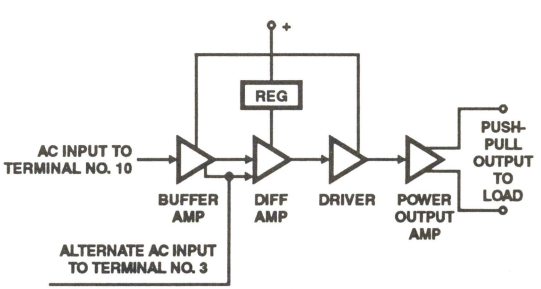


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM OF THE CA3020 AND CA3020A

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A key to the operation of the circuit is the voltage regulator consisting of diodes D_1, D_2, and D_3 and resistors R_{10} and R_{11}. The three diodes are designed to provide accurately controlled voltages to the differential amplifier so that the proper idling current for class B operation is established in the output stage. The characteristics of these monolithic diodes closely match those of the driver and output stages so that proper bias voltages are applied over the entire military temperature range of -55°C to +125°C. The close thermal coupling of the circuit assures against thermal runaway within the prescribed temperature and dissipation ratings of the devices.

The differential amplifier operates in a class A mode to supply the power gain and phase inversion required for the push-pull class B driver and output stages. In normal operation, an AC signal is capacitively coupled to terminal 3, and terminal 2 is AC grounded through a suitable capacitor. When the signal becomes positive, transistor Q_2 is turned on and its collector voltage changes in a negative direction. The same current flows out of the emitter of Q_2 and tends to flow to ground through resistor R_2. However, the impedance of R_2 is high compared to the input impedance of the emitter of Q_8, and an alternate path is available to ground through the emitter-to-base junction of transistor Q_3 and then through the bypass capacitor from terminal 2 to ground. Because this path has a much lower impedance than R_2, most of the current takes this alternate route. The signal current flowing into the emitter of Q_3 reduces the magnitude of that current and, because the collector current is nearly equal to the emitter current, the collector current in Q_3 drops and the collector voltage rises. Thus, a positive signal on terminal 3 causes a negative AC voltage on the collector of transistor Q_2 and a positive AC voltage on transistor Q_3, and provides the out-of-phase signals required to drive the succeeding stages. It should be noted that the differential amplifier is not balanced; resistor R_3 is ten percent greater than R_1. This unbalance is deliberately introduced to compensate for the fact that all of the current in the emitter of Q_2 does not flow into Q_3. Use of a larger load resistor for transistor Q_3 compensates for the lower current so that the voltage swings on the two collectors have nearly the same magnitude.

The driver stages (transistors Q_4 and Q_5) are emitter follower amplifiers which shift the voltage level between the collectors of the differential-amplifier transistors and the bases of the output transistors and provide the drive current required by the output transistors.

The power transistors (Q_8 and Q_7) are large, high current devices capable of delivering peak currents greater than 0.25A. The emitters are made available to facilitate various modes of operation or to permit the inclusion of emitter resistors for more complete stabilization of the idling current of the amplifier. Inclusion of such resistors also reduces distortion by introducing negative feedback, but reduces the power-output capability by limiting the available drive.

Inclusion of emitter resistors between terminals 5 and 6 and ground also enhances the effectiveness of the internal DC feedback supplied to the bases of transistors Q_2 and Q_3 through resistors R_5 and R_7. Any increase in the idling current in either output transistor is reflected as an increased voltage at its base. This change is coupled to the input through the appropriate resistor to correct for the increased current.

A later section of this Note describes how stable class A operation of the output stages may be obtained.

Operating Characteristics

Supply Voltages and Derating

The CA3020 operates with any supply voltage between +3V and +9V. The CA3020A can also be operated with supply voltages up to +12V with inductive loads or +25V with resistive loads. Figure 3 shows the permissible dissipation rating of the CA3020 and CA3020A as a function of case and ambient temperatures. At supply voltages from +6V to +12V, a heat sink may be required for maximum power output capability. The worst case dissipation $P_{D\,MAX}$ as a function of power output can be calculated as follows:

$$P_{D\,MAX} = (V_{CC1}\,I_{CC1} + V_{CC2}\,I_{CC2}) + (V_{CC2}^2/R_{CC})$$

where V_{CC1} and V_{CC2} are the supply voltages to the differential amplifier and output amplifier stages, respectively; I_{CC1} and I_{CC2} are the corresponding idling currents; and R_{CC} is the collector-to-collector load resistance of the output transformer. This equation is preferred to the conventional formula for the dissipation of a class B output transistor (i.e., 0.84 times the maximum power output) because the $P_{D\,MAX}$ equation accounts for the device standby power and device variability.

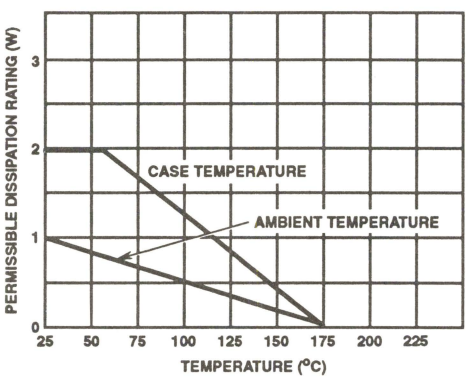
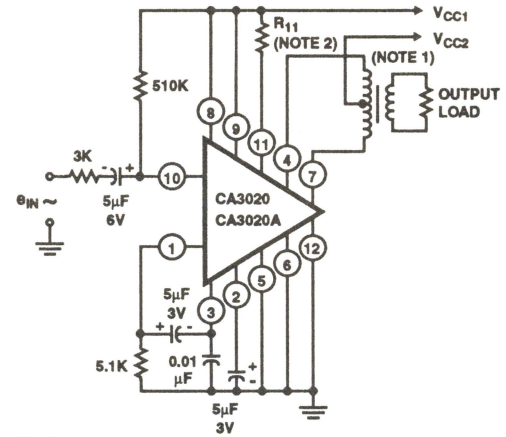


FIGURE 3. DISSIPATION RATING OF THE CA3020 AND CA3020A AS A FUNCTION OF CASE AND AMBIENT TEMPERATURES

Basic Class B Amplifier

Figure 4 shows a typical audio amplifier circuit in which the CA3020 or CA3020A can provide a power output of 0.5W or 1W, respectively. Table 1 shows performance data for both types in this amplifier. The circuit can be used at all voltage and power output levels applicable to the CA3020 and CA3020A.



NOTES:

1. Better coil and transformer DF108A, Thordarson TR-192, or equivalent.
2. See text and tables.

FIGURE 4. BASIC CLASS B AUDIO AMPLIFIER CIRCUIT USING THE CA3020 OR CA3020A.

TABLE 1. TYPICAL PERFORMANCE OF CA3020 AND CA3020A IN CIRCUIT OF FIGURE 4 (NOTE)

CHARACTERISTIC	CA3020	CA3020A	UNITS
Power Supply			
V_{CC1}	9	9	V
V_{CC2}	9	12	V
Zero-Signal Idling Current			
I_{CC1}	15	15	mA
I_{CC2}	24	24	mA
Maximum Signal Current			
I_{CC1}	16	16.6	mA
I_{CC2}	125	140	mA
Maximum Power Output at 10% THD	550	1000	mW
Sensitivity	35	45	mV
Power Gain	75	75	dB
Input Resistance	55	55	kΩ
Efficiency	45	55	%
Signal-to-Noise Ratio	70	66	dB
% Total Harmonic Distortion at 150mW	3.1	3.3	%
Test Signal	1000Hz/600Ω Generator		
Equivalent Collector-to-Collector Load	130	200	Ω
Idling Current Adjust Resistor (R_{11})	1000	1000	Ω

NOTE: Integrated circuit mounted on a beat sink, Wakefield 209 Alum. or equivalent.

The emitter-follower stage at the input of the amplifier in Figure 4 is used as a buffer amplifier to provide a high input impedance. Although many variations of biasing may be applied to this stage, the method shown is efficient and economical. The output of the buffer stage is applied to terminal 3 of the differential amplifier for proper balance of the push-pull drive to the output stages. Terminals 2 and 3 must be bypassed for approximately 1000Ω at the desired low-frequency roll-off point.

At low power levels, the crossover distortion of the class B amplifier can be high if the idling current is low. For low crossover distortion, the idling current should be approximately 12mA to 24mA, depending on the efficiency, idling dissipation, and distortion requirements of the particular application. The idling current may be increased by connection of a jumper between terminals 8 and 9. If higher levels of operating idling current are desired, a resistor (R_{11}) may be used to increase the regulated voltage at terminal 11 by a slight amount with additional current injection from the power supply V_{CC1}.

In some applications, it may be desirable to use the input transistor Q_1 of the CA3020 or CA3020A for other purposes than the basic buffer amplifier shown in Figure 4. In such cases, the input AC signal can be applied directly to terminal 3.

The extended frequency range of the CA3020 and CA3020A requires that a high-frequency AC bypass capacitor be used at the input terminal 3. Otherwise, oscillation could occur at the stray resonant frequencies of the external components, particularly those of the transformers. Lead inductance may be sufficient to cause oscillation if long power-supply leads are not properly AC bypassed at the CA3020 or CA3020A common ground point. Even the bypassing shown may be insufficient unless good high-frequency construction practices are followed.

Figure 5 shows typical power output of the CA3020A at supply voltages of +3V, +6V, +9V, and +12V, and of the CA3020 at +6V and +9V, as measured in the basic class B amplifier circuit of Figure 4. The CA3020A has higher power output for all voltage supply conditions because of its higher peak output current capability.

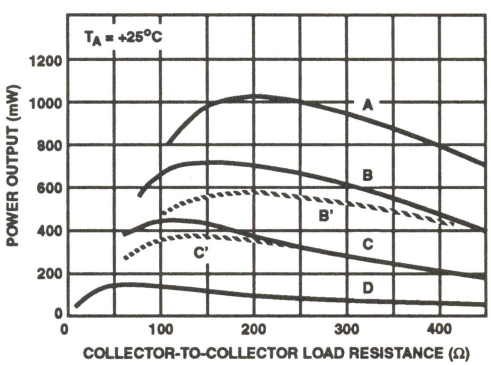


FIGURE 5. POWER OUTPUT OF THE CA3020 AND CA3020A AS A FUNCTION OF COLLECTOR-TO-COLLECTOR LOAD RESISTANCE R_{CC}

TABLE FOR FIGURE 5 CURVES

CURVE		IDLING CURRENT (mA)		POWER SUPPLY VOLTAGE (V)		R_{11}
CA3020	CA3020A	I_{CC1}	I_{CC2}	V_{CC1}	V_{CC2}	(Ω)
-	A	9	10	9	12	00
B'	B	9	10	9	9	00
C'	C	7	6	6	6	00
-	D	8	8	3	3	220

Figure 6 shows total harmonic distortion (THD) as a function of power output for each of the voltage conditions shown in Figure 5. The values of the collector-to-collector load resistance (R_{CC}) and the idling-current adjust resistor (R_{11}) shown in the figure are given merely as a fixed reference; they are not necessarily optimum values. Higher idling-current drain may be desired for low crossover distortion, or a higher value of R_{CC} may be used for better sensitivity with less power-output capability. Because the maximum power output occurs at the same conditions of peak-current limitations, the sensitivities at maximum power output for the curves of Figures 5 and 6 are approximately the same. Increasing the idling current drain by reducing the value of the resistor R_{11} also improves the sensitivity.

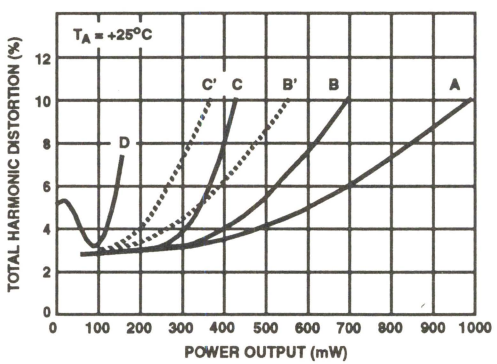


FIGURE 6. TOTAL HARMONIC DISTORTION OF THE CA3020 OR CA3020A AS A FUNCTION OF POWER OUTPUT

TABLE FOR FIGURE 6 CURVES

CURVE		IDLING CURRENT (mA)		POWER SUPPLY VOLTAGE (V)		R_{CC} (Ω)	R_{11} (Ω)
CA3020	CA3020A						
-	A	15	24	9	12	200	1000
B'	B	15	24	9	9	150	1000
C'	C	12	14	6	6	100	1000
-	D	9	9	3	3	50	220

Figure 7 illustrates the improvement in crossover distortion at low power levels. Distortion at 100mW is shown as a function of idling current I_{CC2} (output stages only). There is a small improvement in total harmonic distortion for a large increase in idling current as the current level exceeds 15mA.

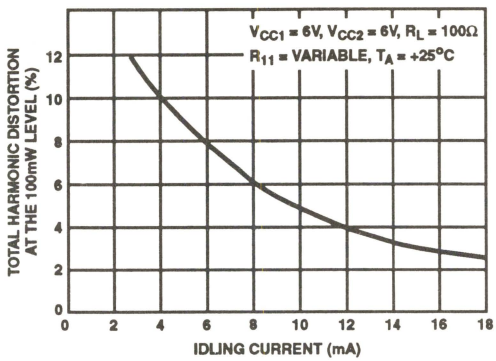


FIGURE 7. TOTAL HARMONIC DISTORTION AS A FUNCTION OF I_{CC2} IDLING CURRENT FOR A SUPPLY VOLTAGE OF 6V AND AN OUTPUT OF 100mW

Applications

Audio Amplifiers

The circuit shown in Figure 4 may be used as a highly efficient class B audio power output circuit in such applications as communications systems, AM or FM radios, tape recorders, intercoms, and linear mixers. Figure 8 shows a modification of this circuit which may be used as a transformerless audio amplifier in any of these applications or in other portable instruments. The features of this circuit are a power output capability of 310mW for an input of 45mV, and a high input impedance of 50,000Ω. The idling-current drain of the circuit is 24mA. The curves of Figure 5 may be used to determine the value of the center-tapped resistive load required for a specified power output level (the indicated load resistance is divided by two).

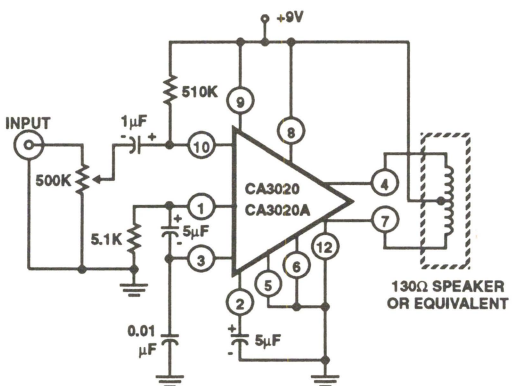


FIGURE 8. 310mW AUDIO AMPLIFIER WITHOUT TRANSFORMERS

The CA3020 or CA3020A provides several advantages when used as a sound output stage or as a preamplifier driver in communications equipment because each type is a compact and low power drain circuit. The squelching requirement in such applications is simple and economical.

Figure 9 shows a practical method of providing squelch to the CA3020 or CA3020A. When the squelch switching transistor Q_S is in the "on" state, the CA3020 or CA3020A is "off" and draws only fractional idling dissipation. The only current that flows is that of the buffer-amplifier transistor Q_1 in the integrated circuit and the saturating current drain of Q_S. For a circuit similar to that of Figure 8, the squelched condition requires an idling current of approximately 7mA, as compared to a normal idling-current drain of 24mA.

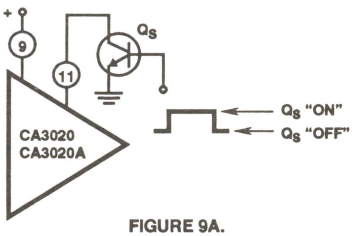


FIGURE 9A.

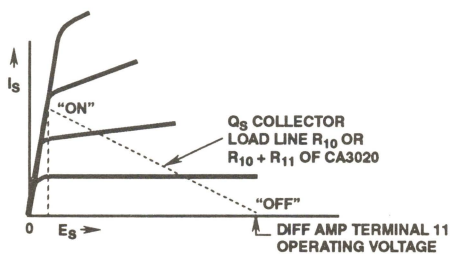
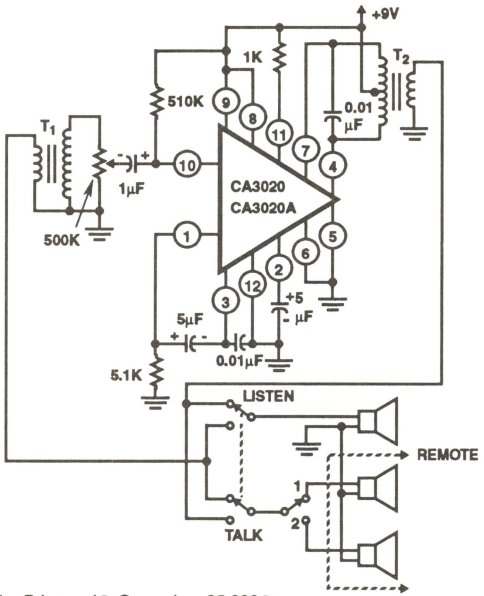


FIGURE 9B.

FIGURE 9. METHOD OF APPLYING SQUELCH TO THE CA3020 OR CA3020A TO SAVE IDLING DISSIPATION

In applications requiring high gain and impedance matching, the CA3020 or CA3020A can be adapted for use without complex circuit modifications. Detectors having low signal outputs or high impedances can be easily matched to the input of the CA3020 or CA3020A buffer amplifier. The typical integrated circuit input impedance of 55kΩ may be too low for crystal output devices, but the sensitivity may be sacrificed to impedance match at the input while still providing adequate drive to the CA3020 or CA3020A. Both types may be used in tape recorders as high-gain amplifiers, bias oscillators, or record and playback amplifiers. The availability of two input terminals permits the use of the CA3020 or CA3020A as a linear mixer, and thus adds to its flexibility in systems that require adaptation to multiple functions, such as communications equipment and tape recorders.

Figure 10 illustrates the use of the audio amplifier shown in Figure 4 in an intercom in which a listen/talk position switch controls two or more remote positions. Only the speakers, the switch, and the input transformer are added to the basic audio amplifier circuit. A suitable power supply for the intercom could be a 9V battery used intermittently rather than continuously.



T1: Primary 4Ω, Secondary 25,000Ω; Stancor A4744 or equivalent.

T2: Better coil and transformer DF1084, Thordarson TR-192, or equivalent

Speakers: 4Ω

FIGURE 10. INTERCOM USING CA3020 OR CA3020A

Wide-Band Amplifiers

A major general-purpose application of the CA3020 and CA3020A is to provide high gain and wide-band amplification. The CA3020 and CA3020A have typically flat gain-bandwidth response to 8MHz. Although the circuits are normally biased for class B operation, only the output stages operate in this mode. If proper DC bias conditions are applied, the output stages may be operated as linear class A amplifiers.

Figure 11 shows the recommended method for achieving an economical and stable class A bias. The differential amplifier portion of the CA3020A is placed at a potential above ground equal to the base-emitter voltage V_{BE} of the integrated circuit transistors (0.5V to 0.7V). In this condition, the output stages have an emitter-current bias approximately equal to the base-to-emitter voltage divided by the emitter-to-ground resistance. The circuit in Figure 11 is a wide-band video amplifier that provides a gain of 38dB at each of the push-pull outputs, or 44dB in a balanced output connection. The 3dB bandwidth of the circuit is 30Hz to 8MHz. Higher gain-bandwidth performance can be achieved if the diode-to-ground voltage drop at terminal 12 is reduced. The lower voltage drop permits the use of a higher ratio of output-stage collector-to-emitter resistors without departure from the desired portion of the class A load line. It is important to note that the temperature coefficient of the terminal 12-to-ground reference element should be sufficiently low to prevent a large change in the current of the output stages.

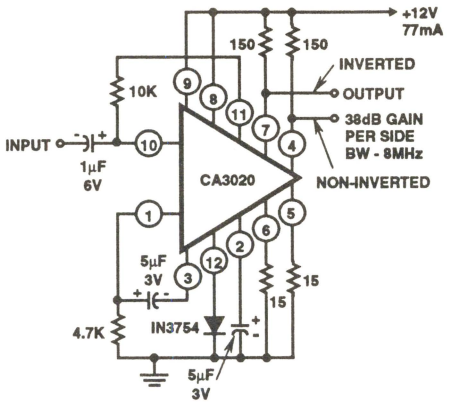


FIGURE 11. WIDE-BAND VIDEO AMPLIFIER ILLUSTRATING ECONOMICAL AND STABLE CLASS A BIAS OF CA3020A

The same method for achieving class A bias is used in the large signal swing output amplifier shown in Figure 12.

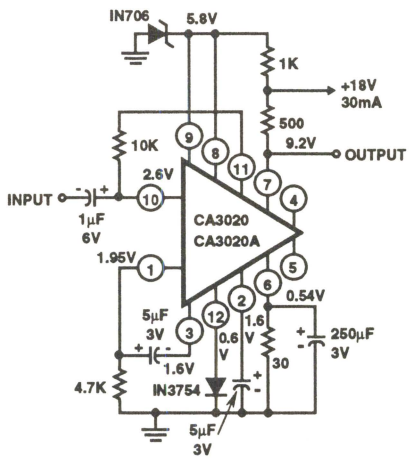


FIGURE 12. LARGE SIGNAL SWING OUTPUT AMPLIFIER USING CA3020 OR CA3020A

Either the CA3020 or the CA3020A may be used in this circuit with power supplies below +18V; the CA3020A can also be used with B+ voltages up to 25V with non-inductive loads. The circuit of Figure 12 provides a gain of 60dB and a bandwidth of 3.2MHz if the output transistor Q_7 has a bypassed emitter resistor. With an unbypassed output emitter resistor, the gain is 40dB and the bandwidth is 8MHz. The output stage can deliver a $5V_{RMS}$ signal when a supply of +18V is used. For better performance in this type of circuit, the input signal is coupled from the buffer amplifier Q_1 to the input terminal 3 of the differential amplifier. This arrangement provides higher gain because the collector resistor of the differential-amplifier transistor Q_3 is larger than that of Q_2. (This difference results from a requirement of differential drive balance that is not used in this circuit.) In addition, the terminals of the unused output transistor Q_6 help to form an isolating shield between the input at terminal 3 and the output at terminal 7. This cascade of amplifiers has a single phase inversion at the output for much better stability than could be achieved if terminal 4 were used as the output and terminal 3 as the input.

Figure 13 illustrates the use of the CA3020 or CA3020A as a class A linear amplifier. This circuit features a very low output impedance and may be used as a line driver amplifier for wide-band applications up to 8MHz. The circuit requires a 0.12V peak-to-peak input for a single ended output of 1V or a balanced peak-to-peak output of 2V from a 3Ω output impedance at each emitter. The input impedance is specified as 7800Ω, but is primarily a function of the external 10,000Ω resistor that provides bias to Q_1 from the regulating terminal 11.

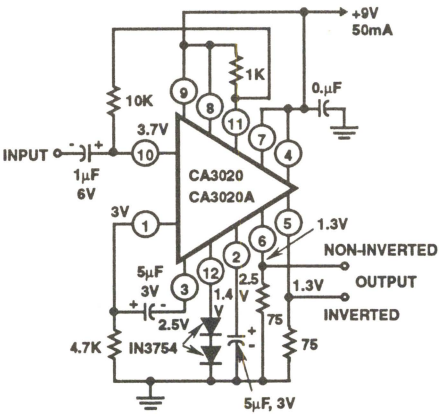


FIGURE 13. CLASS A LINEAR AMPLIFIER USING CA3020 OR CA3020A

Figure 14 illustrates the practical use of the CA3020 or CA3020A as a tuned amplifier. This circuit uses DC biasing similar to that shown previously, and has a gain of 70dB at a frequency of 160kHz. The CA3020 or CA3020A can be used as a tuned RF amplifier or oscillator at frequencies well beyond the 8MHz bandwidth of the basic circuit.

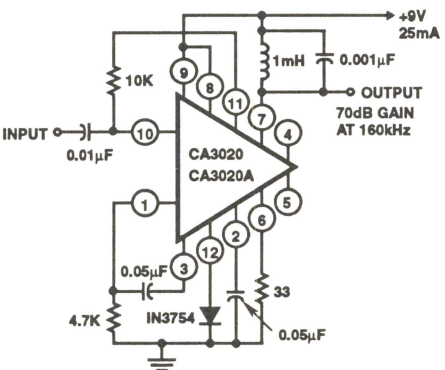


FIGURE 14. 160KHz TUNED AMPLIFIER USING THE CA3020 OR CA3020A

Driver Amplifiers

The high power-pin and power-output capabilities of the CA3020 and CA3020A make these integrated circuits highly suitable for use as drivers for higher power stages. In most applications, the full power output capability of the circuit is not required, and large emitter resistors may be used in the output stage to reduce distortion. The CA3020 and CA3020A can drive any transformer coupled load within their respective ratings. Several examples of typical applications are given below.

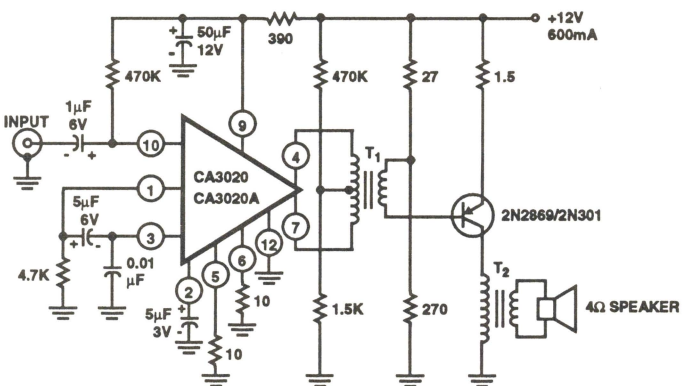
Figure 15 illustrates the use of the CA3020 or CA3020A to drive a germanium power output transistor to a 2.5W level. Because the integrated circuit is required to deliver a maximum power output of less than 50mW, an unbypassed emitter resistor can be used in the output stage to reduce distortion. Sensitivity for an output of 2.5W is 3mV; this figure can be improved at a slight increase in distortion by reduction of the 4.7Ω resistors between terminals 5 and 6 and ground.

Because so little of the power output capability of the CA3020 or CA3020A is used, higher power class B stages can easily he accommodated by selection of suitable output transistors and appropriate transformers.

Figure 16 shows a medium power class B audio amplifier in which the CA3020 or CA3020A is used as a driver. The output stage uses a pair of TO-3-type germanium output transistors which must be mounted on a heat sink for reliable operation. Idling current for the entire system is 70mA from the 35V supply. Sensitivity is 10mV for an output of 10W.

Motor Controller and Servo Amplifier

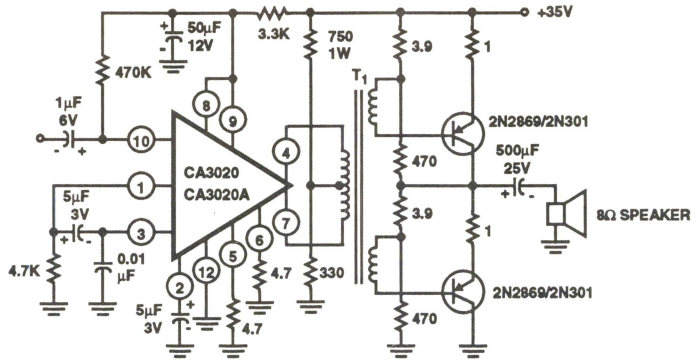
The CA3020 or CA3020A may he used as a 40Hz to 400Hz motor controller and servo amplifier, as shown in Figure 17.



T1: primary impedance, 10,000Ω; center-tapped at 160Ω; primary direct current, 2mA; Thordarson TR-207 (entire secondary), or equivalent.

T2: primary impedance, 20Ω;primary direct current, 0.6A; secondary, 4Ωs; Thordarson TR-304, Stancor TP62, or equivalent.

FIGURE 15. 2.5W CLASS A AUDIO AMPLIFIER USING THE CA3020 OR CA3020A AS A DRIVER AMPLIFIER



T1: primary impedance, 4,000Ω; center-tapped; secondary impedance, 600Ω; center-tapped, split; Thordarson TR-454 or equivalent.

FIGURE 16. 10W SINGLE-ENDED CLASS B AUDIO AMPLIFIER USING THE CA3020 OR CA3020A AS A DRIVER AMPLIFIER

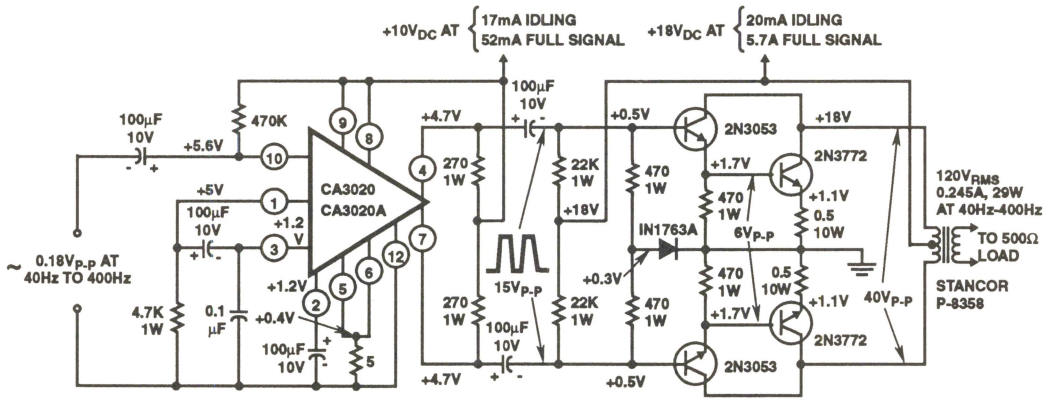


FIGURE 17. MOTOR CONTROLLER AND SERVO AMPLIFIERR USING CA3020 OR CA3020A

Harris Semiconductor

APPNOTE

No. AN6048.1 April 1994

Harris Intelligent Power

SOME APPLICATIONS OF A PROGRAMMABLE POWER SWITCH/AMPLIFIER

Authors: L.R. Campbell and H.A. Wittlinger

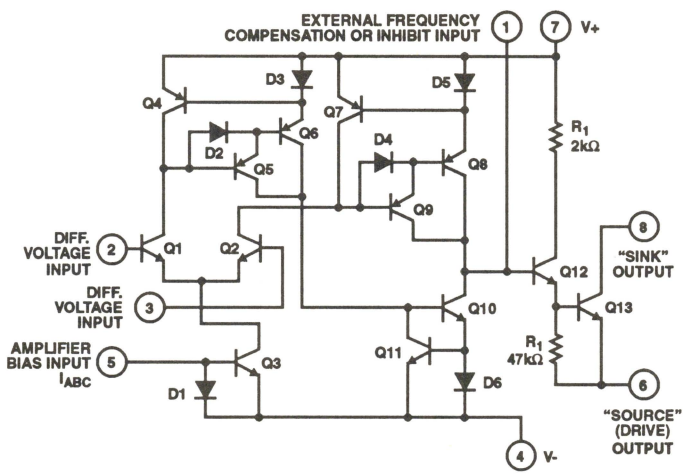
The CA3094 unique monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts of peak power of 10W to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in the following circuit applications:

- Class A Instrumentations and Power Amplifiers
- Class A Driver-Amplifier for Complementary Power Transistors
- Wide Frequency Range Power Multivibrators
- Current- or Voltage Controlled Oscillators
- Comparators (Threshold Detectors)
- Voltage Regulators
- Analog Timers (Long Time Delays)
- Alarm Systems
- Motor-Speed Controllers
- Thyristor Firing Circuits
- Battery Charger Regulator Circuit
- Ground Fault Interrupter Circuits

Circuit Description

The CA3094 series of devices offers a unique combination of circuit flexibility and power-handling capability. Although these monolithic ICs dissipate only a few microwatts when quiescent, they have a high current-output capability (100mA average, 300mA peak) in the active state, and the premium-grade devices can operate at supply voltages up to 44V.

Figure 1 shows a scematic diagram of the CA3094. The portion of the circuit preceding transistors Q12 and Q13 is the preamplifier section and is generically similar to that of the CA3080 Operational Transconductance Amplifier (OTA) [1,2]. The CA3094 circuits can be gain-programmed by either digital and/or analog signals applied to a separate Amplifier-Bias-Current (I_{ABC}) terminal (No. 5 in Figure 1) to control circuit sensitivity. Response of the amplifier is essentially liner as a function of the current at terminal 5. This additional signal input "port" provides added flexibility in may applications. Thus, the output of the amplifier is a function of input signals applied differentially at terminals 2 and 3 and/or in a singly-ended configuration at terminal 5. The output portion of the monolithic circuit in the CA3094 consists of a Darling connected transistor pair with access provided to both the collector and emitter terminals to provide capability to "sink" and/or "source" current.



OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"Source"	6	2	3
"Sink"	8	3	2

FIGURE 1. CA3094 CIRCUIT SCHEMATIC DIAGRAM

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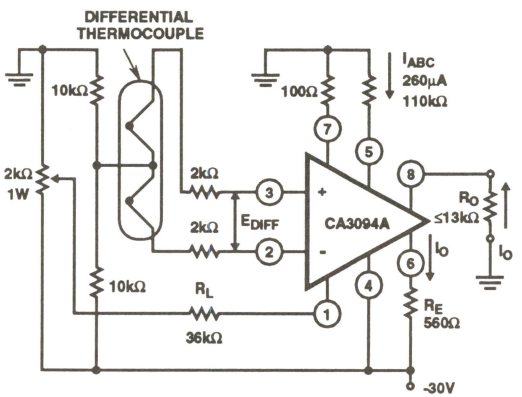
The CA3094 series of circuits consists of six types that differ only in voltage-handling capability and package options, as shown below; other electrical characteristics ar identical.

PACKAGE OPTIONS	MAXIMUM VOLTAGE RATING
CA3094S, CA3094T	24V
CA3094AS, CA3094AT	36V
CA3094BS, CA3094BT	44V

The suffix "S" indicates circuits packaged in TO-5 enclosures with leads formed to an 8 lead dual in line configuration (0.1 inch pin spacing). The suffix "T" indicates circuits packaged in 8 lead TO-5 enclosures with straight leads. The generic CA3094 type designation is used throughout the Note.

Class A Instrumentation Amplifiers

One of the more difficult instrumentation problems frequently encountered is the conversion of a differential input signal to a single-ended output signal. Although this conversion can be accomplished in a straightforward design through the use of classical op-amps, the stringent matching requirements of resistor ratios in feedback networks make the conversion particularly difficult from a practical standpoint. Because the gain of the preamplifier section in the CA3094 can be defined as the product of the transconductance and the load resistance ($g_m R_L$), feedback is not needed to obtain predictable open-loop gain performance. Figure 2 shows the CA3094 in this basic type of circuit.



NOTES:

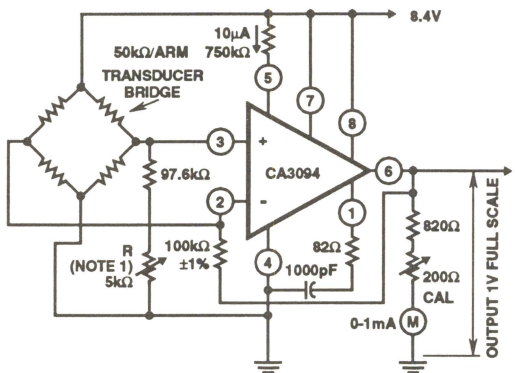
1. Preamp gain (A_V) = $g_m R_L$ = (5) (10^{-3}) (36) (10^3) = 180 (Output at terminal 1).
2. For linear operation: Differential Input ≤| ±26mV |
   (With approx. 1% deviation from linearity).
3. Output voltage (E_O) = A_V ($\pm e_{DIFF}$) = (180) (±26mV) = ±4.7V
4. $$I_O \approx \frac{4.7V}{560\Omega} = 8.35mA \qquad I_O \approx \frac{(g_m R_L)\ (e_{DIFF})}{R_E}$$

FIGURE 2. OPEN LOOP INSTRUMENTATION AMPLIFIER WITH DIFFERENTIAL INPUT AND SINGLE ENDED OUTPUT

The gain of the preamplifier section (to terminal No. 1) is $g_m R_L = (5 \times 10^{-3})\ (36 \times 10^3) = 180$. The transconductande g_m is a function of the current into terminal No. 5, I_{ABC}, the amplifier-bias-current. In this circuit an I_{ABC} of 260μA results in a g_m of 5mS. The operating point of the output stage is controlled by the 2kΩ potentiometer. With no differential input signal (e_{DIFF} = 0), this potentiometer is adjusted to obtain a quiescent output current I_O of 12mA. This output current is established by the 560Ω emitter resistor, R_E, as follows:

$$I_O \approx \frac{(g_m R_L)\ (e_{DIFF})}{R_E}$$

Under the conditions described, an input swing e_{DIFF} of ±26mV produces a variation in the output current I_O of ±8.35mA. The nominal quiescent output voltage is 12mA times 560Ω or 6.7V. This output level drifts approximately -4mV, or -0.0595%, for each °C change in temperature. Output drift is caused by temperature induced variations in the base emitter voltage of the two output transistors, Q12 and Q13.



NOTE:

1. Set to optimize CMRR.

FIGURE 3. SINGLE SUPPLY DIFFERENTIAL BRIDGE AMPLIFIER

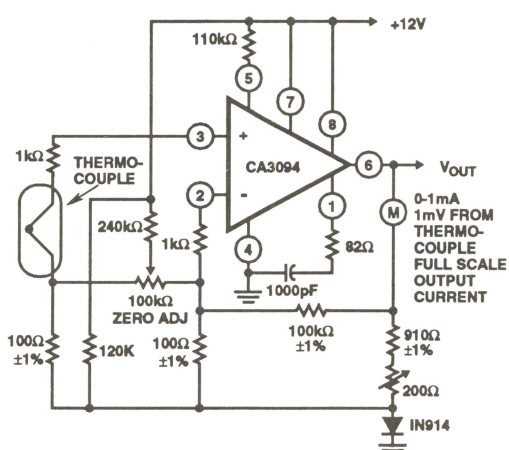


FIGURE 4. SINGLE SUPPLY AMPLIFIER FOR THERMO-COUPLE SIGNALS

Figure 3 shows the CA3094 used in conjunction with a resistive-bridge input network; and Figure 4 shows a single-supply amplifier for thermocouple signals. The RC networks connected between terminals 1 and 4 in Figure 3 and Figure 4 provide compensation to assure stable operation.

The components of the RC network are chosen so that

$$\frac{1}{2\pi RC} \approx 2MHz$$

Class A Power Amplifiers

The CA3094 is attractive for power-amplifier service because the output transistor can control current up to 100mA (300mA peak), the premium devices.

CA3094B can operate at supply voltages up to 44V, and the TO-5 package can dissipate power up to 1.6W when equipped with a suitable heat sink that limits the case temperature to 55°C.

Figure 5 shows a Class A amplifier circuit using the CA3094A that is capable of delivering 280mW to a 350Ω resistive load. This circuit has a voltage gain of 60db and a 3db band width of about 50kHz. Operation is stable without the use of a phase-compensation network. Potentiometer R is used to establish the quiescent operating point for class A operation.

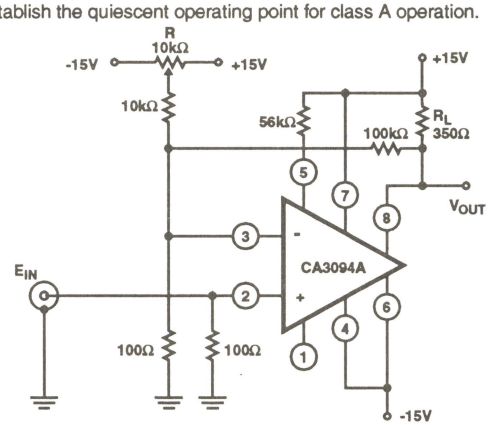
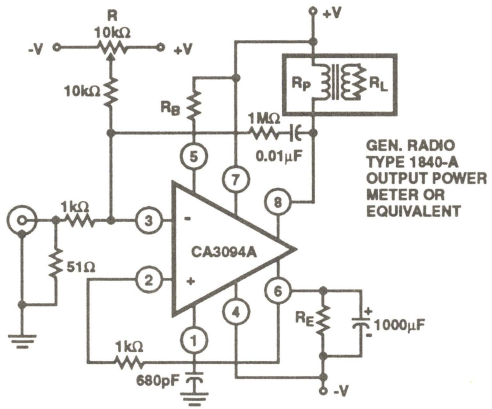


FIGURE 5. CLASS A AMPLIFIER -280mW CAPABILITY INTO A RESISTIVE LOAD

The circuit of Figure 6 illustrates the use of the CA3094 in a class a power-amplifier circuit driving a transformer-coupled load. With dual power supplies of +7.5V and -7.5V, a base resistor R_B of 30kΩ, and an emitter resistor R_E of 50Ω, CA3094 dissipation is typically 625mW. With supplies of +10V and -10V, R_B of 40kΩ, and R_E of 45Ω, the dissipation is 1.5W. Total harmonic distortion is 0.4% at a power output level of 220mW with a reflected load resistance R_P of 310Ω, and is 1.4% for an output of 600mW with an R_P of 128Ω. The setting of potentiometer R establishes the quiescent operating point for class A operation. The 1kΩ resistor connected between terminals 6 and 2 provides DC feedback to stabilize the collector current of the output transistor. The AC gain is established bye the ratio of the 1MΩ resistor connected between terminals 8 and 3 the 1kΩ resistor connected to terminal 3. Phase compensation is provided by the 680pF capacitor connected to terminal 1.



TYPICAL DATA

DEVICE DISSIPATION	625MW	1.5W
R_B	30kΩ	40kΩ
V+	+7.5V	+10V
V-	-7.5V	-10V
R_E	50Ω	45Ω
P_O	220mW	600mW
THD	0.4%	1.4%
RP	310Ω	128Ω

FIGURE 6. CLASS A AMPLIFIER WITH TRANSFORMER COUPLED LOAD

Class A Driver Amplifier for Complementary Power Transistors

The CA3094 configuration and characteristics are ideal for driving complementary power-output transistors;[3] a typical circuit is shown in Figure 7. This circuit can provide 12W of audio power output into an 8Ω load with intermodulation distortion (IMD) of 0.2% when 60Hz and 2kHz signals are mixed in a 4:1 ratio. Intermodulation distortion is shown as a function of power output in Figure 8.

The large amount of loop gain and the flexibility of feedback arrangements with the CA3094 make it possible to incorporate the tone controls into a feedback network that is closed around the entire amplifier system. The tone controls in the circuit of Figure 7 are part of the feedback network connected from the amplifier output (junction of the 330Ω and 47Ω resistors driven by the emitters of Q2 and Q3) to terminal 3 of the CA3094. Figure 9 shows voltage gain as a function of frequency with tone controls adjusted for "flat" response and for responses at the extremes of tone-control rotation. The use of tone controls incorporated in the feedback network results in excellent signal to noise ratio. Hum and noise are typically 700μV (83db down) at the output.

In addition to the savings resulting from reduced parts count circuit size, the use of the CA3094 leads to further savings in the power supply system. Typical values of power supply rejection and common mode rejection are 90db and 100db, respectively. An amplifier with 40db gain and 90db power supply rejection would require a 31mV power-supply ripple to produce 1mV of hum at the output. Therefore, no filtering is required other than that provided by the energy storage capacitors at the output of the rectifier system shown in Figure 7.

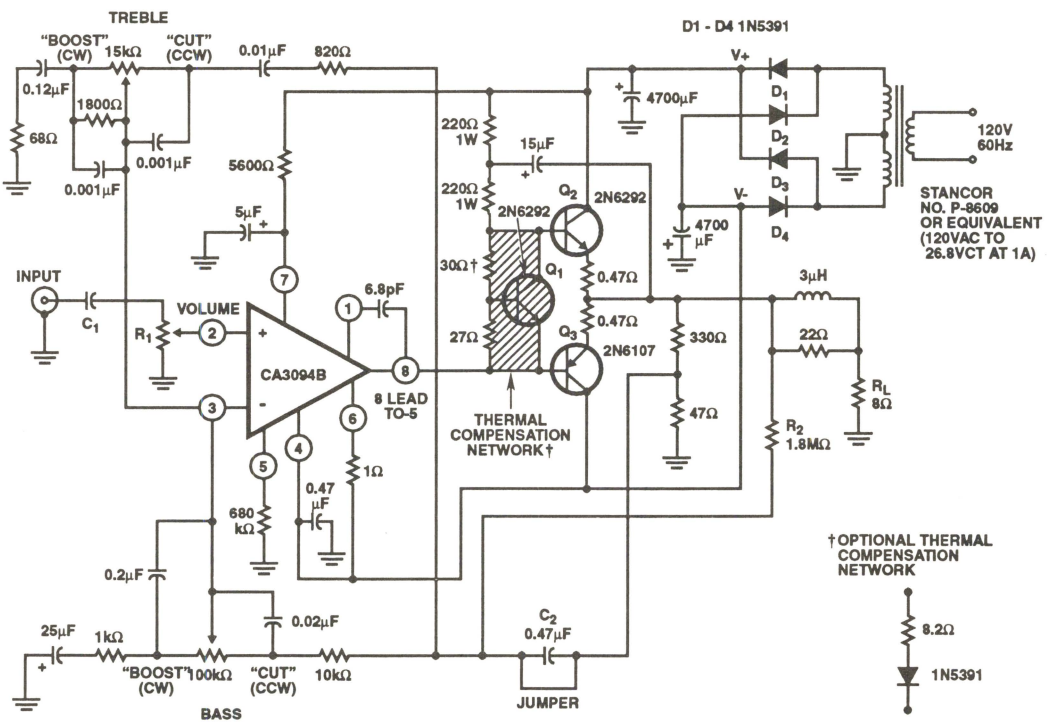
For application in which the operating temperature range is limited (e.g., consumer service the thermal compensation network (shaded area) can be replaced by a more economical configuration consisting of a resistor diode combination (8.2Ω and 1N5391) as shown in Figure 7.

Power Multivibrators (Astable and Monostable)

the CA3094 is suitable for use in power multivibrators because its high current output transistor can drive low impedance circuits while the input circuitry and the frequency determining elements are operating at micropower levels. A typical example of an astable multivibrator using the CA9034 with a dual power supply is shown in Figure 10. The output frequency f_{OUT} is determined as follows:

$$f_{OUT} = \frac{1}{2RC_{IN}\left[(2R1/R2)+1\right]}$$

If R2 is equal to 3.08 R1, then f_{OUT} is simply the reciprocal of RC.



TYPICAL PERFORMANCE DATA FOR 12W AUDIO AMPLIFIER CIRCUIT

Power Output (8Ω load, Tone Control set at "Flat")
- Music (at 5% THD, regulated supply) 15W
- Continuous (at 0.2% IMD, 60Hz and 2kHz mixed in a 4:1 ratio, unregulated supply)
- See Figure 8 in AN6048 . . . . . 12W

Total Harmonic Distortion
- At 1W, unregulated supply 0.05%
- At 12W, unregulated supply 0.57%

Voltage Gain 40dB
Hum and Noise (below continuous power output) 83dB
Input Resistance 250kΩ
Tone Control Range . . . . . See Figure 9 in AN6048

NOTES:
1. For standard input: Short C_2; R_1 = 250kΩ, C_1 = 0.047μF; remove R_2.
2. For ceramic cartridge input: C_1 = 0.0047μF, R_1 = 2.5MΩ, remove jumper from C_2; leave R_2.

FIGURE 7. 12W AUDIO AMPLIFIER CIRCUIT FEATURING TRUE COMPLEMENTARY SYMMETRY OUTPUT STAGE WITH CA3094 IN DRIVER STAGE

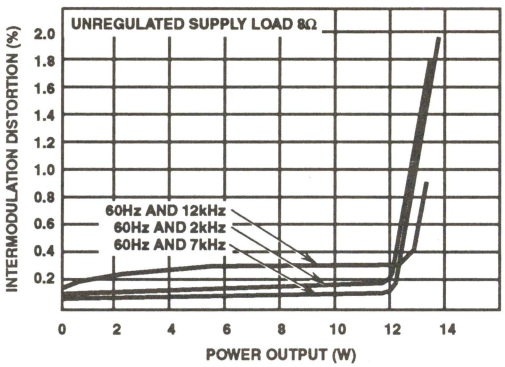


FIGURE 8. INTERMODULATION DISTORTION vs POWER OUTPUT

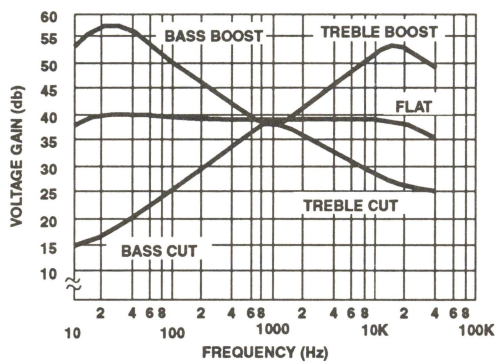


FIGURE 9. VOLTAGE GAIN vs FREQUENCY

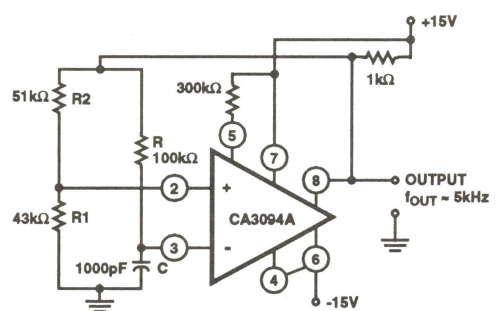


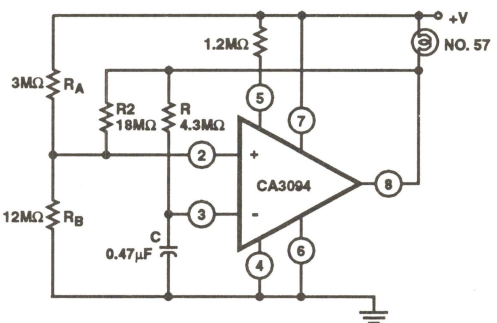
FIGURE 10. ASTABLE MULTIVIBRATOR USING DUAL SUPPLY

Figure 11 is a single supply astable multivibrator circuit which illustrates the use of the CA3094 for flashing an incandescent lamp. With the component values shown, this circuit produces one flash per second with a 25% "on" time while delivering output current in excess of 100mA. During the 75% "off" time it idles with micropower consumption. The flashing rate can be maintained with in ±2% of the nominal value over a battery voltage range from 6V to 15V and a temperature excursion from 0°C to 70°C. The CA3094 series of circuits can supply peak-power output in excess of 10W when used in this type of circuit. The frequency of oscillation f_{OSC} is determined by the resistor rations, as follows:

$$f_{OSC} = \frac{1}{(2RCIn)\ [(2R1/R2) + 1]}$$

where:

$$R1 = \frac{R_A R_B}{R_A + R_B}$$



NOTES:

1. 1 Flash/Sec.

$$f_{OSC} = \frac{1}{(2RCIn)\ [(2R1/R2) + 1]}$$

where:

$$R1 = \frac{R_A R_B}{R_A + R_B}$$

2. 25% Duty Cycle
3. Frequency Independent of V+ from 6V - 15V DC

FIGURE 11. ASTABLE MULTIVIBRATOR USING SINGLE SUPPLY

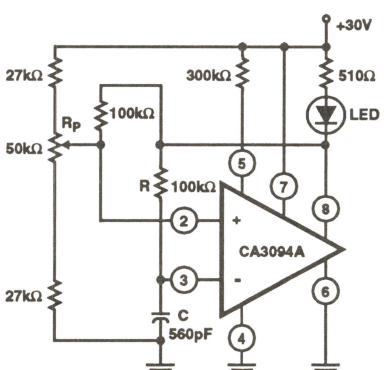


FIGURE 12. ASTABLE POWER MULTIVIBRATOR WITH PROVISIONS FOR VARYING DUTY CYCLE

Provisions can easily be made in the circuit of Figure 11 to vary the multivibrator pulse length while maintaining an essentially constant pulse repetition rate. The circuit shown

in Figure 12 incorporates a potentiometer R_P for varying the width of pulses generated by the astable multivibrator driving light emitting diode (LED).

Figure 13 shows a circuit incorporating independent controls (R_{ON} and R_{OFF}) to establish the "on" and "off" periods of the current supplied to the LED. The network between points "A" and "B" is analogous in function to that of the 100kΩ resistor R in Figure 12.

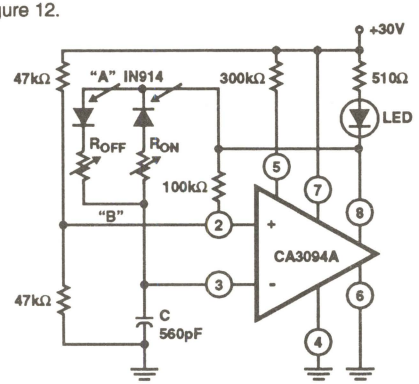


FIGURE 13. ASTABLE POWER MULTIVIBRATOR WITH PROVISIONS FOR INDEPENDENT CONTROL OF LED "ON-OFF" PERIODS

The CA3094 is also suitable for use in monostable multivibrators as shown in Figure 14. In essence, this circuit is a pulse counter in which the duration of the output pulses is independent of trigger pulse duration. The meter reading is a function of the pulse repetition rate which can be monitored with the speaker.

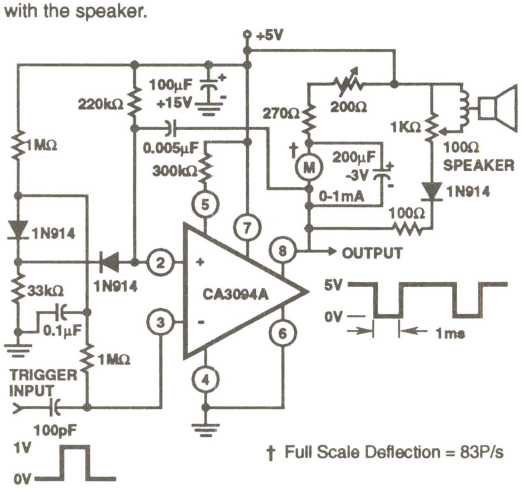


FIGURE 14. POWER MONOSTABLE MULTIVIBRATOR

Current or Voltage Controlled Oscillators

Because the transconductance of the CA9034 varies linearly as a function of the amplifier bias current (I_{ABC}) supplied to terminal 5, the design of a current or voltage controlled oscillator is straightforward, a shown in Figure 15. Figure 16 and Figure 17 show oscillator frequency as a function of I_{ABC} for a current controlled oscillator for two different values of capacitor C in FIgure 15. The addition of an appropriate resistor (R) in series with terminal 5 in Figure 15 converts the circuit into a voltage controlled oscillator. Linearity with respect to either current or voltage control is within 1% over the middle half of the characteristics. However, variation in the symmetry of the output pulses was a function of frequency is an inherent characteristic of the circuit in Figure 15, and leads to distortion when this circuit is used to drive the phase detector in phase-locked-loop applications. This type distortion can be eliminated by interposing an appropriate flip-flop between the output of the oscillator and the phase locked discriminator circuits.

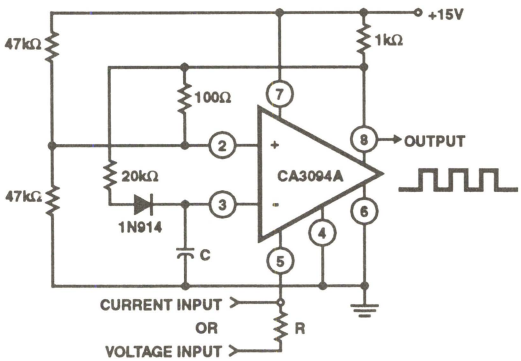


FIGURE 15. CURRENT OR VOLTAGE CONTROLLED OSCILLATOR

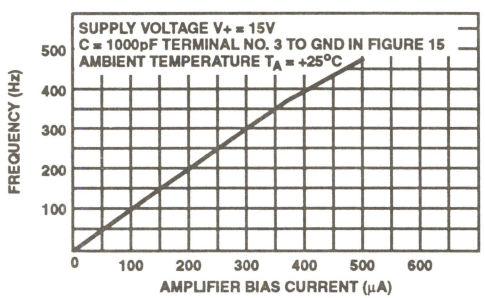


FIGURE 16. FREQUENCY AS A FUNCTION OF I_{ABC} FOR C = 1000pF FOR CIRCUIT IN FIGURE 15

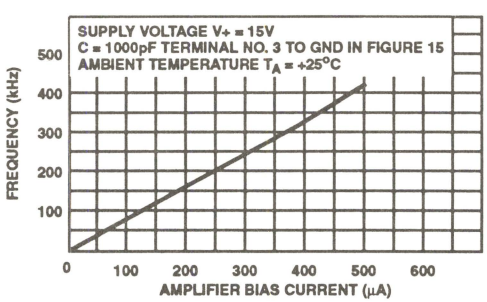


FIGURE 17. FREQUENCY AS A FUNCTION OF I_{ABC} FOR C = 100pF FOR CIRCUIT IN FIGURE 15

Comparators (Threshold Detectors)

Comparator circuits are easily implemented with the CA43094, as shown by the circuits in Figure 18. The circuit of Figure 18A is arranged for dual supply operation; the input voltage exceeds the positive threshold, the output voltage swings essentially to the negative supply voltage rail (it is assumed that there is negligible resistive loading on the output terminal). an input voltage that exceeds the negative threshold value results in a positive voltage output essentially equal to the positive supply voltage. The circuit in Figure 18B, connected for single supply operation, functions similarly.

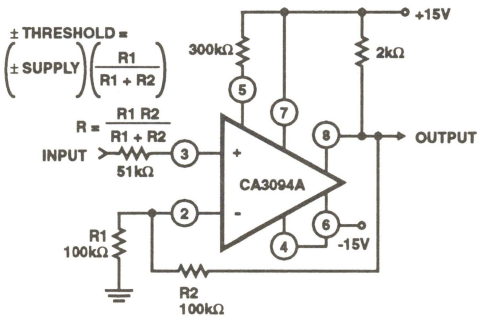


FIGURE 18A. DUAL SUPPLY

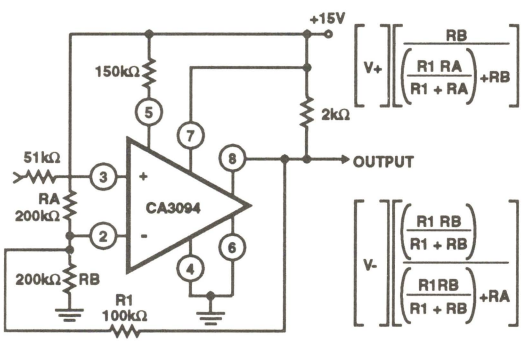


FIGURE 18B. SINGE SUPPLY

FIGURE 18. COMPARATORS (THRESHOLD DETECTORS) DUAL AND SINGLE SUPPLY TYPES

Figure 19 shows a dual limit threshold detector circuit in which the high level limit is established by potentiometer R1 and the low level limit is set by potentiometer R2 to actuate the CA3080 low limit detector.[1, 2] A positive output signal exceeds either the high limit or the low limit values established by the appropriate potentiometer settings. This output voltage is approximately 12V with the circuit shown.

The high current handling capability of the CA3094 makes it useful in Schmitt power trigger circuits such as that shown in Figure 20. In this circuit, a relay coil is switched whenever the input signal traverses a prescribed upper or lower trip point, as defined by the following expressions:

$$\text{Upper Trip Point} = 30\left(\frac{R3}{R1 + R2 + R3}\right)$$

$$\text{Lower Trip Point} \cong (30 - 0.026R1)\frac{R3}{R2 + R3}$$

The circuit is applicable, for example, to automatic ranging. With the values shown in Figure 20, the relay coil is energized when the input exceeds approximately 5.9V and remains energized until the input signal drops below approximately 5.5V.

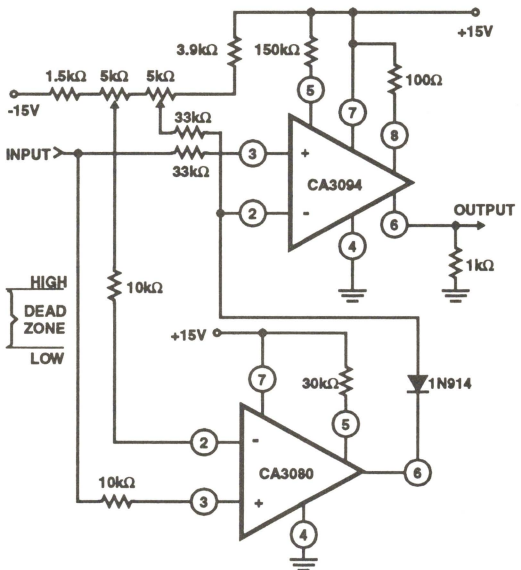


FIGURE 19. DUAL LIMIT THRESHOLD DETECTOR

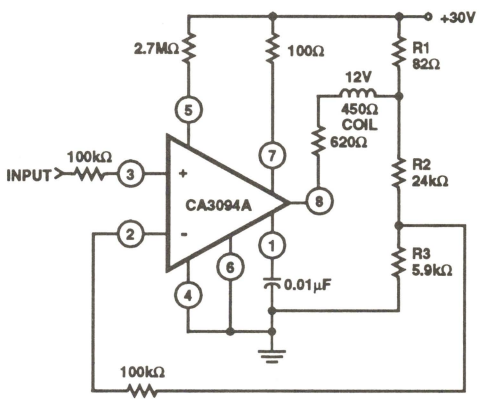


FIGURE 20. PRECISION SCHMITT POWER TRIGGER CIRCUIT

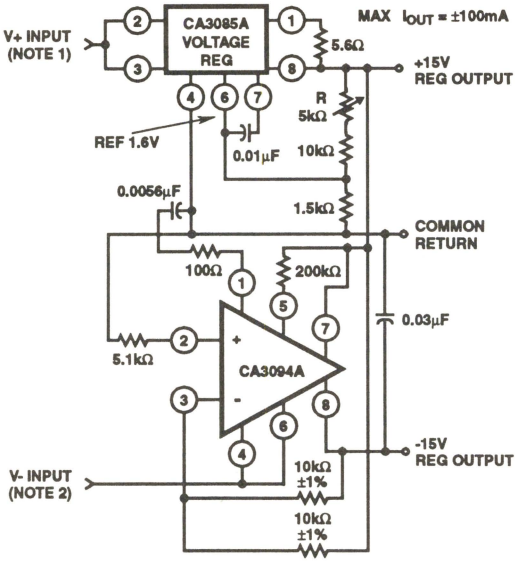
Power Supply Regulators

The CA3094 is an ideal companion device to the CA3085 series regulator circuits[4] in dual voltage tracking regulators that handle currents up to 100mA. In the circuit of Figure 21, the magnitude of the regulated positive voltage provided by the CA3085A is adjusted voltage supplies the power for the CA3094A negative regulator and also supplies a reference voltage to its terminal 3 to provide tracking. This circuit provides a maximum line regulation equal to 0.075% per volt of input voltage change and a maximum load regulation of 0.075% of the output voltage.

Figure 22 shows a regulated high voltage supply similar to the type used to supply power for Geiger-Mueller tubes. The CA3094, used as an oscillator, drives a step-up transformer which develops suitable high voltages for rectification in the IN4007 diode network. A sample of the regulated output voltage is fed to the CA3080A operational transconductance amplifier through the 198MΩ and 910kΩ divider to control the pulse repetition rate of the CA3094. Adjustment of potentiometer R determines the magnitude of the regulated output voltage. Regulation of the desired output voltage is maintained within 1% despite load current variations of 5μA to 26μA. The DC to DC conversion efficiency is about 48%.

Timers

The programmability feature inherent in the CA3094 (and operational transconductance amplifiers in general) simplifies the design of presettable timers such as the one shown in Figure 23. Long timing intervals (e.g. up to 4hrs) are achieved by discharging a timing capacitor C1 into the signal input terminal (e.g. No. 3) of the CA3094. This discharge current is controlled precisely by the magnitude of the amplifier bias current I_{ABC} programmed into terminal 5 through a resistor selected by switch S2. Operation of the circuit is initiated by charging capacitor C1 through the momentary closing of switch S1. Capacitor C1 starts discharging and continues discharging until voltage E1 is less than voltage E2. The differential input transistors in the CA3094 then change state, and terminal 2 draws sufficient current to reverse the polarity of the output



NOTES:

1. V+ input range = 19V to 30V for 15V output
2. V- input range = -16 to -30V for -15V output
3. REGULATION:

$$\text{MAX LINE} = \frac{\Delta V_{OUT}}{\left[V_{OUT}(\text{INITIAL})\right]\Delta V_{IN}} \times 100 = 0.075\%/V$$

$$\text{MAX LINE} = \frac{\Delta V_{OUT}}{V_{OUT}(\text{INITIAL})} \times 100 = 0.075\%\ V_{OUT}$$

(I_L FROM 1mA to 50mA)

FIGURE 21. DUAL VOLTAGE TRACKING REGULATOR

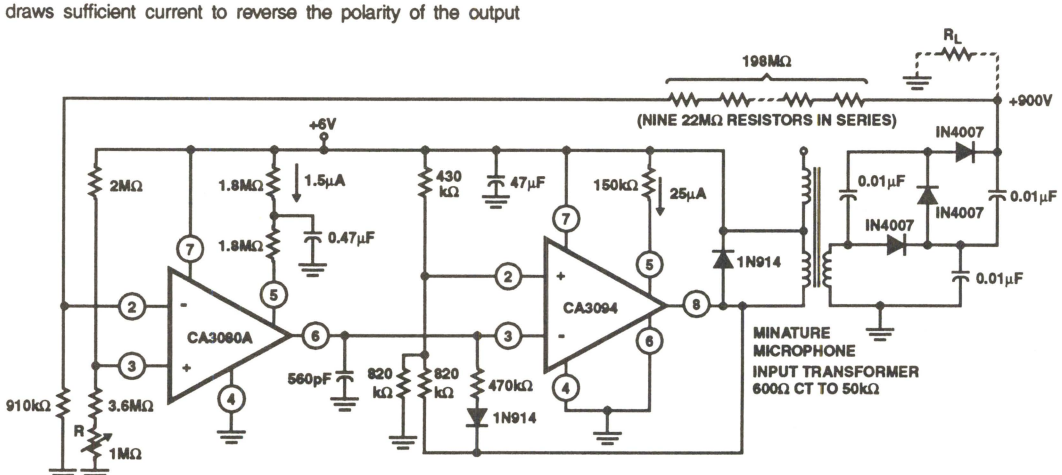
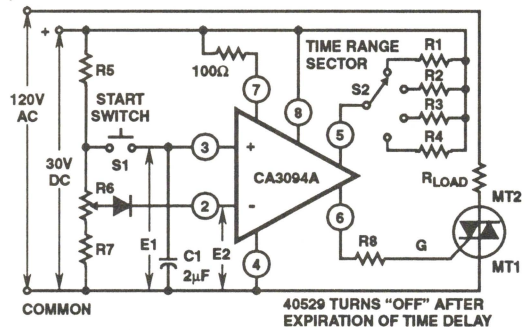


FIGURE 22. REGULATED HIGH VOLTAGE SUPPLY

voltage (terminal 6). Thus, the CA3094 not only has provision for readily presetting the time delay, but also provides significant output current to drive control devices such as thyristors. Resistor R5 limits the initial charging current for C1. Resistor R5 limits the initial charging current for C1. Resistor R7 establishes a minimum voltage of at least 1V at terminal 2 to insure operation within the common mode input range of the device. The diode limits the maximum differential input voltage to 5V. Gross changes in time range selection are made with switch S2, and vernier trimming adjustments are made with potentiometer R6.



TIME	RESISTOR VALUE	
3Min	R1 = 0.5MΩ	R5 = 2.7kΩ
30Min	R2 = 5.1MΩ	R6 = 50kΩ
2Hrs	R3 = 22MΩ	R7 = 2.7kΩ
4Hrs	R4 = 44MΩ	R8 = 1.5kΩ

FIGURE 23. PRESETTABLE ANALOG TIMER

In some timer applications, such as that shown in Figure 24, a meter readout of the elapsed time is desirable. This circuit uses the CA3094 and CA3083 transistor array[5] to control the meter and a load switching triac. The timing cycle starts with the momentary closing of the start switch to charge capacitor C1 to an initial voltage determined by the 50kΩ vernier timing adjustment. During the timing cycle the output of the CA3094, which is also the collector voltage of Q1, is "high". The base drive for Q1 is supplied from the positive supply through a 91kΩ resistor. The emitter of Q1, through the 75Ω resistor, supplies gate-trigger current to the triac. Diode connected transistors Q4 and Q5 are connected so that transistor Q1 acts as a constant current source to drive the triac. As capacitor C1 discharges, the CA3094 output voltage at terminal 6 decreases until it becomes less than the V_{CESAT} of Q1. At this point the flow of drive current to the triac ceases and the timing cycle is ended. The 20kΩ resistor between terminals 2 and 6 of the CA3094 is a feedback resistor. Diode connected transistor Q2 and Q3 and their associated networks serve to compensate for non-linearities in the discharge circuit network by bleeding corrective current into the 20kΩ feedback resistor. Thus, current flow in the meter is essentially linear with respect to the timing period. The time periods as a function of R1 and indicated on the Time-Range Selection Switch in Figure 24.

Alarm Circuit

Figure 25 shows an alarm circuit utilizing two "senor" lines. In the "no-alarm" state, the potential at terminal 5 (I_{ABC}) is driven with sufficient current though resistor R5 to keep the output voltage "high". If either "sensor" line is opened, shorted to ground, or shorted to the other sensor line, the

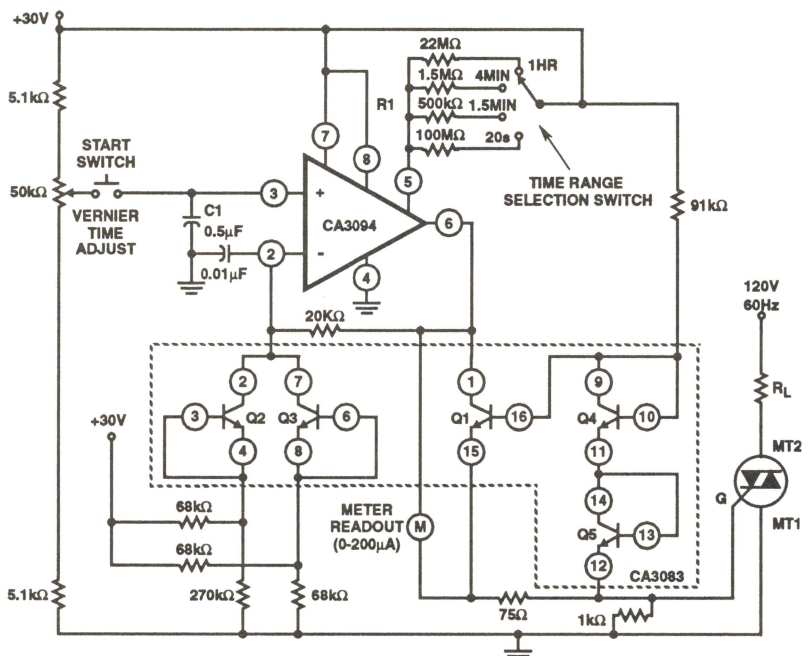


FIGURE 24. PRESETTABLE TIMER WITH LINEAR READOUT

output goes "low" and activates some type of alarm system. The back-to-back diodes connected between terminals 2 and 3 protect the CA3094 input terminals against excessive differential voltages.

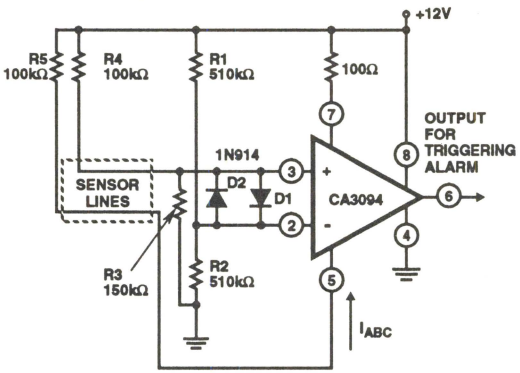


FIGURE 25. ALARM SYSTEM

Motor-Speed Controller System

Figure 26 illustrates the use of the CA3094 in a motor-speed controller system. Circuity associated with rectifiers D1 and D2 comprises a full wave rectifier which develops a train of half-sinusoid voltage pulse to power the dc motor. The motor speed depends on the peak value of the half-sinusoids and the period of time (during each half cycle) the SCR is conductive.

The SCR conduction, in turn, is controlled by the time duration of the positive signal supplied to the SCR by the phase comparator. The magnitude of the positive dc voltage supplied to terminal 3 of the phase comparator depends on motor-speed error as detected by a circuit such as that shown in Figure 27. This dc voltage is compared to that of a fixed amplitude ramp wave generated synchronously with the ac line voltage frequency. The comparator output at terminal 6 is "high" (to trigger the SCR into conduction) during the period when the ramp potential is less than that of the error voltage on terminal 3. The motor current conduction period is increased as the error voltage at terminal 3 is increased in the positive direction. Moter-speed accuracy of ±1% is easily obtained with this system.

Motor-Speed Error Detector

Figure 27A shows a motor-speed error detector suitable for use with the circuit of Figure 26. A CA3080 operational transconductance amplifier is used as a voltage comparator. The reference for the comparator is established by setting the potentiometer R so that the voltage at terminal 3 is more positive than that at terminal 2 when the motor speed is too low. An error voltage E1 is derived from a tachometer driven by the motor. When the motor speed is too low, the voltage at terminal 2 of the voltage comparator is less positive than that at terminal 3, and the output voltage at terminal 6 goes "high". When the motor speed is too high, the opposite input conditions exist, and the output voltage at terminal 6 goes "low". Figure 27B also shows these conditions graphically, with a linear transition region between the "high" and "low" output levels. This linear

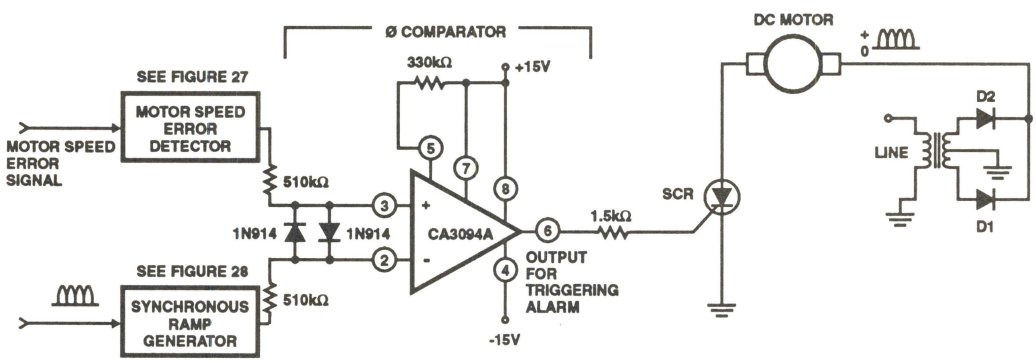
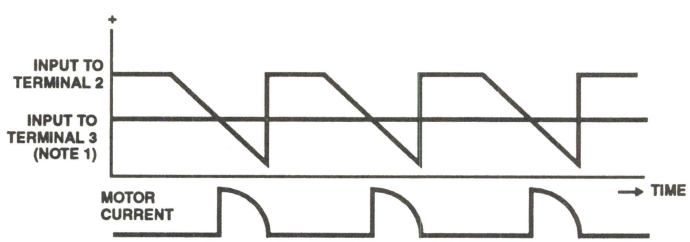


FIGURE 26A.



NOTE:

1. This level will vary depending on motor speed. (See Text).

FIGURE 26B.

FIGURE 26. MOTOR SPEED CONTROLLER SYSTEM

transition region is known as "proportional bandwidth". The slope of this region is determined by the proportional bandwidth control to establish the error correction response time.

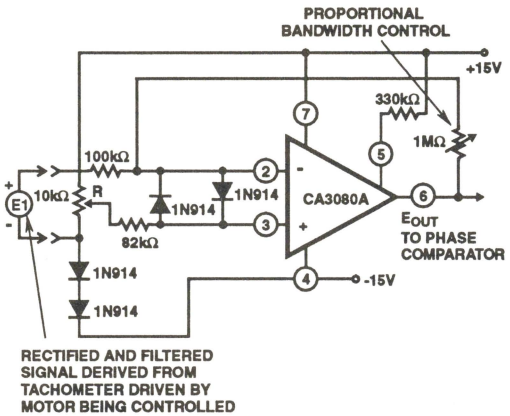


FIGURE 27A. VOLTAGE COMPARATOR

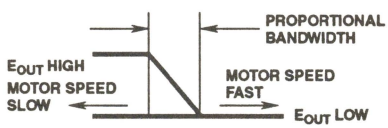


FIGURE 27B.

FIGURE 27. MOTOR SPEED ERROR DETECTOR

Synchronous Ramp Generator

Figure 28 shows a schematic diagram and signal waveforms for a synchronous ramp generator suitable for use with the motor controller circuit of Figure 26. Terminal 3 is biased at approximately +2.7V (above the negative supply voltage). The input signal E_{IN} at terminal 2 is a sample of the half-sinusoids (at line frequency) used to power the motor in Figure 26. A synchronous ramp signal is produced by using the CA3094 to charge and discharge capacitor C1 in response to the synchronous toggling of E_{IN}. The charging current for C1 is supplied by terminal 6. When terminal 2 swings more positive than terminal 3, transistors Q12 and Q13 in the CA3094 (Figure 1) lose their base drive and become non-conductive. Under these conditions, C1 discharges linearly through the external diode D3 and Q10, D6 path in the CA3094 to produce the ramp wave. The E_{OUT} signal is supplied to the phase comparator in Figure 26.

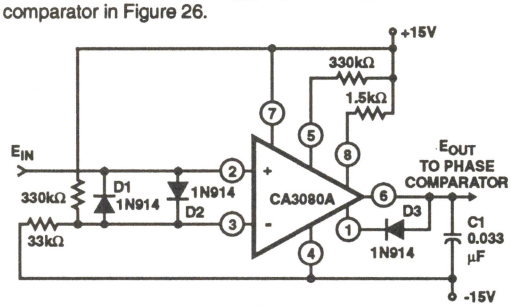


FIGURE 28A.

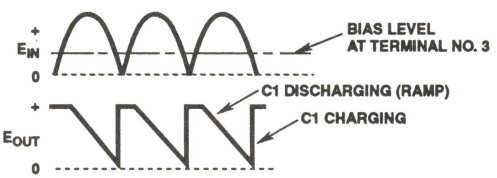


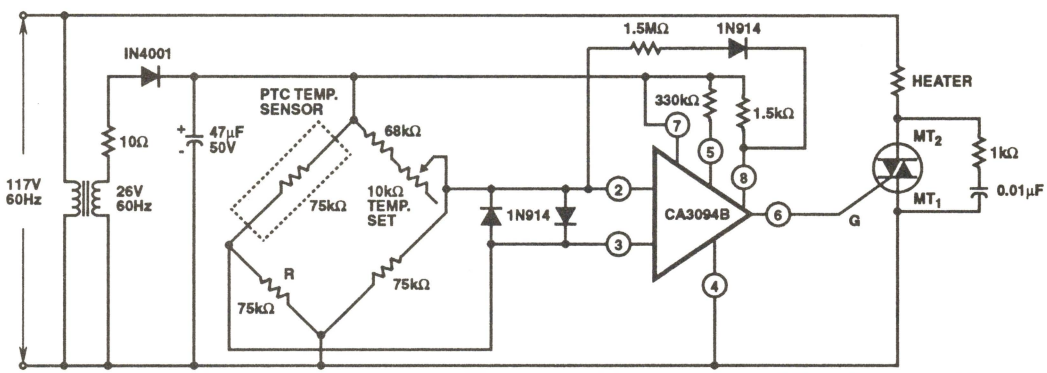
FIGURE 28B.

FIGURE 28. SYNCHRONOUS RAMP GENERATOR WITH INPUT AND OUTPUT WAVEFORMS

Thyristor Firing Circuits

Temperature Controller

In the temperature control system shown in Figure 29, the differential input of the CA3094 is connected across a bridge circuit comprised of a PTC (positive temperature coefficient) temperature sensor, two 75kΩ resistors, and an arm containing the temperature set control. When the temperature is "low", the resistance of the PTC type sensor is also low; therefore, terminal 3 is more positive than terminal 2 and an output current from terminal 6 of the CA3094 drives the triac into conduction. When the temperature is "high", the input



NOTE: All Resistors are 1/2W.

FIGURE 29. TEMPERATURE CONTROLLER

conditions are reversed and the triac is cut off. Feedback from terminal 8 provides hysteresis to the control point to prevent rapid cycling of the system. The 1.5kΩ resistor between terminal 8 and the positive supply limits the triac gate current and develops the voltage for the hysteresis feedback. The excellent power supply rejection and common mode rejection ratios of the CA3094 permit accurate repeatability of control despite appreciable power supply ripple. The circuit of Figure 29 is equally suitable for use with NTC (negative temperature coefficient) sensors provided the positions of the sensor and the associated resistor R are interchanged in the circuit. The diodes connected back to back across the input terminals of the CA3094 protect the device against excessive differential input signals.

Thyristor Control from AC Bridge Sensor

Figure 30 shows a line operated thyristor firing circuit controlled by a CA3094 that operates from an AC Bridge sensor. This circuit is particularly suited to certain classes of sensors that cannot be operated from DC. The CA3094 is inoperative when the high side of the AC line is negative because there is no I_{ABC} supply to terminal 5. When the sensor bridge is unbalanced so that terminal 2 is more positive than terminal 3, the output stage of the CA3094 is cut off when the AC line swing s positive, and the output level at terminal 8 of the CA3094 goes "high". Current from the line flows through the IN3193 diode to charge the 100µF reservoir capacitor, and also provides current to drive the triac into conduction. During the succeeding negative swing of the AC line, there is sufficient remanent energy in the reservoir capacitor to maintain conduction in the triac.

When the bridge is unbalanced in the opposite direction so that terminal 3 is more positive than terminal 2, the output of the CA3094 at terminal 8 is driven sufficiently "low" to "sink" the current supplied through the 1N4003 diode so that the triac gate cannot be triggered. Resistor R1 supplies the hysteresis feedback to prevent rapid cycling between turn on and turn off.

Battery Charger Regulator Circuit

The circuit for battery charger regulator circuit using the CA3094 is shown in Figure 31. This circuit accurately limits the peak output voltage to 14V, as established by the zener diode connected across terminals 3 and 4. When the output voltage rises slightly above 14V, signal feedback through a 100kΩ resistor to terminal 2 reduces the current drive supplied to the 2N3054 pass transistor from terminal 6 of the CA3094. An incandescent lamp serves as the indicator of charging current flow. Adequate limiting provisions protect the circuit against damage under load short conditions. The advantage of the circuit over certain the types of regulator circuits is that the reference voltage supply doesn't drain the battery when the power supply is disconnected. This feature is important in portable service applications, such as in a trailer where a battery is kept "on-charge" when the trailer is parked and power is provided from an AC line.

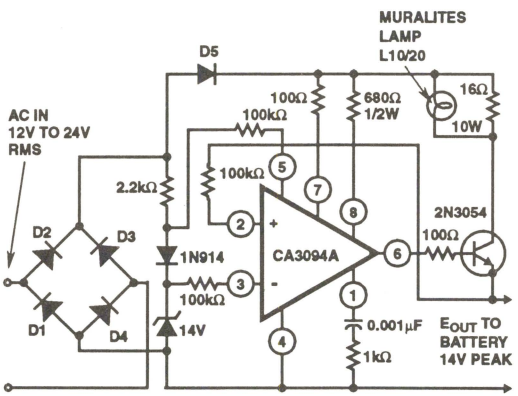


FIGURE 31. BATTERY CHARGER REGULATOR CIRCUIT

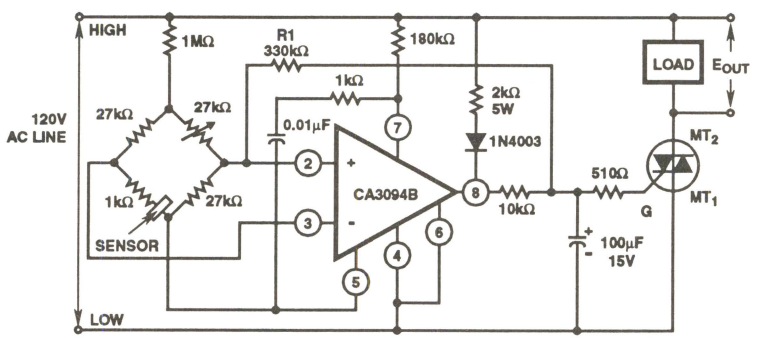
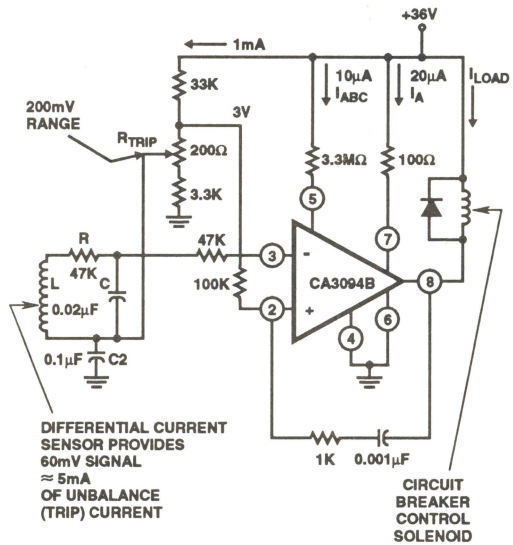


FIGURE 30. LINE OPERATED THYRISTOR FIRING CIRCUIT CONTROLLED BY AC BRIDGE SENSOR



NOTES:

1. All resistors in Ω, 1/2W, 10%.
2. RC selected for 3db point at 200Hz.
3. C2 = AC by-pass.
4. Offset ADJ included in R_{TRIP}.
5. Input impedance from 2 to 3 equals 800K.
6. With no input signal terminal 8 (Output) at +36V.

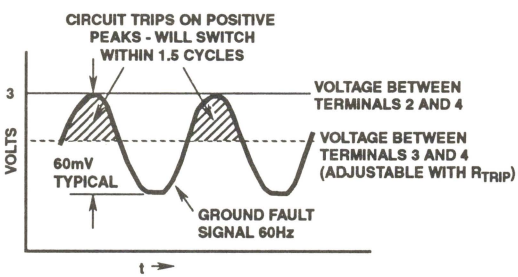


FIGURE 32. GROUND FAULT INTERRUPTER (GFI) AND WAVEFORM PERTINENT TO GROUND FAULT DETECTOR

Ground Fault Interrupters (GFI)

Ground fault interrupter systems are used to continuously monitor the balance of current between the high and neutral lines of power distribution networks. Power is interrupted whenever the unbalance exceeds a preset value (e.g., 5mA). An unbalance of current can occur then, for example, defective insulation in the high side of the line permits leakage of current to an earth ground. GFI systems can be used to reduce the danger of electrocution from accidental contact with "high" line because the unbalance caused by the leakage of current from the "high" line through a human body to ground results in an interruption of current flow.

The CA3094 is ideally suited for GFI applications because it can be operated from a single supply, has adequate sensitivity, and can drive a relay or thyristor directly to effect power interruption. Figure 32 shows a typical GFI circuit. Vernier adjustment of the trip point is made by the R_{TRIP} potentiometer. When the differential current sensor supplies a signal that exceeds the selected trip-point voltage level (e.g., 60mV), the CA3094 is toggled "on" and terminal 8 goes "low" to energize the circuit breaker trip coil. Under quiescent conditions, the entire circuit consumes approximately 1mA. The resistor R, connected to one leg of the current sensor, provides current limiting to protect the CA3094 against voltage spikes as large as 100V. Figure 32 also shows the pertinent waveform for the GFI circuit.

Because hazards of severe electrical shock are a potential danger to the individual user in the event of malfunctions in GFI apparatus, it is mandatory that the highest standard of good engineering practice be employed in designing equipment for this service. Every consideration in design and application must be given to the potentially serious consequences of component malfunction in such equipment. Use of "reliability through redundancy" concepts and so called "fail-safe" features is encouraged.

References

[1] Harris Published Data for CA3080 and CA3080A, File No. 475.

[2] Applications of the CA3080 and CA3080A High Performance Operational Transconductance Amplifiers, AN6668.

[3] L. Kaplan and H. A. Wittlinger, "An IC Operational Transconductance Amplifier (OTA) with Power Capability". Paper originally presented at the IEEE Chicago Springs Conference on Broadcast and TV Receivers, June 1972. Reprinted as AN6077.

[4] Harris Published Data for CA3085, File No. 491.

[5] Harris Published Data for CA3083, File No. 481.

Harris Semiconductor

APPNOTE

No. AN6077.1 April 1994

Harris Intelligent Power

AN IC OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) WITH POWER CAPABILITY

Authors: L. Kaplan and H. Wittlinger

In 1969, the first triple operational transconductance amplifier or OTA was introduced. The wide acceptance of this new circuit concept prompted the development of the single, highly linear operational transconductance amplifier, the CA3080. Because of its extremely linear transconductance characteristics with respect to amplifier bias current, the CA3080 gained wide acceptance as a gain control block. The CA3094 improved on the performance of the CA3080 through the addition of a pair of transistors; these transistors extended the current carrying capability to 300mA, peak. This new device, the CA3094, is useful in an extremely broad range of circuits in consumer and industrial applications; this paper describes only a few of the many consumer applications.

What Is an OTA?

The OTA, operational transconductance amplifier, concept is as basic as the transistor; once understood, it will broaden the designer's horizons to new boundaries and make realizable designs that were previously unobtainable. Figure 1 shows an equivalent diagram of the OTA. The differential input circuit is the same as that found on many modern operational amplifiers. The remainder of the OTA is composed of current mirrors as shown in Figure 2. The geometry of these mirrors is such that the current gain is unity. Thus, by highly degenerating the current mirrors, the output current is precisely defined by the differential input amplifier. Figure 3 shows the output current transfer characteristic of the amplifier. The shape of this characteristic remains constant and is independent of supply voltage. Only the maximum current is modified by the bias current.

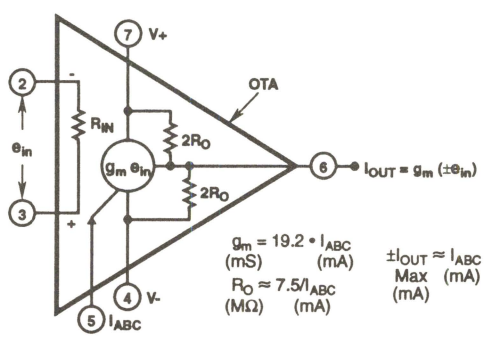


FIGURE 1. EQUIVALENT DIAGRAM OF THE OTA

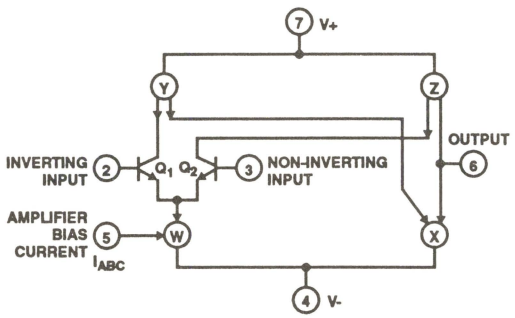


FIGURE 2. CURRENT MIRRORS W, X, Y AND Z USED IN THE OTA

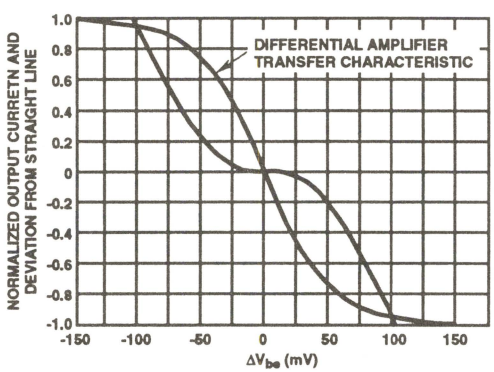


FIGURE 3. THE OUTPUT CURRENT TRANSFER CHARACTERISTIC OF THE OTA IS THE SAME AS THAT OF AN IDEALIZED DIFFERENTIAL AMPLIFIER

The major controlling factor in the OTA is the input amplifier bias current I_{ABC}; as explained in Figure 1, the total output current and g_m are controlled by this current. In addition, the input bias current, input resistance, total supply current, and output resistance are all proportional to this amplifier bias current. These factors provide the key to the performance of this most flexible device, an idealized differential amplifier, i.e., a circuit in which differential input to single ended output conversion can be realized. With this knowledge of the basics of the OTA, it is possible to explore some of the applications of the device.

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DC Gain Control

The methods of providing DC gain control functions are numerous. Each has its advantage simplicity, low cost, high level control, low distortion. Many manufacturers who have nothing better to offer propose the use of a four quadrant multiplier. This is analogous to using an elephant to carry a twig. It may be elegant but it takes a lot to keep it going! When operated in the gain control mode, one input of the standard transconductance multiplier is offset so that only one half of the differential input is used; thus, one half of the multiplier is being thrown away.

The OTA, while providing excellent linear amplifier characteristics, does provide a simple means of gain control. For this application the OTA may be considered the realization of the ideal differential amplifier in which the full differential amplifier g_m is converted to a single ended output. Because the differential amplifier is ideal, its g_m is directly proportional to the operating current of the differential amplifier; in the OTA the maximum output current is equal to the amplifier bias current I_{ABC}. Thus, by varying the amplifier bias current, the amplifier gain may be varied: $A = g_m R_L$ where R_L is the output load resistance. Figure 4 shows the basic configuration of the OTA DC gain control circuit.

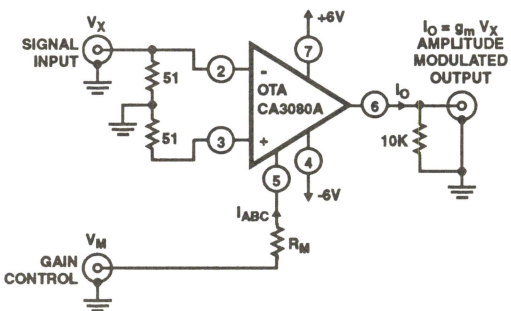


FIGURE 4. BASIC CONFIGURATION OF THE OTA DC GAIN CONTROL CIRCUIT

As long as the differential input signal to the OTA remains under 50mV peak-to-peak, the deviation from a linear transfer will remain under 5 percent. Of course, the total harmonic distortion will be considerably less than this value. Signal excursions beyond this point only result in an undesired "compressed" output. The reason for this compression can be seen in the transfer characteristic of the differential amplifier in Figure 3. Also shown in Figure 3 is a curve depicting the departure from a linear line of this transfer characteristic.

The actual performance of the circuit shown in Figure 4 is plotted in Figure 5. Both signal to noise ratio and total harmonic distortion are shown as a function of signal input. Figures 5B and 5C show how the signal handling capability of the circuit is extended through the connection of diodes on the input as shown in Figure 6[2]. Figure 7 shows total system gain as a function of amplifier bias current for several values of diode current. Figure 8 shows an oscilloscope reproduction of the CA3080 transfer characteristic as applied to the circuit of Figure 4. The oscilloscope reproduction of Figure 9 was obtained with the circuit shown in Figure 6. Note the improvement in linearity of the transfer characteristic. Reduced input impedance does result from this shunt connection. Similar techniques could be used on the OTA output, but then the output signal would be reduced and the correction circuitry further removed from the source of non linearity. It must be emphasized that the input circuitry is differential.

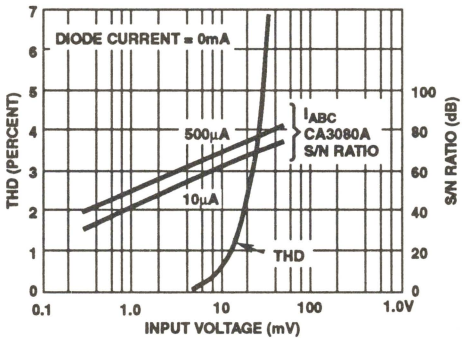


FIGURE 5A.

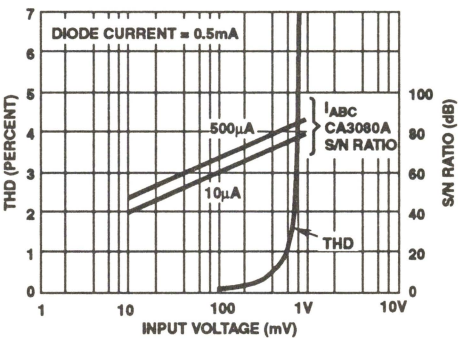


FIGURE 5B.

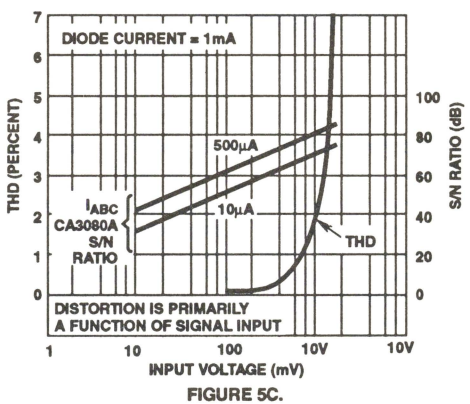
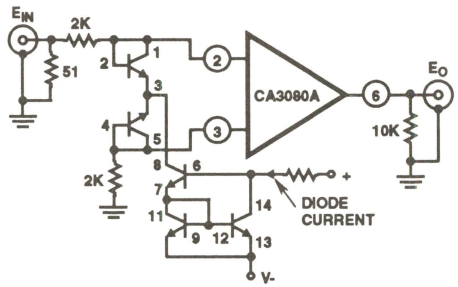


FIGURE 5C.

FIGURE 5. PERFORMANCE CURVES FOR THE CIRCUIT OF FIGURES 4 AND 6



Transistors from CA3046 array
AGC System with extended input range

FIGURE 6. A CIRCUIT SHOWING HOW THE SIGNAL HANDLING CAPABILITY OF THE CIRCUIT OF FIGURE 4 CAN BE EXTENDED THROUGH THE CONNECTION OF DIODES ON THE INPUT

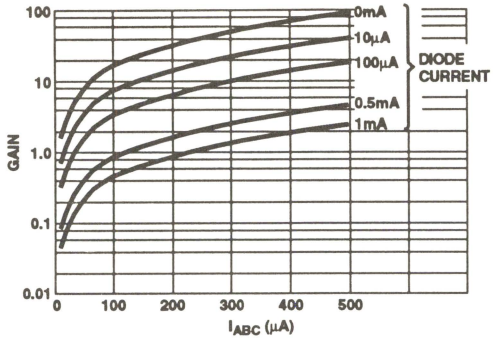
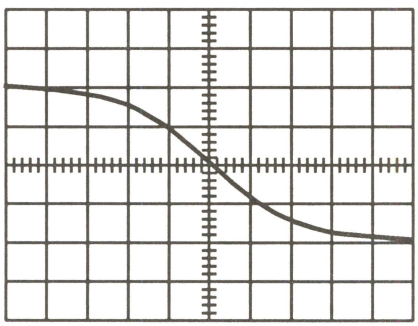
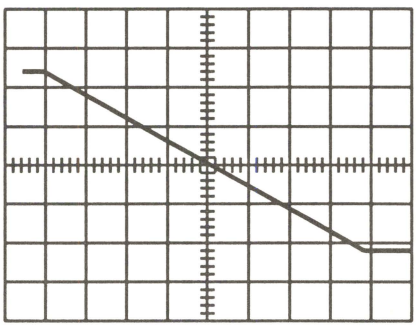


FIGURE 7. TOTAL SYSTEM GAIN AS A FUNCTION OF AMPLIFIER BIAS CURRENT FOR SEVERAL VALUES OF DIODE CURRENT



Horizontal: 25mV/Div. Vertical: 50μA/Div.
I_{ABC} = 100μA

FIGURE 8. OSCILLOSCOPE REPRODUCTION OF THE CA3080 TRANSFER CHARACTERISTIC AS APPLIED TO THE CIRCUIT OF FIGURE 4



Horizontal: 0.5V/Div. Vertical: 50μA/Div.
I_{ABC} = 100μA, Diode Current = 1mA

FIGURE 9. OSCILLOSCOPE REPRODUCTION OF THE CA3080 TRANSFER CHARACTERISTIC AS APPLIED TO THE CIRCUIT OF FIGURE 6

Simplified Differential Input to Single Ended Output Conversion

One of the more exacting configurations for operational amplifiers is the differential to single-ended conversion circuit. Figure 10 shows some of the basic circuits that are usually employed. The ratios of the resistors must be precisely matched to assure the desired common mode rejection. Figure 11 shows another system using the CA3080 to obtain this conversion without the use of precision resistors. Differential input signals must be kept under 126mV for better than 5 percent nonlinearity. The common mode range is that of the CA3080 differential amplifier. In addition, the gain characteristic follows the standard differential amplifier g_m - temperature coefficient of -0.3%/°C. Although the system of Figure 11 does not provide the precise gain control obtained with the standard operational amplifier approach, it does provide a good simple compromise suitable for many differential transducer amplifier applications.

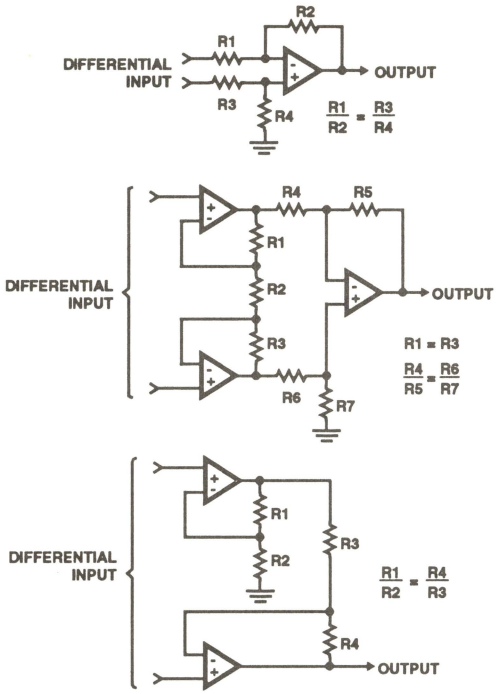
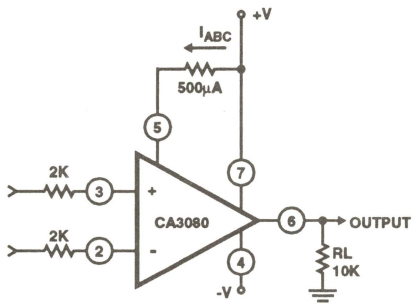


FIGURE 10. SOME TYPICAL DIFFERENTIAL TO SINGLE-ENDED CONVERSION CIRCUITS



NOTES:

1. $A = g_m R_L$
   AT 500μA, I_{ABC}
2. $g_m \approx 10mS$
3. $\therefore$ $A = 10mS \times 10K = 100$

FIGURE 11. A DIFFERENTIAL TO SINGLE ENDED CONVERSION CIRCUIT WITHOUT PRECISION RESISTORS

The CA3094

The CA3094 offers a unique combination of characteristics that suit it ideally to use as a programmable gain block for audio power amplifiers. It is a transconductance amplifier in which gain and open-loop bandwidth can be controlled between wide limits. The device has a large reserve of output-current capability, and breakdown and power dissipation ratings sufficiently high to allow it to drive a complementary pair of transistors. For example, a 12W power amplifier stage (8Ω load) can be driven with peak currents of 35mA (assuming a minimum output transistor beta of 50) and supply voltages of ±18V. In this application, the CA3094A is operated substantially below its supply voltage rating of 44V max. and its dissipation rating of 1.6W max. Also in this application, a high value of open-loop gain suggests the possibility of precise adjustment of frequency response characteristics by adjustment of impedances in the feedback networks.

Implicit Tone Controls

In addition to low distortion, the large amount of loop gain and flexibility of feedback arrangements available when using the CA3094 make it possible to incorporate the tone controls into the feedback network that surrounds the entire amplifier system. Consider the gain requirements of a phonograph playback system that uses a typical high quality magnetic cartridge.[3] A desirable system gain would result in from 2W to 5W of output at a recorded velocity of 1cm/s. Magnetic pickups have outputs typically ranging from 4mV to 10mV at 5cm/s. To get the desired output, the total system needs about 72dB of voltage gain at the reference frequency.

Figure 12 is a block diagram of a system that uses a passive or "losser" type of tone control circuit that is inserted ahead of the gain control. Figure 13 shows a system in which the tone controls are implicit in the feedback circuits of the power amplifier. Both systems assume the same noise input voltage at the equalizer and main-amplifier inputs. The feedback system shows a small improvement (3.8dB) in signal-to-noise ratio at maximum gain but a dramatic improvement (20dB) at the zero gain position. For purposes of comparison, the assumption is made that the tone controls are set "flat" in both cases.

Cost Advantages

In addition to the savings resulting from reduced parts count and circuit size, the use of the CA3094 leads to further savings in the power supply system. Typical values of power supply rejection and common-mode rejection are 90dB and 100dB, respectively. An amplifier with 40dB of gain and 90dB of power supply rejection would require 316mV of power supply ripple to produce 1mV of hum at the output. Thus, no further filtering is required other than that given by the energy storage capacitor at the output of the rectifier system.

Power Amplifier Using the CA3094

A complete power amplifier using the CA3094 and three additional transistors is shown schematically in Figure 14. The amplifier is shown in a single-channel configuration, but power supply values are designed to support a minimum of two channels. The output section comprises Q1 and Q2, complementary epitaxial units connected in the familiar "bootstrap" arrangement. Capacitor C3 provides added base drive for Q1 during positive excursions of the output. The circuit can be operated from a single power supply as well as from a split supply as shown in Figure 15. The changes required for 14.4V operation with a 3.2Ω speaker are also indicated in the diagram.

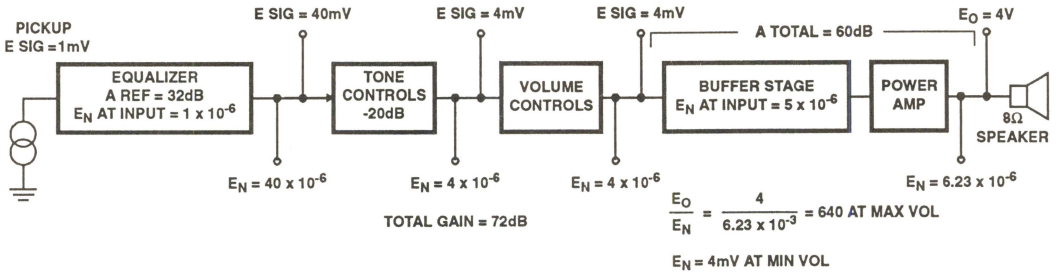


FIGURE 12. BLOCK DIAGRAM OF A SYSTEM USING A "LOSSER" TYPE TONE CONTROL CIRCUIT

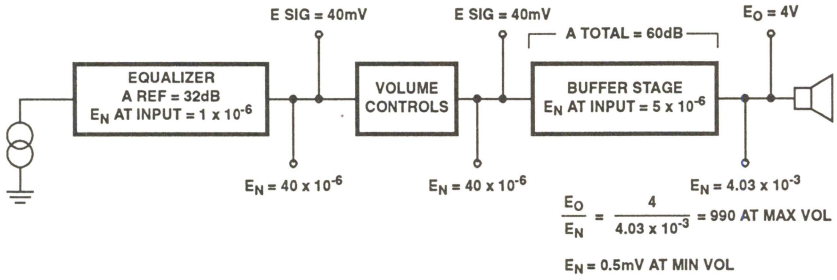


FIGURE 13. A SYSTEM IN WHICH TONE CONTROLS ARE IMPLICIT IN THE FEEDBACK CIRCUIT OF THE POWER AMPLIFIER

The amplifier may also be modified to accept input from ceramic phonograph cartridges. For standard inputs (equalizer preamplifiers, tuners, etc.) C1 is 0.047µF, R1 is 250kΩ, and R2 and C2 are omitted. For ceramic-cartridge inputs, C1 is 0.0047µF, R1 is 2.5MΩ, and the jumper across C2 is removed.

Output Biasing

Instead of the usual two-diode arrangement for establishing idling currents in Q1 and Q2, a "V_{be} Multiplier", transistor Q3, is used. This method of biasing establishes the voltage between the base of Q1 and the base of Q2 at a constant multiple of the base to emitter voltage of a single transistor while maintaining a low variational impedance between its collector and emitter (see Appendix A). If transistor Q3 is mounted in intimate thermal contact with the output units, the operating temperature of the heat sink forces the V_{be} of Q3 up and down inversely with heat-sink temperature. The voltage bias between the bases of Q1 and Q2 varies inversely with heat sink temperature and tends to keep the idling current in Q1 and Q2 constant.

A bias arrangement that can be accomplished at lower cost than those already described replaces the V_{be} multiplier with a 1N5391 diode in series with an 8.2Ω resistor. This arrangement does not provide the degree of bias stability of the V_{be} multiplier, but is adequate for many applications.

Tone-Controls

The tone controls, the essential elements of the feedback system, are located in two sets of parallel paths. The bass network includes R3, R4, R5, C4, and C5. C6 blocks the dc from the feedback network so that the DC gain from input to the feedback takeoff point is unity. The residual DC output voltage at the speaker terminals is then

$$R1\frac{R11 + R12}{R12}$$

where R1 is the source resistance. The input bias current is then

$$\frac{I_{ABC}}{2\beta} = \frac{(V_{CC} + V_{BE})}{2\beta R6}$$

The treble network consists of R7, R8, R9, R10, C7, C8, C9, and C10. Resistors R7 and R9 limit the maximum available cut and boost, respectively. The boost limit is useful in curtailing heating due to finite turn-off time in the output units. The limit is also desirable when there are tape recorders nearby. The cut limit aids the stability of the amplifier by cutting the loop gain at higher frequencies where phase shifts become significant.

In cases in which absolute stability under all load conditions is required, it may be necessary to insert a small inductor in the output lead to isolate the circuit from capacitive loads. A 3µH inductor (1A) in parallel with a 22Ω resistor is adequate. The derivation of circuit constants is shown in Appendix B. Curves of control action versus electrical rotation are also given.

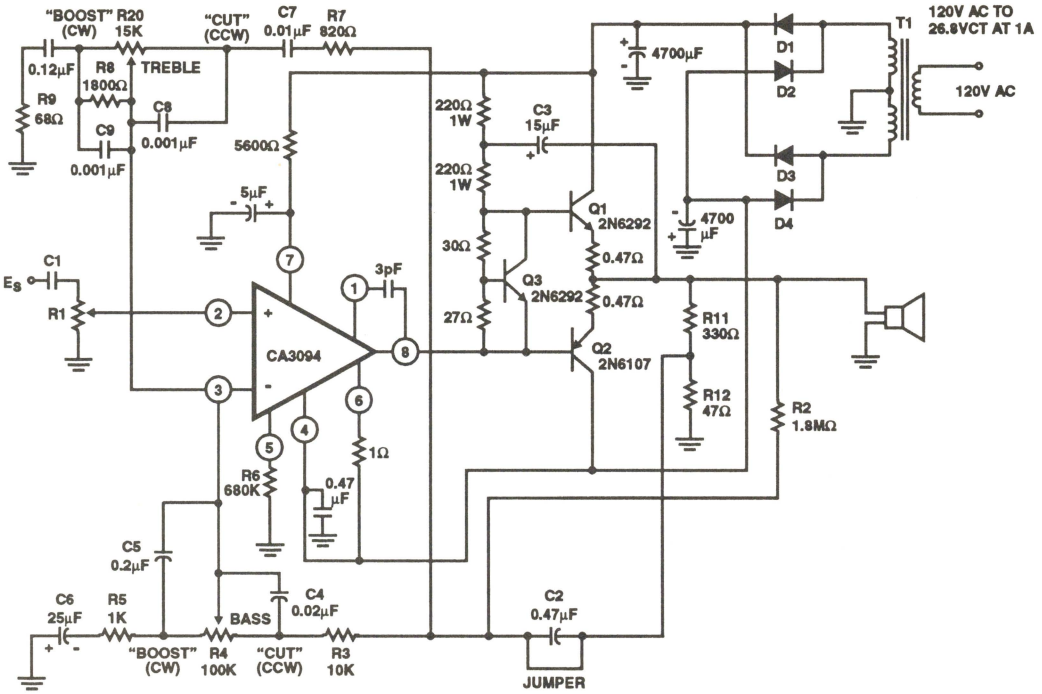


FIGURE 14. A COMPLETE POWER AMPLIFIER USING THE CA3094 AND THREE ADDITIONAL TRANSISTORS

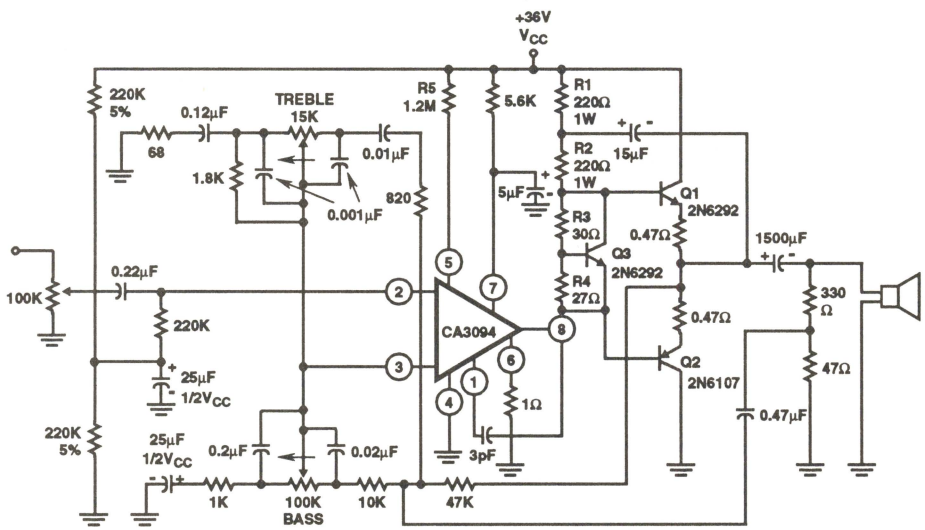


FIGURE 15. A POWER AMPLIFIER OPERATED FROM A SINGLE SUPPLY

Performance

Figure 16 is a plot of the measured response of the complete amplifier at the extremes of tone control rotation. A comparison of Figure 16 with the computed curves of Figure B4 (Appendix B) shows good agreement. The total harmonic distortion of the amplifier with an unregulated power supply is shown in Figure 17; IM distortion is plotted in Figure 18. Hum and noise are typically 700μV at the output, or 83dB down.

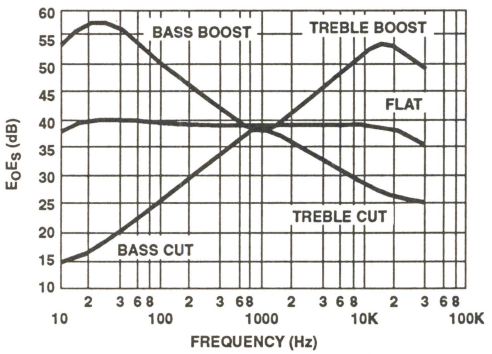


FIGURE 16. THE MEASURED RESPONSE OF THE AMPLIFIER AT EXTREMES OF TONE CONTROL ROTATION

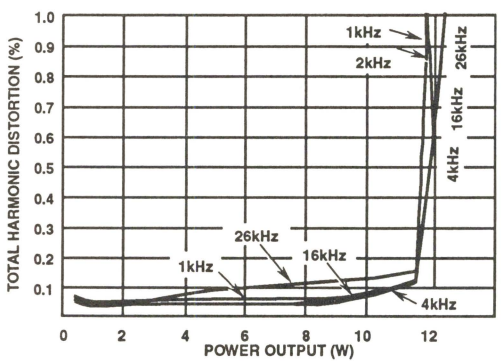


FIGURE 17. TOTAL HARMONIC DISTORTION OF THE AMPLIFIER WITH AN UNREGULATED POWER SUPPLY

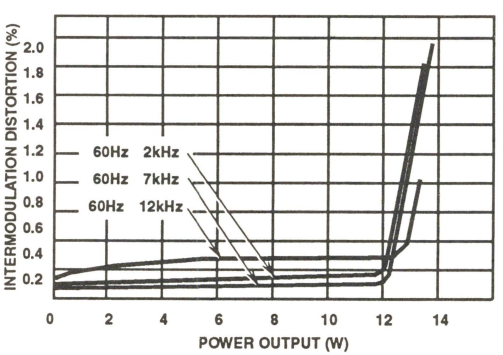


FIGURE 18. IM DISTORTION OF THE AMPLIFIER WITH AN UNREGULATED SUPPLY

Companion RIAA Preamplifier

Many available preamplifiers are capable of providing the drive for the power amplifier of Figure 14. Yet the unique characteristics of the amplifier, its power supply, input impedance, and gain make possible the design of an RIAA preamplifier that can exploit these qualities. Since the input impedance of the amplifier is essentially equal to the value of the volume control resistance (250kΩ), the preamplifier need not have high output current capability. Because the gain of the power amplifier is high (40dB) the preamplifier gain only has to be approximately 30dB at the reference frequency (1kHz) to provide optimum system gain.

Figure 19 shows the schematic diagram of a CA3080 preamplifier. The CA3080, a low cost OTA, provides sufficient open-loop gain for all the bass boost necessary in AIAA compensation. For example, a g_m of 10mS with a load resistance of 250kΩ provides an open-loop gain of 68dB, thus allowing at least 18dB of loop gain at the lowest frequency. The CA3080 can be operated from the same power supply as the main amplifier with only minimal decoupling because of the high power supply rejection inherent in the device circuitry. In addition, the high voltage swing capability at the output enables the CA3080 preamplifier to handle badly over modulated (over-cut) recordings without overloading. The accuracy of equalization is within ±1dB of the RIAA curve, and distortion is virtually immeasurable by classical methods. Overload occurs at an output of 7.5V, which allows for undistorted inputs of up to 186mV (260mV peak).

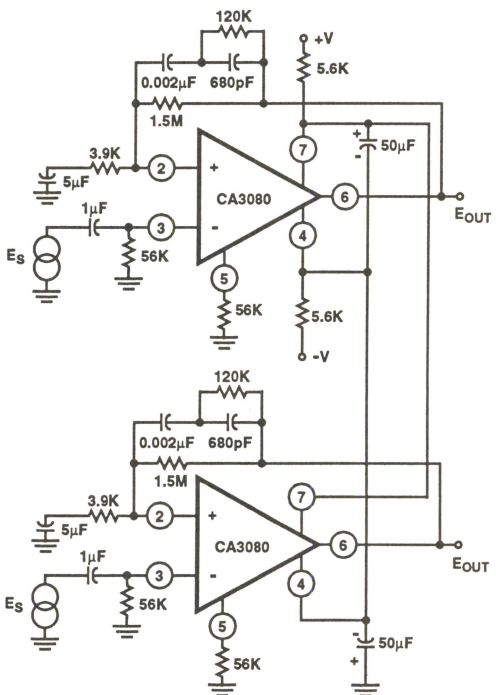


FIGURE 19. A CA3080 PREAMPLIFIER

Appendix A - V_{be} Multiplier

The equivalent circuit for the V_{be} multiplier is shown in Figure A1. The voltage E1 is given by:

$$E1 = \frac{R1I}{\beta+1} + V_{be}\left[1 + \frac{R1}{R2(\beta+1)}\right] \quad (A1)$$

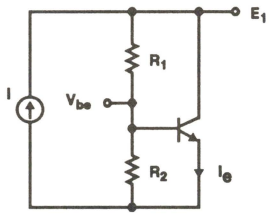


FIGURE A1. EQUIVALENT CIRCUIT FOR THE V_{be} MULTIPLIER

The value of V_{be} is itself dependent on the emitter current of the transistor, which is, in turn, dependent on the input current I since:

$$I_e = I - \frac{V_{be}}{R2} \quad (A2)$$

The derivative of Equation A1 with respect to I yields the incremental impedance of the V_{be} multiplier:

$$\frac{dE1}{dI} = Z = \frac{R1}{\beta+1} + \left[1 + \frac{BR1}{(\beta+1)R2}\right]\left[\frac{K3R2}{R2I_e + K3}\right] \quad (A3)$$

where K3 is a constant of the transistor Q1 and can be found from:

$$V_{be} = K3 \ln I_e - K2 \quad (A4)$$

Equation A4 is but another form of the diode equation:

$$I_e = I_S e^{\left[\frac{qV_{be}}{KT} - 1\right]} \quad (A5)$$

Using the values shown in Figure 14 plus data on the 2N6292 (a typical transistor that could be used in the circuit), the dynamic impedance of the circuit at a total current of 40mA is found to be 4.6Ω. In the actual design of the V_{be} multiplier, the value of IR2 must be greater than V_{be} or the transistor will never become forward biased.

Appendix B - Tone Controls

Figure B1 shows four operational amplifier circuit configurations and the gain expressions for each. The asymptotic low frequency gain is obtained by letting S approach zero in each case:

Bass Boost: $A_{LOW} = \frac{R1+R2+R3}{R2}$

Bass Cut: $A_{LOW} = \frac{R1+R2+R3}{R2+R3}$

Treble Boost: $A_{LOW} = \frac{C1+C4}{C4}$

Treble Cut: $A_{LOW} = \frac{C1+C4}{C4}$

The asymptotic high-frequency gain is obtained by letting S increase without limit in each expression:

Bass Boost: $A_{HIGH} = \frac{R1+R2}{R2}$

Bass Cut: $A_{HIGH} = \frac{R1+R2}{R2}$

Treble Boost: $A_{HIGH} = 1 + C1\left(\frac{C3+C4}{C3C4}\right)$

Treble Cut: $A_{HIGH} = \frac{C2 + \frac{C1C4}{C1+C4}}{C1+C2}$

Note that the expressions for high frequency gain are identical for both bass circuits, while the expressions for low frequency gain are identical for the treble circuits.

Figure B2 shows cut and boost bass and treble controls that have the characteristics of the circuits of Figure B1. The value R_{EFF} in the treble controls of Figure B1 is derived from the parallel combination of R1 and R2 of Figure B2 when the control is rotated to its maximum counterclockwise position. When the control is rotated to its maximum clockwise position, the value is equal to R1.

To compute the circuit constants, it is necessary to decide in advance the amounts of boost and cut desired. The gain expressions of Figure B1 indicate that the slope of the amplitude versus frequency curve in each case will be 6dB per octave (20dB per decade). If the ratios of boosted and cut gain are set at 10, i.e.:

Bass Circuit: $A_{LOW(Boost)} = 10A_{MID}$

$$A_{LOW(Cut)} = \frac{A_{MID}}{10}$$

Treble Circuit: $A_{HIGH(Boost)} = 10A_{MID}$

$$A_{HIGH(Cut)} = \frac{A_{MID}}{10}$$

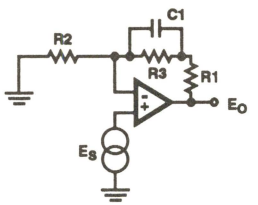
then the following relationships result:

Bass Circuit: $R1 = 10R2$

$R3 = 99R2$

Treble Circuit: $C1 = 10C4$

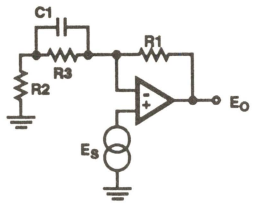
$$C2 = \frac{10C4}{99}$$



$$A = \left(\frac{R1+R2+R3}{R2}\right)\left[\frac{1+SC_1\frac{(R2R3+R1R3)}{(R1+R2+R3)}}{1+SR3C1}\right]$$

$$A_{LOW\ FREQUENCY} = \frac{R1+R2+R3}{R2}$$

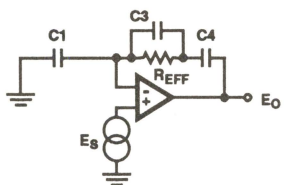
FIGURE B1 (A). BASS BOOST



$$A = \left(\frac{R1+R2+R3}{R2+R3}\right)\left[\frac{1+SC_2\frac{(R2R3+R1R3)}{(R1+R2+R3)}}{1+SC2\left(\frac{R2R3}{R2+R3}\right)}\right]$$

$$A_{LOW\ FREQUENCY} = \frac{R1+R2+R3}{R2+R3}$$

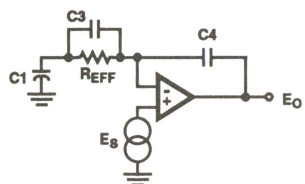
FIGURE B1 (B). BASS CUT



$$A = \left(\frac{C1+C4}{C4}\right)\left[\frac{1+SR_{EFF}\frac{(C1\ C4+C3\ C4+C1\ C3)}{(C1+C4)}}{1+SR_{EFF}C3}\right]$$

$$A_{LOW\ FREQUENCY} = \frac{C1+C4}{C4}$$

FIGURE B1 (C). TREBLE BOOST



$$A = \left(\frac{C1+C4}{C4}\right)\left[\frac{1+SR_{EFF}\frac{(C1\ C4+C2\ C4+C1\ C2)}{(C1+C4)}}{1+SR_{EFF}(C1+C2)}\right]$$

$$A_{LOW\ FREQUENCY} = \frac{C1+C4}{C4}$$

FIGURE B1 (D). TREBLE CUT

FIGURE B1. FOUR OPERATIONAL AMPLIFIER CIRCUIT CONFIGURATIONS AND THE GAIN EXPRESSIONS FOR EACH

The unaffected portion of the gain (A high for the bass control and A low for the treble control) is 11 in each case.

To make the controls work symmetrically, the low and high frequency break points must be equal for both boost and cut.

Thus:

Bass Control: $\frac{C1\ R3\ (R1+R2)}{R1+R2+R3} = \frac{C2\ R2\ R3}{R2+R3}$

and $C1\ R3 = \frac{C2\ R3\ (R1+R2)}{R1+R2+R3}$

since $R3 \cong R2 + R3$, $C2 = 10C1$

Treble Control: $R1\ \frac{(C1\ C4+C3\ C4+C1\ C3)}{C1+C4}$

$$= \frac{R1\ R2}{R1+R2}(C1+C2)$$

and $R2C3 = \left(\frac{R1\ R2}{R1+R2}\right)\frac{(C1\ C4+C2\ C4+C1\ C2)}{(C1+C4)}$

since $C1 \cong 100C2, C2 = C3$ and $C1 = 10C4, R1 = 9R2$

To make the controls work in the circuit of Figure 14, breaks were set at 1000Hz:

for the base control $0.1C1R1 = \frac{1}{2\pi \times 1000}$

and for the treble control $R1C3 = \frac{1}{2\pi \times 1000}$

Response and Control Rotation

In a practical design, it is desirable to make "flat" response correspond to the 50% rotation position of the control, and to have an aural sensation of smooth variation of response on either side of the mechanical center. It is easy to show that the "flat" position of the bass control occurs when the wiper are is advanced to 91% of its total resistance. The amplitude response of the treble control is, however, never completely "flat"; a computer was used to generate response curves as controls were varied.

Figure B3 is a plot of the response with bass and treble tone controls combined at various settings of both controls. The values shown are the practical ones used in the actual design. Figure B4 shows the information of Figure B3 replot-

ted as a function of electrical rotation. The ideal taper for each control would be the complement of the 100Hz plot for the bass control and the 10kHz response for the treble control. The mechanical center should occur at the crossover point in each case.

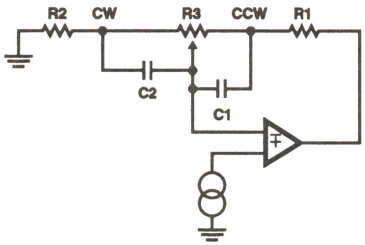


FIGURE B2 (A). BASS CONTROL

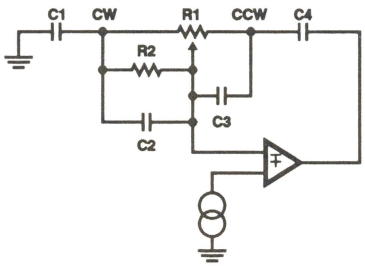


FIGURE B2 (B). TREBLE CONTROL

FIGURE B2. CUT AND BOOST BASS AND TREBLE CONTROLS THAT HAVE THE CHARACTERISTICS OF THE CIRCUITS IN FIGURE B1

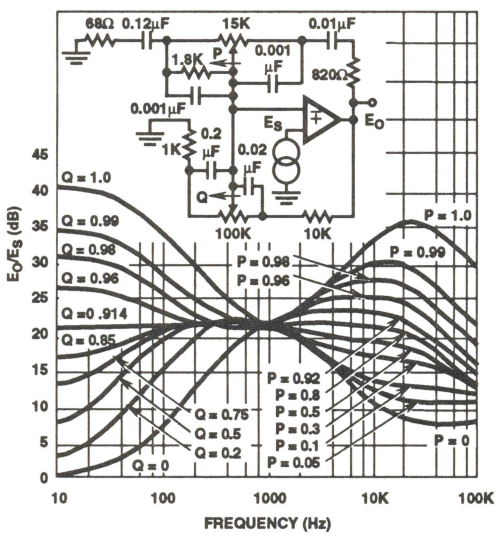


FIGURE B3. A PLOT OF THE RESPONSE OF THE CIRCUIT OF FIGURE 14 WITH BASS AND TREBLE TONE CONTROLS COMBINED AT VARIOUS SETTINGS OF BOTH CONTROLS

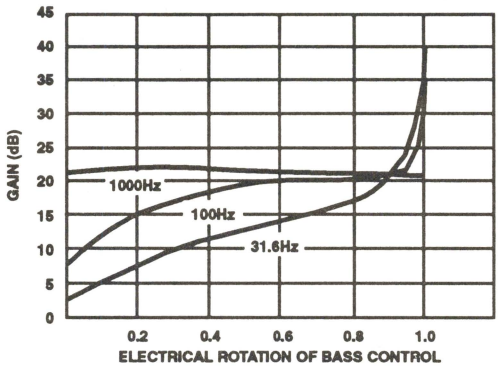


FIGURE B4 (A).

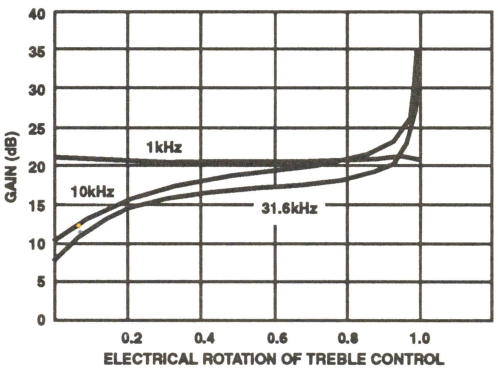


FIGURE B4 (B).

FIGURE B4. THE INFORMATION OF FIGURE B3 PLOTTED AS A FUNCTION OF ELECTRICAL ROTATION

References

[1] AN6668, "Applications of the CA3080 and CA3080A High Performance Operational Transconductance Amplifiers," H. A. Wittlinger, Harris Semiconductor.

[2] "A New Wide-Band Amplifier Technique," B. Gilbert, IEEE Journal of Solid State Circuits, Vol. SC-3, No. 4, December, 1968.

[3] "Trackability," James A. Kogar, Audio, December, 1966.

Harris Semiconductor

APPNOTE

No. AN6157.1 April 1994

Harris Intelligent Power

APPLICATIONS OF THE CA3085 SERIES MONOLITHIC IC VOLTAGE REGULATORS

Authors: A.C.N. Sheng and L.R. Avery

The Harris CA3085, CA3085A, and CA3085B monolithic IC's are positive-voltage regulators capable of providing output currents up to 100mA over the temperature range from -55°C to +125°C. They are supplied in 8 lead TO-5 type packages. The following tabulation shows some key characteristics and salient differences between devices in the CA3085 Series.

TYPE	V_{IN} (V_I) RANGE (V)	V_{OUT} (V_O) RANGE (V)	MAX. I_{OUT} (I_O) (mA)	MAX LOAD REGULATION (% V_O)
CA3085	7.5 - 30	1.8 - 26	12*	0.1
CA3085A	7.5 - 40	1.7 - 36	100	0.15
CA3085B	7.5 - 50	1.7 - 46	100	0.15

*This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

In addition to these differences, the range of some specified performance parameters is more tightly controlled in the CA3085B than in the CA3085A, and more in the CA3085A than in the CA3085.

This note describes the basic circuit of the CA3085 series devices and some typical applications that include a high current regulator, constant current regulations, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting, A circuit in which the CA3085 is used as a general-purpose amplifier is also shown.

Circuit Description

The block diagram of the CA3085 series circuits is shown in Figure 1. Fundamentally, the circuit consists of a frequency compensated error-amplifier which compares an internally generated reference voltage with a sample of the output voltage and controls a series-pass amplifier to regulate the output. The starting circuit assures stable latch-in of the voltage-reference circuitry. The current-limiting portion of the circuit is an optional feature that protects the IC in the event of overload.

Terminal 5 provides a source of stable reference voltage for auxiliary use; a current of about 250μA can be supplied to an external circuit without significantly disturbing reference-voltage stability. If necessary, filtering of the inherent noise of the reference-voltage circuit can be accomplished by connecting a suitable bypass capacitor between terminals 5 and 4.

Terminal 6 (the "inverting input" in accordance with operational-amplifier terminology) is the input through which a sample of the regulated output voltage is applied.

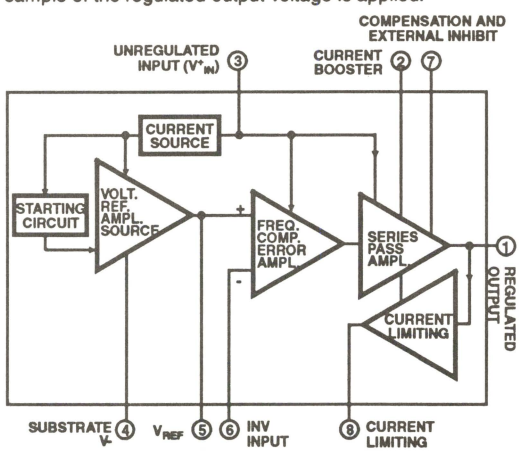


FIGURE 1. BLOCK DIAGRAM OF CA3085 SERIES

The collector of the series-pass output transistor is brought out separately at terminal 2 ("current booster") to provide base drive for an external p-n-p transistor; this approach is one method of regulating currents greater than 100mA.

Because the voltage regulator is essentially an operational amplifier having considerable feedback, frequency compensation is necessary in some circuits to prevent oscillations. Terminal 7 is provided for if external frequency compensation is necessary. Terminal 7 can also be used to "inhibit" (strobe, squelch, pulse, key) the operation of the series-pass amplifier.

Brief Description of CA3085 Schematic Diagram

The schematic diagram of the CA3085 series circuits is shown in Figure 2. The left-hand section includes the starting circuit, the voltage reference circuit, and the constant-current circuit. The center section is basically an elementary operational amplifier which serves as the voltage-error

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amplifier controlling the series-pass. Darlington pair (Q13, Q14) shown in the right-hand section when controlled by an appropriate external sensing network, transistor Q15, serves to provide protective current-limiting characteristics by diverting base drive from the series pass circuit. For operation at the highest current levels, terminals 2 and 3 are tied together to eliminate the voltage drop which would otherwise be developed across resistor R5.

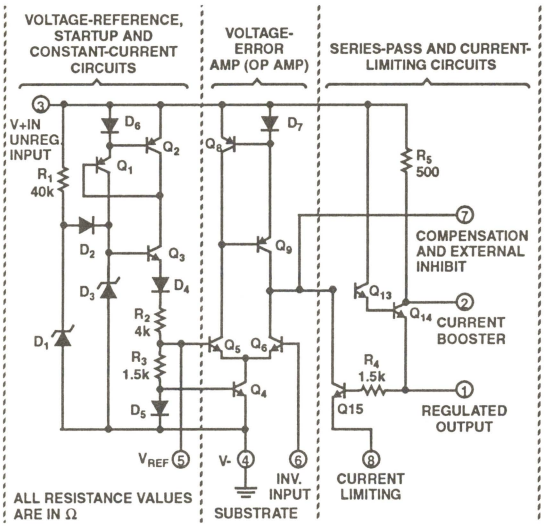


FIGURE 2. SCHEMATIC DIAGRAM OF CA3085 SERIES

Voltage Reference Circuits

The basic voltage referenced element used in the CA3085 is zener diode D3. It provides a nominal reference voltage of 5.5V and exhibits a positive temperature coefficient of approximately 2.5mV/°C. If this reference voltage were used directly in conjunction with the error-amplifier (Q5, Q6, etc.), the IC would exhibit two major undesirable characteristics: (1) its performance with temperature variations would be poor, and (2) its use as a regulator would be restricted to circuits in which the minimum regulated output voltages are in excess of 5.5V. Consequently, it is necessary to provide means of compensating for the positive temperature coefficient of D3 and at the same time provide for obtaining a stable source of lower reference voltage. Both temperature compensation and the reduction of the reference voltage are accomplished by means of the series divider network consisting of the base-emitter junction of Q3, diode D4, resistors R2 and R3, and diode 5.

The voltage developed across D3 drives the divider network and a voltage of approximately 4V is developed between the cathode of D4 and the cathode of D5 (terminal 4). The current through this divider network is held nearly constant with temperature because of the combined temperature coefficients of the zener diode (D3), Q3 base-emitter junction, D4, D5, and the resistors R2 and R3. This constant current through the diode D5 and the resistor R3 produces a voltage drop between terminals 4 and 5 that results in the reference voltage (≈ 1.6V) having an effective temperature coefficient of about 0.0035%/°C.

The reference diode D3 receives a currant of approximately 620μA from a constant-current circuit consisting of Q3 and the current-mirror* D6, Q1, and Q2. Current to start-up the constant-current source initially is provided by auxiliary zener diode D1 and R1. Diode D2 blocks current from the R1-D1 source after latch-in of the constant-current source establishes a stable reference potential, and thereby prevents modulation of the reference voltage by ripple voltage on the unregulated input voltage.

Voltage-Error Amplifier

Transistors Q5 and Q6 comprise the basic differential amplifier that is used as a voltage-error amplifier to compare the stable reference voltage applied at the base of Q5 with a sample of the regulator output voltage applied at terminal 6. The D5-Q4 combination is a current-mirror which maintains essentially constant-current flow to Q5 and Q6 despite variations in the unregulated input voltage. The Q8, Q9, and D7 network provides a "mirrored" active collector load for Q5 and Q6 and also provides a variable single-ended drive to the Q13 and Q14 series-pass transistors in accordance with the difference signal developed between the bases of Q5 and Q6. The open-loop gain of the error-amplifier is greater than 1000.

Series-Pass and Current-Limiting Circuits

In the normal mode of operation, or in the current-boost mode when terminals 2 and 3 are tied together, the Darlington pair Q13-Q14 performs the basic series-pass regulating function between the unregulated input voltage and the regulated output voltage at terminal 1. In the current-limiting mode transistor Q15 provides current-limiting to protect the CA3085 and/or limit the load current. To provide current-limiting protection, a resistor (e.g., 5Ω) is connected between terminals 1 and 8; terminal 8 becomes the source of regulated output voltage. As the voltage drop across this resistor increases, base drive is supplied to transistor Q15 so that it becomes increasingly conductive and diverts base drive from the Q13-Q14 pass transistor to reduce output current accordingly. Resistor R4 is provided to protect Q15 against overdrive by limiting its base current under transient and load-short conditions.

Because the CA3085 regulator is essentially an op-amp having considerable feedback, frequency compensation may be required to prevent oscillations. Stability must also be maintained despite line and load transients, even during operation into reactive loads (e.g., filter capacitors). Provisions are included in the CA3085 so that a small-value capacitor may be connected between terminals 6 and 7 to compensate the regulator, when necessary, by "rolling-off" the amplifier frequency-response. Terminal 7 is also used to externally "inhibit" operation of the CA3085 by diverting base current supplied to Q13-Q14, thereby permitting the use of keying, strobing, programming, and/or auxiliary overload-protection circuits.

Applications

A Simple Voltage Regulator

Figure 3 shows the schematic diagram of a simple regulated power supply using the CA3085. The ac supply voltage is stepped down by T1, full-wave rectified by the diode bridge circuit, and smoothed by the large electrolytic capacitor C1 to provide unregulated dc to the CA3085 regulator circuit. Frequency compensation of the error-amplifier is provided by capacitor C2. Capacitor C3 bypasses residual noise in the reference-voltage source, and thus decreases the incremental noise-voltage in the regulator circuit output.

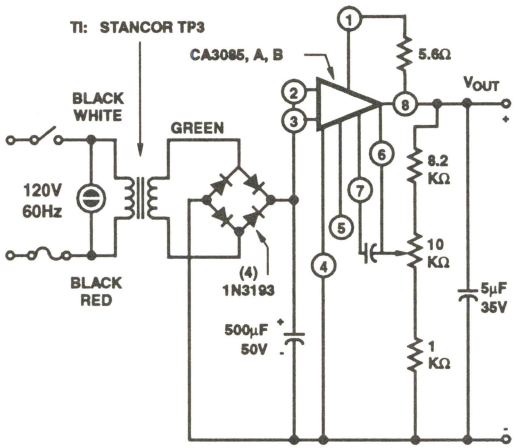


FIGURE 3. BASIC POWER SUPPLY

Because the open-loop gain of the error-amplifier is very high (greater than 1000), the output voltage may be directly calculated from the following expression:

$$V_O = \frac{(R2 + R1)}{R1} V_{REF} \qquad \text{(EQ. 1)}$$

In the circuit shown in Figure 3, the output voltage can be adjusted from 1.8V to 20V by varying R2. The maximum output current is determined by R_{SC}; load-regulation characteristics for various values of R_{SC} are shown in Figure 4.

When this circuit is used to provide high output currents at low output voltages, care must be exercised to avoid excessive IC dissipation. In the circuit of Figure 3, this dissipation control can be accomplished by increasing the primary-to-secondary transformer ratio (a reduction in V_I) or by using a dropping resistor between the rectifier and the CA3085 regulator. Figure 5 gives data on dissipation limitation (V_I - V_O vs. I_O) for CA3085 series circuits. The short-circuit current is determined as follows:

$$I_{SC} = \frac{V_{BE}}{R_{SC}} \approx \frac{0.7}{R_{SC}} \text{ amperes} \qquad \text{(EQ. 2)}$$

The line-and-load regulation characteristics for the circuit shown in Figure 3 are approximately 0.05 percent of the output voltage.

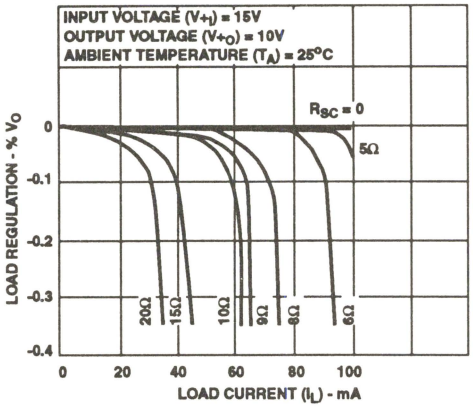


FIGURE 4. LOAD REGULATION CHARACTERISTICS FOR CIRCUIT OF FIGURE 3

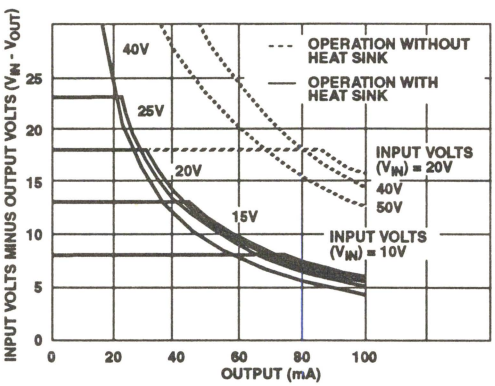


FIGURE 5. DISSIPATION LIMITATION (V_I - V_O vs I_O) FOR CA3085 SERIES CIRCUITS

High-Current Voltage Regulator

When regulated voltages at currents greater than 100mA are required, the CA3085 can be used in conjunction with an external n-p-n pass transistor as shown in the circuits of Figure 6. In these circuits the output current available from the regulator is increased in accordance with the h_{FE} of the external n-p-n pass transistor. Output currents up to 8A can be regulated with these circuits. A Darlington power transistor can be substituted for the 2N5497 transistor when currents greater than 8A are to be regulated.

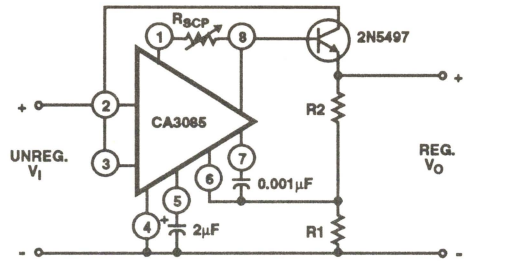


FIGURE 6A. WITH SIMPLIFIED SHORT-CIRCUIT PROTECTION

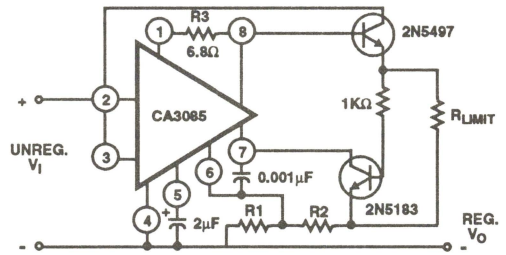


FIGURE 6B. WITH AUXILLIARY SHORT-CIRCUIT PROTECTION

FIGURE 6. HIGH-CURRENT VOLTAGE REGULATOR USING n-p-n PASS TRANSISTOR

A simplified method of short circuit protection is used in connection with the circuit of Figure 6A. The variable resistor R_{SCP} serves two purposes: 1) it can be adjusted to optimize the base drive requirements (h_{FE}) of the particular 2N5497 transistor being used, and 2) in the event of a short circuit in the regulated output voltage the base drive current in the 2N5497 will increase, thereby increasing the voltage drop across R_{SCP}. As this voltage drop increases the short circuit protection system within the CA3085 correspondingly reduces the output current available at terminal 8, as described previously. It should be noted that the degree of short circuit protection depends on the value of R_{SCP}, i.e., design compromise is required in choosing the value of R_{SCP} to provide the desired base drive for the 2N5497 while maintaining the desired short circuit protection. Figure 6B shows an alternate circuit in which an additional transistor (2N2102) and two resistors have been added as an auxiliary short circuit protection feature. Resistor R3 is used to establish the desired base drive for the 2N5497, as described above. Resistor R_{LIMIT} now controls the short circuit output current because, in the event of a short circuit, the voltage drop developed across its terminals increases sufficiently to increase the base drive to the 2N2102 transistor. This increase in base drive results in reduced output from the CA3085 because collector current flow in the 2N2102 diverts base drive from the Darlington output stage of the CA3085 (see Figure 2) through terminal 7. The load regulation of this circuit is typically 0.025 per cent with 0 to 3A load-current variation; line regulation is typically 0.025%/V change in input voltage.

Voltage Regulator with Low V_I - V_O Difference

In the voltage regulators described in the previous section, it is necessary to maintain a minimum difference of about 4V between the input and output voltages. In some applications this requirement is prohibitive. The circuit shown in Figure 7 can deliver an output current in the order of 2A with a V_I - V_O difference of only one volt.

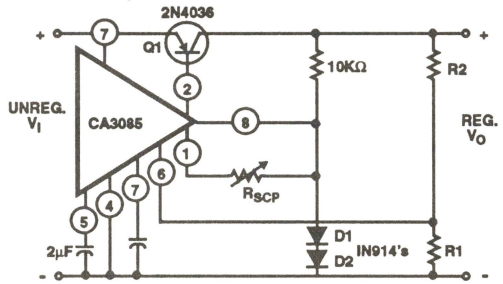


FIGURE 7. VOLTAGE REGULATOR FOR LOW V_I - V_O DIFFERENCE

It employs a single external p-n-p transistor having its base and emitter connected to terminals 2 and 3, respectively, of the CA3085. In this circuit, the emitter of the output transistor (Q14 in Figure 2) in the CA3085 is returned to the negative supply rail through an external resistor (R_{SCP}) and two series-connected diodes (D1, D2). These forward biased diodes maintain Q6 in the CA3085 within linear-mode operation. The choice of resistors R1 and R2 is made in accordance with Equation 1. Adequate frequency compensation for this circuit is provided by the 0.01µF capacitor connected between terminal 7 of the CA3085 and the negative supply rail.

Figure 8 which shows the output impedance of the circuit of Figure 7 as a function of frequency, illustrates the excellent ripple-rejection characteristics of this circuit at frequencies below 1kHz. Lower output impedances at the higher frequencies can be provided by connecting an appropriate capacitor across the output voltage terminals. The addition of a capacitor will, however, degrade the ability of the system to react to transient-load conditions.

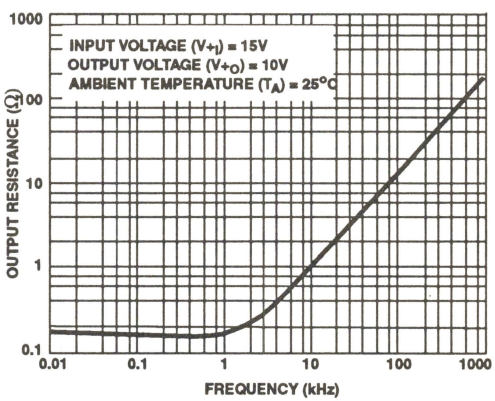


FIGURE 8. OUTPUT RESISTANCE vs FREQUENCY FOR CIRCUIT OF FIGURE 7

High Voltage Regulator

Figure 9 shows a circuit that uses the CA3085 as a voltage reference and regulator control device for high-voltage power supplies in which the voltages to be regulated are well above the input-voltage ratings of the CA3085 series circuits. The external transistors Q1 and Q2 require voltage ratings in excess of the maximum input voltage to be regulated. Series-pass transistor Q2 is controlled by the collector current of Q1, which in turn is controlled by the normally regulated current output supplied by the CA3085. The input voltage for the CA3085 regulator at terminal 3 is supplied through dropping resistor R3 and the clamping zener diode D1. The values for resistor R1 and R2 are determined in accordance with Equation 1.

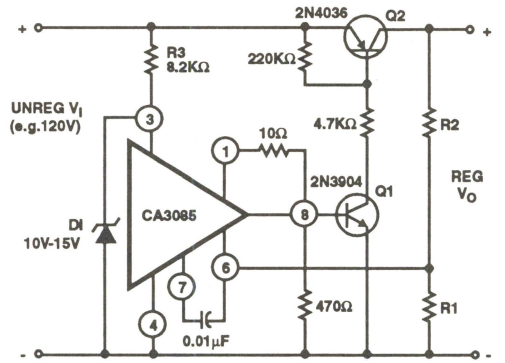


FIGURE 9. HIGH VOLTAGE REGULATOR

Negative Voltage Regulator

The CA3085 is used as a negative-supply voltage regulator in the circuit shown in Figure 10. Transistor Q3 is the series pass transistor. It should be noted that the CA3085 is effectively connected across the load side of the regulated system. Diode D1 is used initially in a "circuit-starter" function; transistor Q2 "latches" D1 out of its starter-circuit function so that the CA3085 can assume its role in controlling the pass transistor Q3 by means of Q1.

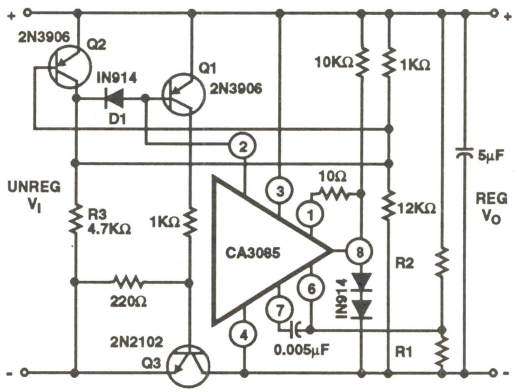


FIGURE 10. NEGATIVE VOLTAGE REGULATOR

Operation of the circuit is as follows: current through R3 and D1 provides base drive for Q1, which in turn provides base drive for the pass-transistor Q3. By this means operating potential for the CA3085 is developed between the collector of Q3 (terminal 4 of the CA3085) and the positive supply-rail (terminal 3 of the CA3085). When the output voltage has risen sufficiently to maintain operation of the CA3085 (approx. 7.5V), transistor Q2 is driven into conduction by the base drive supplied from the 1KΩ-12KΩ voltage divider. As Q2 becomes conductive, it diverts the base drive being supplied to Q1 through the R3-D1 path, and diode D1 ceases to conduct. Under these conditions, base-current drive to Q1 through terminal 2 of the CA3085 regulates the base drive to Q3. Values of R1 and R2 are determined in accordance with Equation 1.

The circuit shown in Figure 11 is similar to that of Figure 10, except for the addition of a constant-current limiting circuit consisting of transistor Q4, a 1KΩ resistor, and resistor R_{SCP}. When the load current increases above a particular design value, the corresponding increase in the voltage drop across resistor R_{SCP} provides additional base drive to transistor Q4. Thus, as transistor Q4 becomes increasingly conductive, its collector current diverts sufficient base drive from Q3 to limit the current in the pass transistor feeding the regulated load. With the types of transistors shown in Figures 10 and 11, maximum currents in the order of 5A can be regulated.

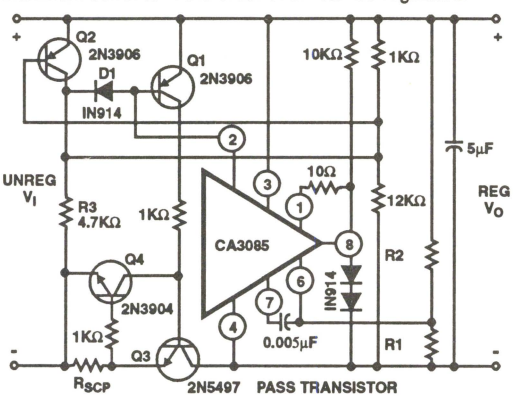


FIGURE 11. NEGATIVE VOLTAGE REGULATOR WITH CONSTANT CURRENT LIMITING CIRCUIT

High-Output-Current Voltage Regulator With "Foldback" Current-Limiting (Also known as "Switch-Back" Current-Limiting)

In high-current voltage regulators employing constant current limiting (e.g., Figures 6 and 7), it is possible to develop excessive dissipation in the series-pass transistor when a short circuit develops across the output terminals. This situation can be avoided by the use of the "foldback" current-limiting circuitry as shown in Figure 12. In this circuit, terminal 8 of the CA3085 senses the output voltage, and terminal 1 is tied to a tap on a voltage-divider network connected between the emitter of the pass-transistor (Q3) and ground. The current-foldback trip-point is established by the value of resistor R_{SC}.

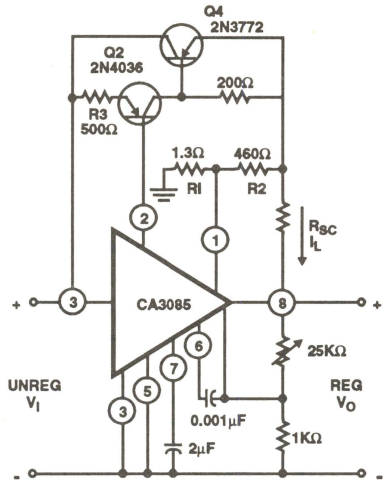


FIGURE 12. HIGH OUTPUT CURRENT VOLTAGE REGULATOR WITH "FOLDBACK" CURRENT LIMITING

The protective tripping action is accomplished by forward-biasing Q15 in the CA3085 (see Figure 2). Conditions for tripping circuit operation are defined by the following expressions:

$$V_{BE(Q15)} = \text{(voltage at terminal 1) - (output voltage)}$$

$$= \left[(V_O + I_L R_{SC}) \frac{R1}{R1 + R2} \right] - V_O \qquad \text{(EQ. 3)}$$

$$\text{If } \frac{R1}{R1 + R2} = K, \text{ then}$$

$$V_{SE(Q15)} = (V_O + I_L R_{SC}) K - V_O = KV_O + KI_L R_{SC} - V_O$$

and therefore

$$R_{SC} = \frac{V_O + V_{BE(Q15)} - KV_O}{KI_L} \qquad \text{(EQ. 4)}$$

Under load short-circuit conditions, terminal 8 is forced to ground potential and current flows from the emitter of Q14 in the CA3085, establishing terminal 1 at one V_{SE}-drop [≡0.7V] above ground and Q15 in a partially conducting state. The current through Q14 necessary to establish this one V_{SE} condition is the sum of currents flowing to ground through R1 and [R2 + R_{SC}]. Normally R_{SC} is much smaller than R2 and can be ignored; therefore, the equivalent resistance R_{eq} to ground is the parallel combination of R1 and R2.

The Q14 current is then given by:

$$I_{Q14} = \frac{V_{BE(Q15)}}{R_{EQ}} = \frac{V_{BE(Q15)}}{\frac{R1R2}{R1 + R2}} = \frac{0.7\,[1.3 + 0.46]}{1.3 \times 0.46} \quad 2.06\text{mA} \qquad \text{(EQ. 5)}$$

This current provides a voltage between terminals 2 and 3 as follows: Ω

$$V_{2\text{-}3} = I_{Q14} \times 250\Omega = 2.06 \times 10^{-3} \times 250 = 0.515\text{V} \qquad \text{(EQ. 6)}$$

The effective resistance between terminals 2 and 3 is 250Ω because the external 500Ω resistor R3 is in parallel with the internal 500Ω resistor R5. It should be understood that the $V_{2\text{-}3}$ potential of 0.515V is insufficient to maintain the external p-n-p transistor Q2 in conduction, and, therefore, Q3 has no base drive. Thus the output current is reduced to zero by the protective circuitry. Figure 13 shows the foldback characteristic typical of the circuit of Figure 12.

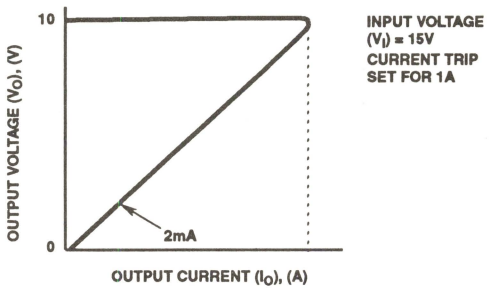


FIGURE 13. TYPICAL "FOLDBACK" CURRENT-LIMITING CHARACTERISTIC FOR CIRCUIT OF FIGURE 12

An alternative method of providing "foldback" current-limiting is shown in Figure 14. The operation of this circuit is similar to that of Figure 12 except that the foldback-control transistor Q2 is external to the CA3085 to permit added flexibility in protection-circuit design.

Under low load conditions Q2 is effectively reverse-biased by a small amount, depending upon the values of R3 and R4. As the small amount, depending upon the values of R3 and R4. As the load current increases the voltage drop across R_{trip} increases, thereby raising the voltage at the base of Q1, and Q2 starts to conduct. As Q2 becomes increasingly conductive it diverts base current from transistors Q13 and Q14 in the CA3085, and thus reduces base drive to the external pass-transistor Q1 with a consequent reduction in the output voltage. The point at which current-limiting occurs, I_{tnp}, is calculated as follows:

$V_{BE(Q1)}$ = voltage at terminal 8 - V_O (assuming a low value for R_{TRIP})

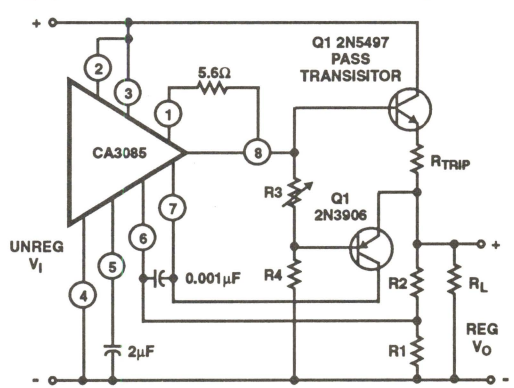


FIGURE 14. HIGH-OUTPUT-CURRENT VOLTAGE REGULATOR USING AUXILIARY TRANSISTOR TO PROVIDE "FOLDBACK" CURRENT LIMITING

$$V_{BE(Q2)} = \text{voltage at terminal 8} \left(\frac{R4}{R3 + R4} \right) - V_O$$

$$= \left[V_O + I_L R_{TRIP} + V_{BE(Q1)} \right] \left[\frac{R4}{R3 + R4} \right] - V_O$$

$$\text{if } K = \frac{R4}{R3 + R4}, \text{ then the trip current is given by:}$$

$$I_{trip} = \frac{V_{BE(Q2)} - K[V_O + V_{BE(Q1)}] + V_O}{KR_{TRIP}} \qquad \text{(EQ. 7)}$$

In the circuit in Figure 12 the load current goes to zero when a short circuit occurs. In the circuit of Figure 14 the load current is significantly reduced but does not go to zero. The value for I_{SC} is computed as follows:

$$I_{SC} = \frac{V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)} \right] R1 = V_{BE(Q1)} + I_{SC}R_{TRIP}}{R_{TRIP}}$$

$$\frac{V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)} \right] R1 = V_{BE(Q1)}}{R_{TRIP}} \qquad \text{(EQ. 8)}$$

Figure 15 shows that the transfer characteristic of the load current is essentially linear between the "trip-point" and the "short-circuit" point.

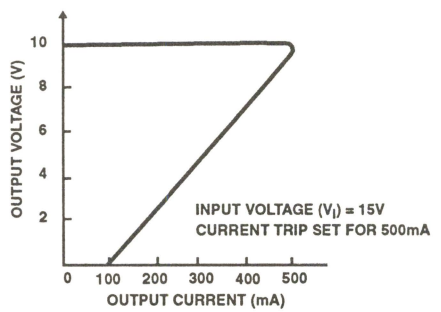


FIGURE 15. TYPICAL FOLDBACK CURRENT-LIMITING CHARACTERISTIC FOR CIRCUIT OF FIGURE 14

High-Voltage Regulator Employing Current "Snap-Back" Protection

In high-voltage regulators (e.g., see Figure 9), "foldback" current-limiting cannot be used safely because the high voltage across the pass transistor can cause second breakdown despite the reduction in current flow. To adequately protect the pass transistor in this type of high-voltage regulator, the so-called "snap-back" method of current limiting can be employed to reduce the current to zero in a few microseconds, and thus prevent second-breakdown destruction of the device.

The circuit diagram of a high-voltage regulator employing current "snap-back" protection is shown in Figure 16. The basic regulator circuit is similar to that shown in Figure 9.

The additional circuitry in the circuit of Figure 16 quickly interrupts base drive to the pass transistor in event of load fault. The point of current-trip is established as follows:

$$I_{trip} = \frac{V_{BE(Q1)}}{R_{SC}} \qquad \text{(EQ. 9)}$$

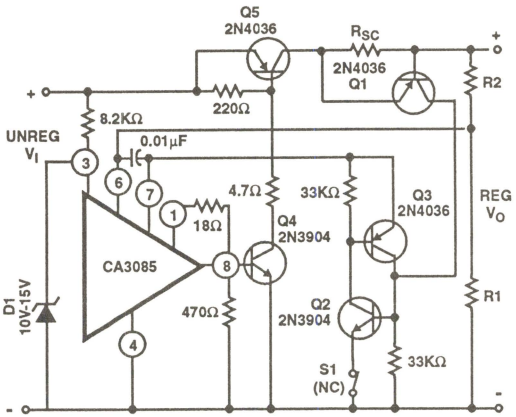


FIGURE 16. HIGH-VOLTAGE REGULATOR INCORPORATING CURRENT "SNAP-BACK" PROTECTION

Thus, when a sufficient voltage drop is developed across R_{SC}, transistor Q1 becomes conductive and current flows into the base of Q2 so that it also becomes conductive. Transistor Q3, in turn, is driven into conduction, thereby latching the Q2-Q3 combination (basic SCR action) so that it diverts (through terminal 7) base drive from the output stage (Q13, Q14) in the CA3085. By this means, base drive is diverted from Q4 and the pass transistor Q5. To restore regulator operation, normally closed switch S1 is momentarily opened and unlatches Q2-Q3.

Switching Regulator

When large input-to-output voltage differences are necessary, the regulators described above are inefficient because they dissipate significant power in the series-pass transistor. Under these conditions, high-efficiency operation can be achieved by using a switching-type regulator of the generic type shown in Figure 17A. Transistor Q1 acts as a keyed switch and operates in either a saturated or cut-off condition to minimize dissipation. When transistor Q1 is conductive, diode D1 is reversed-biased and current in the inductance L1 increases in accordance with the following relationship:

$$i_L = \frac{1}{L} \int_{t_0}^{t_1} V dt \qquad \text{(EQ. 10)}$$

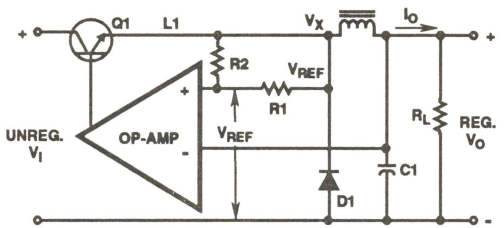


FIGURE 17A. SELF-OSCILLATING SWITCHING REGULATOR

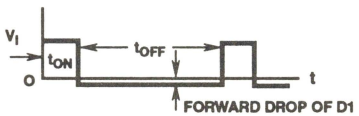


FIGURE 17B. VOLTAGE AT POINT V_X

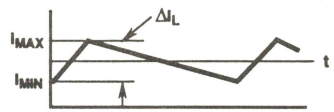


FIGURE 17C. INDUCTOR CURRENT I_{LI}

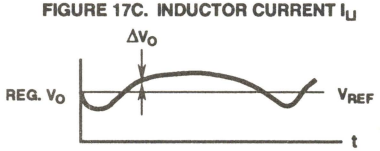


FIGURE 17D. OUTPUT VOLTAGE

FIGURE 17. SWITCHING REGULATOR AND ASSOCIATED WAVEFORMS

Where V is the voltage across the inductance L1. The current through the inductance charges the capacitor C1 and supplies current to the load. The output voltage rises until it slightly exceeds the reference voltage V_{ref}. At this point the op-amp removes base drive to Q1 and the unregulated input voltage V1 is "switched off". The energy stored in the inductor L1 now causes the voltage at V_x to swing in the negative direction and current flows through diode D1, while continuing to supply current into the load R_L. As the current in the inductor falls below the load current, the capacitor C1 begins to discharge and V_O decreases. When V_O falls slightly below the value of V_{REF}, the op-amp turns on Q1 and the cycle is repeated. It should be apparent that the output voltage oscillates about V_{REF} with an amplitude determined by R1 and R2. Actually, the value of V_{REF} varies from being slightly more positive than V_{REF} when Q1 is conducting, to being slightly more negative than V_{REF} when D1 is conducting. The voltage and current waveforms are shown in Figure 17B, C, and D.

Design Example

The following specifications are used in decomputations for a switching regulator:

V_I = 30V, V_O = 5V, I_O = 500mA,
switching frequency = 20kHz,
output ripple = 100mV

If it is assumed that transistor Q1 is in steady-state saturated operation with a low voltage-drop, the current in the inductor is given by Eq.10, as follows:

$$i_L = \frac{1}{L}\int_{t_0}^{t1} V dt = \left(\frac{V_I - V_O}{L_1}\right) t_{ON} \qquad \text{(EQ. 11)}$$

When transistor Q1 is off, the current in the inductor is given by:

$$i_L \cong \frac{(V_O + V_{D1})\, t_{OFF}}{L1} \qquad \text{(EQ. 12)}$$

From Equation 11,

$$L_1 = \frac{(V_I - V_O)}{i_L} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \qquad \text{(EQ. 13)}$$

If i_{max} is 1.3 I_L, then during t_{on} the current in the inductor (i_L) will be 0.5A x 1.3 = 0.65A; therefore, Δi_L = 0.15A.

Substitution in Equation 13 yields

$$L_1 = \frac{(30 - 5)}{0.15} \cdot \frac{1}{(20 \times 10^3)} \cdot \frac{5}{30} \cdot \quad 1.4\text{mH} \qquad \text{(EQ. 14)}$$

Current discharge from the capacitor C1 is given by:

$$i_C = C\frac{dv}{dt}$$

$$\text{Thus, } \Delta i_C = C\frac{\Delta v}{\Delta t} \quad \text{or } C = \frac{\Delta i_C\, \Delta t}{\Delta v}$$

Since $i_C = i_L$ and $\Delta t = t_{OFF}$, then

$$C = \frac{\Delta i_L\, t_{OFF}}{\Delta v} \qquad \text{(EQ. 15)}$$

Substitution for the value of iL from Equation 13 yields

$$C = \frac{\left(\frac{V_I - V_O}{L1}\right) \cdot \frac{1}{f} \cdot \left(\frac{V_O}{V_I}\right) \cdot t_{OFF}}{\Delta v} \qquad \text{(EQ. 16)}$$

The total period $T = t_{OFF} + t_{ON}$, and $T = \frac{1}{f}$ Therefore,

$$t_{OFF} = \frac{1}{f} - t_{ON} \qquad \text{(EQ. 17)}$$

For optimum efficiency t_{on} should be

$$\cong \left(\frac{V_O}{V_I}\right) T \cong \left(\frac{V_O}{V_I}\right) \frac{1}{f} \qquad \text{(EQ. 18)}$$

Substitution for t_{on} in Equation 18 yields

$$t_{OFF} = \frac{1}{f} - \left(\frac{V_O}{V_I}\right)\frac{1}{f} = \frac{1}{f}\left(1 - \frac{V_O}{V_I}\right) \qquad \text{(EQ. 19)}$$

Substitution for t_{on} in Equation 16 yields

$$C = \frac{\frac{(V_I - V_O)}{L_1} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \cdot \frac{1}{f} \cdot \left(1 - \frac{V_O}{V_I}\right)}{\Delta v} \qquad \text{(EQ. 20)}$$

Substitution of numerical values in Equation 20 produces the following value for C:

$$C = \frac{\frac{30 - 5}{1.4 \times 10^{-3}} \cdot \frac{1}{20 \times 10^{3}} \cdot \frac{5}{30} \cdot \frac{1}{20 \times 10^{3}} \cdot \left(1 - \frac{5}{30}\right)}{10^{-1}} = 63\mu F$$

A switching-regulator circuit using the CA3085 is shown in Figure 18. The values of L and C (1.5mH and 50mF, respectively) are commercially available components having values approximately equal to the computed values in the previous design example.

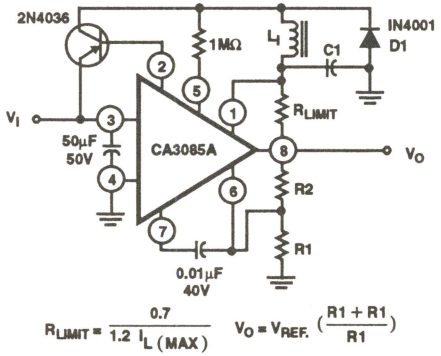


FIGURE 18. TYPICAL SWITCHING REGULATOR CIRCUIT

Current Regulators

The CA3085 series of voltage regulators can be used to provide a constant source or sink current. A regulated-current supply capable of delivering up to 100mA is shown in Figure 19A . The regulated load current is controlled by R1 because the current flowing through this resistor must establish a voltage difference between terminals 6 and 4 that is equal to the internal reference voltage developed between terminals 5 and 4.

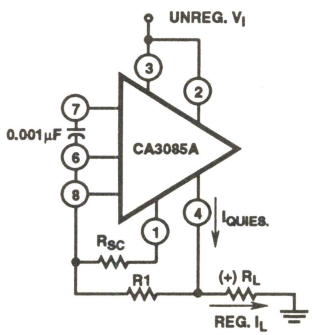


FIGURE 19A. CURRENT REGULATOR

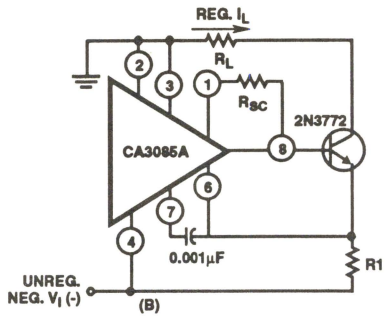


FIGURE 19B. HIGH-CURRENT REGULATOR

FIGURE 19. CONSTANT CURRENT REGULATORS

The actual regulated current, reg I_L is the sum of the quiescent regulator current and the current through R1, i.e.,

$$\text{reg } I_L = I_{QUIESCENT} + I_{R1}$$

Figure 19B shows a high-current regulator using the CA3085 in conjunction with an external n-p-n transistor to regulate currents up to 3A. In this circuit the quiescent regulator current does not flow through the load and the output current can be directly programmed by R1, i.e.,

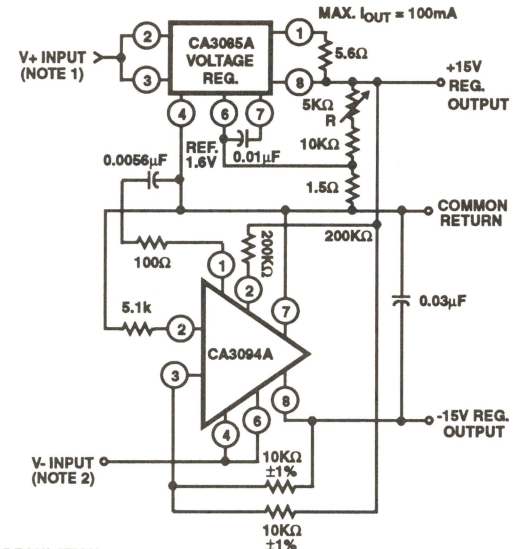
$$\text{Reg } I_L = \frac{V_{REF}}{R1}$$

With this regulator currents between 1mA and 3A can be programmed directly. At currents below 1mA inaccuracies may occur as a result of leakage in the external transistor.

A Dual-Tracking Voltage Regulator

A dual-tracking voltage regulator using a CA3085 and a CA3094A is shown in Figure 20. The CA3094A is basically an op-amp capable of supplying 100mA of output current. Specifications for the CA3094A appear in datasheet file number 598.

The positive output voltage is regulated by a CA3085 operating in a configuration essentially similar to that described in connection with Figure 3. Resistor R is used as a vernier adjustment of output voltage. The negative output voltage is regulated by the CA3094A, which is "slaved" to the regulated positive voltage supplied by the CA3085. It should be noted that the non-inverting input of the CA3094A and the negative supply terminal of the CA3085 are connected to a common ground reference. The "slaving" potential for the CA3094A is derived from an accurate 1:1 voltage-divider network comprised of two 10KΩ resistors connected between the +15V and the -15V output terminals. The junction of these two resistors is connected to the inverting input of the CA3094A. The voltage at this junction is compared with the voltage at the non-inverting input, and the CA3094A then automatically adjusts the output current at the negative terminal to maintain a negative regulated output voltage essentially equal to the regulated positive output voltage. Typical performance data for this circuit are shown in Figure 20.



REGULATION:

$$\text{MAX. LINE} = \frac{\Delta V_{OUT}}{\left[V_{OUT}\,(\text{INITIAL})\right]\Delta V_{IN}} \times 100 = 0.075\%/V$$

$$\text{MAX. LOAD} = \frac{\Delta V_{OUT}}{\left[V_{OUT}\,(\text{INITIAL})\right]\Delta V_{IN}} \times 100 = 0.075\%/V_{OUT} \quad (I_L \text{ FROM } 1\mu A \text{ TO } 50mA)$$

NOTE:

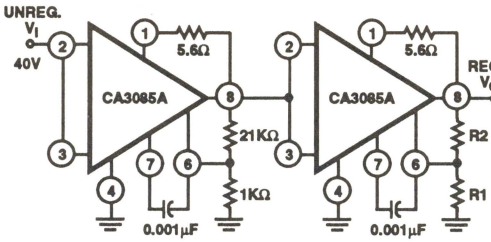
1. V+ Input Range = 19V to 30V for 15V Output
2. V- Input Range = -16V to -30V for -15V Output

FIGURE 20. DUAL-VOLTAGE TRACKING REGULATOR

The basic circuit of Figure 20 can be modified to regulate dissimilar positive and negative voltages (e.g., +15V, -5V) by appropriate selection of resistor ratios in the voltage-divider network discussed previously. As an example, to provide tracking of the -15V and -5V regulated voltages with the circuit of Figure 20, it is only necessary to replace the 10KΩ resistor connected between terminals 3 and 8 of the CA3094A with a 3.3KΩ resistor.

Regulators With High Ripple Rejection

When the reference-voltage source in the CA3085 is adequately filtered, the typical ripple rejection provided by the circuit is 56dB. It is possible to achieve higher ripple-rejection performance by cascading two stages of the CA3085, as shown in Figure 21. The voltage-regulator circuit in Figure 21A provides 90dB of ripple rejection. The output voltage is adjustable over the range from 1.8V to 30V by appropriate adjustment of resistors R1 and R2. Higher regulated output currents up to 1A can be obtained with this circuit by adding an external n-p-n transistor as shown in Figure 21B.



90dB RIPPLE REJECTION
LINE REG. <0.0001%/ V_I
LOAD REG. <0.1% V_O FOR LOAD CURRENTS UP TO 50mA
V_O RANGE FROM 1.8V TO 30V

FIGURE 21A. VOLTAGE REGULATOR WITH HIGH RIPPLE REJECTION

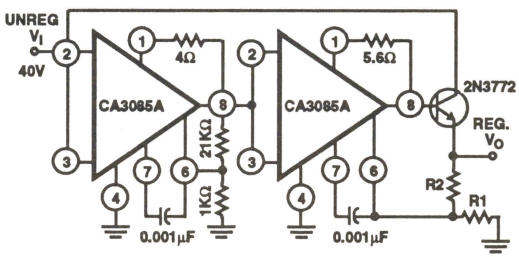


FIGURE 21B. HIGH-CURRENT VOLTAGE REGULATOR WITH HIGH RIPPLE REJECTION

The CA3085 As A Power Source For Sensors

Certain types of sensor applications require a regulated power source. Additionally, low-impedance sensors can consume significant power. An example of a circuit with these requirements, in which a CA3085 provides regulated power for a low-impedance sensor and the CA3059 zero-voltage switch, is shown in Figure 22. Terminal 12 on the CA3059 provides the ac trigger-signal which actuates the zero-voltage switch synchronously with the power line to control the load-switching triac. Specifications for the CA3059 appear in datasheet file number 490.

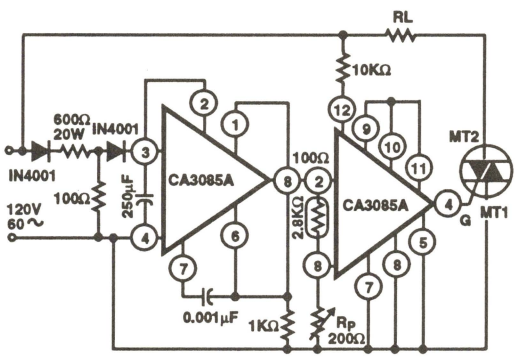


FIGURE 22. VOLTAGE REGULATOR FOR SENSOR AND ZERO-VOLTAGE SWITCH

The CA3085 As A General-Purpose Amplifier

As described above, the CA3085 series regulators contain a high-gain linear amplifier having a current-output capability up to 100mA. The premium type (CA3085B) can operate at supply voltages up to 50V. When equipped with an appropriate radiator or heat sink, the TO-5 package of these devices can dissipate up to 1.6W at 55°C. A very stable internal voltage-reference source is used to bias the high-gain amplifier and/or provide an external voltage-reference despite extreme temperature or supply-voltage variations. These factors, plus economics, prompt consideration of this circuit for general-purpose uses, such as amplifiers, relay controls, signal-lamp controls, and thyristor firing.

As an example, Figure 23 shows the application of the CA3085 in a general-purpose amplifier. Under the conditions shown, the circuit has a typical gain of 70bB with a flat response to at least 100kHz without the RC network connected between terminals 6 and 7. The RC network is useful as a tone control or to "roll-off" the amplifier response for other reasons. Current limiting is not used in this circuit. The network connected between terminals 8 and 6 provides both dc and ac feedback. This circuit is also applicable for directly driving an external discrete n-p-n power transistor.

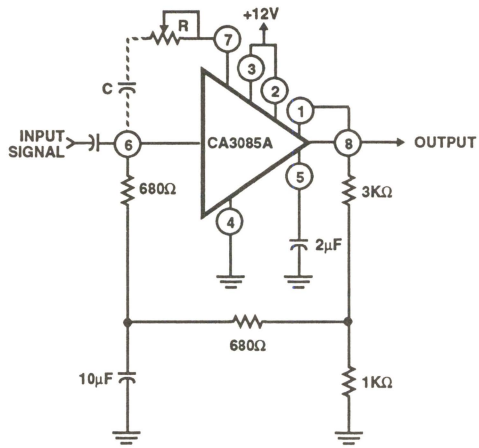


FIGURE 23. GENERAL-PURPOSE AMPLIFIER USING CA3085A

Harris Semiconductor

APPNOTE

No. AN6182.1 April 1994

Harris Intelligent Power

FEATURES AND APPLICATIONS OF INTEGRATED CIRCUIT ZERO-VOLTAGE SWITCHES (CA3059 AND CA3079)

Authors: A.C.N. Sheng, G.J. Granieri, J. Yellin, and T. McNulty

CA3059 and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse AC power control and power switching applications. These integrated circuit switches operate from an AC input voltage of 24, 120, 208 to 230, or 277V at 50, 60, or 400Hz.

The CA3059 and CA3079 are supplied in a 14 terminal dual-in-line plastic package.

Zero-voltage switches (ZVS) are particularly well suited for use as thyristor trigger circuits. These switches trigger the thyristors at zero-voltage points in the supply voltage cycle. Consequently, transient load current surges and radio frequency interference (RFI) are substantially reduced. In addition, use of the zero-voltage switches also reduces the rate of change of on state current (di/dt) in the thyristor being triggered, an important consideration in the operation of thyristors. These switches can be adapted for use in a variety of control functions by use of an internal differential comparator to detect the difference between two externally developed voltages. In addition, the availability of numerous terminal connections to internal circuit points greatly increases circuit flexibility and further expands the types of AC power control applications to which these integrated circuits may be adapted. The excellent versatility of the zero-voltage switches is demonstrated by the fact that these circuits have been used to provide transient free temperature control in self cleaning ovens, to control gun muzzle temperature in low temperature environments, to provide sequential switching of heating elements in warm air furnaces, to switch traffic signal lights at street intersections, and to effect other widely different AC power control functions.

Functional Description

Zero-voltage switches are multistage circuits that employ a diode limiter, a zero crossing (threshold) detector, an on/off sensing amplifier (differential comparator), and a Darlington output driver (thyristor gating circuit) to provide the basic switching action. The DC operating voltages for these stages is provided by an internal power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. An important feature of the zero-voltage switches is that the output trigger pulses can be applied directly to the gate of a triac or a silicon controlled rectifier (SCR). The CA3059 features an interlock (protection) circuit that inhibits the application of these pulses to the thyristor in the event that the external sensor should be inadvertently opened or shorted. An external inhibit connection (terminal No. 1) is also available so that an external signal can be used to inhibit the output drive. This feature is not included in the CA3079; otherwise, the three integrated circuit zero-voltage switches are electrically identical.

Overall Circuit Operation

Figure 1 shows the functional interrelation of the zero-voltage switch, the external sensor, the thyristor being triggered, and the load elements in an on/off type of AC power control system. As shown, each of the zero-voltage switches incorporates four functional blocks as follows:

Limiter Power Supply - Permits operation directly from an AC line.

Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional control capability may easily be implemented in this section.

Zero Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at a zero-voltage point and thereby eliminates radio frequency interference (RFI) when used with resistive loads.

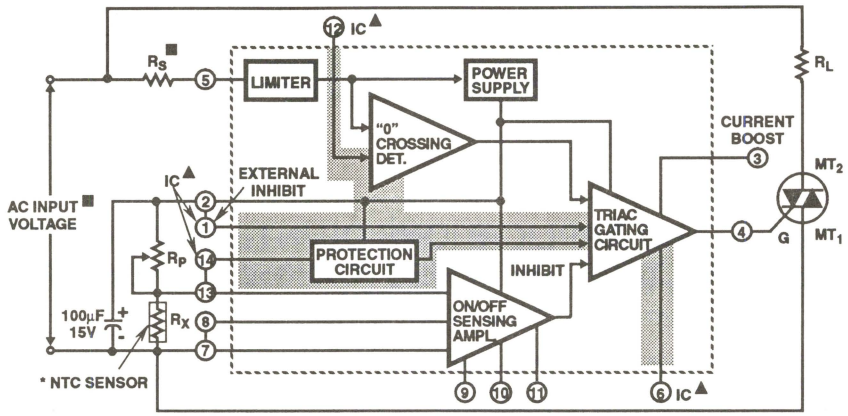
Triac Gating Circuit - Provides high current pulses to the gate of the power controlling thyristor.

In addition, the CA3059 provides the following important auxiliary functions (shown in Figure 1):

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to terminal 1.
3. High power DC comparator operation is provided by overriding the action of the zero crossing detector. This override is accomplished by connecting terminal 12 to terminal 7. Gate current to the thyristor is continuous when terminal 13 is positive with respect to terminal 9.

Figure 2 shows the detailed circuit diagram for the integrated circuit zero-voltage switches. (The diagrams shown in Figures 1 and 2 are representative of all three zero-voltage switches, i.e., the CA3059 and CA3079; the shaded areas indicate the circuitry that is not included in the CA3079.)

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* NEGATIVE TEMPERATURE COEFFICIENT

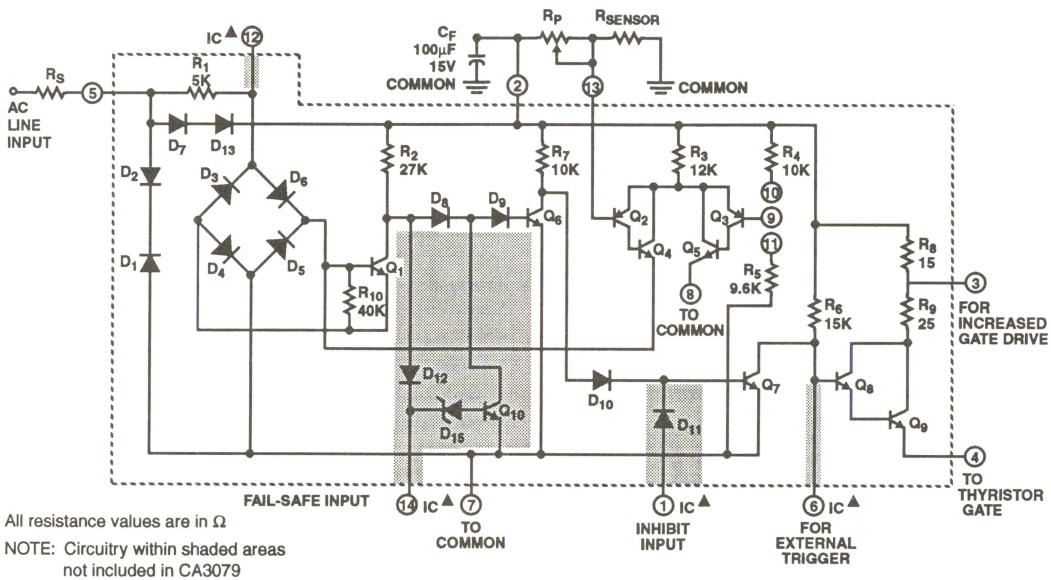
AC INPUT VOLTAGE (50/60 OR 400Hz) (V AC)	INPUT SERIES RESISTOR (R_S) (kΩ)	DISSIPATION RATING FOR R_S (W)
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE: Circuitry within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal connection - DO NOT USE (CA3079 only)

FIGURE 1. FUNCTIONAL BLOCK DIAGRAMS OF THE ZERO-VOLTAGE SWITCHES CA3059 AND CA3079



All resistance values are in Ω

NOTE: Circuitry within shaded areas not included in CA3079

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)

FIGURE 2. SCHEMATIC DIAGRAM OF ZERO-VOLTAGE SWITCHES CA3059 AND CA3079

The limiter stage of the zero-voltage switch clips the incoming AC line voltage to approximately ±8V. This signal is then applied to the zero-voltage crossing detector, which generates an output pulse each time the line voltage passes through zero. The limiter output is also applied to a rectifying diode and an external capacitor, C_F, that comprise the DC power supply. The power supply provides approximately 6V as the V_{CC} supply to the other stages of the zero-voltage switch. The on/off sensing amplifier is basically a differential comparator. The thyristor gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a "high" voltage, i.e., the line voltage must be approximately zero volts, the sensing amplifier output must be "high", the external voltage to terminal 1 must be a logical "0", and, for the CA3059, the output of the fail-safe circuit must be "high". Under these conditions, the thyristor (triac or SCR) is triggered when the line voltage is essentially zero volts.

Thyristor Triggering Circuits

The diodes D_1 and D_2 in Figure 2 form a symmetrical clamp that limits the voltages on the chip to ±8V; the diodes D_7 and D_{13} form a half-wave rectifier that develops a positive voltage on the external storage capacitor, C_F.

The output pulses used to trigger the power switching thyristor are actually developed by the zero crossing detector and the thyristor gating circuit. The zero crossing detector consists of diodes D_2 and through D_6, transistor Q_1, and the associated resistors shown in Figure 2. Transistors Q_1 and Q_6 through Q_9 and the associated resistors comprise the thyristor gating circuit and output driver. These circuits generate the output pulses when the AC input is at a zero-voltage point so that RFI is virtually eliminated when the zero-voltage switch and thyristor are used with resistive loads.

The operation of the zero crossing detector and thyristor gating circuit can be explained more easily if the on state (i.e., the operating state in which current is being delivered to the thyristor gate through terminal 4) is considered as the operating condition of the gating circuit. Other circuit elements in the zero-voltage switch inhibit the gating circuit unless certain conditions are met, as explained later.

In the on state of the thyristor gating circuit, transistors Q_8 and Q_9 are conducting, transistor Q_7 is off, and transistor Q_6 is on. Any action that turns on transistor Q_7 removes the drive from transistor Q_8 and thereby turns off the thyristor. Transistor Q_7 may be turned on directly by application of a minimum of ±1.2V at 10μA to the external inhibit input, terminal 1. (If a voltage of more than 1.5V is available, an external resistance must be added in series with terminal 1 to limit the current to 1mA.) Diode D_{10} isolates the base of transistor Q_7 from other signals when an external inhibit signal is applied so that this signal is the highest priority command for normal operation. (Although grounding of terminal 6 creates a higher priority inhibit function, this level is not compatible with normal DTL or TTL logic levels.) Transistor Q_7 may also be activated by turning off transistor Q_6 to allow current flow from the power supply through resistor R_7 and diode D_{10} into the base of Q_7. Transistor Q_6 is normally maintained in conduction by current that flows into its base through resistor R_2 and diodes D_8 and D_9 when transistor Q_1 is off.

Transistor Q_1 is a portion of the zero crossing detector. When the voltage at terminal 5 is greater than +3V, current can flow through resistor R_1, diode D_6, the base-to-emitter junction of transistor Q_1, and diode D_4 to terminal 7 to turn on Q_1. This action inhibits the delivery of a gate-drive output signal at terminal 4. For negative voltages at terminal 5 that have magnitudes greater than 3V, the current flows through diode D_5, the emitter-to-base junction of transistor Q_1, diode D_3, and resistor R_1, and again turns on transistor Q_1. Transistor Q_1 is off only when the voltage at terminal 5 is less than the threshold voltage of approximately ±2V. When the integrated circuit zero-voltage switch is connected as shown in Figure 2, therefore, the output is a narrow pulse which is approximately centered about the zero-voltage time in the cycle, as shown in Figure 3. In some applications, however, particularly those that use either slightly inductive or low power loads, the thyristor load current does not reach the latching current value† by the end of this pulse. An external capacitor C_X connected between terminal 5 and 7, as shown in Figure 4, can be used to delay the pule to accommodate such loads. The amount of pulse stretching and delay is shown in Figures 5(a) and 5(b).

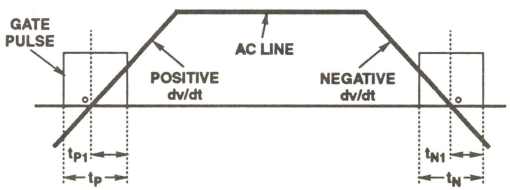


FIGURE 3. WAVEFORM SHOWING OUTPUT PULSE DURATION OF THE ZERO-VOLTAGE SWITCH.

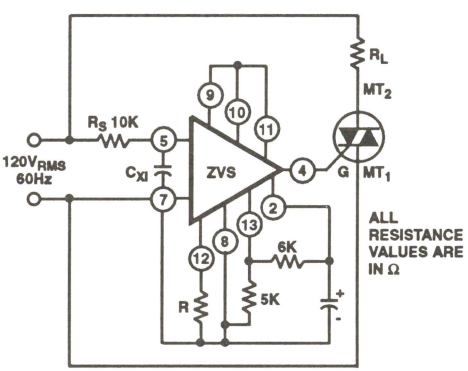


FIGURE 4. USE OF A CAPACITOR BETWEEN TERMINALS 5 AND 7 TO DELAY THE OUTPUT PULSE OF THE ZERO-VOLTAGE SWITCH

† The latching current is the minimum current required to sustain conduction immediately after the thyristor is switched from the off to the on state and the gate signal is removed.

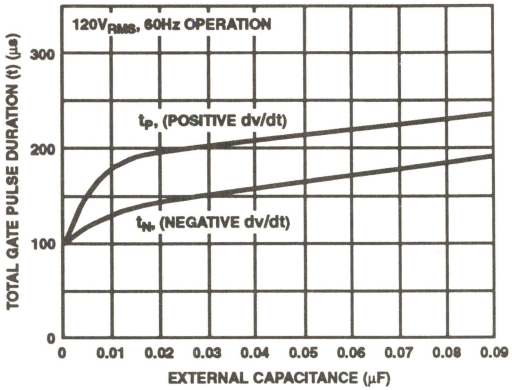


FIGURE 5A.

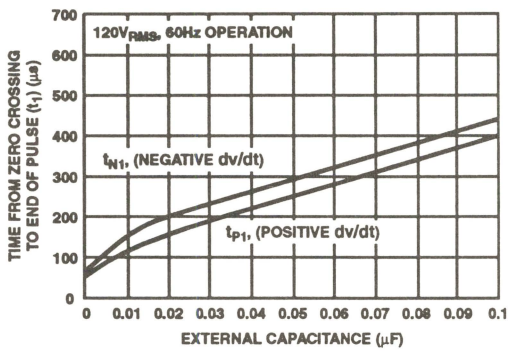


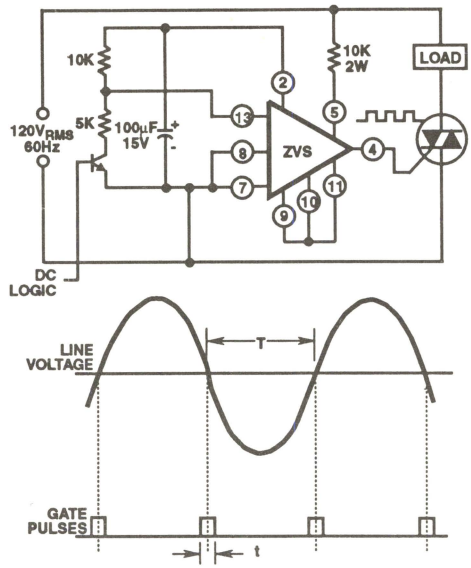
FIGURE 5B.

FIGURE 5. CURVES SHOWING EFFECT OF EXTERNAL CAPACITANCE ON A. THE TOTAL OUTPUT PULSE DURATION, AND B. THE TIME FROM ZERO CROSSING TO THE END OF THE PULSE

Continuous gate current can be obtained if terminal 12 is connected to terminal 7 to disable the zero crossing detector. In this mode, transistor Q_1 is always off. This mode of operation is useful when comparator operation is desired or when inductive loads must be switched. (If the capacitance in the load circuit is low, most RFI is eliminated.) Care must be taken to avoid overloading of the internal power supply in this mode. A sensitive gate thyristor should be used, and a resistor should be placed between terminal 4 and the gate of the thyristor to limit the current, as pointed out later under Special Application Considerations.

Special Application Considerations

Figure 6 indicates the timing relationship between the line voltage and the zero-voltage switch output pulses. At 60Hz, the pulse is typically 100µs wide; at 400Hz, the pulse width is typically 12µs. In the basic circuit shown, when the DC logic signal is "high", the output is disabled; when it is "low", the gate pulses are enabled.



FREQ. (Hz)	T (ms)	t (µs)
60	8.3	100
400	1.25	12

FIGURE 6. TIMING RELATIONSHIP BETWEEN THE OUTPUT PULSES OF THE ZERO-VOLTAGE SWITCH AND THE AC LINE VOLTAGE

On/Off Sensing Amplifier

The discussion thus far has considered only cases in which pulses are present all the time or not at all. The differential sense amplifier consisting of transistors Q_2, Q_3, Q_4, and Q_5 (shown in Figure 2) makes the zero-voltage switch a flexible power control circuit. The transistor pairs Q_2-Q_4 and Q_3-Q_5 form a high beta composite p-n-p transistors in which the emitters of transistors Q_4 and Q_5 act as the collectors of the composite devices. These two composite transistors are connected as a differential amplifier with resistor R_3 acting as a constant current source. The relative current flow in the two "collectors" is a function of the difference in voltage between the bases of transistors Q_2 and Q_3. Therefore, when terminal 13 is more positive than terminal 9, little or no current flows in the "collector" of the transistor pair Q_2-Q_4. When terminal 13 is negative with respect to terminal 9, most of the current flows through that path, and none in terminal 8. When current flows in the transistor pair Q_2-Q_4, through the base emitter junction of transistor Q_1, and finally through the diode D_4 to terminal 7. Therefore, when V_{13} is equal to or more negative than V_9, transistor Q_1 is on, and the output is inhibited.

In the circuit shown in Figure 1, the voltage at terminal 9 is derived from the supply by connection of terminals 10 and 11 to form a precision voltage divider. This divider forms one side of a transducer bridge, and the potentiometer R_P and the negative temperature coefficient (NTC) sensor form the other side. At

low temperatures, the high resistance of the sensor causes terminal 13 to be positive with respect to terminal 9 so that the thyristor fires on every half cycle, and power is applied to the load. As the temperature increases, the sensor resistance decreases until a balance is reached, and V_{13} approaches V_9. At this point, the transistor pair Q_2-Q_4 turns on and inhibits any further pulses. The controlled temperature is adjusted by variation of the value of the potentiometer R_P For cooling service, either the positions of R_P and the sensor may be reversed or terminals 9 and 13 may be interchanged.

The low bias current of the sensing amplifier permits operation with sensor impedances of up to 0.1MΩ at balance without introduction of substantial error (i.e., greater than 5 percent). The error may be reduced if the internal bridge elements, resistors R_4 and R_5, are not used, but are replaced with resistances which equal the sensor impedance. The minimum value of sensor impedance is restricted by the current drain on the internal power supply. Operation of the zero-voltage switch with low impedance sensors is discussed later under Special Application Considerations. The voltage applied to terminal 13 must be greater than 1.8V at all times to assure proper operation.

Protection Circuit

A special feature of the CA3059 zero-voltage switch is the inclusion of an interlock type of circuit. This circuit removes power from the load by interrupting the thyristor gate drive if the sensor either shorts or opens. However, use of this circuit places certain constraints upon the user. Specifically, effective protection circuit operation is dependent upon the following conditions:

1. The circuit configuration of Figure 1 is used, with an internal supply, no external load on the supply, and terminal 14 connected to terminal 13.
2. The value of potentiometer R_P and of the sensor resistance must be between 2000Ω and 0.1MΩ.
3. The ratio of sensor resistance and R_P must be greater than 0.33 and less than 3.0 for all normal conditions. (If either of these ratios is not met with an unmodified sensor, a series resistor or a shunt resistor must be added to avoid undesired activation of the circuit.)

The protective feature may be applied to other systems when operation of the circuit is understood. The protection circuit consists of diodes D_{12} and D_{15} and transistor Q_{10}. Diode D_1 activates the protection circuit if the sensor shown in Figure 1 shorts or its resistance drops too low in value, as follows: Transistor Q_6 is on during an output pulse so that the junction of diodes D_8 and D_{12} is 3 diode drops (approximately 2V) above terminal 7. As long as V_{14} is more positive or only 0.15 volt negative with respect to that point, diode D_{12} does not conduct, and the circuit operates normally. If the voltage at terminal 14 drops to 1 volt, the anode of diode D_8 can have a potential of only 1.6 to 1.7V, and current does not flow through diodes D_8 and D_9 and transistor Q_6. The thyristor then turns off.

The actual threshold is approximately 1.2V at room temperature, but decreases 4mV per degree C at higher temperatures. As the sensor resistance increases, the voltage at terminal 14 rises toward the supply voltage. At a voltage of approximately 6V, the zener diode D_{15} breaks down and turns on transistor Q_{10}, which then turns off transistor Q_6 and the thyristor. If the supply voltage is not at least 0.2 volt more positive than the breakdown voltage of diode D_{15}, activation of the protection circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, as may the selection of the wrong external supply voltage. Figure 7 shows a guide for the proper operation of the protection circuit when an external supply is used with a typical integrated circuit zero-voltage switch.

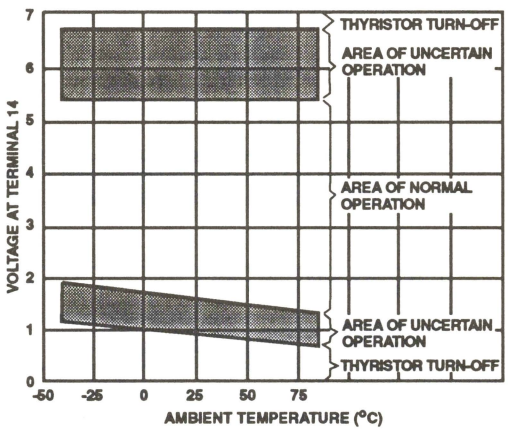


FIGURE 7. OPERATING REGIONS FOR BUILT-IN PROTECTION CIRCUITS OF A TYPICAL ZERO-VOLTAGE SWITCH.

Special Application Considerations

As pointed out previously, the Harris integrated circuit zero-voltage switches (CA3059 and CA3079) are exceptionally versatile units than can be adapted for use in a wide variety of power control applications. Full advantage of this versatility can be realized, however, only if the user has a basic understanding of several fundamental considerations that apply to certain types of applications of the zero-voltage switches.

Operating Power Options

Power to the zero-voltage switch may be derived directly from the AC line, as shown in Figure 1, or from an external DC power supply connected between terminals 2 and 7, as shown in Figure 8. When the zero-voltage switch is operated directly from the AC line, a dropping resistor R_S of 5,000Ω to 10,000Ω must be connected in series with terminal 5 to limit the current in the switch circuit. The optimum value for this resistor is a function of the average current drawn from the internal DC power supply, either by external circuit elements or by the thyristor trigger circuits, as shown in Figure 9. The chart shown in Figure 1 indicates the value and dissipation rating of the resistor R_S for AC line voltages 24, 120, 208 to 230, and 277V.

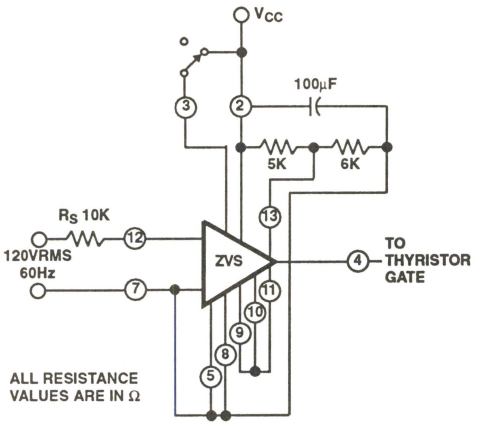


FIGURE 8. OPERATION OF THE ZERO-VOLTAGE SWITCH FROM AN EXTERNAL DC POWER SUPPLY CONNECTED BETWEEN TERMINALS 2 AND 7.

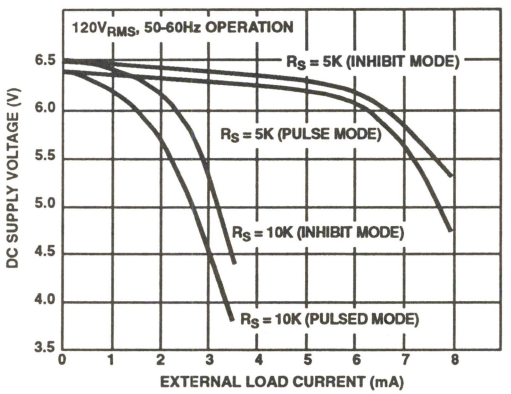


FIGURE 9. DC SUPPLY VOLTAGE AS A FUNCTION OF EXTERNAL LOAD CURRENT FOR SEVERAL VALUES

Half Cycling Effect

The method by which the zero-voltage switch senses the zero crossing of the AC power results in a half cycling phenomenon at the control point. Figure 10 illustrates this phenomenon. The zero-voltage switch senses the zero-voltage crossing every half cycle, and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3ms, however, the differential amplifier in the zero-voltage switch may change state and inhibit any further output pulses. The uncertainty region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac during the negative excursion of the AC line voltage.

When a sensor with low sensitivity is used in the circuit, the zero-voltage switch is very likely to operate in the linear mode. In this mode, the output trigger current may be sufficient to trigger the triac on the positive going cycle, but insufficient to trigger the device on the negative going cycle of the triac supply voltage. This effect introduces a half cycling phenomenon, i.e., the triac is turned on during the positive half cycle and turned off during the negative half cycle.

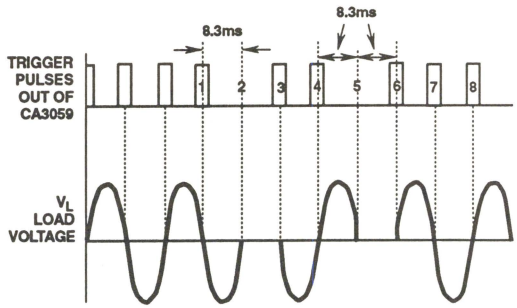
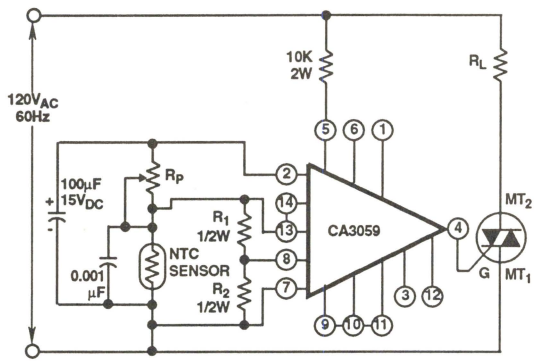


FIGURE 10. HALF CYCLING PHENOMENON IN THE ZERO-VOLTAGE SWITCH

Several techniques may be used to cope with the half cycling phenomenon. If the user can tolerate some hysteresis in the control, then positive feedback can be added around the differential amplifier. Figure 11 illustrates this technique. The tabular data in the figure lists the recommended values of resistors R1 and R2 for different sensor impedances at the control point.



THERMISTOR →

NTC	R1	R2
5K	12K	12K
12K	68K	12K
100K	200K	18K

FIGURE 11. CA3059 ON-OFF CONTROLLER WITH HYSTERESIS

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Figure 12 may be employed. In this configuration, external transistor Q_1 can be used to provide an auxiliary timed delay function.

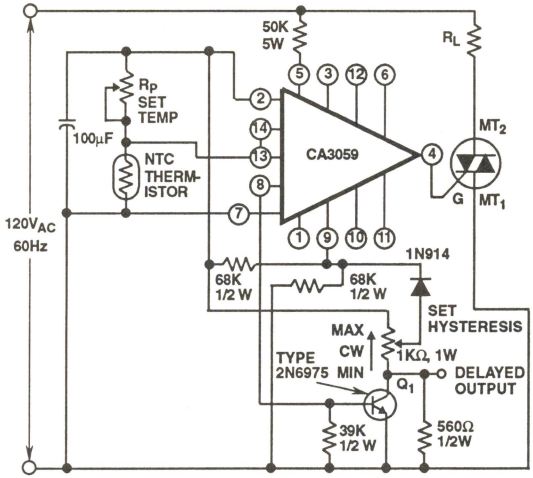


FIGURE 12. CA3059 ON/OFF CONTROLLER WITH CONTROLLED HYSTERESIS

For applications that require complete elimination of half cycling without the addition of hysteresis, the circuit shown in Figure 13 may be employed. This circuit uses a CA3098E integrated circuit programmable comparator with a zero-voltage switch. A block diagram of CA3098E is shown in Figure 14. Because the CA3098E contains an integral flip-flop, its output will be in either a "0" or "1" state. Consequently the zero-voltage switch cannot operate in the linear mode, and spurious half cycling operation is prevented. When the signal input voltage at terminal 8 of the CA3098E is equal to or less than the "low" reference voltage (LR), current flows from the power supply through resistor R_1 and R_2, and a logic "0" is applied to terminal 13 of the zero-voltage switch. This condition turns off the triac. The triac remains off until the signal input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop so that a logic "1" is applied to terminal 13 of the zero-voltage switch, and triggers the triac on.

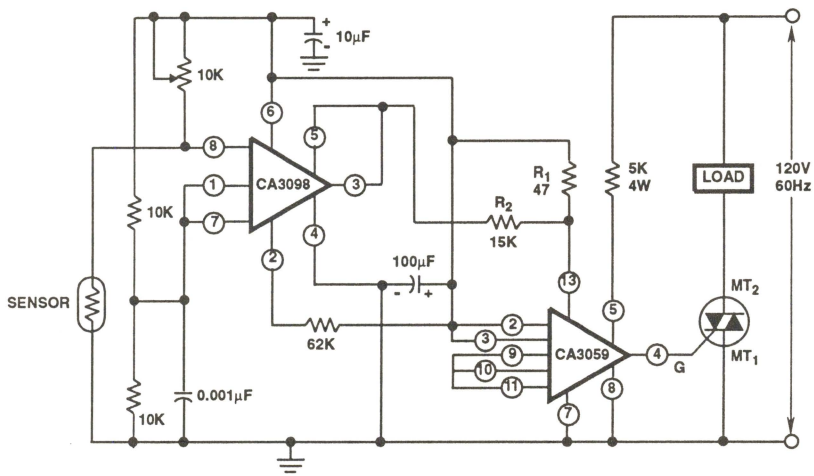


FIGURE 13. SENSITIVE TEMPERATURE CONTROL

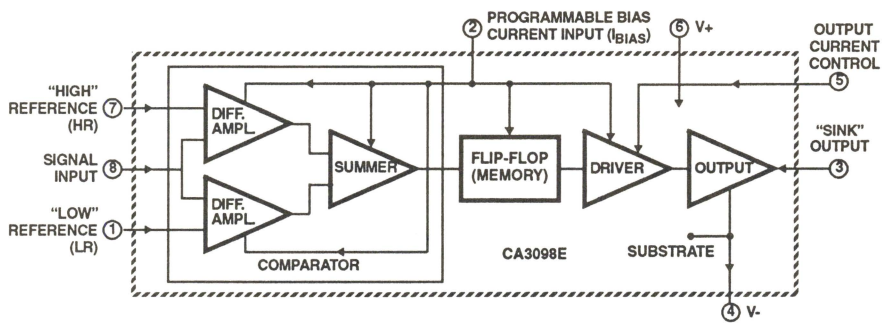


FIGURE 14. BLOCK DIAGRAM OF CA3098 PROGRAMMABLE SCHMITT TRIGGER

"Proportional Control" Systems

The on/off nature of the control shown in Figure 1 causes some overshoot that leads to a definite steady state error. The addition of hysteresis adds further to this error factor. However, the connections shown in Figure 15A. can be used to add proportional control to the system. In this circuit, the sense amplifier is connected as a free running multivibrator. At balance, the voltage at terminal 13 is much less than the voltage at terminal 9. The output will be inhibited at all times until the voltage at terminal 13 rises to the design differential voltage between terminals 13 and 9; then proportional control resumes. The voltage at terminal 13 is as shown in Figure 15B). When this voltage is more positive than the threshold, power is applied to the load so that the duty cycle is approximately 50 percent. With a 0.1MΩ sensor and values of R_P = 01.MΩ, R_2 = 10,000Ω, and C_{EXT} = 10μF, a period greater than 3 seconds is achieved. This period should be much shorter than the thermal time constant of the system. A change in the value of any of these elements changes the period, as shown in Figure 16. As the resistance of the sensor changes, the voltage on terminal 13 moves relative to V_9. A cooling sensor moves V_{13} in a positive direction. The triac is on for a larger portion of the pulse cycle and increases the average power to the load.

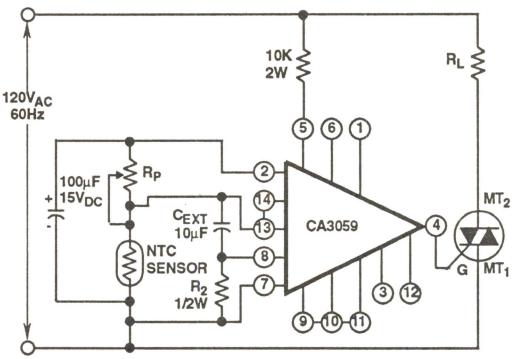


FIGURE 15A.

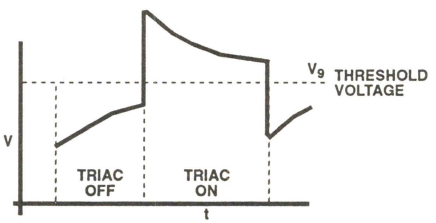


FIGURE 15B.

FIGURE 15. USE OF THE CA3059 IN A TYPICAL HEATING CONTROL WITH PROPORTIONAL CONTROL: A. SCHEMATIC DIAGRAM, AND B. WAVEFORM OF VOLTAGE AT ERMINAL 13

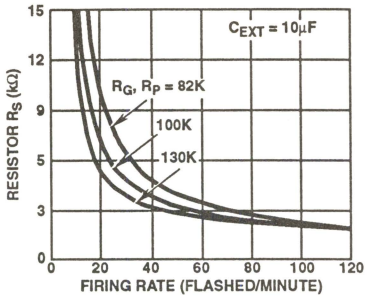


FIGURE 16. EFFECT OF VARIATIONS IN TIME CONSTANT ELEMENTS ON PERIOD

As in the case of the hysteresis circuitry described earlier, some special applications may require more sophisticated systems to achieve either very precise regions of control or very long periods.

Zero-voltage switching control can be extended to applications in which it is desirable to have constant control of the temperature and a minimization of system hysteresis. A closed loop top burner control in which the temperature of the cooking utensil is sensed and maintained at a particular value is a good example of such an application; the circuit for this control is shown in Figure 17. In this circuit, a unijunction oscillator is outboarded from the basic control by means of the internal power supply of the zero-voltage switch. The output of this ramp generator is applied to terminal 9 of the zero-voltage switch and establishes a varied reference to the differential amplifier. Therefore, gate pulses are applied to the triac whenever the voltage at terminal 13 is greater than the voltage at terminal 9. A varying duty cycle is established in which the load is predominantly on with a cold sensor and predominantly off with a hot sensor. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system but longer than the period of the 60Hz line. Figure 18, which contains various waveforms for the system of Figure 17, indicates that a typical variance of ±0.5°C might be expected at the sensor contact to the utensil. Overshoot of the set temperature is minimized with approach, and scorching of any type is minimized.

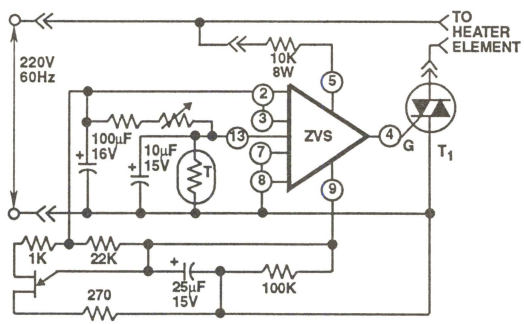


FIGURE 17. SCHEMATIC DIAGRAM OF PROPORTIONAL ZERO-VOLTAGE SWITCHING CONTROL

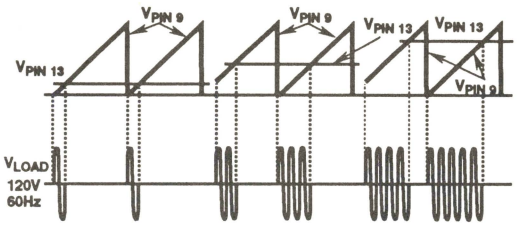


FIGURE 18. WAVEFORMS FOR THE CIRCUIT OF FIGURE 17.

Effect of Thyristor Load Characteristics

The zero-voltage switch is designed primarily to gate a thyristor that switches a resistive load. Because the output pulse supplied by the switch is of short duration, the latching current of the triac becomes a significant factor in determining whether other types of loads can be switched. (The latching current value determines whether the triac will remain in conduction after the gate pulse is removed.) Provisions are included in the zero-voltage switch to accommodate inductive loads and low power loads. For example, for loads that are less than approximately $4A_{rms}$ or that are slightly inductive, it is possible to retard the output pulse with respect to the zero-voltage crossing by insertion of the capacitor C_X from terminal 5 to terminal 7. The insertion of capacitor C_X permits switching of triac loads that have a slight inductive component and that are greater than approximately 200W (for operation from an AC line voltage of $120V_{rms}$). However, for loads less than 200W (for example, 70W), it is recommended that the user employ sensitive gate triacs with the zero-voltage switch because of the low latching current requirement of this triac.

For loads that have a low power factor, such as a solenoid valve, the user may operate the zero-voltage switch in the DC mode. In this mode, terminal 12 is connected to terminal 7, and the zero crossing detector is inhibited. Whether a "high" or "low" voltage is produced at terminal 4 is then dependent only upon the state of the differential comparator within the integrated circuit zero-voltage switch, and not upon the zero crossing of the incoming line voltage. Of course, in this mode of operation, the zero-voltage switch no longer operates as a zero-voltage switch. However, for may applications that involve the switching of low current inductive loads, the amount of RFI generated can frequently be tolerated.

For switching of high current inductive loads, which must be turned on at zero line current, the triggering technique employed in the dual output over-under temperature controller and the transient free switch controller described subsequently in this Note is recommended.

Switching of Inductive Loads

For proper driving of a thyristor in full cycle operation, gate drive must be applied soon after the voltage across the device reverses. When resistive loads are used, this reversal occurs as the line voltage reverses. With loads of other power factors, however, it occurs as the current through the load becomes zero and reverses.

There are several methods for switching an inductive load at the proper time. If the power factor of the load is high (i.e., if the load is only slightly inductive), the pulse may be delayed by addition of a suitable capacitor between terminals 5 and 7, as described previously. For highly inductive loads, however, this method is not suitable, and different techniques must be used.

If gate current is continuous, the triac automatically commutates because drive is always present when the voltage reverses. This mode is established by connection of terminals 7 and 12. The zero crossing detector is then disabled so that current is supplied to the triac gate whenever called for by the sensing amplifier. Although the RFI eliminating function of the zero-voltage switch is inhibited when the zero crossing detector is disabled, there is no problem if the load is highly inductive because the current in the load cannot change abruptly.

Circuits that use a sensitive gate triac to shift the firing point of the power triac by approximately 90 degrees have been designed. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

The circuit shown in Figure 19 uses a CA3086 integrated circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two V_{BE} drops, or 1.3V. When A is positive, transistors Q_3 and Q_4 conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, transistors Q_1 and Q_2 conduct. When the voltage at point A is less than ±1.3V, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in resistor R_3, and the output is inhibited.

The circuit shown in Figure 19 forms a pulse of gate current and can supply high peak drive to power triacs with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitable inductive because the zero crossing detector is disabled and initial turn on occurs at random.

The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3V; therefore, the output of the zero-voltage switch is inhibited, as described above. The resistor divider R_1 and R_2 should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one third of the instantaneous on state voltage (V_T) of the thyristor. For most thyristors, V_T (max) is less than 2V, and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit is still being

driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4V, one portion of the CA3086 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the latching current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

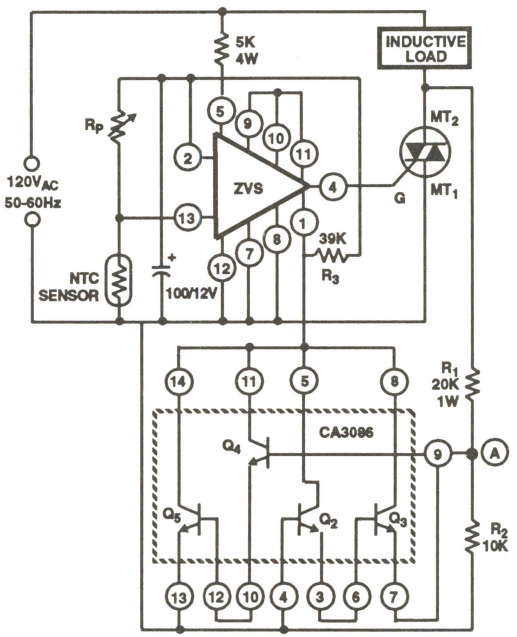


FIGURE 19. USE OF THE CA3059 TOGETHER WITH 3086 FOR SWITCHING INDUCTIVE LOADS

Provision of Negative Gate Current

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar (I+ and II- modes). Sensitivity is degraded when the polarities are opposite (I- and III+ modes). Although Harris triacs are designed and specified to have the same sensitivity in both I- and III+ modes, some other types have very poor sensitivity in the III+ condition. Because the zero-voltage switch supplies positive gate pulses, it may not directly drive some high current triacs of these other types.

The circuit shown in Figure 20A. uses the negative going voltage at terminal 3 of the zero-voltage switch to supply a negative gate pulse through a capacitor. The curve in Figure 20B. shows the approximate peak gate current as a function of gate voltage V_G. Pulse width is approximately 80µs.

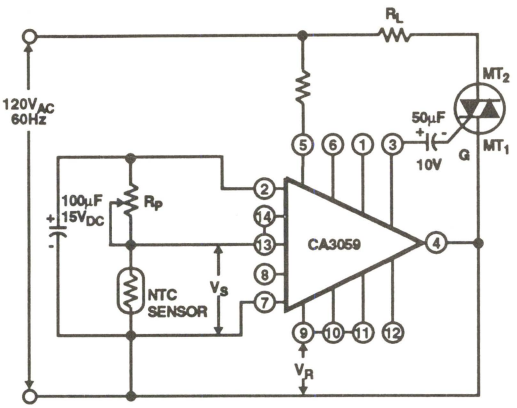


FIGURE 20A.

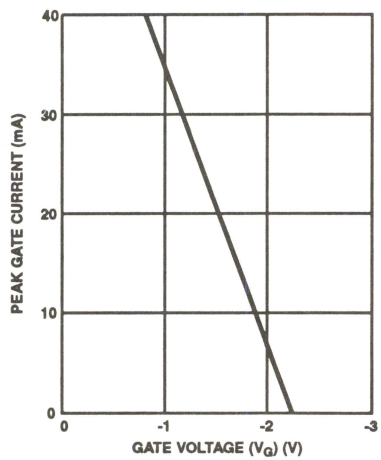


FIGURE 20B.

FIGURE 20. USE OF THE CA3059 TO PROVIDE NEGATIVE GATE PULSES: A. SCHEMATIC DIAGRAM; B. PEAK GATE CURRENT (FAT TERMINAL 3) AS A FUNCTION OF GATE VOLTAGE

Operation with Low Impedance Sensors

Although the zero-voltage switch can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000Ω are used. Typical sensitivity is one percent for a 5000Ω sensor and increases to three percent for a 0.1MΩ sensor.

Low impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000Ω sensor with its associated 5000Ω series resistor draws less than 1mA. On the other hand, a 300Ω sensor draws a current of 8 to 10mA from the power supply.

Figure 21 shows the 600Ω load line of a 300Ω sensor on a redrawn power supply regulation curve for the zero-voltage switch. When a 10,000Ω series resistor is used, the voltage

across the circuit is less than 3V and both sensitivity and output current are significantly reduced. When a 5000Ω series resistor is used, the supply voltage is nearly 5V, and operation is approximately normal. For more consistent operation, however, a 4000Ω series resistor is recommended.

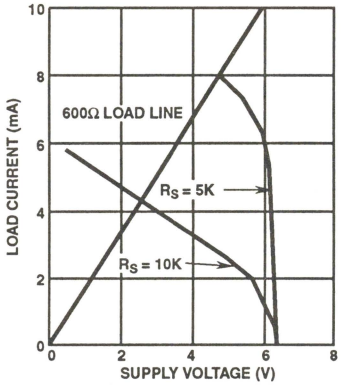


FIGURE 21. POWER SUPPLY REGULATION OF THE CA3059 WITH A 300Ω SENSOR (600Ω LOAD) FOR TWO VALUES OF SERIES RESISTOR.

Although positive temperature coefficient (PTC) sensors rated at 5kΩ are available, the existing sensors in ovens are usually of a much lower value. The circuit shown in Figure 22 is offered to accommodate these inexpensive metal wound sensors. A schematic diagram of the CA3080 integrated circuit operation transconductance amplifier used in Figure 22, is shown in Figure 23. With an amplifier bias current, I_{ABC}, of 100μA, a forward transconductance of 2mΩ is achieved in this configuration. The CA3080 switches when the voltage at terminal 2 exceeds the voltage at terminal 3. This action allows the sink current, I_S, to flow from terminal 13 of the zero-voltage switch (the input impedance to terminal 13 of the zero-voltage switch is approximately 50kΩ); gate pulses are no longer applied to the triac because Q_2 of the zero-voltage switch is on. Hence, if the PTC sensor is cold, i.e., in the low resistance state, the load is energized. When the temperature of the PTC sensor increases to the desired temperature, the sensor enters the high resistance state, the voltage on terminal 2 becomes greater than that on terminal 3, and the triac switches the load off.

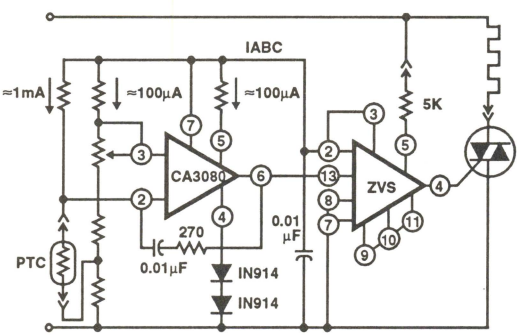


FIGURE 22. SCHEMATIC DIAGRAM OF CIRCUIT FOR USE WITH LOW RESISTANCE SENSOR

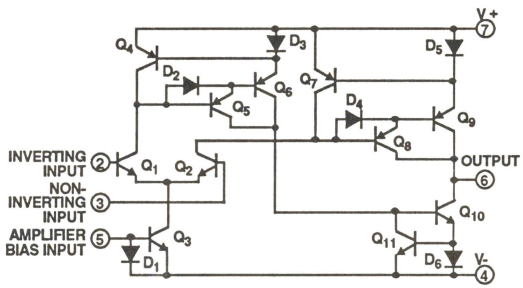


FIGURE 23. SCHEMATIC DIAGRAM OF THE CA3080

Further cycling depends on the voltage across the sensor. Hence, very low values of sensor and potentiometer resistance can be used in conjunction with the zero-voltage switch power supply without causing adverse loading effects and impairing system performance.

Interfacing Techniques

Figure 24 shows a system diagram that illustrates the role of the zero-voltage switch and thyristor as an interface between the logic circuitry and the load. There are several basic interfacing techniques. Figure 25A. shows the direct input technique. When the logic output transistor is switched from the on state (saturated) to the off state, the load will be turned on at the next zero-voltage crossing by means of the interfacing zero-voltage switch and the triac. When the logic output transistor is switched back to the on state, zero crossing pulses from the zero-voltage switch to the triac gate will immediately cease. Therefore, the load will be turned off when the triac commutates off as the sine wave load current goes through zero. In this manner, both the turn-on and turn-off conditions for the load are controlled.

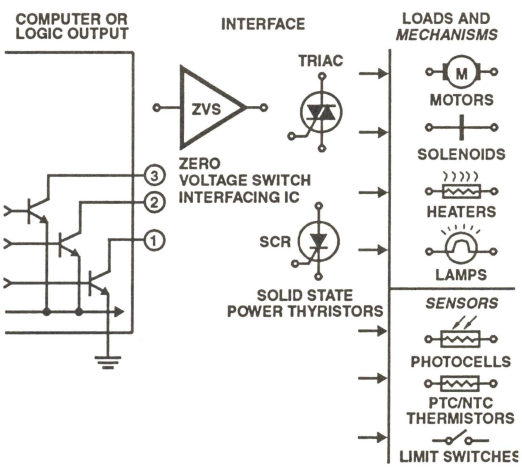


FIGURE 24. THE ZERO-VOLTAGE SWITCH AND THYRISTOR AS AN INTERFACE

When electrical isolation between the logic circuit and the load is necessary, the **Isolated-Input** technique shown in Figure 25B. is used. In the technique shown, optical coupling is used

to achieve the necessary isolation. The logic output transistor switches the light source portion of the isolator. The light sensor portion changes from a high impedance to a low impedance when the logic output transistor is switched from off to on. The light sensor is connected to the differential amplifier input of the zero-voltage switch, which senses the change of impedance at a threshold level and switches the load on as in Figure 25A.

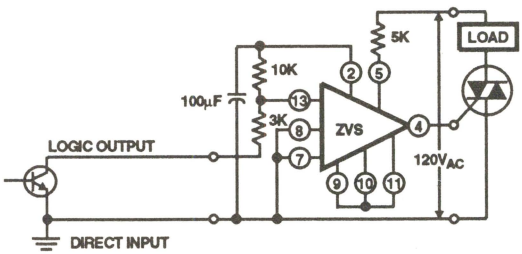


FIGURE 25A.

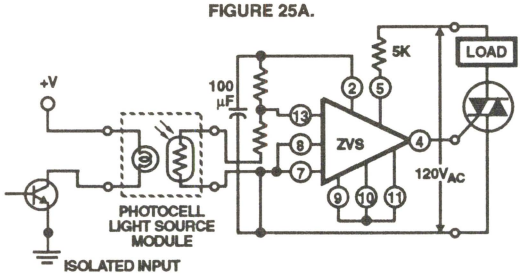


FIGURE 25B.

FIGURE 25. BASIC INTERFACING TECHNIQUES: A. DIRECT INPUT; B. ISOLATED INPUT

Sensor Isolation

In many applications, electrical isolation of the sensor from the AC input line is desirable. Several isolation techniques are shown in Figures 26, 27, and 28.

Transformer Isolation - In Figure 26, a pulse transformer is used to provide electrical isolation of the sensor from incoming AC power lines. The pulse transformer T_1 isolates the sensor from terminal No. 1 of the triac Y_1, and transformer T_2 isolates the CA3059 from the power lines. Capacitor C_1 shifts the phase of the output pulse at terminal No. 4 in order to retard the gate pulse delivered to triac Y_1 to compensate for the small phase shift introduced by transformer T_1.

Many applications require line isolation but not zero-voltage switching. A line isolated temperature controller for use with inductive or resistive loads that does not include zero-voltage switching is shown in Figure 27.

In temperature monitoring or control applications the sensor may be a temperature dependent element such as a resistor, thermistor, or diode. The load may be a lamp, bell, horn, recorder or other appropriate device connected in a feedback relationship to the sensor.

For the purpose of the following explanation, assume that the sensor is a resistor having a negative temperature coefficient and that the load is a heater thermally coupled to the sensor, the object being to maintain the thermal coupling medium at a desired reference temperature. Assume initially that the temperature at the coupling medium is low.

The operating potentials applied to the bridge circuit produce a common mode potential, V_{CM}, at the input terminals of the CA3094. Assuming the bridge to have been initially balanced (by adjustment of R_4), the potential at point A will

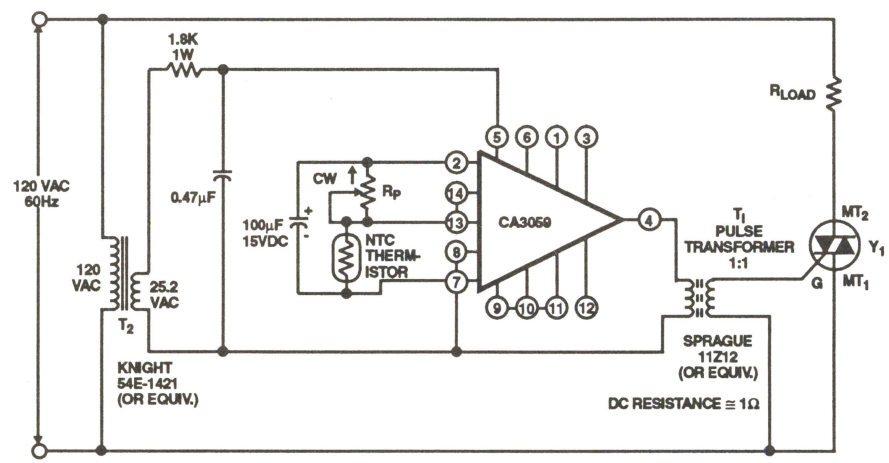


FIGURE 26. ZERO-VOLTAGE SWITCH, ON/OFF CONTROLLER WITH AN ISOLATED SENSOR

increase when temperature is low since it was assumed that the sensor has a negative temperature coefficient. The potential at the noninverting terminal, being greater than that at the inverting terminal at the amplifier, causes the multivibrator to oscillate at approximately 10kHz. The oscillations are transformer coupled through a current limiting resistor to the gate of the thyristor, and trigger it into conduction.

When the thyristor conducts, the load receives AC input power, which tends to increase the temperature of the sensor. This temperature increase decreases the potential at point A to a value below that at point B and the multivibrator is disabled, which action, in turn, turns off the thyristor. The temperature is thus controlled in an of/off fashion.

Capacitor C_1 is used to provide a low impedance path to ground for feedback induced signals at terminal No. 5 while blocking the direct current bias provided by resistor R_1. Resistor R_2 provides current limiting. Resistor R_3 limits the secondary current of the transformer to prevent excessive current flow to the control terminal of the CA3094.

Photocoupler Isolation - In Figure 28, a photocoupler provides electrical isolation of the sensor logic from the incoming AC power lines. When a logic "1" is applied at the input of the photocoupler, the triac controlling the load will be turned on whenever the line voltage passes through zero. When a logic"0" is applied to the photocoupler, the triac will turn off and remain off until a logic "1" appears at the input of the photocoupler.

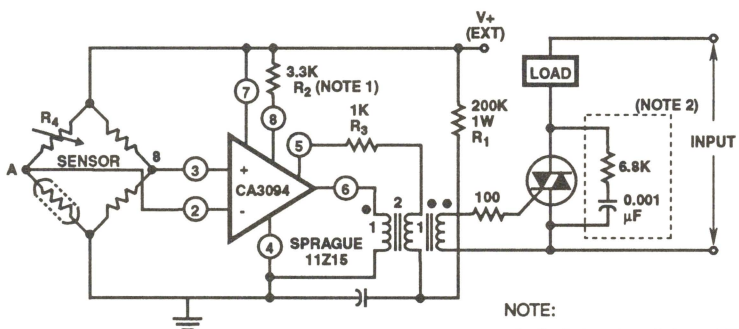


FIGURE 27. A LINE ISOLATED TEMPERATURE CONTROLLER FOR USE WITH INDUCTIVE OR RESISTIVE LOADS; THIS CONTROLLER DOES NOT INCLUDE ZERO-VOLTAGE SWITCHING.

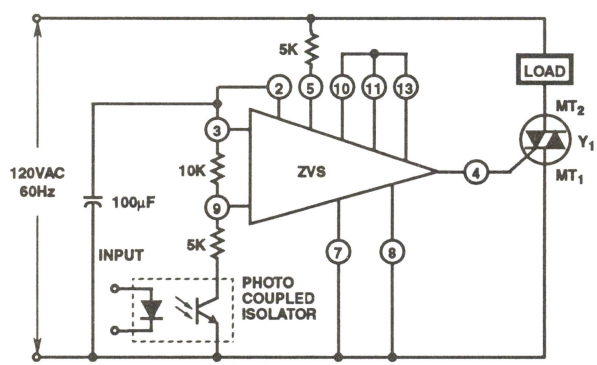


FIGURE 28. ZERO-VOLTAGE SWITCH, ON/OFF CONTROLLER WITH PHOTOCOUPLER

Temperature Controllers

Figure 29 shows a triac used in an of/off temperature controller configuration. The triac is turned on at zero-voltage whenever the voltage V_S exceeds the reference voltage V_R. The transfer characteristic of this system, shown in Figure 30A., indicates significant thermal overshoots and undershoots, a well known characteristic of such a system. The differential or hysteresis of this system, however, can be further increased, if desired, by the addition of positive feedback.

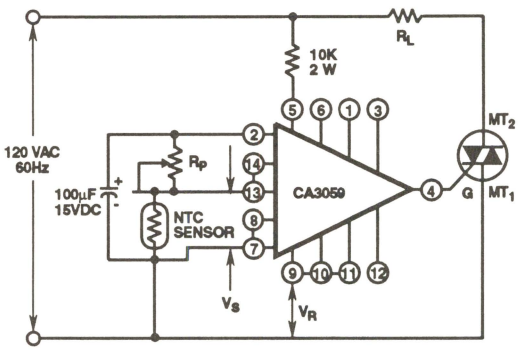


FIGURE 29. CA3059 ON/OFF TEMP. CONTROLLER

For precise temperature control applications, the proportional control technique with synchronous switching is employed. The transfer curve for this type of controller is shown in Figure 30B. In this case, the duty cycle of the power supplied to the load is varied with the demand for heat required and the thermal time constant (inertia) of the system. For example, when the temperature setting is increased in an of/off type of controller, full power (100 percent duty cycle) is supplied to the system This effect results in significant temperature excursions because there is no anticipatory circuit to reduce the power gradually before the actual set temperature is achieved. However, in a proportional control technique, less power is supplied to the load (reduced duty cycle) as the error signal is reduced (sensed temperature approaches the set temperature).

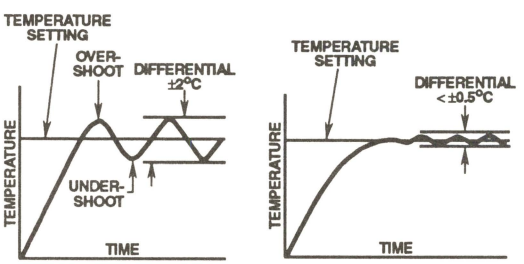


FIGURE 30A. FIGURE 30B.

FIGURE 30. TRANSFER CHARACTERISTICS OF A. ON/OFF AND B. PROPORTIONAL CONTROL SYSTEMS

Before such a system is implemented, a time base is chosen so that the on time of the triac is varied within this time base. The ratio of the on-to-off time of the triac within this time interval depends on the thermal time constant of the system and the selected temperature setting. Figure 31 illustrates the principle of proportional control. For this operation, power is supplied to the load until the ramp voltage reaches a value greater than the DC control signal supplied to the opposite side of the differential amplifier. The triac then remains off for the remainder of the time base period. As a result, power is "proportioned" to the load in a direct relation to the heat demanded by the system.

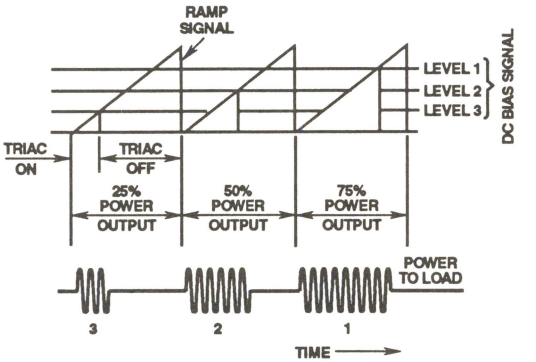
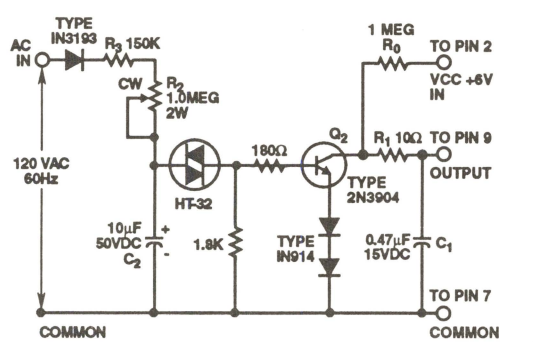


FIGURE 31. PRINCIPLES OF PROPORTIONAL CONTROL

For this application, a simple ramp generator can be realized with a minimum number of active and passive components. A ramp having good linearity is not required for proportional operation because of the nonlinearity of the thermal system and the closed loop type of control. In the circuit shown in Figure 32, the ramp voltage is generated when the capacitor C_1 charges through resistors R_0 and R_1. The time base of the ramp is determined by resistors R_2 and R_3, capacitor C_2, and the breakover voltage of the Teccor HT-32 diac.



All Resistors 1/2 Watt Unless Otherwise Specified

Pin Connections Refer to the CA3059

FIGURE 32. RAMP GENERATOR

When the voltage across C_2 reaches approximately 32V, the diac switches and turns on the 2N3904 transistor and 1N914 diodes. The capacitor C_1 then discharges through the collector-to-emitter

junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through adjustment of R_2. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with respect to the period of the 60Hz line voltage. Figure 33 shows a triac connected for the proportional mode.

Figure 34(a) shows a dual output temperature controller that drives two triacs. When the voltage V_S developed across the temperature sensing network exceeds the reference voltage V_{R1}, motor No. 1 turns on. When the voltage across the network drops below the reference voltage V_{R2}, motor No. 2 turns on. Because the motors are inductive, the currents I_{M1} lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Figure 34(b).

The problem of driving inductive loads such as these motors by the narrow pulses generated by the zero-voltage switch is solved by use of the sensitive gate triac. The high sensitivity of this device (3mA maximum) and low latching current (approximately 9mA) permit synchronous operation of the temperature controller circuit. In Figure 34(a), it is apparent that, though the gate pulse V_G of triac Y_1 has elapsed, triac Y_2 is switched on by the current through R_{L1}. The low latching current of the sensitive gate triac results in dissipation of only 2W in R_{L1}, as opposed to 10 to 20W when devices that have high latching currents are used.

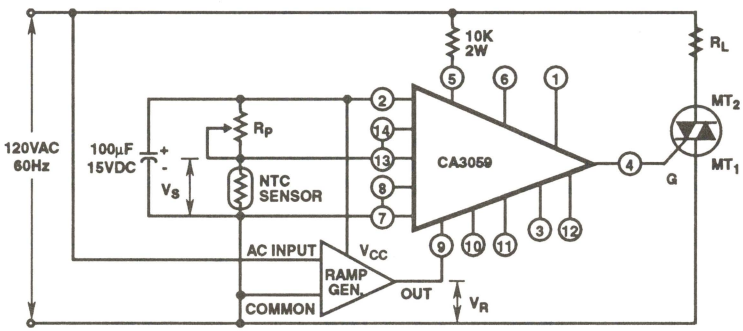


FIGURE 33. CA3059 PROPORTIONAL TEMPERATURE CONTROLLER

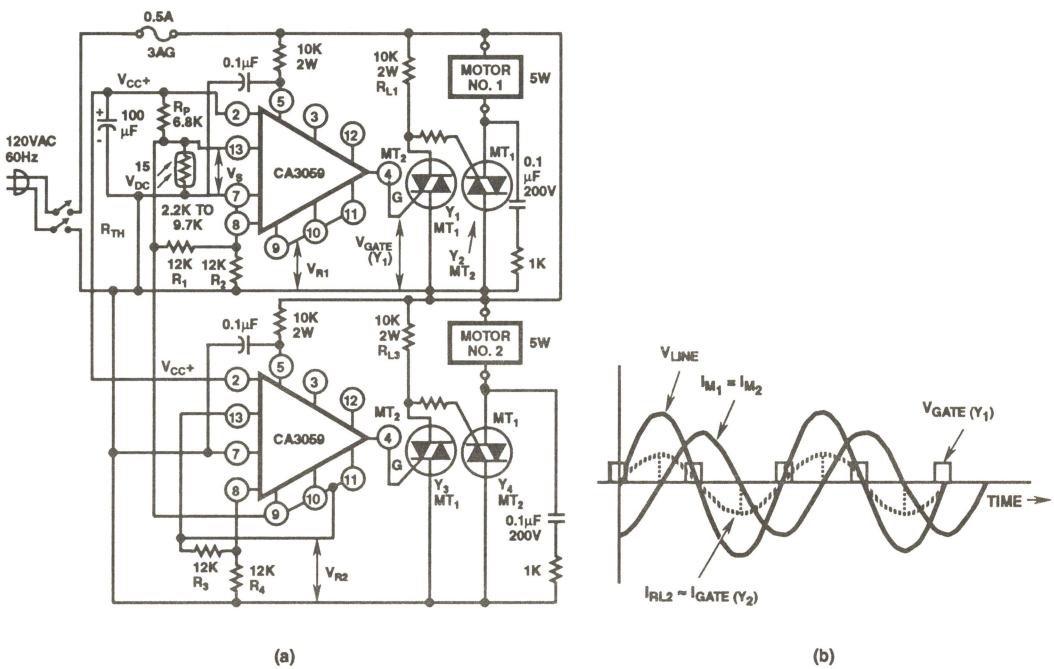


FIGURE 34. DUAL OUTPUT, OVER-UNDER TEMPERATURE CONTROLLER (a) CIRCUIT, (b) VOLTAGE AND CURRENT WAVEFORMS

Electric Heat Application

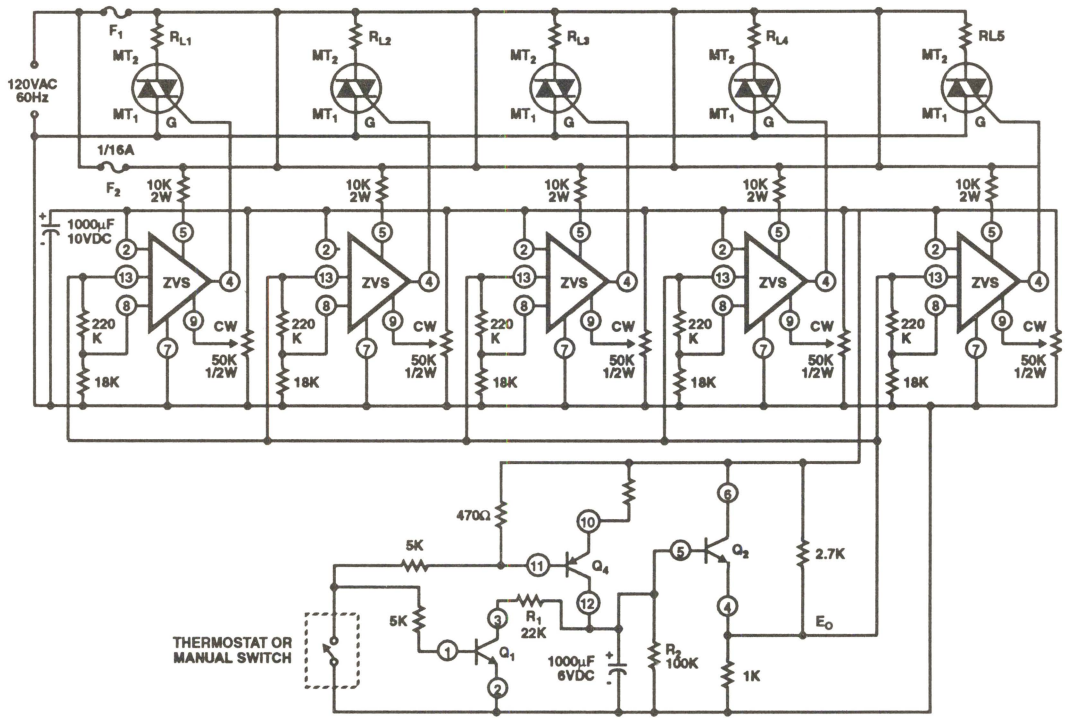
For electric heating applications, the 40A triac and the zero-voltage switch constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wear-out from the switching transients. The salient features of the 40A triac are as follows:

1. 300A single surge capability (for operation at 60Hz).
2. A typical gate sensitivity of 20mA in the I(+) and III(+) modes.
3. Low on state voltage of 1.5V maximum at 40A.
4. Available V_{DROM} equal to 600V.

Figure 35 shows the circuit diagram of a synchronous switching heat staging controller that is used for electric heating systems. Loads as heavy as 5kW are switched sequentially at zero-voltage to eliminate RFI and prevent a dip in line voltage that would occur if the full 25kW were to be switched simultaneously.

Transistor Q_1 and Q_4 are used as a constant current source to charge capacitor C in a linear manner. Transistor Q_2 acts as a buffer stage. When the thermostat is closed, a ramp voltage is provided at output E_O. At approximately 3 second intervals, each 5kW heating element is switched onto the power system by its respective triac. When there is no further demand for heat, the thermostat opens, and capacitor C discharges through R1 and R2 to cause each triac to turn off in the reverse heating sequence. It should be noted that some half cycling occurs before the heating element is switched fully on. This condition can be attributed to the inherent dissymmetry of the triac and is further aggravated by the slow rising ramp voltage applied to one of the inputs. The timing diagram in Figure 36 shows the turn-on and turn-off sequence of the heating system being controlled.

Seemingly, the basic method shown in Figure 35 could be modified to provide proportional control in which the number of heating elements switched into the system, under any given thermal load, would be a function of the BTU's required by the system or the temperature differential between an indoor and outdoor sensor within the total system environment. That is, the closing of the thermostat would not switch in all the heating elements within a short time interval, which inevitable results in undesired temperature excursions, but would switch in only the number of heating elements required to satisfy the actual heat load.



All Resistors 1/2W, Unless Otherwise Specified.
Transistors Q_1, Q_2 and Q_4 are Part of CA3096E Integrated Circuit N-P-N/P-N-P Transistor Array.

FIGURE 35. SYNCHRONOUS SWITCHING HEAT STAGING CONTROLLER USING A SERIES OF ZERO-VOLTAGE SWITCHES

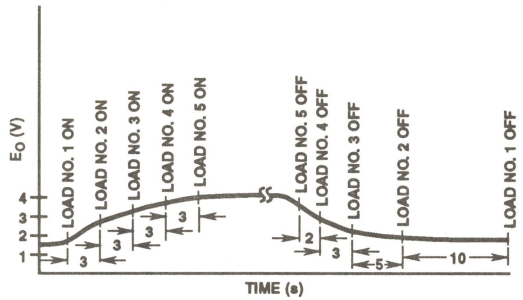


FIGURE 36. RAMP VOLTAGE WAVEFORM FOR THE HEAT STAGING CONTROLLER

Oven/Broiler Control

Zero-voltage switching is demonstrated in the oven control circuit shown in Figure 37. In this circuit, a sensor element is included in the oven to provide a closed loop system for accurate control of the oven temperature.

As shown in Figure 37, the temperature of the oven can be adjusted by means of potentiometer R_1, which acts, together with the sensor, as a voltage divider at terminal 13. The voltage at terminal 13 is compared to the fixed bias at terminal 9 which is set by internal resistors R_4 and R_5. When the oven is cold and the resistance of the sensor is high, transistors Q_2 and Q_4 are off, a pulse of gate current is applied to the triac, and heat is applied to the oven. Conversely, as the desired temperature is reached, the bias at terminal 13 turns the triac off. The closed loop feature then cycles the oven element on and off to maintain the desired temperature to approximately ±2°C of the set value. Also, as has been noted, external resistors between terminals 13 and 8, and 7 and 8, can be used to vary this temperature and provide hysteresis. In Figure 11, a circuit that provides approximately 10 percent hysteresis is demonstrated.

In addition to allowing the selection of a hysteresis value, the flexibility of the control circuit permits incorporation of other features. A PTC sensor is readily used by interchanging terminals 9 and 13 of the circuit shown in Figure 37 and substituting the PTC for the NTC sensor. In both cases, the sensor element is directly returned to the system ground or common, as is often desired. Terminal 9 can be connected by external resistors to provide for a variety of biasing, e.g., to match a lower resistance sensor for which the switching point voltage has been reduced to maintain the same sensor current.

To accommodate the self-cleaning feature, external switching, which enables both broiler and oven units to be paralleled, can easily be incorporated in the design. Of course, the potentiometer must be capable of a setting such that the sensor, which must be characterized for the high, self-clean temperature, can monitor and establish control of the high temperature, self-clean mode. The ease with which this self-clean mode can be added makes the overall solid state systems cost competitive with electromechanical systems of comparable capability. In addition, the system incorporates solid-state reliability while being neater, more easily calibrated, and containing less costly system wiring.

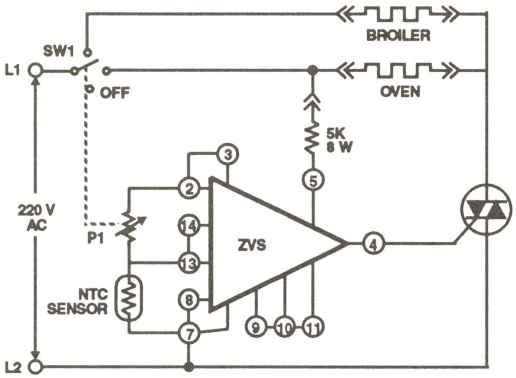


FIGURE 37. SCHEMATIC DIAGRAM OF BASIC OVEN CONTROL

Integral Cycle Temperature Controller (No half cycling)

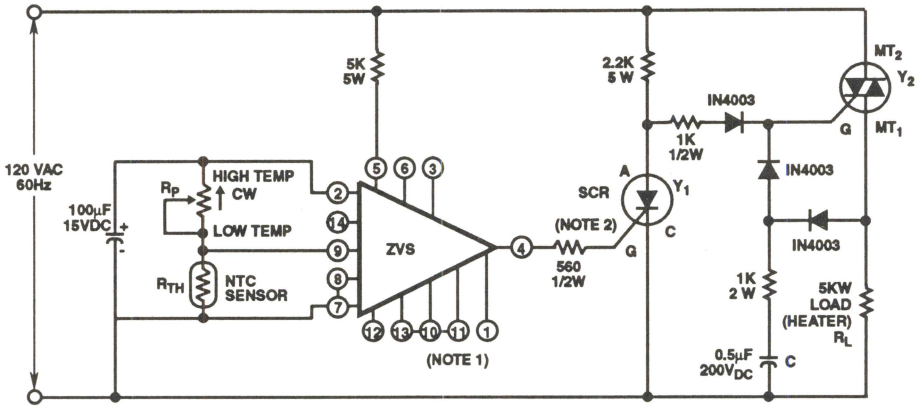
If a temperature controller which is completely devoid of half cycling and hysteresis is required, then the circuit shown in Figure 38 may be used. This type of circuit is essential for applications in which half cycling and the resultant DC component could cause overheating of a power transformer on the utility lines.

In the integral cycle controller, when the temperature being controlled is low, the resistance of the thermistor is high, and an output signal at terminal 4 of zero volts is obtained. The SCR (Y_1), therefore, is turned off. The triac (Y_2) is then triggered directly from the line on positive cycles of the AC voltage. When Y_2 is triggered and supplies power to the load R_L, capacitor C is charged to the peak of the input voltage. When the AC line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half cycle to provide only integral cycles of AC power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the zero-voltage switch. The SCR then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned off. The cycle repeats when the SCR is again turned OFF by the zero-voltage switch.

The circuit shown in Figure 39 is similar to the configuration in Figure 38 except that the protection circuit incorporated in the zero-voltage switch can be used. In this new circuit, the NTC sensor is connected between terminals 7 and 13, and transistor Q_0 inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR (Y_1). The internal power supply of the zero-voltage switch supplies bias current to transistor Q_0.

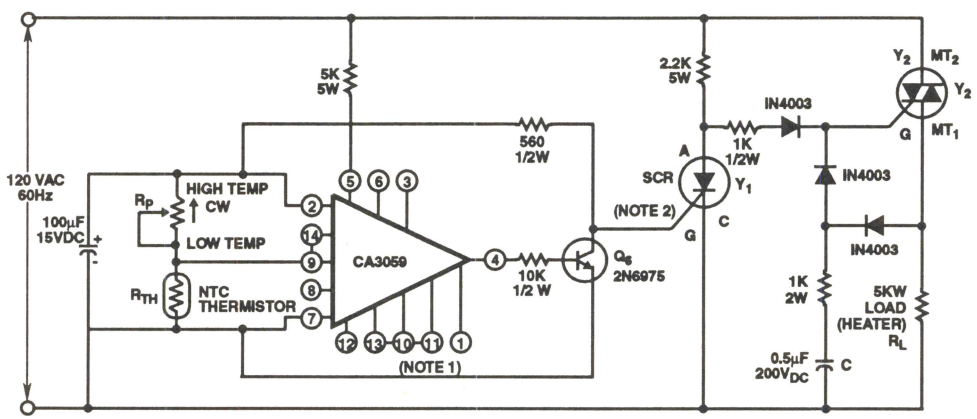
Of course, the circuit shown in Figure 39 can readily be converted to a **true proportional integral cycle temperature controller** simply by connection of a positive going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed in this Note.



NOTE:

1. For proportional operation open terminals 10, 11 and 13, and connect positive ramp voltage to terminal 13.
2. SCR selected for I_{GT} = 6mA maximum.

FIGURE 38. INTEGRAL CYCLE TEMPERATURE CONTROLLER IN WHICH HALF CYCLING EFFECT IS ELIMINATED



NOTE:

1. For proportional operation open terminals 9, 10 and 11, and connect positive ramp voltage to terminal 9.
2. SCR selected for I_{GT} = 6mA maximum.

FIGURE 39. CA3059 INTEGRAL CYCLE TEMPERATURE CONTROLLER THAT FEATURES A PROTECTION CIRCUIT AND NO HALF CYCLING EFFECT

Thermocouple Temperature Control

Figure 40 shows the CA3080A operating as a preamplifier for the zero-voltage switch to form a zero-voltage switching circuit for use with thermocouple sensors.

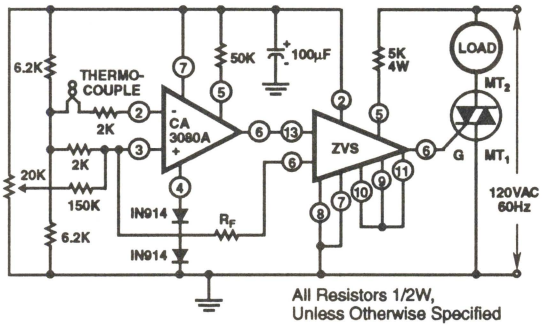
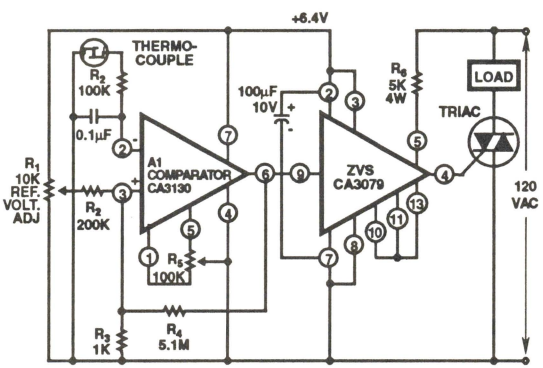


FIGURE 40. THERMOCOUPLE TEMPERATURE CONTROL WITH ZERO-VOLTAGE SWITCHING

Thermocouple Temperature Control with Zero-Voltage Load Switching

Figure 41 shows the circuit diagram of a thermocouple temperature control system using zero-voltage load switching. It should be noted that one terminal of the thermocouple is connect to one leg of the supply line. Consequently, the thermocouple can be "ground referenced", provided the appropriate leg of the AC line is maintained at ground. The comparator, A_1 (a CA3130), is powered from a 6.4V source of potential provided by the zero-voltage switch (ZVS) circuit (a CA3079). The ZVS, in turn, is powered off-line through a series dropping resistor R_6. Terminal 4 of the ZVS provides trigger pulses to the gate of the load switching triac in response to an appropriate control signal at terminal 9.



Hysteresis = R3/R4 x 6.4V = 1K/5.1M x 6.4V = 1.25mV

FIGURE 41. THERMOCOUPLE TEMPERATURE CONTROL WITH ZERO-VOLTAGE SWITCHING

The CA3130 is an ideal choice for the type of comparator circuit shown in Figure 41 because it can "compare" low voltages (such as those generated by a thermocouple) in the proximity of the negative supply rail. Adjustment of potentiometer R_1 drives the voltage divider network R_3, R_4 so that reference voltages over the range of 0 to 20mV can be applied to noninverting terminal 3 of the comparator. Whenever the voltage developed by the thermocouple at terminal 2 is more positive than the reference voltage applied at terminal 3, the comparator output is toggled so as to sink current from terminal 9 of the ZVS; gate pulses are then no longer applied to the triac. As shown in Figure 41, the circuit is provided with a control point "hysteresis" of 1.25mV.

Nulling of the comparator is performed by means of the following procedure: Set R_1 at the low end of its range and short the thermocouple output signal appropriately. If the triac is in the conductive mode under these conditions, adjust nulling potentiometer R_5 to the point at which triac conduction is interrupted. On the other hand, if the triac is in the nonconductive mode under the conditions above, adjust R_5 to the point at which triac conduction commences. The thermocouple output signal should then be unshorted, and R_1 can be set to the voltage threshold desired for control circuit operation.

Machine Control and Automation

The earlier section on interfacing techniques indicated several techniques of controlling AC loads through a logic system. Many types of automatic equipment are not complex enough or large enough to justify the cost of a flexible logic system. A special circuit, designed only to meet the control requirements of a particular machine, may prove more economical. For example, consider the simple machine shown in Figure 42; for each revolution of the motor, the belt is advanced a prescribed distance, and the strip is then punched. The machine also has variable speed capability.

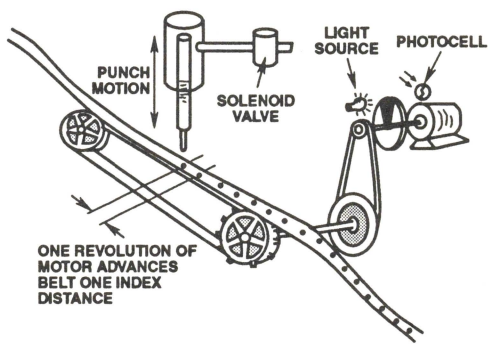


FIGURE 42. STEP-AND-PUNCH MACHINE

The typical electromechanical control circuit for such a machine might consist of a mechanical cambank driven by a separate variable speed motor, a time delay relay, and a few logic and power relays. Assuming use of industrial grade controls, the control system could get quite costly and large. Of greater importance is the necessity to eliminate transients generated each time a relay or switch energizes and deenergizes the solenoid and motor. Figure 43 shows such transients, which might not affect the operation of this machine, but could affect the more sensitive solid-state equipment operating in the area.

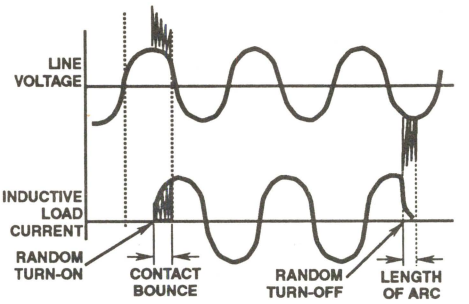


FIGURE 43. TRANSIENTS GENERATED BY RELAY CONTACT BOUNCE AND NONZERO TURN OFF OF INDUCTIVE LOAD.

A more desirable system would use triacs and zero-voltage switching to incorporate the following advantages:

1. Increased reliability and long life inherent in solid-state devices as opposed to moving parts and contacts associated with relays.
2. Minimized generation of EMI/RFI using zero-voltage switching techniques in conjunction with thyristors.
3. Elimination of high voltage transients generated by relay contact bounce and contacts breaking inductive loads, as shown in Figure 42.
4. Compactness of the control system.

The entire control system could be on one printed circuit board, and an overall cost advantage would be achieved. Figure 44 is a timing diagram for the proposed solid-state machine control, and Figure 45 is the corresponding control schematic. A variable speed machine repetition rate pulse is set up using either a unijunction oscillator or a transistor a stable multivibrator in conjunction with a 10ms one shot multivibrator. The first zero voltage switch in Figure 45 is used to synchronize the entire system to zero-voltage crossing. Its output is inverted to simplify adaptation to the rest of the circuit. The center zero-voltage switch is used as an interface for the photocell, to control one revolution of the motor. The gate drive to the motor triac is continuous DC, starting at zero voltage crossing. The motor is initiated when both the machine rate pulse and the zero-voltage sync are at low voltage. The bottom zero-voltage switch acts as a time delay for pulsing the solenoid. The inhibit input, terminal 1, is used to assure that the solenoid will not be operated while the motor is running. The time delay can be adjusted by varying the reference level (50K potentiometer) at terminal 13 relative to the capacitor charging to that level on terminal 9. The capacitor is reset by the SCR during the motor operation. The gate drive to the solenoid triac is direct current. Direct current is used to trigger both the motor and solenoid triacs because it is the most desirable means of switching a triac into an inductive load. The output of the zero-voltage switch will be continuous DC by connecting terminal 12 to common. The output under DC operation should be limited to 20mA. The motor triac is synchronized to zero crossing because it is a high current inductive load and there is a change of generating RFI. The solenoid is a very low current inductive load, so there would be little chance of generating RFI; therefore, the initial triac turn-on can be random which simplifies the circuitry.

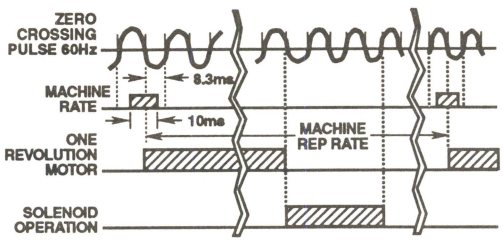


FIGURE 44. TIMING DIAGRAM FOR SOLID-STATE MACHINE CONTROL

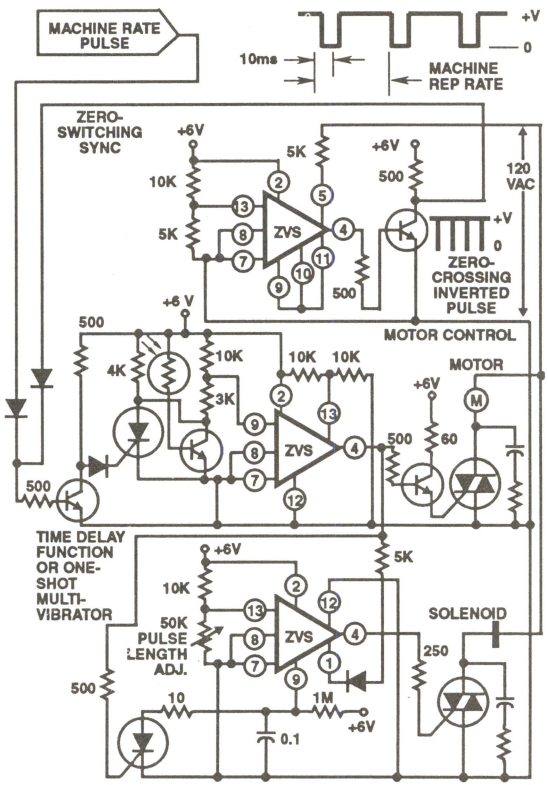


FIGURE 45. SCHEMATIC OF PROPOSED SOLID-STATE MACHINE CONTROL

This example shows the versatility and advantages of the Harris zero-voltage switch used in conjunction with triacs as interfacing and control elements for machine control.

400Hz Triac Applications

The increased complexity of aircraft control systems, and the need for greater reliability than electromechanical switching can offer, has led to the use of solid-state power switching in

aircraft. Because 400Hz power is used almost universally in aircraft systems, Harris offers a complete line of triacs rated for 400Hz applications. Use of the Harris zero-voltage switch in conjunction with these 400Hz triacs results in a minimum of RFI, which is especially important in aircraft.

Areas of application for 400Hz triacs in aircraft include:

1. Heater controls for food warming ovens and windshield defrosters
2. Lighting controls for instrument panels and cabin illumination
3. Motor controls and solenoid controls
4. Power supply switches

Lamp dimming is a simple triac application that demonstrates an advantage of 400Hz power over 60Hz power. Figure 46 shows the adjustment of lamp intensity by phase control of the 60Hz line voltage. RFI is generated by the step functions of power each half cycle, requiring extensive filtering. Figure 47 shows a means of controlling power to the lamp by the zero-voltage switching technique. Use of 400Hz power makes possible the elimination of complete or half cycles within a period (typically 17.5ms) without noticeable flicker. Fourteen different levels of lamp intensity can be obtained in this manner. A line synced ramp is set up with the desired period and applied to terminal No. 9 of the differential amplifier within the zero-voltage switch, as shown in Figure 48. The other side of the differential amplifier (terminal No. 13) uses a variable reference level, set by the 50K potentiometer. A change of the potentiometer setting changes the lamp intensity.

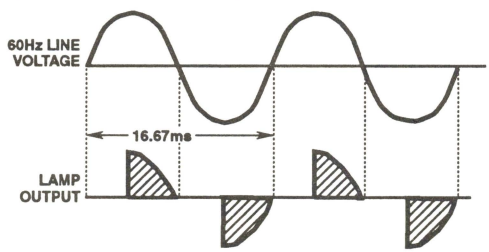


FIGURE 46. WAVEFORMS FOR 60Hz PHASE CONTROLLED LAMP DIMMER

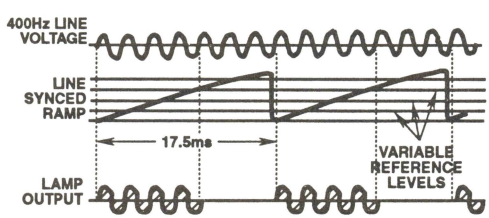


FIGURE 47. WAVEFORMS FOR 400Hz ZERO-VOLTAGE SWITCHED LAMP DIMMER

In 400Hz applications it may be necessary to widen and shift the zero-voltage switch output pulse (which is typically 12ms wide and centered on zero-voltage crossing), to assure that sufficient latching current is available. The 4K resistor (terminal No. 12 to common) and the 0.015µF capacitor (terminal No. 5 to common) are used for this adjustment.

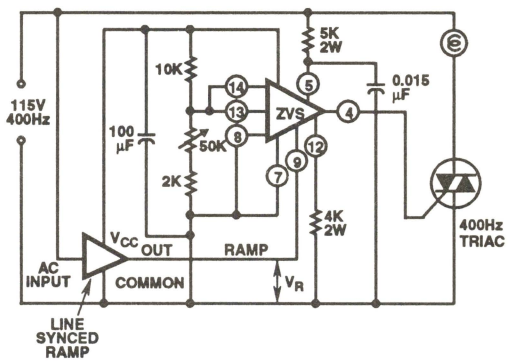


FIGURE 48. CIRCUIT DIAGRAM FOR 400Hz ZERO-VOLTAGE SWITCHED LAMP DIMMER

Solid-State Traffic Flasher

Another application which illustrates the versatility of the zero-voltage switch, when used with Harris thyristors, involves switching traffic control lamps. In this type of application, it is essential that a triac withstand a current surge of the lamp load on a continuous basis. This surge results from the difference between the cold and hot resistance of the tungsten filament. If it is assumed that triac turn-on is at 90 degrees from the zero-voltage crossing, the first current surge peak is approximately ten times the peak steady state rms value.

When the triac randomly switches the lamp, the rate of current rise di/dt is limited only by the source inductance. The triac di/dt rating may be exceeded in some power systems. In many cases, exceeding the rating results in excessive current concentrations in a small area of the device which may produce a hot spot and lead to device failure. Critical applications of this nature require adequate drive to the triac gate for fast turn on. In this case, some inductance may be required in the load circuit to reduce the initial magnitude of the load current when the triac is passing through the active region. Another method may be used which involves the switching of the triac at zero line voltage. This method involves the supply of pulses to the triac gate only during the presence of zero voltage on the AC line.

Figure 49 shows a circuit in which the lamp loads are switched at zero line voltage. This approach reduces the initial di/dt, decreases the required triac surge current ratings, increases the operating lamp life, and eliminates RFI problems. This circuit consists of two triacs, a flip-flop (FF-1), the zero-voltage switch, and a diac pulse generator. The flashing rate in this circuit is controlled by potentiometer R, which provides between 10 and 120 flashes per minute. The state of FF-1 determines the triggering of triacs Y_1 or Y_2 by the output pulses at terminal 4 generated by the zero crossing circuit. Transistors Q_1 and Q_2 inhibit these pulses to the gates of the triacs until the triacs turn on by the logical "1" (V_{CC} high) state of the flip-flop.

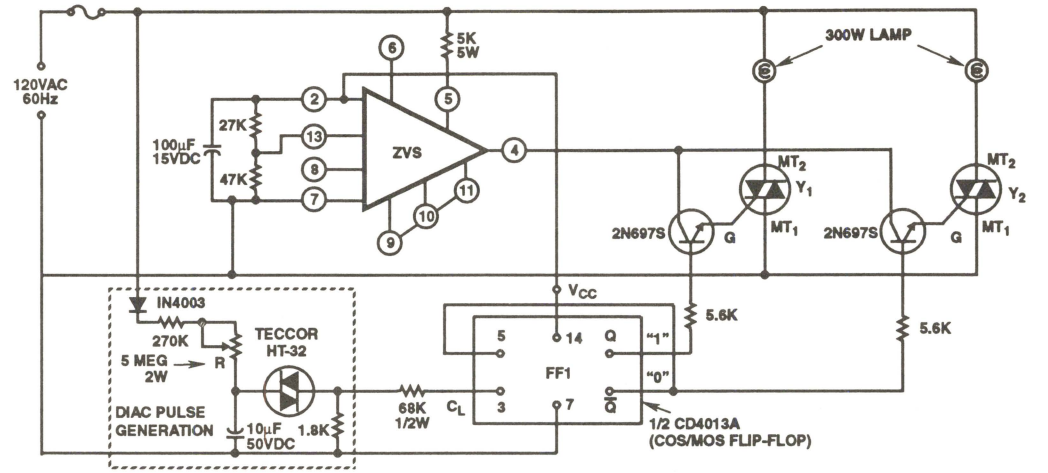


FIGURE 49. SYNCHRONOUS SWITCHING TRAFFIC FLASHER

The arrangement describe can also be used for a synchronous, sequential traffic controller system by addition of one triac, one gating transistor, a "divide-by-three" logic circuit, and modification in the design of the diac pulse generator. Such a system can control the familiar red, amber, and green traffic signals that are found at many intersections.

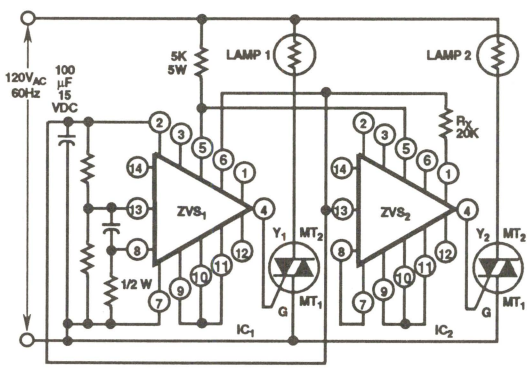


FIGURE 50. SYNCHRONOUS LIGHT FLASHER

Synchronous Light Flasher

Figure 50 shows a simplified version of the synchronous switching traffic light flasher shown in Figure 49. Flash rate is set by use of the curve shown in Figure 16. If a more precise flash rate is required, the ramp generator described previously may be used. In this circuit, ZVS_1 is the master control unit and ZVS_2 is slaved to the output of ZVS_1 through its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on ZVS_1 is high and ZVS_2 is inhibited by the current in R_X. When lamp No. 1 is off, ZVS_2 is not inhibited, and triac Y_2 can fire. The power supplies operate in parallel. The on/off sensing amplifier in ZVS_2 is not used.

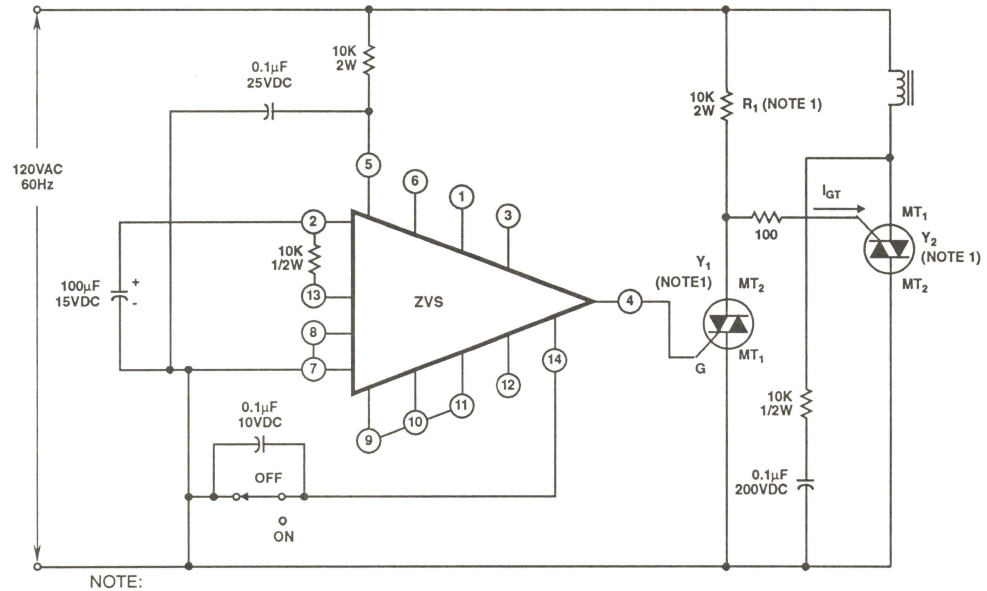
Transient Free Switch Controllers

The zero-voltage switch can be used as a simple solid-state switching device that permits AC currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Figure 51 is connected so that, after the control terminal 14 is opened, the electronic logic waits until the power line voltage reaches a zero crossing before power is applied to the load Z_L. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

The circuit shown in Figure 52 is connected to provide the opposite control logic to that of the circuit shown in Figure 51. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

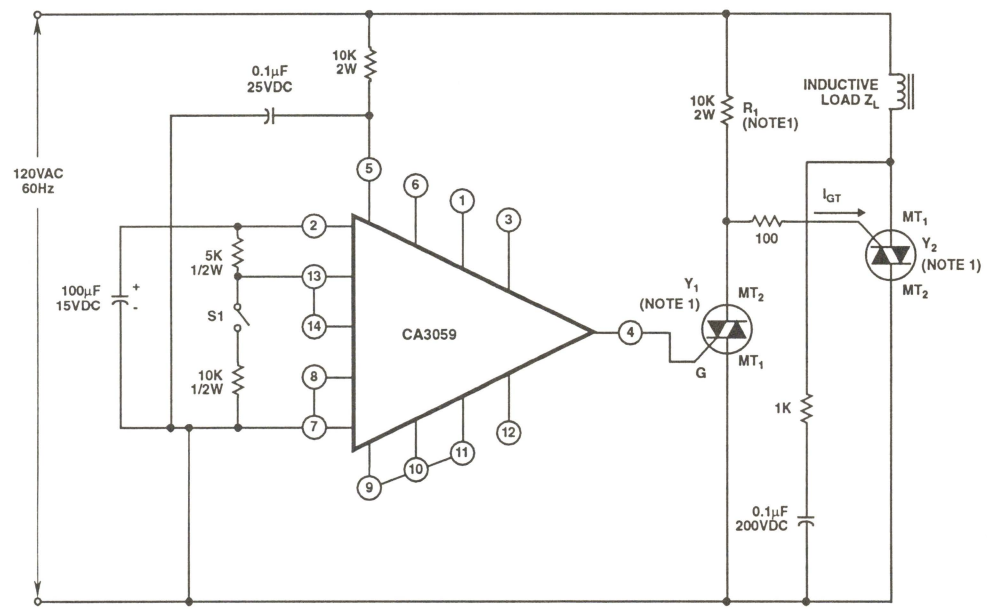
In both configurations, the maximum rms load current that can be switched depends on the rating of triac Y_2.



NOTE:

1. If Y_2, For Example, is a 40A TRIAC, then R_1 must be Decreased to Supply Sufficient I_{GT} for Y_2.

FIGURE 51. ZERO-VOLTAGE SWITCH TRANSIENT FREE SWITCH CONTROLLER IN WHICH POWER IS SUPPLIED TO THE LOAD WHEN THE SWITCH IS OPEN



NOTE:

1. If Y_2, For Example, is a 40A TRIAC, then R_1 must be Decreased to Supply Sufficient I_{GT} for Y_2.

FIGURE 52. ZERO-VOLTAGE SWITCH TRANSIENT FREE SWITCH CONTROLLER IN WHICH POWER IS APPLIED TO THE LOAD WHEN THE SWITCH IS CLOSED

Differential Comparator for Industrial Use

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic "one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The zero-voltage switch is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the zero-voltage switch, and the circuit becomes a differential comparator.

Figure 53 shows the circuit arrangement for use of the zero-voltage switch as a differential comparator. In this application, no external DC supply is required, as is the case with most commercially available integrated circuit comparators; of course, the output current capability of the zero-voltage switch is reduced because the circuit is operating in the DC mode. The 1000Ω resistor R_G, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3mA.

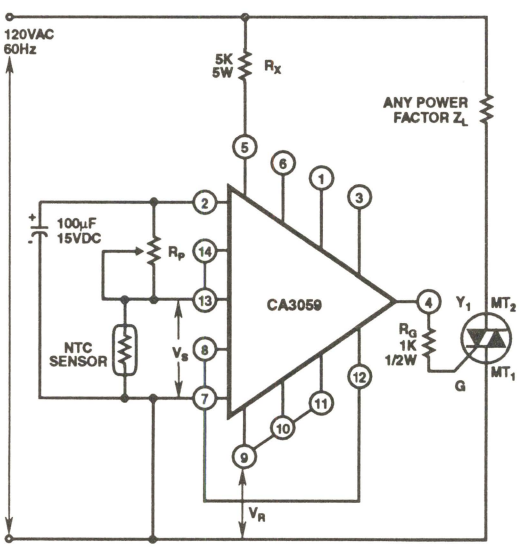


FIGURE 53. DIFFERENTIAL COMPARATOR USING THE CA3059 INTEGRATED CIRCUIT ZERO-VOLTAGE SWITCH

When the zero-voltage switch is connected in the DC mode, the drive current for terminal 4 can be determined from a curve of the external load current as a function of DC voltage from terminals 2 and 7. Of course, if additional output current is required, an external DC supply may be connected between terminals 2 and 7, and resistor R_X (shown in Figure 53) may be removed.

The chart below compares some of the operating characteristics of the zero-voltage switch, when used as a comparator, with a typical high performance commercially available integrated circuit differential comparator.

PARAMETERS	ZERO-VOLTAGE SWITCH (TYP. VALUE)	TYP. INTEGRATED CIRCUIT COMPARATOR (710)
Sensitivity	30mV	2mV
Switching Speed (Rise Time)	>20μs	90ns
Output Drive Capability	4.5V at ≤4mA (Note 1)	3.2V at ≤5.0mA

NOTE:

1. Refer to Figure 20; R_X equals 5000Ω.

Power One Shot Control

Figure 54 shows a circuit which triggers a triac for one complete half cycle of either the positive or negative alternation of the AC line voltage. In this circuit, triggering is initiated by the push button PB-1, which produces triggering of the triac near zero voltage even though the button is randomly depressed during the AC cycle. The triac does not trigger again until the button is released and again depressed. This type of logic is required for the solenoid drive of electrically operated stapling guns, impulse hammers, and the like, where load current flow is required for only one complete half cycle. Such logic can also be adapted to keyboard consoles in which contact bounce produces transmission of erroneous information.

In the circuit of Figure 54, before the button is depressed, both flip-flop outputs are in the "zero" state. Transistor Q_G is biased on by the output of flip-flop FF-1. The differential comparator which is part of the zero-voltage switch is initially biased to inhibit output pulses. When the push button is depressed, pulses are generated, but the state of Q_G determines the requirement for their supply to the triac gate. The first pulse generated serves as a "framing pulse" and does not trigger the triac but toggles FF-1. Transistor Q_G is then turned off. The second pulse triggers the triac and FF-1 which, in turn, toggles the second flip-flop FF-2. The output of FF-2 turns on transistor Q_7, as shown in Figure 55, which inhibits any further output pulses. When the push-button is released, the circuit resets itself until the process is repeated with the button. Figure 56 shows the timing diagram for the described operating sequence.

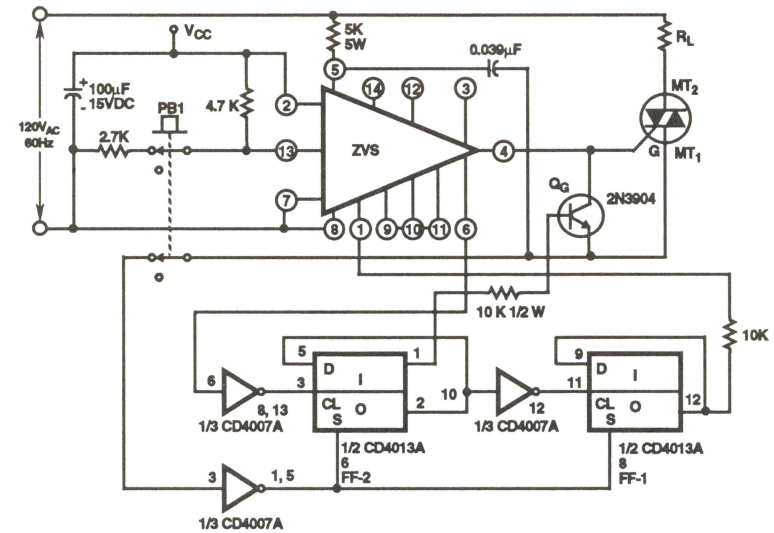


FIGURE 54. BLOCK DIAGRAM OF A POWER ONE SHOT CONTROL USING A ZERO-VOLTAGE SWITCH

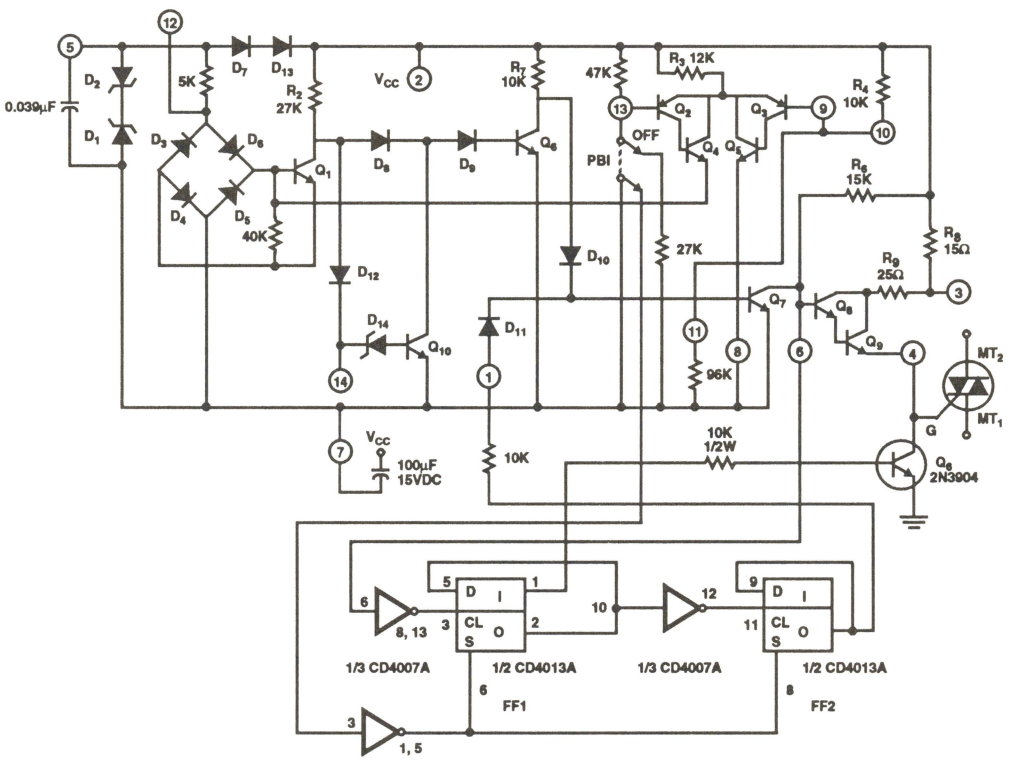


FIGURE 55. CIRCUIT DIAGRAM FOR THE POWER ONE SHOT CONTROL SHOWING CA3059 WITH PERIPHERAL COMPONENTS

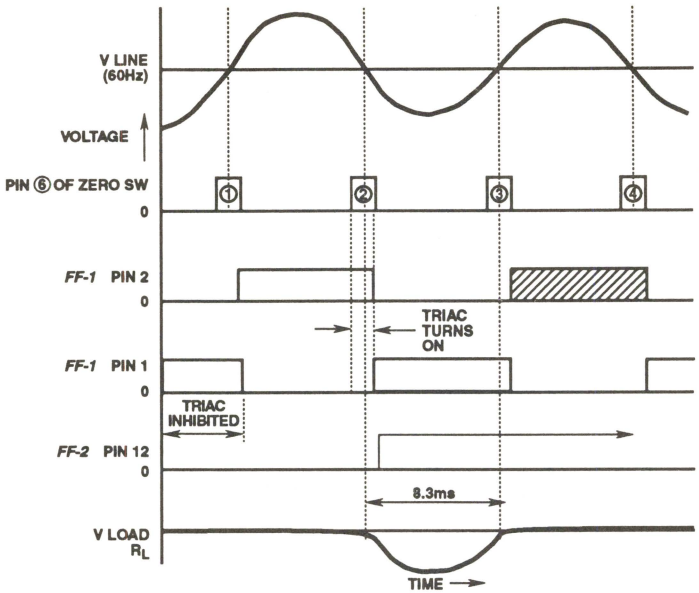


FIGURE 56. TIMING DIAGRAM FOR THE POWER ONE SHOT CONTROL

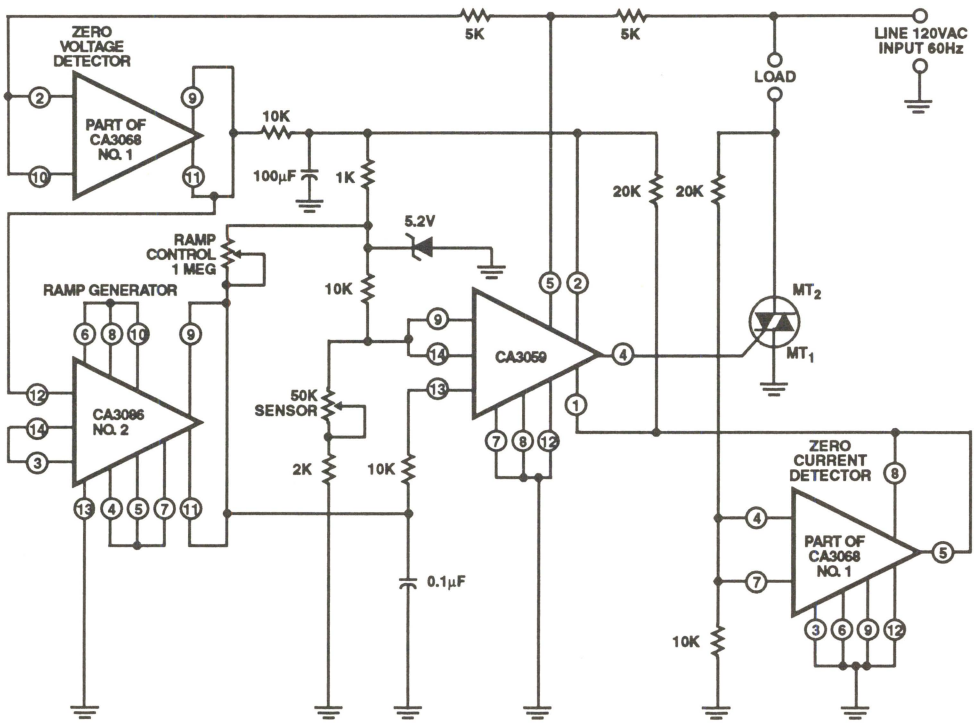


FIGURE 57. PHASE CONTROL CIRCUIT USING A CA3059 AND TWO CA3086 INTEGRATED CIRCUITS

Phase Control Circuit

Figure 57 shows a circuit using a CA3059 zero-voltage switch together with two CA3086 integrated circuit arrays to form a phase control circuit. This circuit is specifically designed for speed control of AC induction motors, but may also be used as a light dimmer. The circuit, which can be operated from a line frequency of 50Hz to 400Hz, consists of a zero-voltage detector, a line synchronized ramp generator, a zero current detector, and a line derived control circuit (i.e., the zero-voltage switch). The zero-voltage detector (part of CA3086 No. 1) and the ramp generator (CA3086 No. 2) provide a line synchronized ramp voltage output to terminal 13 of the zero-voltage switch. The ramp voltage, which has a starting voltage of 1.8V, starts to rise after the line voltage passes the zero point. The ramp generator has an oscillation frequency of twice the incoming line frequency. The slope of the ramp voltage can be adjusted by variation of the resistance of the 1MΩ ramp control potentiometer. The output phase can be controlled easily to provide 180° firing of the triac by programming the voltage at terminal 9 of the zero-voltage switch. The basic operation of the zero-voltage switch driving a thyristor with an inductive load was explained previously in the discussion on switching of inductive loads.

On/Off Touch Switch

The on/off touch switch shown in Figure 58 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the on plate is touched, current flows between the two halves of the grid, causing a positive shift in the output voltage (terminal 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero crossing triac driver. When a positive pulse occurs at terminal No. 7 of the CA3240E, the triac is turned on and held on by the CA3059 and associated positive feedback circuitry (51kΩ resistor and 36kΩ/42kΩ voltage divider). When the pulse occurs at terminal No. 1, the triac is turned off and held off in a similar manner. Note that power for the CA3240E is derived from the CA3059 internal power supply. The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while maintaining sufficiently high circuit impedance to protect against electrical shock.

Triac Power Controls for Three Phase Systems

This section describes recommended configurations for power control circuits intended for use with both inductive and resistive balanced three phase loads. The specific design requirements for each type of loading condition are discussed.

In the power control circuits described, the integrated circuit zero-voltage switch is used as the trigger circuit for the power triacs. The following conditions are also imposed in the design of the triac control circuits:

1. The load should be connected in a three wire configuration with the triacs placed external to the load; either delta or wye arrangements may be used. Four wire loads in wye configurations can be handled as three independent single phase systems. Delta configurations in which a triac is connected within each phase rather than in the incoming lines can also be handled as three independent single phase systems.
2. Only one logic command signal is available for the control circuits. This signal must be electrically isolated from the three phase power system.
3. Three separate triac gating signals are required.
4. For operation with resistive loads, the zero-voltage switching technique should be used to minimize any radio frequency interference (RFI) that may be generated.

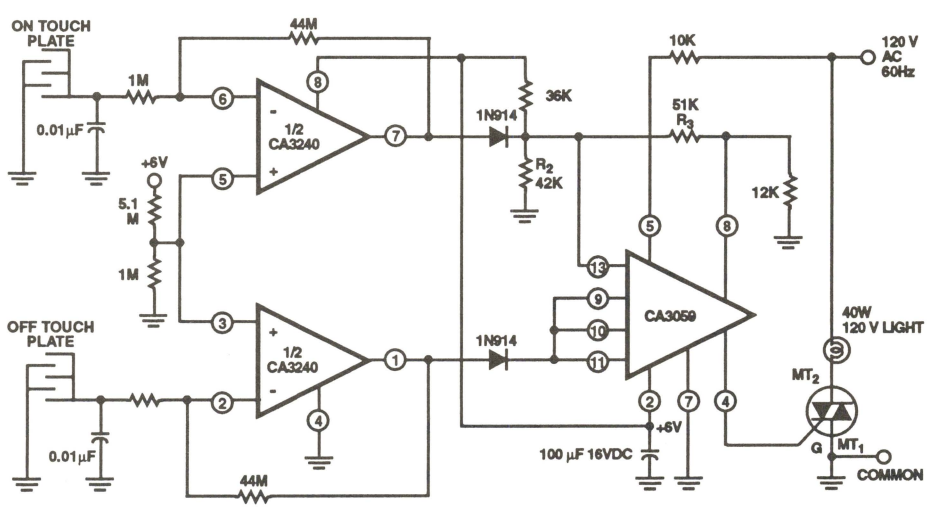


FIGURE 58. ON/OFF TOUCH SWITCH

Isolation of DC Logic Circuitry

As explained earlier under **Special Application Considerations**, isolation of the DC logic circuitry* from the AC line, the triac, and the load circuit is often desirable even in many single phase power control applications. In control circuits for polyphase power systems, however, this type of isolation is essential, because the common point of the DC logic circuitry cannot be referenced to a common line in all phases.

* The DC logic circuitry provides the low level electrical signal that dictates the state of the load. For temperature controls, the DC logic circuitry includes a temperature sensor for feedback. The Harris integrated circuit zero-voltage switch, when operated in the DC mode with some additional circuitry, can replace the DC logic circuitry for temperature controls.

In the three phase circuits described in this section, photo optic techniques (i.e., photo coupled isolators) are used to provide the electrical isolation of the DC logic command signal from the AC circuits and the load. The photo coupled isolators consist of an infrared light emitting diode aimed at a silicon photo transistor, coupled in a common package. The light emitting diode is the input section, and the photo transistor is the output section. The two components provide a voltage isolation typically of 1500V. Other isolation techniques, such as pulse transformers, magnetoresistors, or reed relays, can also be used with some circuit modifications.

Resistive Loads

Figure 59 illustrates the basic phase relationships of a balanced three phase resistive load, such as may be used in heater applications, in which the application of load power is controlled by zero-voltage switching. The following conditions are inherent in this type of application:

1. The phases are 120 degrees apart; consequently, all three phases cannot be switched on simultaneously at zero voltage.
2. A single phase of a wye configuration type of three wire system cannot be turned on.
3. Two phases must be turned on for initial starting of the system. These two phases form a single phase circuit which is out of phase with both of its component phases. The single phase circuit leads on phase by 30 degrees and lags the other phase by 30 degrees.

These conditions indicate that in order to maintain a system in which no appreciable RFI is generated by the switching action from initial starting through the steady state operating condition, the system must first be turned on, by zero-voltage switching, as a single phase circuit and then must revert to synchronous three phase operation.

Figure 60 shows a simplified circuit configuration of a three phase heater control that employs zero-voltage synchronous switching in the steady state operating condition, with random starting. In this system, the logic command to turn on the system is given when heat is required, and the command to turn off the system is given when heat is not required. Time proportioning heat control is also possible through the use of logic commands.

The three photo coupled inputs to the three zero-voltage switches change state simultaneously in response to a "logic command". The zero-voltage switches then provide a positive pulse, approximately 100µs in duration, only at a zero-voltage crossing relative to their particular phase. A balanced three phase sensing circuit is set up with the three zero-voltage switches each connected to a particular phase on their common side (terminal 7) and referenced at their high side (terminal 5), through the current limiting resistors R_4, R_5, and R_6, to an established artificial neutral point. This artificial neutral point is electrically equivalent to the inaccessible neutral point of the wye type of three wire load

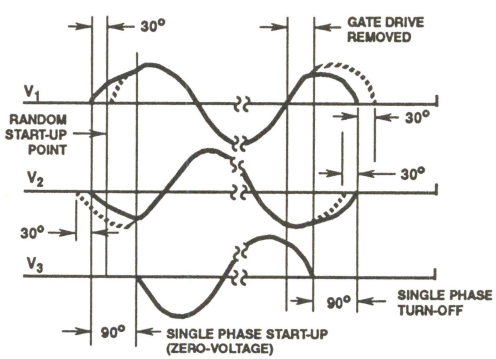


FIGURE A.

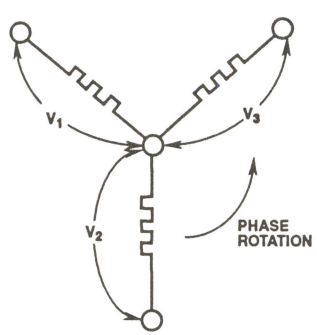


FIGURE B.

NOTE: The dashed lines indicate the normal relationship of the phases under steady state conditions. The deviation at start up and turn off should be noted.

FIGURE 59. VOLTAGE PHASE RELATIONSHIP FOR A THREE PHASE RESISTIVE LOAD WHEN THE APPLICATION OF LOAD POWER IS CONTROLLED BY ZERO-VOLTAGE SWITCHING: A. VOLTAGE WAVEFORMS, B. LOAD CIRCUIT ORIENTATION OF VOLTAGES.

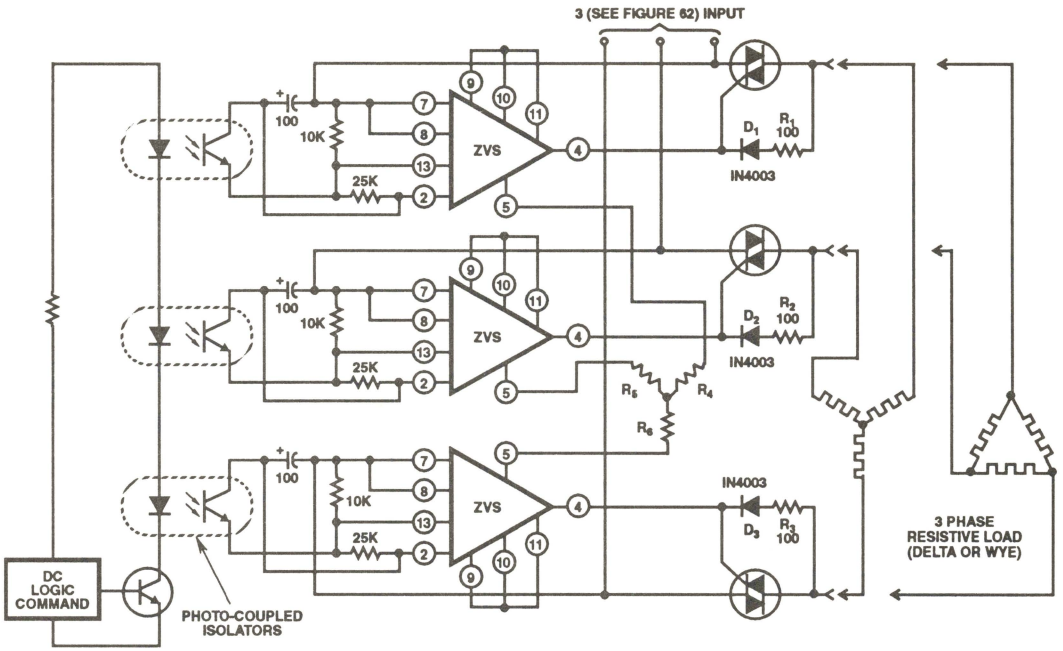


FIGURE 60. SIMPLIFIED DIAGRAM OF A THREE PHASE HEATER CONTROL THAT EMPLOYS ZERO-VOLTAGE SYNCHRONOUS SWITCHING IN THE STEADY STATE OPERATING CONDITIONS

and, therefore, is used to establish the desired phase relationships. The same artificial neutral point is also used to establish the proper phase relationships for a delta type of three wire load. Because only one triac is pulsed on at a time, the diodes (D_1, D_2, and D_3) are necessary to trigger the opposite polarity triac, and, in this way, to assure initial latching on of the system. The three resistors (R_1, R_2, and R_3) are used for current limiting of the gate drive when the opposite polarity triac is triggered on by the line voltage.

In critical applications that require suppression of all generated RFI, the circuit shown in Figure 61 may be used. In addition to synchronous steady state operating conditions, this circuit also incorporates a zero-voltage starting circuit. The start up condition is zero-voltage synchronized to a single phase, 2 wire, line-to-line circuit, comprised of phases A and B. The logic command engages the single phase start up zero-voltage switch and three phase photo coupled isolators OC1-3, OC1-4, OC1-5 through the photo coupled isolators OC1-1 and OC1-2. The single phase zero-voltage switch, which is synchronized to phases A and B, starts the system at zero voltage. As soon as start up is accomplished, the three photo coupled isolators OC1-3, OC1-4, and OC1-5 take control, and three phase synchronization begins. When the "logic command" is turned off, all control is ended, and the triacs automatically turn off when the sine wave current decreases to zero. Once the first phase turns off, the other two will turn off simultaneously, 90° later, as a single phase line-to-line circuit, as is apparent from Figure 59.

Inductive Loads

For inductive loads, zero-voltage turn on is not generally required because the inductive current cannot increase instantaneously; therefore, the amount of RFI generated is usually negligible. Also, because of the lagging nature of the inductive current, the triacs cannot be pulse fired at zero voltage. There are several ways in which the zero-voltage switch may be interfaced to a triac for inductive load applications. The most direct approach is to use the zero-voltage switch in the DC mode, i.e., to provide a continuous DC output instead of pulses at points of zero-voltage crossing. This mode of operation is accomplished by connection of terminal 12 to terminal 7, as shown in Figure 62. The output of the zero-voltage switch should also be limited to approximately 5mA in the DC mode by the 750Ω series resistor. Use of a sensitive gate triac is recommended for this application. Terminal 3 is connected to terminal 2 to limit the steady state power dissipation within the zero-voltage switch. For most three phase inductive load applications, the current handling capability of the 2.5A triac is not sufficient. Therefore, a higher current sensitive gate triac is used as a trigger triac to turn on any other currently available power triac that may be used. The trigger triac is used only to provide trigger pulses to the gate of the power triac (one pulse per half cycle); the power dissipation in this device, therefore, will be minimal.

Simplified circuits using pulse transformers and reed relays will also work quite satisfactorily in this type of application. The RC networks across the three power triacs are used for suppression of the commutating dv/dt when the circuit operates into inductive loads.

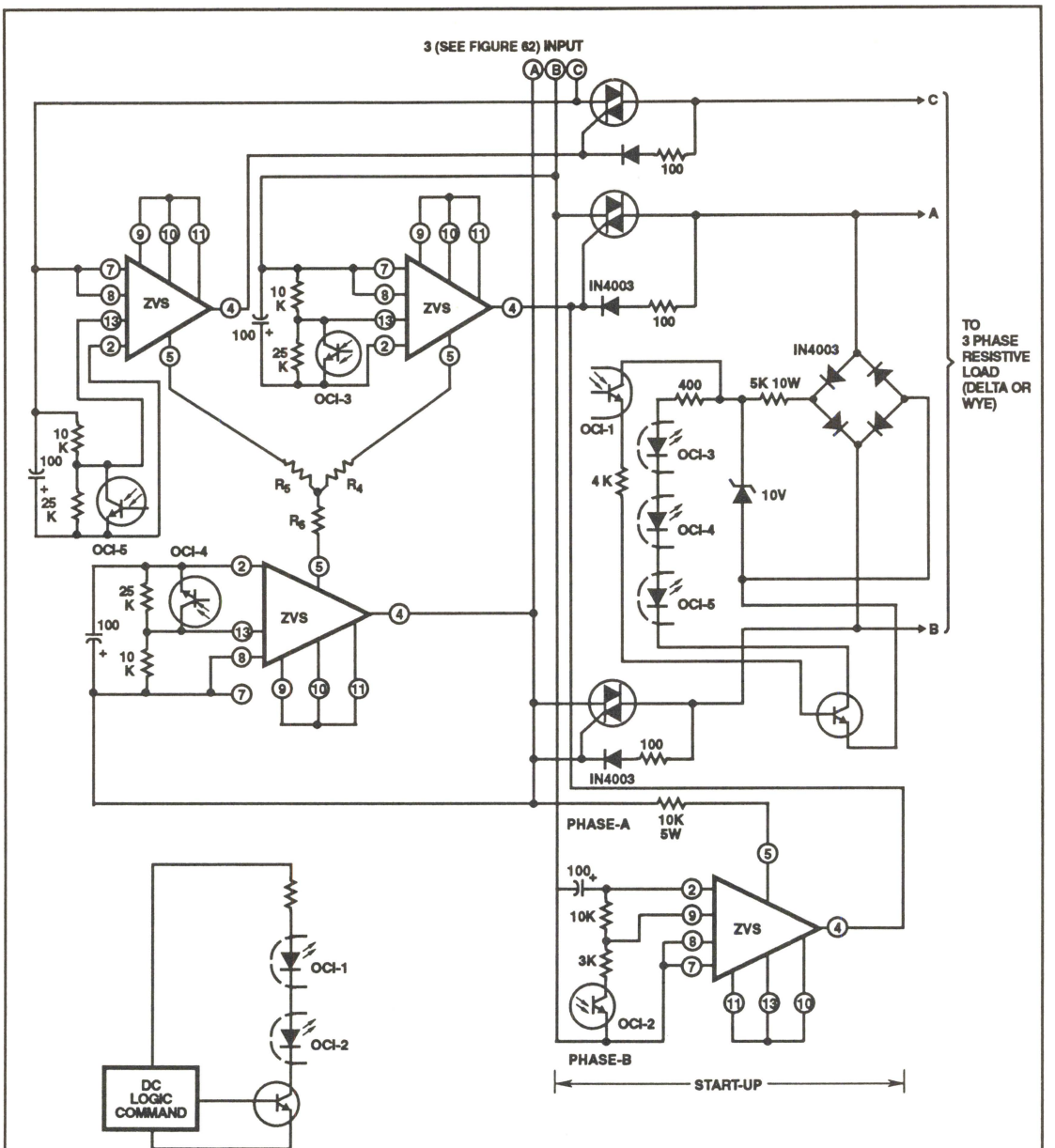


FIGURE 61. THREE PHASE POWER CONTROL THAT EMPLOYS ZERO-VOLTAGE SYNCHRONOUS SWITCHING BOTH FOR STEADY STATE OPERATION AND FOR STARTING

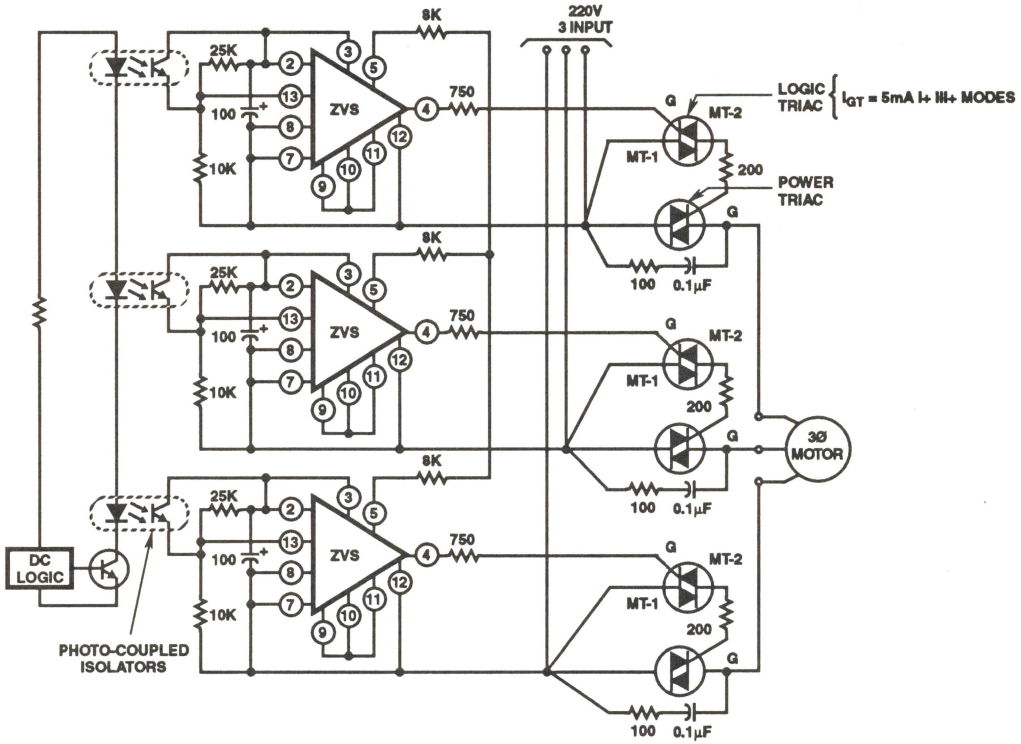


FIGURE 62. TRIAC THREE PHASE CONTROL CIRCUIT FOR AN INDUCTIVE LOAD, i.e., THREE PHASE MOTOR

Harris Semiconductor

APPNOTE

No. AN6915.1 April 1994

Harris Intelligent Power

APPLICATION OF THE CA1524 SERIES PULSE-WIDTH MODULATOR ICs

Author: Carmine Salerno

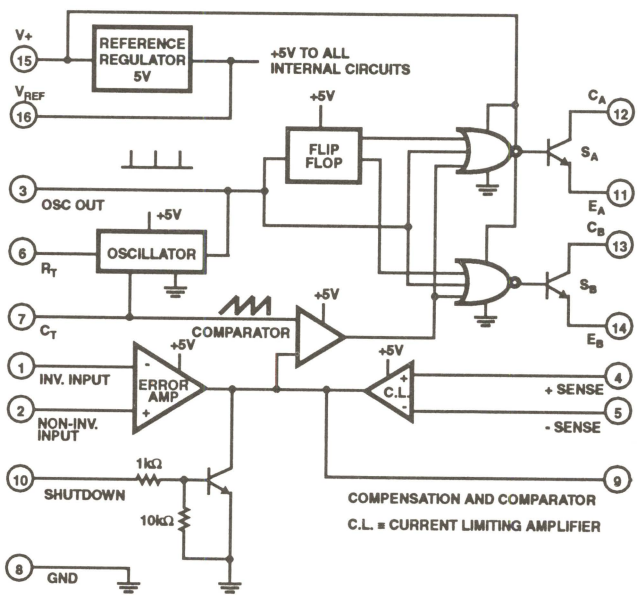
This application note reviews pulse-width modulated (PWM) circuits, and the CA1524 series of pulse-width modulator ICs particularly intended for this type of application. It also includes descriptions of basic switching-regulator circuits, the generic CA1524 Series IC, its use in a variable switched power supply application, together with a variety of its unique circuit applications.

The CA1524, CA2524, and CA3524 Series, a family of integrated circuits containing a pulse-width modulator and related control circuits, are particularly applicable to switching regulators, flyback converters, dc-to-dc converters and the like. These ICs operate with a power supply in the 8V to 40V range for use in both low and high power regulators. The CA1524 series ICs contain the following circuit functions: 5V temperature compensated zener reference, precision RC oscillator, transconductance error amplifier, current-limiting amplifier, control comparator, shutdown circuit, and dual output transistor switches. The circuit's functions make these devices attractive for a wide variety of other applications; e.g., low frequency pulse generators, automotive temperature voltage regulators, battery chargers, electronic bathroom scales, etc.

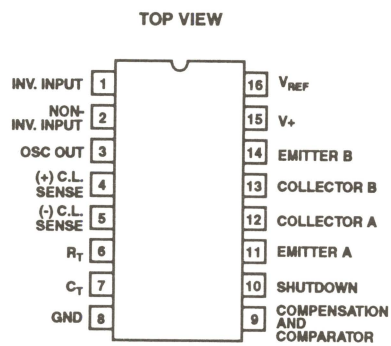
The CA1524 family of ICs is supplied in 16 lead plastic and ceramic (frit) packages, and is also available in chip form. Data on these types are found in the datasheet file number 1239.

CA1524 Series IC Features

The CA1524 PWM on-chip functions shown in the functional block diagram of Figure 1 include an error amplifier, a comparator, an oscillator, a flip-flop, and a voltage regulator. The error amplifier senses the difference between the actual and the desired regulator output and applies this signal to the comparator's positive input. The output of this stage is in turn a function of the error signal and the oscillator's ramp voltage.



a) FUNCTIONAL BLOCK DIAGRAM



b) TERMINAL CONNECTION DIAGRAM

FIGURE 1. CA1524 SERIES ICs

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The oscillator's output pulses alternately trigger the flip-flop, whose output ultimately provides the circuits push-pull drive signal via the NOR-gates and the output transistors. The other NOR-gate inputs control the duration of the output pulses. Depending upon the oscillator's output level (high or low) and the comparator's high or low status, the "on" duty-cycle of the NOR gate can vary from 0 to 45 percent. It should be noted, that the NOR gates are on alternately. Thus, by connecting the output transistors in parallel, an effective on time of 0% to 90% and a wide voltage regulation range can be attained.

Comparative Operating Efficiencies In Series-Pass and PWM Types of Voltage Regulators

The series-pass circuit is a classical means of implementing the voltage regulator function; its simple and easy to design, but comparatively inefficient when required to operate over a range of supply voltages and output currents. The need to improve operational efficiency, in recent years, has been one of the major factors motivating engineers to use the PWM type of voltage regulator despite its greater circuit complexity.

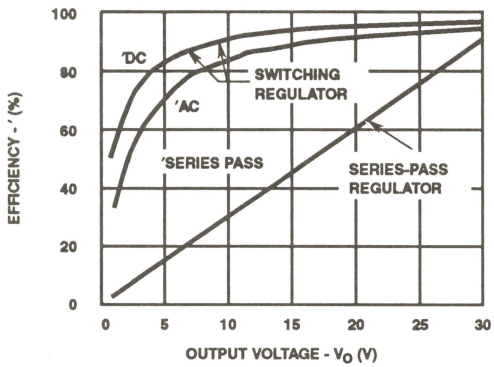
Figure 2 shows the high operating efficiency of the PWM type of voltage regulator design e.g., using CA1524 and compares it with that of a conventional linear series-pass circuit. In a series-pass type of regulated power supply, the pass transistor is biased in the linear region, to permit good line and load regulation and dynamic response, but at a sacrifice in efficiency. This loss in efficiency occurs as a result of the power dissipated in the pass transistor, i.e., the product of the voltage drop and the current flowing through it. In a series-pass regulator, the output current is about equal to the input current, therefore, the overall efficiency ≅ the ratio V_O/V_{IN}.

It is, therefore, apparent that the input/output voltage differential must be kept at a minimum if high efficiency is to be achieved. Dissipation in the pass device is $(V_{IN} - V_{DD})$ I_{PASS}, $(V_{IN} - V_O)$ is typically 2V to 3V. There are additional small operating losses in the IC itself. By way of contrast, the pass transistor for a switching-regulator control circuit is driven between two states, "on" and "off", and since the linear region is not used, loss is essentially limited to the product of the saturation voltage and the current flowing through the pass transistor during its on state. There is a small additional loss that occurs during the on/off transitions.

Additional losses in the switching regulator include diode-voltage losses, inductor-transformer core losses, and copper losses. The overall efficiency is essentially independent of input voltage or input current. A worst case theoretical value of the AC switching and DC transistor losses approaches a value equal to $V_O/(V_O + 2V)$ (assuming a diode V_{BE} and transistor V_{CE}(s) of 1V each). Therefore, a minimum input voltage of $V_O + 2V$ is needed to operate a switching regulator.

Circuit Description

The CA1524, CA2524, and CA3524 monolithic integrated circuits are designed to provide all of the control circuitry necessary for a broad range of switching regulator applications. On-chip functional blocks, shown in Figure 1, include a zener voltage reference, transconductance error amplifier, precision RC oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current limiting and shutdown circuitry. A complete schematic is shown in Figure 4



Pulse Width Modulator (PWM) Switching Regulator	Linear Series-Pass Regulator
$\eta_{DC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_O 1} = \frac{V_O}{V_O + 1}$	$\eta = \frac{P_O}{P_{IN}}$
$\eta_{AC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_O 2} = \frac{V_O}{V_O + 2}$	$\eta = \frac{V_O I_O}{V_{IN} I_{IN}} \cong \frac{V_O}{V_{IN}}$

FIGURE 2. EFFICIENCY CURVES FOR LINEAR (SERIES-PASS) REGULATOR AND PULSE-WIDTH MODULATED SWITCHING REGULATOR (PWM)

Voltage Reference Section

The CA1524 Series devices contain an internal series voltage regulator employing a zener reference to provide a nominal 5 volts output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50mA output current. For higher currents, the circuit of Figure 3 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5V supply by connecting both terminal 15 and 16 to the input voltage, which must not exceed 6V.

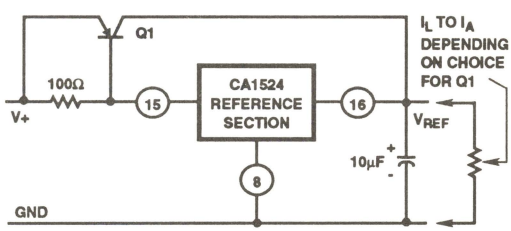


FIGURE 3. CIRCUIT FOR EXPANDING THE REFERENCE CURRENT CAPABILITY

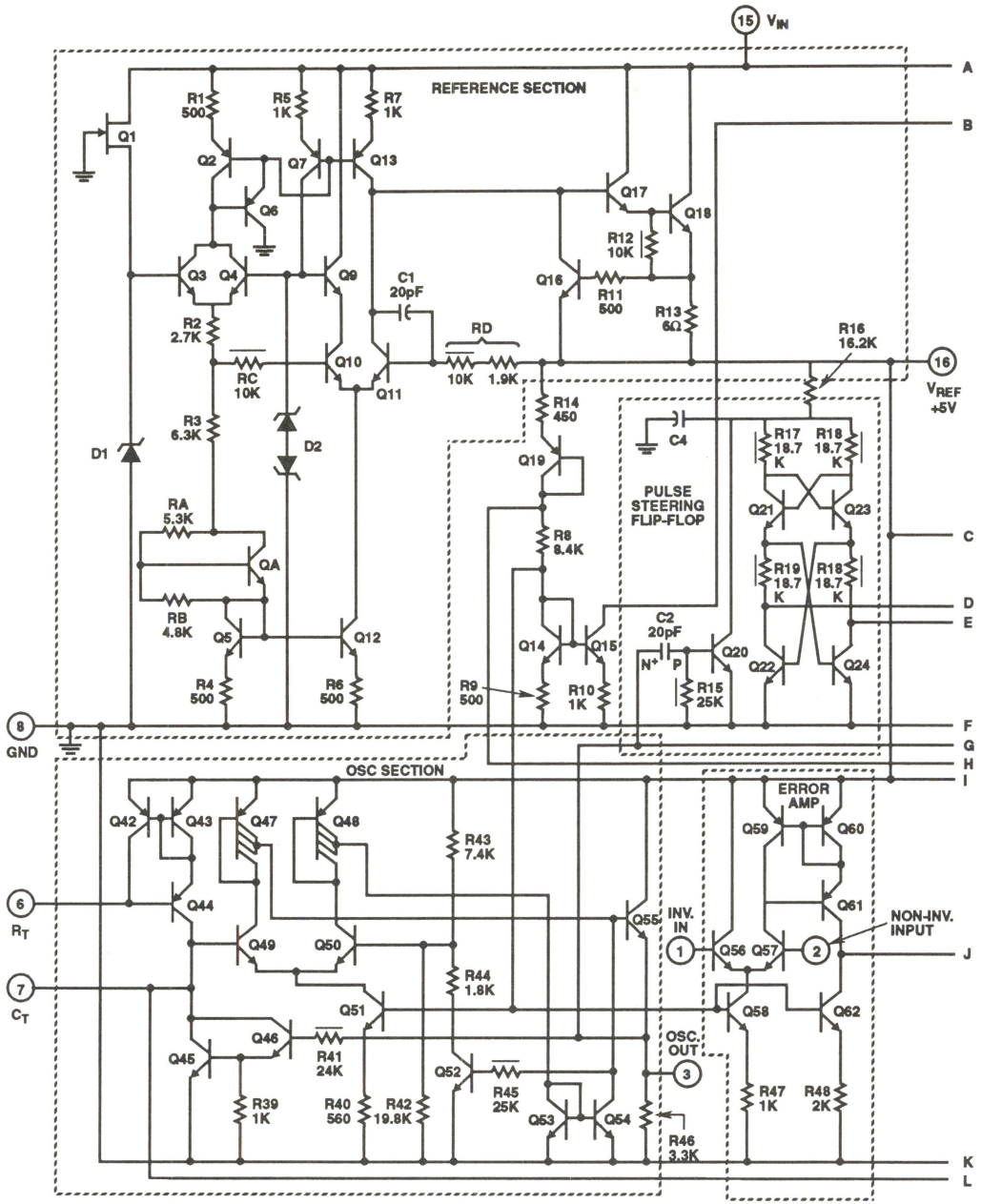


FIGURE 4. SCHEMATIC DIAGRAM OF CA1524 SERIES IC

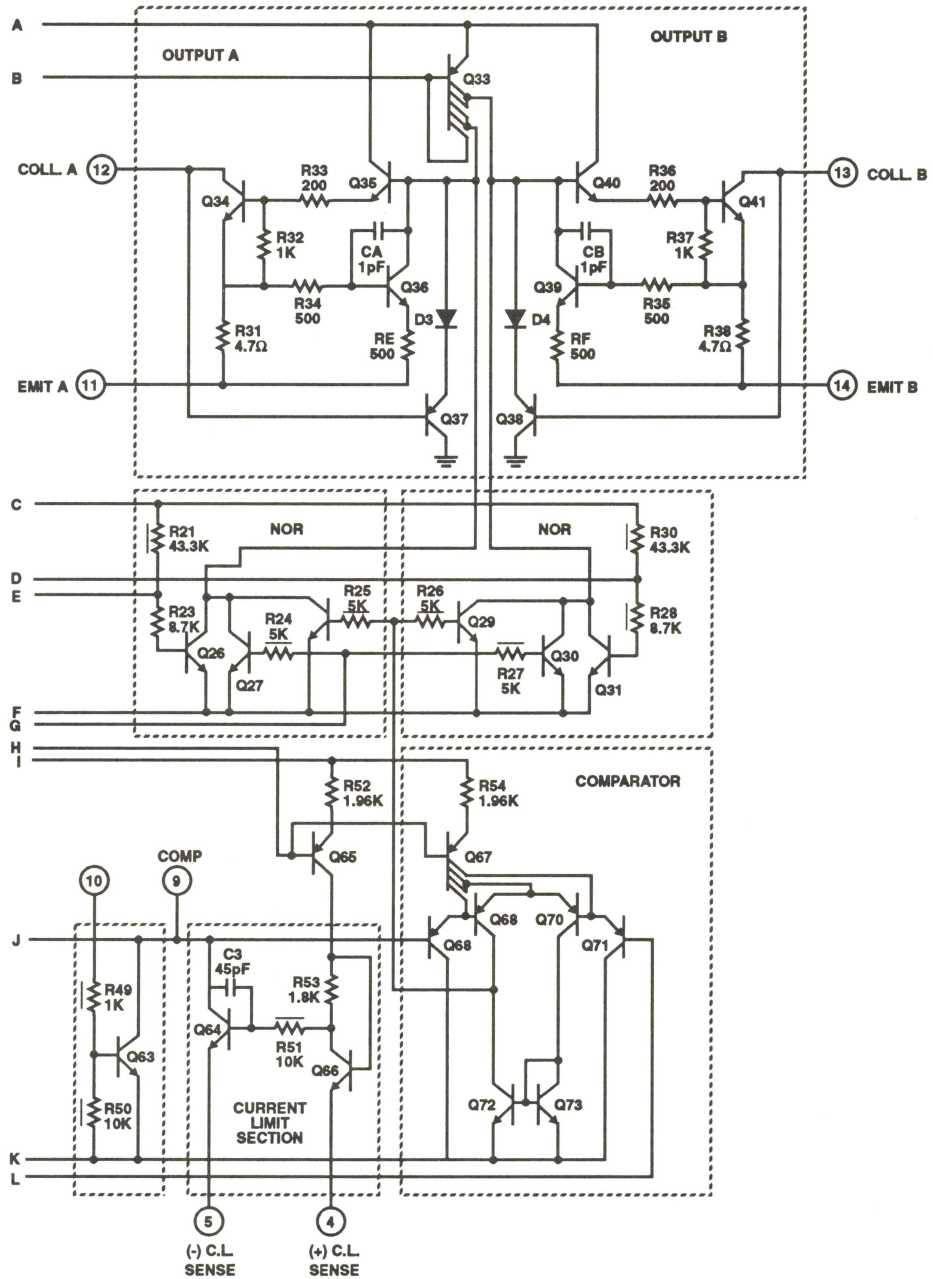


FIGURE 4. SCHEMATIC DIAGRAM OF CA1524 SERIES IC (Continued)

Figure 5 shows the temperature variation of the reference voltage with supply voltages of 8V to 40V and load currents up to 20mA. Load regulation and line regulation curves are shown in Figures 6 and 7, respectively.

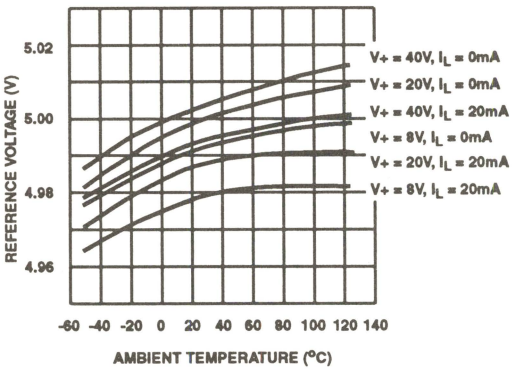


FIGURE 5. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

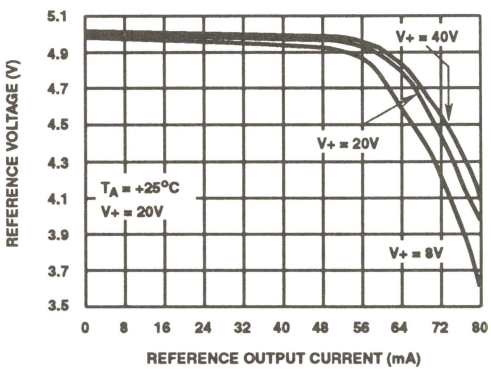


FIGURE 6. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF REFERENCE OUTPUT CURRENT

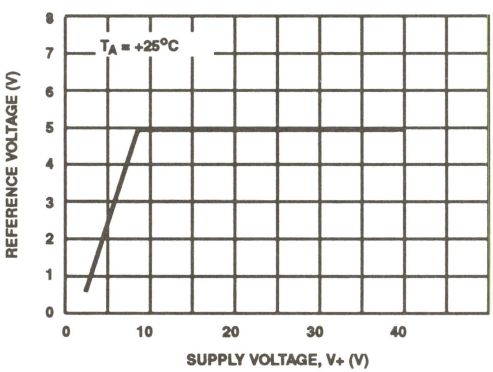


FIGURE 7. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has value that ranges from 0.6 to 3.5V and is used as the reference for the comparator in the device. The charging current is equal to $(5\text{-}2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30µA to 2mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5µs to 5µs for a capacitor range of 0.001 to 0.1µF. The pulse has two internal uses: as a dead-time control or blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which alternately enables the output transistors. The output dead-time relationship is shown in Figure 8, a curve which is useful when a value of dead time for a particular switching transistor has to be established. A larger value of dead time will assure that both output transistors in push-pull, bridge, or forward converter configurations will not conduct simultaneously.

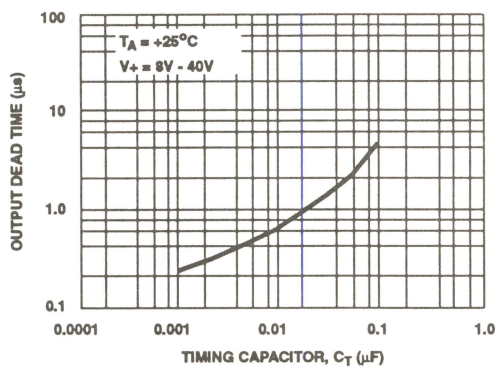


FIGURE 8. TYPICAL OUTPUT STAGE DEAD TIME AS A FUNCTION OF TIMING CAPACITOR VALUE

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100pF (but no greater then 1000pF), from terminal 3 to ground.

This shunt capacitor will expand the dead time from 0.5µs to 5.0µs when required. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2kΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable. To provide an expansion of the dead time without loading the oscillator, the circuit of Figure 9 may be used.

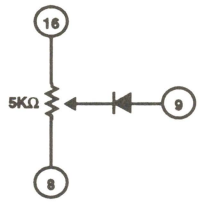


FIGURE 9. CIRCUIT FOR EXPANSION OF DEAD TIME

This diode clamp will limit the output voltage of the error amplifier; it also limits the error amplifier's source output current to about 200μA. Curves for selecting the values of the oscillator resistor (R_T) and the oscillator capacitor (C_T), as a function of oscillator period (t), are shown in Figure 10.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_TC_T$, where R_T is in ohms, C_T is in μF, and t is in μs. Excess lead lengths, which product stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals.

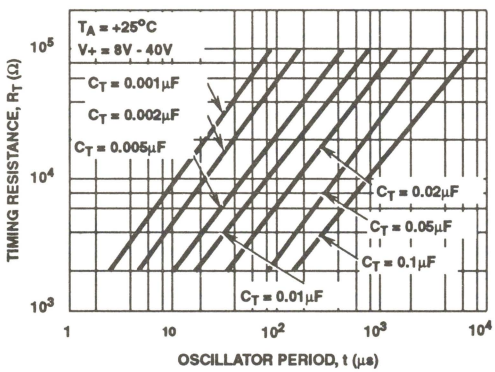


FIGURE 10. TYPICAL OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

For example, to obtain an oscillator period (t), select C_1 = 0.1μF and R_T = 10kΩ. Based on these values the output dead time is 0.7μs. For series regulator applications, the two outputs can be connected in parallel to provide an effective 0% - 90% duty cycle with the output stage frequency being equal to that of the oscillator. Since separate output terminals are provided, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0% - 45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Figure 11.

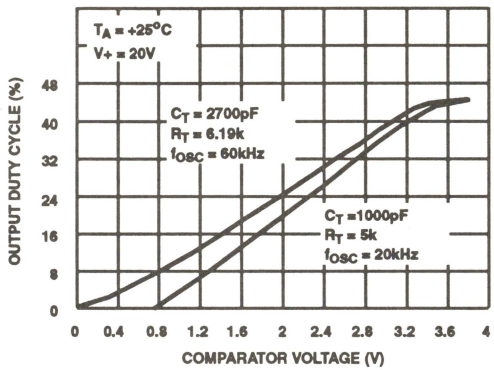


FIGURE 11. TYPICAL DUTY CYCLE AS A FUNCTION OF COMPARATOR VOLTAGE (AT TERMINAL 9)

Error Amplifier Section

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{OUT}, terminal 9, is very high (≅ 5MΩ). The gain is:

$$Av = gmR = 8\ Ic\ R/2KT = 10^4,$$

$$\text{where } R = \frac{R_{OUT}R_L}{R_{OUT} = R_L}\ R_L = \infty,\ Av \cong 10^4$$

Since R_{OUT} is extremely high, the gain can be easily reduced from a nominal 10^4 (80dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Figure 12. The output amplifier terminal is also used to compensate the system for AC stability. The frequency response and phase shift curves are shown in Figure 12. The uncompensated amplifier has a single pole at approximately 250Hz and a unity gain crossover at 3MHz.

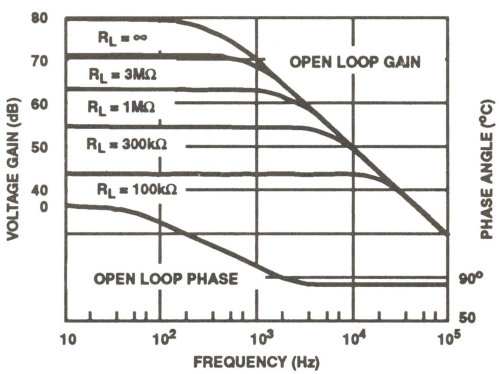


FIGURE 12. OPEN-LOOP ERROR AMPLIFIER RESPONSE CHARACTERISTICS

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a

zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000pF capacitor and a variable series 50kΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5V reference can be used for conventional regulator applications if divided as shown in Figure 13. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

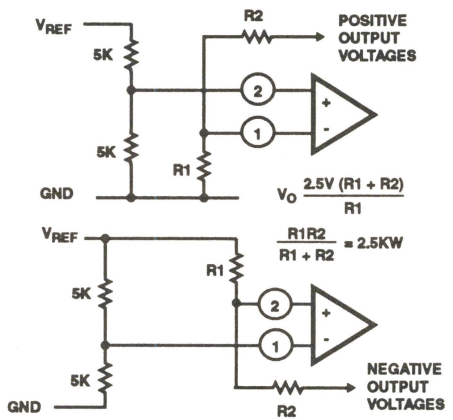


FIGURE 13. ERROR AMPLIFIER BIASING CIRCUITS

Current Limiting Section

The current limiting section consists of two transistors (Q64, Q66) connected to the error amplifier output terminal. By matching the base-to-emitter voltages of Q64 and Q66 and assuming negligible voltage drop across R51:

$$V_{THRESHOLD} = V_{BE}(Q64) + I(Q65)R53 - V_{BE}(Q66)$$
$$= I(Q65)R53 \cong 200mV$$

Although this circuit provides a small threshold with a negligible temperature coefficient, some limitations to its use must be considered. The circuit has a 11 volt common mode range which requires sensing in the ground line. The other factor to consider is that the frequency compensation provided by R51, C3 and Q64 produces a roll-off pole at approximately 300Hz.

Due to the low gain of this circuit, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, the threshold is defined as the input voltage to the current limiting amplifier to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, terminal 4 and 5 may also be used in transformer coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur (See Figure 37). Another application is to ground terminal 5 and use terminal 4 as an additional shutdown terminal: i.e. the output will be off with terminal 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 14. This circuit can reduce the short circuit current (I_{SC}) to approximately 1/3 the maximum available output current (I_{MAX}).

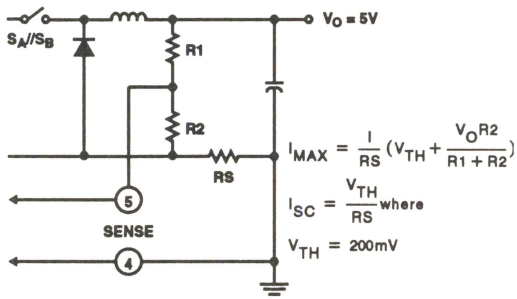


FIGURE 14. FOLDBACK CURRENT-LIMITING CIRCUIT USED TO REDUCE POWER DISSIPATION UNDER SHORTED OUTPUT CONDITIONS

Output Section

The CA1524 Series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100mA for each output and 100mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figures 15 and 16 respectively.

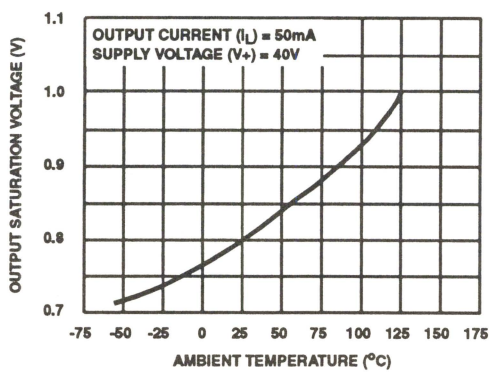


FIGURE 15. TYPICAL OUTPUT SATURATION VOLTAGE AS FUNCTION OF AMBIENT TEMPERATURE

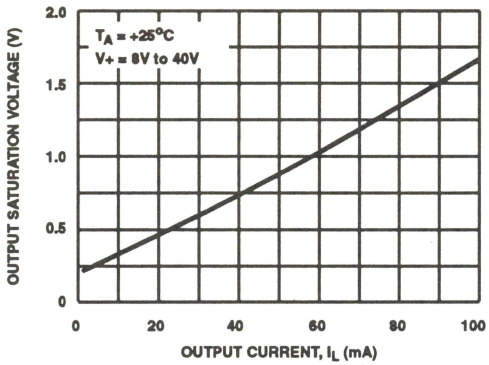


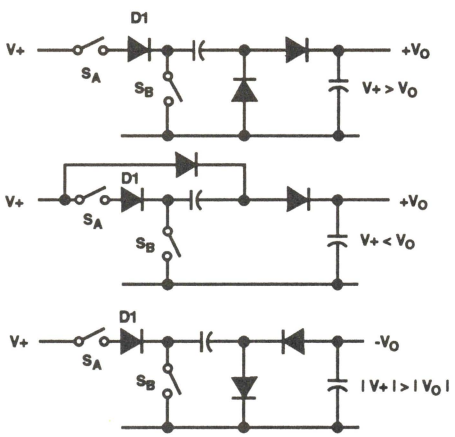
FIGURE 16. TYPICAL OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

There are a number of possible output configurations in the application of the CA1524 to voltage regulator circuits, they fall into three basic classifications:

1. Capacitor diode coupled voltage multipliers
2. Inductor capacitor single ended circuits
3. Transformer coupled circuits

Examples of these configurations are shown in Figures 17, 18 and 19. In each case, the switches can be either the output transistors in the CA1524 or added external transistors, depending on the load current requirements.

Capacitor diode coupled voltage multipliers are particularly useful in those low-power applications where inductive components are undesirable. Although the efficiencies of these voltage multipliers may not be as good as their inductive component counterparts, they are more efficient than the series-pass circuit.



NOTE: Diode D1 Is Necessary To Prevent Reverse Emitter-Base Breakdown of Transistor Switch S_A

FIGURE 17. CAPACITOR-DIODE COUPLED VOLTAGE MULTIPLIER OUTPUT STAGES

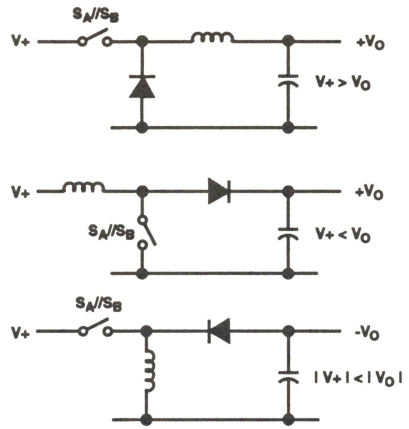


FIGURE 18. SINGLE-ENDED INDUCTOR CIRCUITS WHERE THE TWO OUTPUTS ARE CONNECTED IN PARALLEL (i.e.; SA//SB)

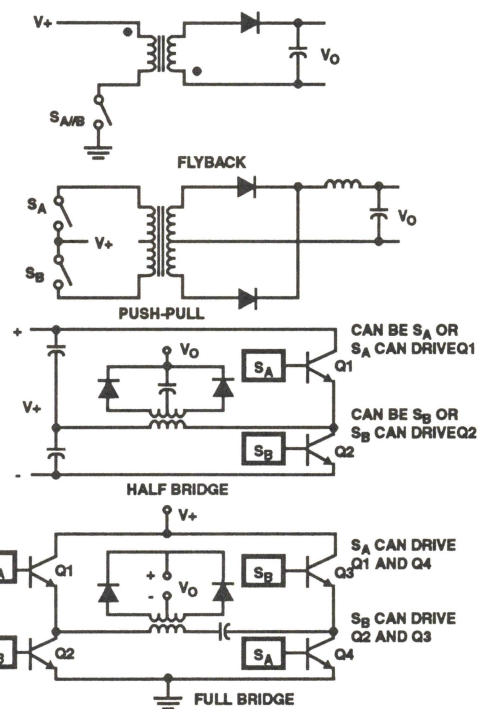


FIGURE 19. TRANSFORMER-COUPLED OUTPUTS

General Applications Considerations

The CA1524, in addition to having all the control circuits for switching regulator applications, employs two output NPN transistors. These transistors are internally current limited

and can be used in a variety of switching regulator configurations.

Three such modes are:

1. Single-ended single stage configurations for forward and flyback converters.
2. Single-ended parallel output stages for switching regulators
3. Dual or individual stage configurations for push-pull, 1/2 bridge circuits, etc.

Single-Ended Applications

The single-ended configuration provides for simple regulator designs in which an LC and diode filter network provide the DC output voltage. The PWM controlled duty cycle can vary from 0% to 45%.

The duty cycle variation depends on the divided reference voltage applied to the error amplifier terminals. This voltage, in turn, adjusts the comparator's trip level to control the ON time. Figure 11 shows the duty cycle variation vs. the error amplifier output voltage (pin 9) for the CA1524.

If the outputs are connected in parallel, the duty cycle can range from 0% to 90% a normal mode for switching regulators. For flyback operation, care must be taken to prevent the on time from exceeding 45% to allow for retrace in the flyback transformer.

Dual-Ended Applications

The dual-ended configuration can be used for the following applications:

1. Push-Pull circuits
2. Voltage Multipliers; (capacitor diode filters)
3. Half or full bridge circuits

The oscillator has a dead band feature to ensure against both output transistors conducting simultaneously. This dead band applies not only to the internal transistors, but for any additional drivers used for push-pull applications.

When using push-pull and bridge circuits, the dead time becomes important. Since the frequency of the oscillator is $1/R_TC_T$, a good method for establishing dead band time is to select f first, C_T second, and then R_T. The value of C_T determines the dead time or discharging rate of C_T. The curves in Figures 8 and 10 are used for this purpose. The oscillator provides a ramp at the C_T terminal with an equivalent dead time pulse at Pin 3 for slaving multiple units. This terminal can also be used as an oscilloscope sync. With an output resistance of 2KΩ at Pin 3, capacitive loading of this terminal will be adequate for most applications, but for larger systems some type of external dead time adjustment must be employed. To provide an expansion of the dead time without loading the oscillator, the simple 5kΩ potentiometer and diode arrangement shown in Figure 9 can be used. The output frequency of each individual output stage is approximately half that of the oscillator frequency. When the stages are connected in parallel, $f_{OSC} = f_{OUT}$.

The selection of components - capacitors, diodes, inductors, transformer cores, etc., depends primarily on the operating frequency of the switching regulator. It is important, therefore, that care be exercised in the selection of these components. Capacitors should have low equivalent series resistance (ESR) and low equivalent series inductance (ESL), because high ESR is the principal cause of capacitor ripple, and high ESL causes high frequency ringing in the MHz region. Most capacitor manufacturers rate capacitance at 120Hz, a frequency quite different from the 20kHz - 100kHz operating frequency of PWM regulator circuits. Because the characteristics of capacitors may change with change in frequency, the careful selection of close tolerance capacitors will tend to offset any degradation in PWM regulator performance resulting from the difference in the frequency rating of capacitor vs PWM regulator circuit operating frequency.

Free-wheeling diode clamps must have fast turn on and low distributed capacitance. The DC resistance of inductors should be kept low to minimize the effects of added losses that may occur at high load currents. In addition, the selection of the size and type of transformer core will also depend on the input voltage range and on the output voltage and current requirements.

Basic Switching Regulators

Figure 20 shows the basic switching regulator, the Buck or Step-Down type. In this type of regulator V_O is always $\leq V_{IN}$. The simplified waveforms for this regulator are shown in Figure 21.

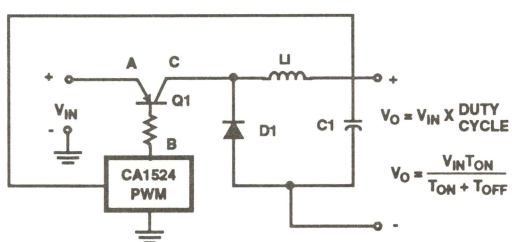
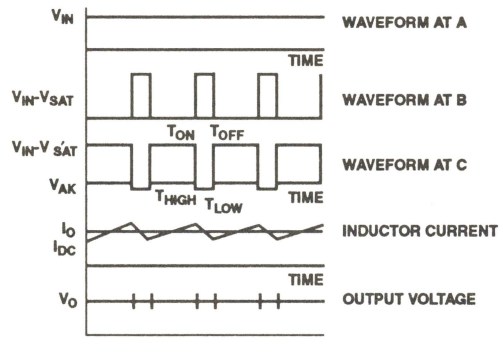


FIGURE 20. BUCK (STEP-DOWN) REGULATOR

The Buck Regulator shown in Figure 20 operates by chopping an unregulated DC voltage. The frequency of the circuit waveforms remains constant but the duty cycle is varied to effect regulation. The output LC filter, together with the free-wheeling diode D1, smooths the chopped waveform. With V_O set at some selected level by means of the reference voltage, the sample of the output voltage applied t the input of the CA1524 error amplifier adjusts the duty cycle in response to changes in load currents. When transistor Q1 is turned on diode D1 is nonconductive and current flows from V_{IN} through L1 to $+V_O$. When Q1 is off, the reserve energy in C1 provides the necessary current to the load. The overall output regulation depends primarily on the characteristics of the CA1524 and on the design of the output filter.

Switching regulator circuits are categorized for single-ended and dual-ended (bridge) applications. The basic circuits shown in Figures 22 through 30 include an inductive element. In these circuits SA represents transistor A, SB transistor B, and SA/SB indicated that both transistors can be connected in parallel. A description of the single-ended and dual-ended bridge configuration is given in subsequent pages.



V_{IN} = Unregulated DC Voltage
V_{SAT} = Saturation Voltage of CA1524 Output Transistor
$V'_{(SAT)PASS}$ = Saturation Voltage of Switching Pass Transistor
V_{AK} = Diode on Voltage
I_O = Output Inductor Current with it's DC Component
V_O = Regulated Output Voltage

FIGURE 21. SIMPLIFIED WAVEFORM FOR BUCK (STEP-DOWN) REGULATOR

Single-Ended Applications

For low-power applications up to 100 watts.

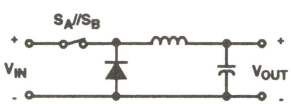


FIGURE 22. BUCK OR STEP-DOWN REGULATOR

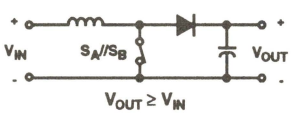


FIGURE 23. BOOST OR STEP-UP REGULATOR

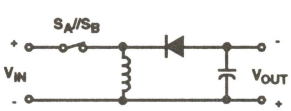
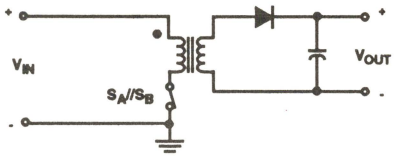
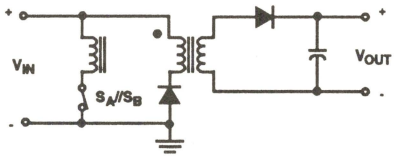


FIGURE 24. VARIATION OF THE BOOST OR STEP-UP REGULATOR RESEMBLES THE FLYBACK REGULATOR AND CAN BE EITHER STEP-UP OR STEP-DOWN

For low-power applications from 50 to 100 watts.



FLYBACK CONVERTER

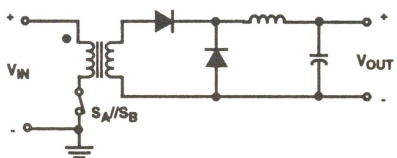


FLYBACK CONVERTER WITH CLAMP WINDING

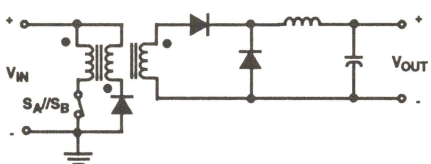
The clamp winding returns excess stored energy to the line, thereby preventing avalanche in the switching transistor.

FIGURE 25. FLYBACK CONVERTER (OPERATING MODEL FOR THIS CONVERTER IS THE BOOST REGULATOR)

For low-to-medium-power applications from 100 to 200 watts.



FORWARD CONVERTER



FORWARD CONVERTER WITH DIODE CLAMP

FIGURE 26. FORWARD CONVERTER (OPERATING MODEL FOR THIS CONVERTER IS THE BUCK REGULATOR)

Dual-Ended (Bridge) Applications

For low-to-medium-power applications from 100 to 200 watts.

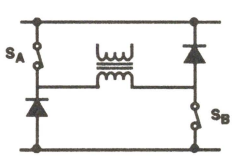


FIGURE 27. FLYBACK OR FORWARD CONVERTER WITH A CLAMP WINDING

For Medium-power applications from 200 to 500 watts.

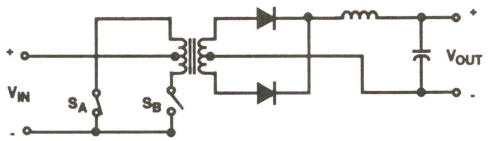


FIGURE 28. PUSH-PULL OR DC-TO-DC CONVERTER

For medium-to-high power applications from 200 to 1000 watts.

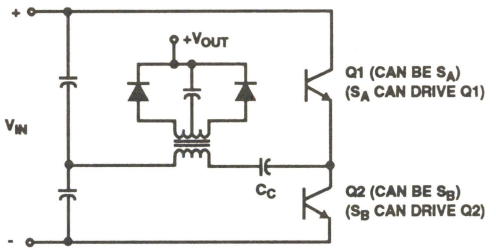


FIGURE 29. HALF-BRIDGE CIRCUIT

Capacitor C_C (1.0µF to 5.0µF range) minimizes transformer saturation problems. Diode clamps can be used across each transistor to reduce the effects of destructive switching transients.

For high-power applications from 500 to 2000 watts.

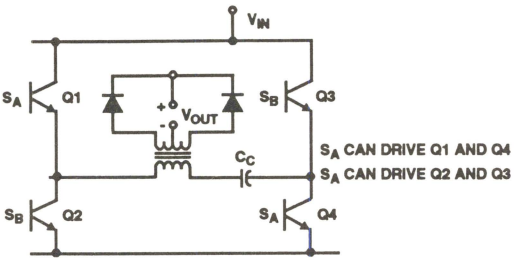


FIGURE 30. FULL-BRIDGE CIRCUIT

Capacitor C_C and diode clamps have same function as in the half-bridge circuit. In the full-bridge circuit full line voltage can be applied to the primary winding to approximately double the power output of the half-bridge circuit.

Regulator Applications

The Variable Switcher

The following review of some of the characteristics and unique design features of a variable switching pulse-width-modulated (PWM) circuit will provide the equipment designer with some of the basic principles of a PWM circuit and its associated circuitry, and a better understanding of the CA1524 Series ICs intended for this type of application.

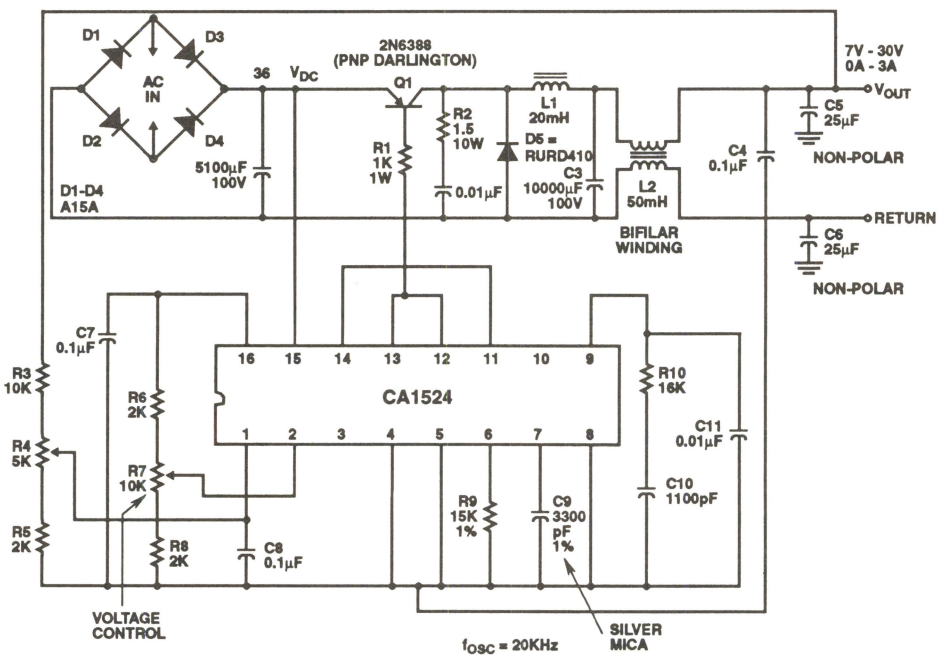


FIGURE 31. THE CA1524 USED AS A 0A TO 5A 7V TO 30V LABORATORY SUPPLY

Although most switching regulator designs and applications imply a fixed output voltage, the CA1524 Series can be applied to a variable-output-voltage power supply.

This type of circuit provides many advantages:

1. Excellent overall efficiency for the full output range; generates less heat, thereby reducing cooling requirements.
2. Input current level ≈ maximum output current level.
3. Limited dependence on V_{IA} (i.e., $V_{IN} \geq V_{OUT}$ max. +2) at the power supply's maximum output current level.
4. Light weight due to small, light cores.
5. Space saver.

and some disadvantages:

1. Low output voltage due to the limited lower end range of the error amplifier (i.e., V_{OUT} min ≠ 0, but = 7V in this particular application).
2. Losses in efficiency when output current levels are within the range of the no load dissipation for the IC and pass transistor.
3. Time lag in changing voltage levels at no load or light loads. This time lag is due to two conditions:
   A. V_C cannot change instantaneously; and
   B. C_T remains charged since it is not performing its function of supply current to the output load when the free wheeling diode conducts.

Basic Circuit Operation

The circuit diagram of the CA1524, used as a variable output voltage power supply is shown in Figure 31. By connecting the two output transistors in parallel, the duty cycle is doubled i.e.; 0° to 90°. Transistor Q1, 2N6388 PNP Darlington Transistor, is used as the switching pass element. Its base is driven by the CA1524's outputs. Variability is obtained by fist presetting the error amplifier inverting input (terminal 1) to 3.4V by appropriate selection of values for resistor network R_3, R_4 and R_5, in accordance with the maximum output voltage desired, e.g.; this particular supply was adjusted so that V_{OUT} (max.) = 30V. By varying the internal reference voltage at the comparator input (Pin 9) or 0.5V to 3.8V is achieved. This output voltage will cause the ON time of the output section to vary accordingly. As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage. The operating frequency of the regulator with R_T = 16KΩ and C_T = 3300pF is 23KHz (T = 43.5μs). The output voltage is directly related to the duty cycle and can be determined by the following equation:

$$V_O = \frac{V_{IN} - V_{(SAT)}\, t_{ON}}{T}$$

where t_{ON} is the "on" time in μs, T is the oscillator period in μs; and Q1 is operating in a saturated mode.

The following table shows both the calculated and measured data for the regulator circuit of Figure 31.

V_O (I_{LOAD} = 3A) (V)	V_{IN}-V_{SAT} (V)	t (μs)	t_{ON} (CALC.) (μs)	t_{ON} (MEAS.) (μs)
30	32.5	43.5	40.15	40.50
20	32.5	43.5	26.77	26.45
10	32.5	43.5	13.88	13.70

As the load current increases, the level of the input voltage to the D5-L1-C3 filter network decreases slightly due to an increase in the saturation voltage of Q1. this change in load causes the ON time of Q1's base to increase in proportion to the decrease in voltage at Q1's collector. This decrease in voltage, in turn, adjusts the output voltage at C_3. Resistor R_7 controls the output voltage level.

The efficiency curve for the variable output voltage power supply is shown in Figure 32 at load currents in the range of 0.5A to 3A over the full output voltage range (7V - 30V). The efficiency of the variable switcher falls short of the ideal due to the losses incurred during the fall time of Q1's collector voltage. Use of a lower frequency would improve efficiency, but would require more expensive inductive and capacitive components. Even though the efficiency values shown in Figure 32 are appreciably lower at the lower output voltages, the overall efficiency of the PWM variable supply is superior to that of the linear variable supply.

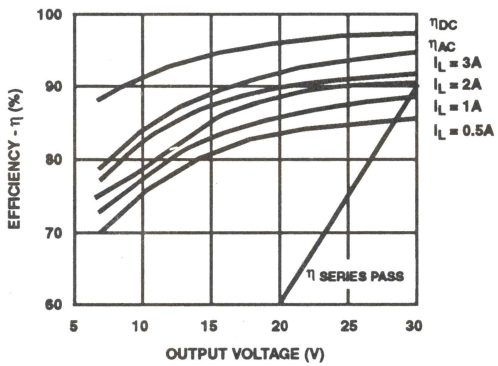


FIGURE 32A.

FIGURE 32. EFFICIENCY CURVE FOR THE VARIABLE OUTPUT VOLTAGE POWER SUPPLY SHOWN IN FIGURE 31

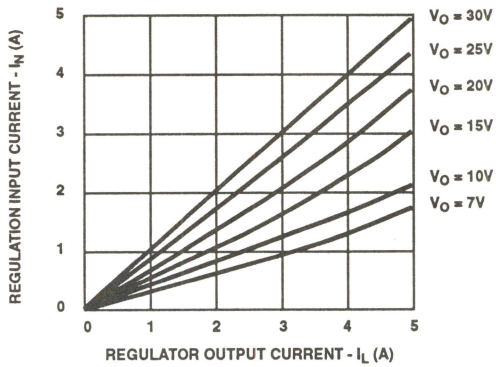


FIGURE 32B.

FIGURE 32. EFFICIENCY CURVE FOR THE VARIABLE OUTPUT VOLTAGE POWER SUPPLY SHOWN IN FIGURE 31

A major factor in the improved efficiency of the switching regulator is that output current does not have to be equal to input current as the output voltage swings between the end points of its range. The curves in Figure 32B show the relationship between the output current and the input current over the full voltage range and demonstrated how the switching regulator accomplishes its high level of efficiency. At some combinations of output voltages and currents, the large reservoir energy capacitor (C_3) supplies the difference between the required load current and available input current (see Figure 31). Note that the switching regulator has a higher efficiency for DC than AC - due primarily to the additional losses caused by the input bridge rectifiers D1 through D4 in Figure 31. However, the advantage of the linear regulator is also apparent, it can provide output voltage down to nearly zero volts.

Figure 33 shows the variation in ON time as a function of output loadings as measured at the base and collector of Q1 respectively. The regulated output voltages are 30, 20, and 10V, respectively with load currents of from 3A to 1A. The lower curve is the inductor current for the same voltages and loads. Note the change in the duty cycle and inductor current level waveforms in response to the short ON time required to supply the 30V output voltage level.

Radio frequency interference (RFI) is usually generated with any switching regulator and certain networks must be added to minimize this interference. R_2 and C_2 (Figure 31) provide a snubber network for the switching current transients of

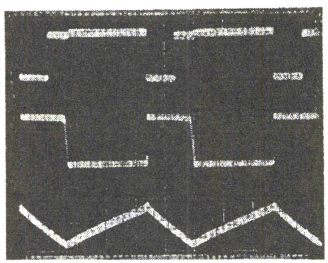


FIGURE 33A. I_{OUT} = 1A, V_{OUT} = 10V

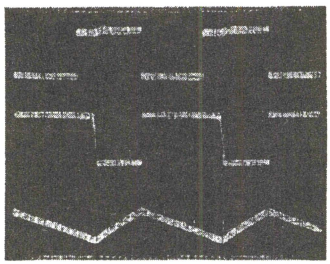


FIGURE 33B. V_{OUT} = 20V

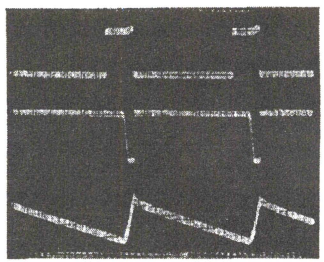


FIGURE 33C. V_{OUT} = 30V

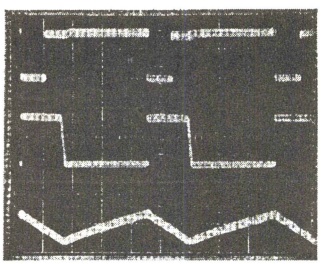


FIGURE 33D. I_{OUT} = 3A, V_{OUT} = 10V

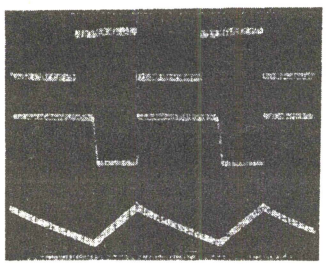


FIGURE 33E. V_{OUT} = 20V

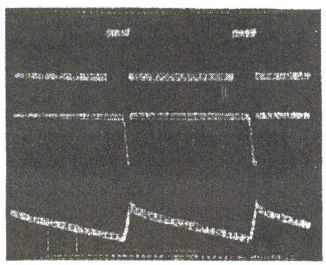


FIGURE 33F. V_{OUT} = 30V

NOTES:

All Photos: V_{IN} = 33Vdc, Horizontal - 10µs/Div
Vertical Scale Factors:
Upper Trace: CA1524 Output Voltage (Pins 12, 13) = 20V/Div
Middle Trace: Q1 Collector Voltage = 20V/Div
Lower Trace: L_1 Current = 0.5A/Div, Figures 33A, B, D, E; 0.1A/Div, Figures 33C, F

Variable output switching power supply design employ pulse width modulation techniques to achieve high performance. Note that "on" times of Q1 and the CA1524 are more dependent on the circuit's output voltage than by the output current to the load.

FIGURE 33. TYPICAL VOLTAGE AND CURRENT WAVEFORMS FOR CA1524 PWM REGULATOR OPERATED WITH P-N-P PASS TRANSISTOR AND SERIES LC AND DIODE FILTER NETWORK

diode D5 to reduce the level of the RFI generated. The output filter network L2 and C4 through C6 provides a bifilar coil which additionally suppresses the switching noise. Varistors and input L-C filters can also be employed.

Pulse-Width Modulator (PWM) Supply Details

The CA1524 provides all sense and control functions in the variable output voltage power supply design of Figure 31. In this application, the ICs two alternately switched output stages (pins 12 and 13) are connected in parallel to drive the switching transistor (Q1). The PWM IC provides an "on" drive signal to Q1 that, in effect, spans a 0% to 90% duty cycle. (The ICs output transistors can each provide a 0% to 45% duty cycle during their alternate "on" periods, but when the outputs are connected in parallel their separate "on" times effectively add serially.) This 0% to 90% duty cycle span makes possible the design's wide output voltage/current range without manual switching.

Other supply features include high operating efficiency (70% to 80%) over the full output voltage/current range. This high efficiency leads to fewer heat dissipation problems; therefore, the design is easier to cool and its reliability is higher than that of conventional linear designs. Additionally, because the circuit switches at a relatively high frequency (approximately 23KHz), circuit capacitors and inductors are small, and the combination of small size components with low power dissipation permits a compact overall design.

The PWM supply does present a few disadvantages. For example, output voltages of less than 7V cannot be attained because the on-chip error amplifier of the PWM device has a limited low-end range. And efficiency suffers when the output load current levels are low enough to nearly equal the active devices' no-load dissipation levels. In addition, a time lag occurs in voltage regulation with no load or light loads because C3 does not supply load current when the commutating diode D5 tries to conduct.

Component and Wiring Considerations

Besides being simple in concept, the regulator in Figure 31 is easy to construct and align. Layout isn't critical except in the ground returns where high circulating currents could cause problems. Note the indicated chassis and earth grounding points. The circuit diagram shows two separate return lines, one for all components in the power section and one for the control section. This arrangement is essential to assure good line and load regulation as well as minimal output noise. Keep the DC output well away from the switching circuits (switching occurs at 23kHz).

To align the supply of Figure 31, first set the PWM error amplifier's inverting input (pin 2) to approximately 33V by means of R7. (This voltage is the maximum value for the voltage control potentiometer). Then adjust the output of R4 to pin 1 to 3.4V. This value yields a maximum supply output of 30V. When the voltage control potentiometer is varied from minimum to maximum, the ICs comparator input voltage at pin 9 varies from 0.5V to 3.8V. This voltage controls the PWMs on-to-off ratio and, therefore, the conduction time of switching transistor Q1. During operation, the control voltage is set to the desired supply output voltage, and the output to the PWM feedback network consisting of R3 through R5 controls the timing.

Other Applications

Single-Ended Switching Regulator

The CA1524 in the circuit of Figure 34 has both output stages connected in parallel to produce an effective 0% - 90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be

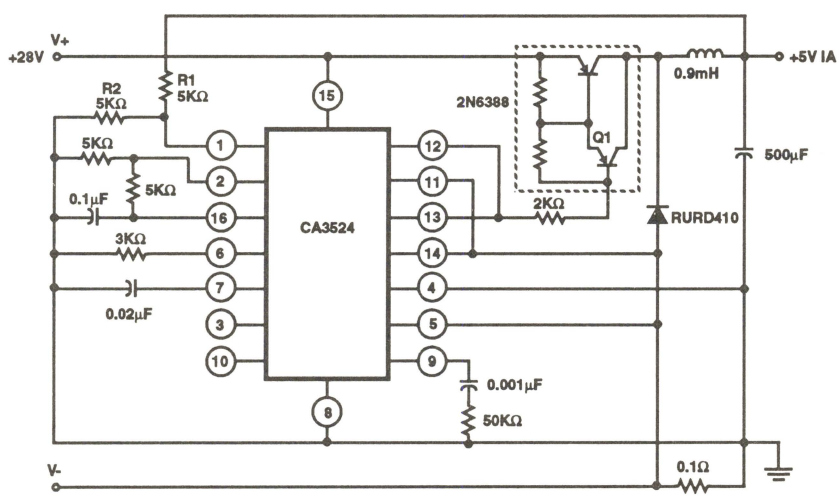


FIGURE 34. SINGLE-ENDED LC SWITCHING REGULATOR CIRCUIT

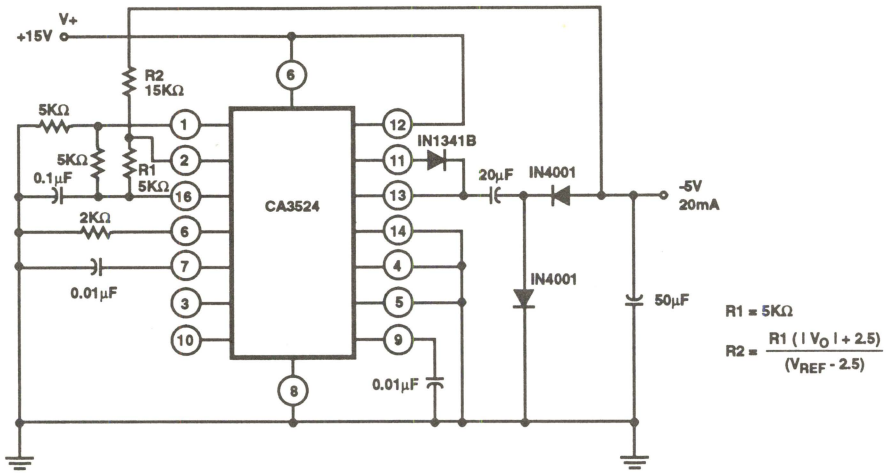


FIGURE 35. CAPACITOR DIODE OUTPUT CIRCUIT

TABLE 1. INPUT vs OUTPUT VOLTAGE AND FEEDBACK RESISTOR VALUES FOR I_L = 40mA

(For capacitor diode output circuit shown in Figure 35)

V_O (V)	R2 (kΩ)	V+ (Min) (V)	V_O (V)	R2 (kΩ)	V+ (Min) (V)
-0.5	6	8	-11	27	18
-2.5	10	9	-12	29	19
-3.0	11	10	-13	31	20
-4.0	13	11	-14	33	21
-5.0	15	12	-15	35	22
-6.0	17	13	-16	37	23
-7.0	19	14	-17	39	24
-8.0	21	15	-18	41	25
-9.0	23	16	-19	43	26
-10	25	17	-20	45	27

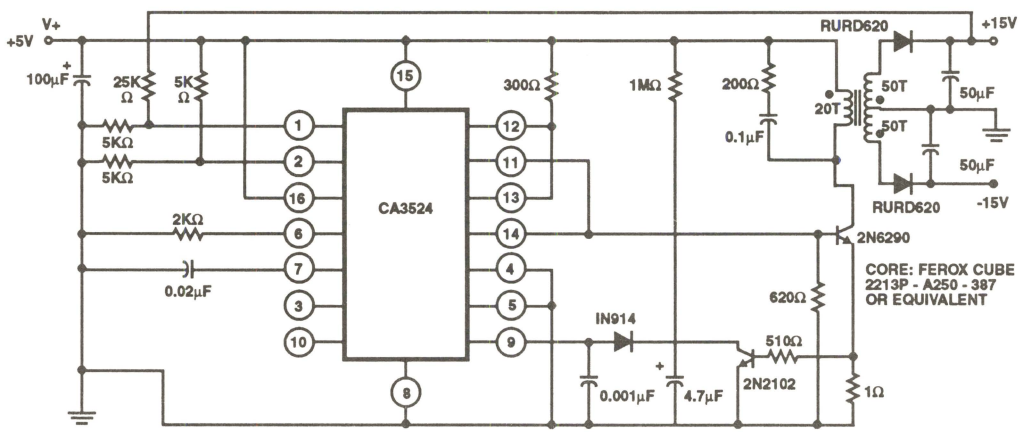


FIGURE 36. FLYBACK CONVERTER CIRCUIT

obtained by adjusting R1 ad R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9A by the sense resistor R3.

Capacitor Diode Output Circuit

A capacitor diode output filter is used in Figure 35 to convert +15Vdc to -5Vdc at output currents up to 50mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table 1 gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5V to -20V with an output current of 40mA.

Flyback Converter

Figure 36 shows a flyback converter circuit for generating a dual 15V output at 20mA from a 5V regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Figure 37. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low Frequency Pulse Generator

Figure 38 shows the CA1524 being used as a low frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5V (or 2.5V) pulse of 0% to 45% (or 0% to 90%) on time is possible over a frequency range of 150Hz to 500Hz. Switch S1 is used to go from a 5V output pulse (S1 closed) to a 2.5V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75Hz to 250Hz respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0% to 90% with the output frequency range from 150Hz to 500Hz. The frequency is adjusted by R_1; R_2 controls duty cycle.

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figures 39 and 40 uses half (Q2) of the CA1524 output in a low voltage switching regulator (2.2V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5V internal regulator and a wide operating range of 8V to 40V, a single 9V battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal as S becomes greater. The CA3160 AC amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a DC voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

References

For additional information concerning regulator designs and pulse width modulator applications, and for a list of integrated circuits and power transistors suitable for series switching applications, refer to the following publications:

1. "CA1524 Series ICs Offer Efficiency in Power Supply Design".
2. Data Sheet for the CA1524, Regulating Pulse Width Modulator, File Number 1239.2
3. Application Note, ICAN-6605, "Power Devices in Off-the-Line High-Frequency Inverter/Converter Circuits". R Minton, I. Martin, and J. Vara.
4. Application Note, ICAN-6743, "900 Watt, Off-the-Line, Half-Bridge Converter Using Only Two 15A Switch Max High Voltage Power Transistors", R.B. Jarl and K.R. Kemp.
5. Application Note, ICAN-6843, "A 450 Watt, 40kHz, 240VAC to 5VDC Forward Converter Using a New Type of Transistor", R.B. Jarl and W.R. Witte
6. EDN Design Ideas, EDN Publication, December 16, 1981, "Pulse Width Modulators Measure Weights", C.P. Salerno and P.J. Stabile, RCA Solid State Division, Somerville, N.J.
7. EDN Design Ideas, EDN Publication, August 19, 1981, "Apply Pulse Width Modulators to Produce Variable DC Voltages", C. Field, R. Jarl, C. Salerno, RCA Solid State Division, Somerville, N.J.
8. "A General Unified Approach to Modeling Switching Converter Power Stages:, R.D. Middlebrook and S. Cun, IEEE Proceedings, June 1976.
9. "Switching and Linear Power Converter Design", A.I. Pressman, Hayden Publications, 1977.
10. "Linear/Switching Voltage Regulator Handbook", Second Edition, Motorola.

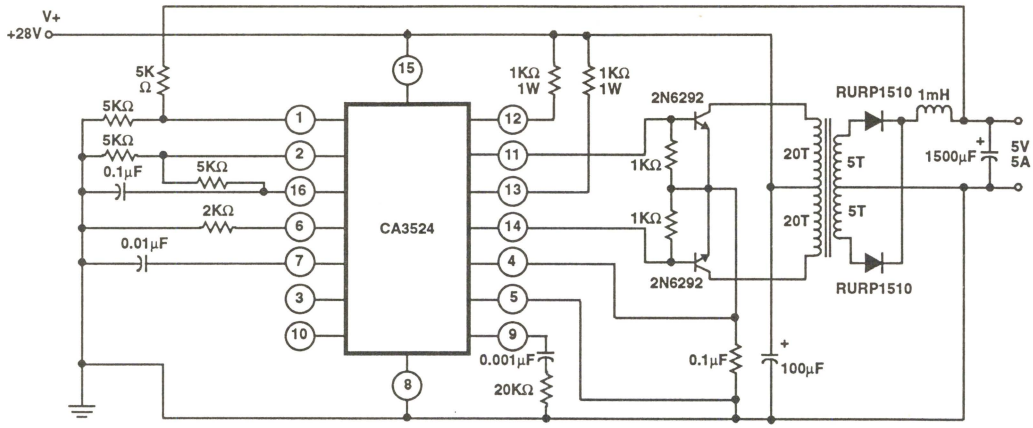
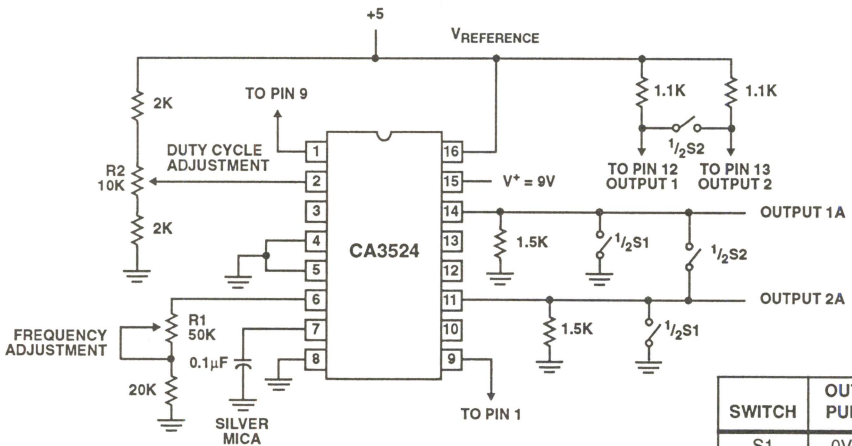


FIGURE 37. PUSH-PULL TRANSFORMER COUPLED CONVERTER



SWITCH	OUTPUT PULSES	DUTY CYCLE
S1	0V - 5V	0% - 45%
S2	-	0% - 90%

FIGURE 38. LOW FREQUENCY PULSE GENERATOR

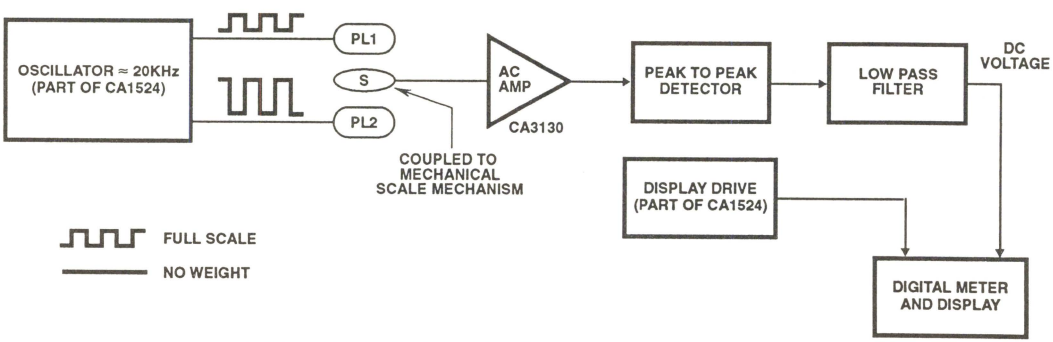


FIGURE 39. BLOCK DIAGRAM - DIGITAL READOUT SCALE CIRCUIT

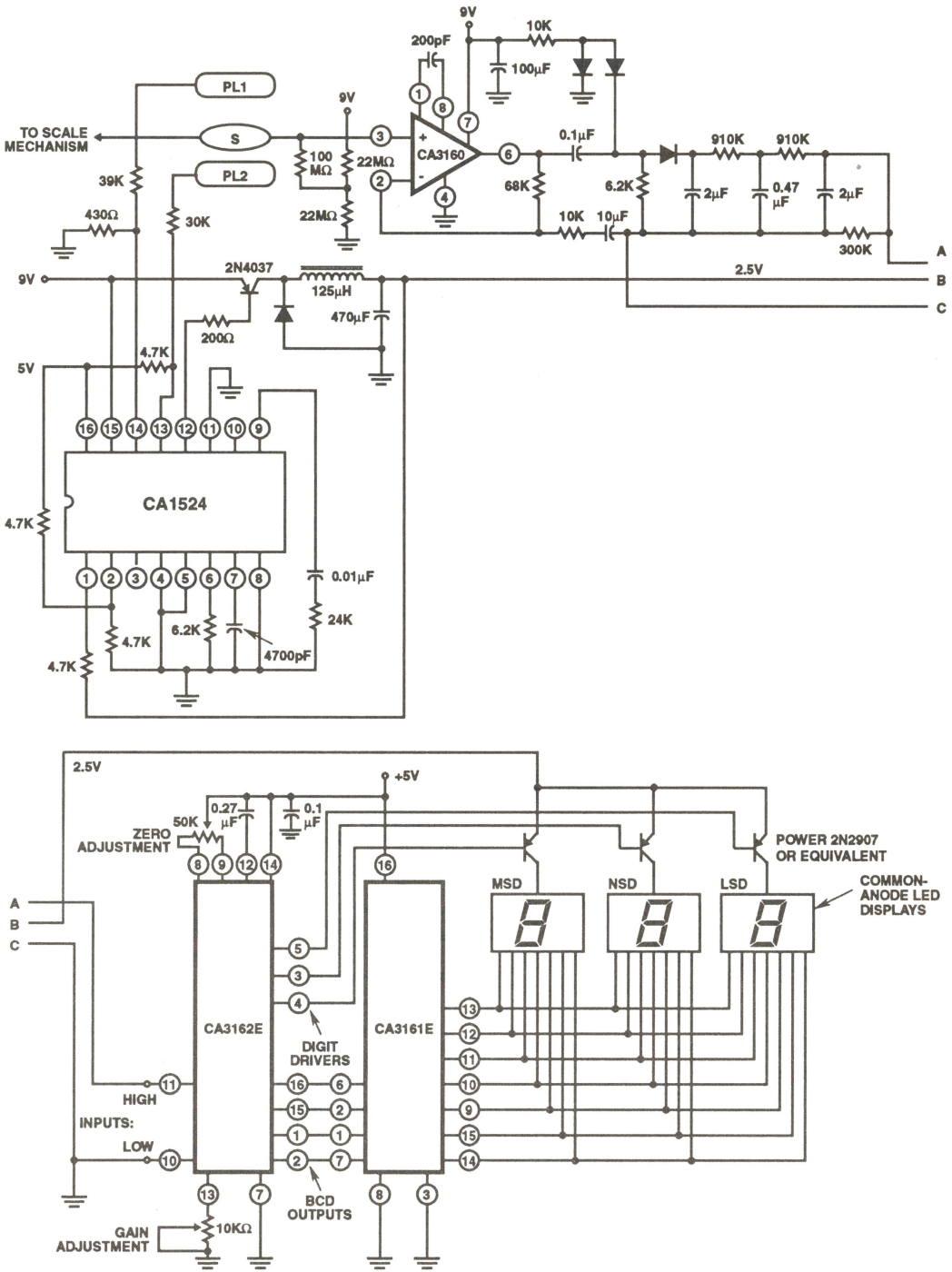


FIGURE 40. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE

Harris Semiconductor

APPNOTE

No. AN7174.1 March 1994

Harris Intelligent Power

THE CA1524 PULSE-WIDTH MODULATOR-DRIVER FOR AN ELECTRONIC SCALE

Authors: C. P. Salerno and P. J. Stabile

The CA1524 pulse-width modulator integrated circuit presently in use in voltage-regulator applications can also be employed as the driving source for an electronic scale. As shown in the block and schematic diagrams of Figures 1 and 2, half of the output of the CA1524, Q2, is used in a low-voltage (2.2 volts) switching regulator that drives the LEDs displaying the weight measured. The remaining output stage, Q1, is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5V internal regulator and is able to operate over a wide voltage range, 8V to 40V, a single 9V battery is sufficient to power the total system. The two sampling plates, PL1 and PL2, are driven by oppositely phased signals (the frequency is held constant but the duty cycle may change) from the pulse-width modulator integrated circuit CA1524. The sensor, S, located between the two plates forms with them an effective divider network of the capacitance bridge type.

As the plate S is moved, the amount of movement depending on the weight of the object on the scale, a change in capacitance occurs. This change is reflected as a voltage to the AC amplifier, the integrated circuit CA3160. At the null position, the signals for PL1 and PL2, as detected at S, are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 AC amplifier provides a buffer fro the small signal change noted at S. The output of the CA3160 is converted to a DC voltage by peak-to-peak detector. A detector of this type is needed because the duty cycle of the sampled waveform is subject to change. The detector signal is filtered further and displayed, by means of the CA3161E and the CA3162E digital readout system, as the weight of the object on the scale.

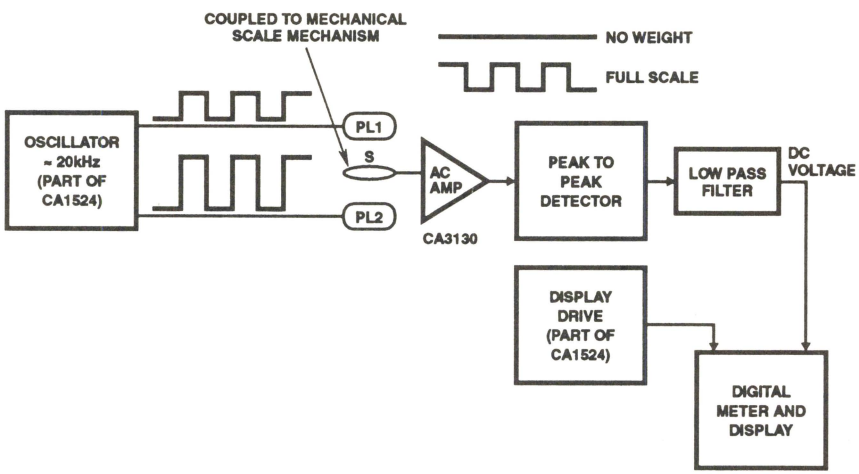


FIGURE 1. BLOCK DIAGRAM - DIGITAL READOUT SCALE CIRCUIT

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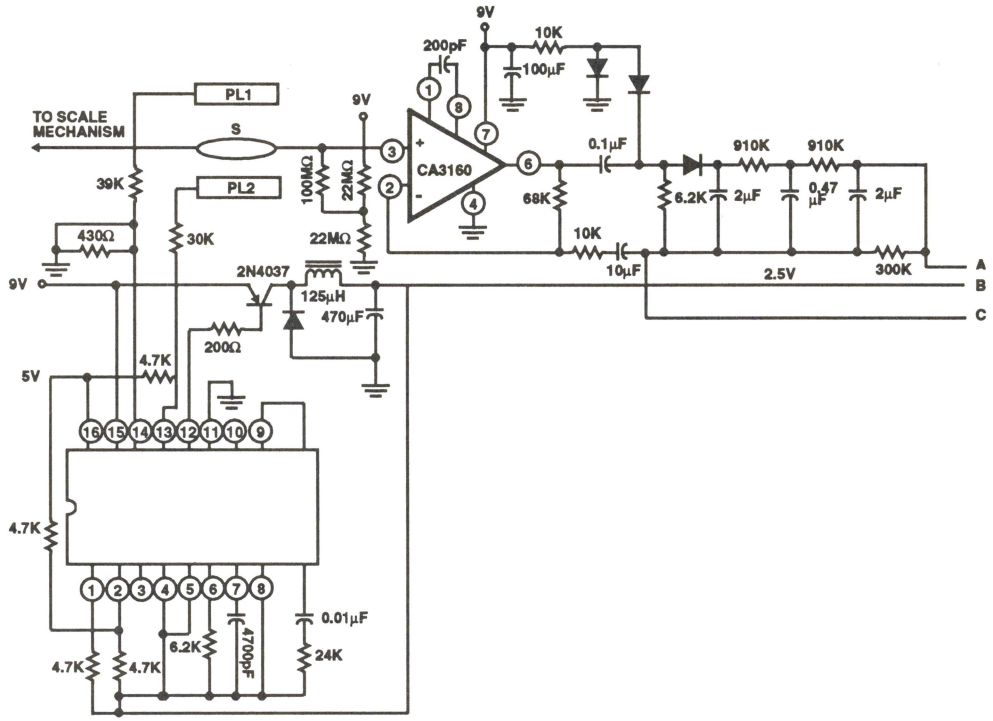


FIGURE 2A.

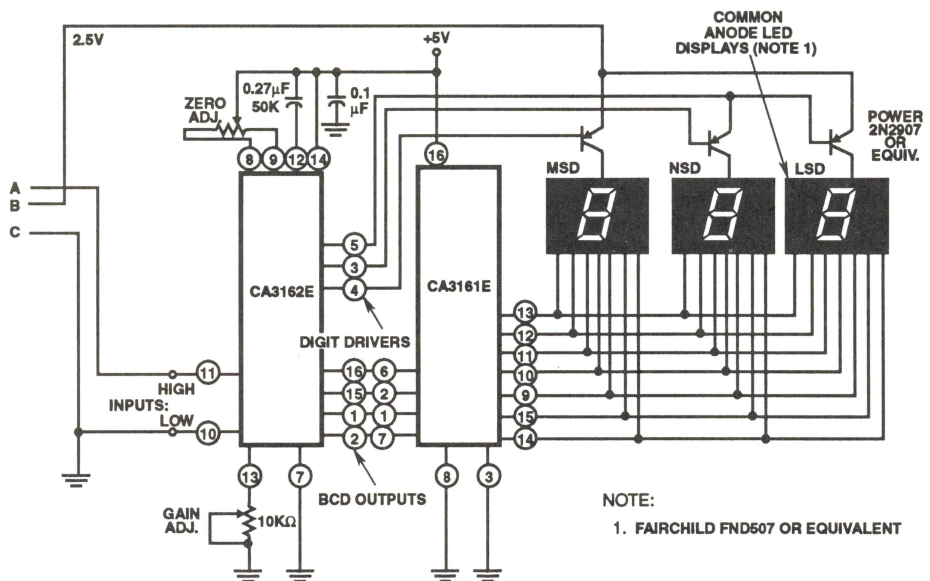


FIGURE 2B.

FIGURE 2. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE

Harris Semiconductor

APPNOTE

No. AN7244.2 September 1993

Harris Power MOSFETs

UNDERSTANDING POWER MOSFETs

Author: Tom McNulty

Power MOSFETs (**M**etal **O**xide **S**emiconductor, **F**ield **E**ffect **T**ransistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the body by silicon contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor present a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Figure 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Figure 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely different from that of a bipolar transistor, which always retain its n-p-n characteristic.

By virtue of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful by-product of the MOSFET process is the internal parasitic diode formed between source and drain, Figure 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

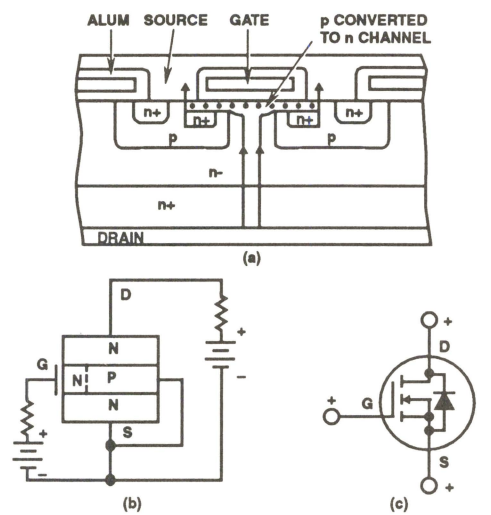


FIGURE 1. THE MOSFET, A VOLTAGE-CONTROLLED DEVICE WITH AN ELECTRICALLY ISOLATED GATE, USES MAJORITY CARRIERS TO MOVE CURRENT FROM SOURCE TO DRAIN (A). THE KEY TO MOSFET OPERATION IS THE CREATION OF THE INVERSION CHANNEL BENEATH THE GATE WHEN AN ELECTRIC CHARGE IS APPLIED TO THE GATE (B). BECAUSE OF THE MOSFETs CONSTRUCTION, AN INTEGRAL DIODE IS FORMED ON THE DEVICE (C), AND THE DESIGNER CAN USE THIS DIODE FOR A NUMBER OF CIRCUIT FUNCTIONS.

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Structure

Harris Power MOSFETs are manufactured using a vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cell varies according to the dimensions of the chip. For example, a 120-mil^2 chip contains about 5,000 cells; a 240-mil^2 chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(ON)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(ON)}$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_N, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(ON)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(ON)}$ value:

$r_{DS(ON)} = R_N/N$, where N is the number of cells.

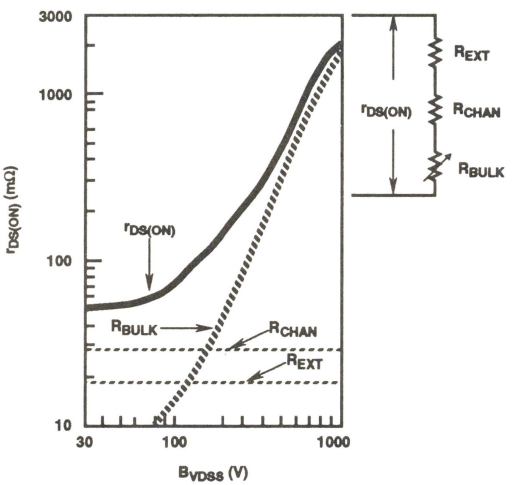


FIGURE 2. THE DRAIN-TO-SOURCE RESISTANCE ($r_{DS(ON)}$ OF A MOSFET IS NOT ONE BUT THREE SEPARATE RESISTANCE COMPONENTS)

TABLE 1. PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

B_{VDSS}	40V	150V	500V
$R_{CHANNEL}$	50%	23%	2.4%
R_{BULK}	35%	70%	97%
$R_{EXTERNAL}$	15%	7%	<1%

In reality, $r_{DS(ON)}$ is composed of three separate resistances. Figure 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(ON)}$. The value of $r_{DS(ON)}$ at any point of the curve is found by adding the values of the three components at that point:

$$r_{DS(ON)} = R_{BULK} + R_{CHAN} + R_{EXT}$$

where R_{CHAN} represents the resistance of the channel beneath the gate, and R_{EXT} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{BULK} represents the resistance resulting from the narrow neck of n material between the two players, as shown in Figure 1(a), plus the resistance of the current path below the neck and through the body of the device to the drain.

Note in Figure 2 that R_{CHAN} and R_{EXT} are completely independent of voltage, while R_{BULK} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(ON)}$ is dominated by the sum of R_{CHAN} and R_{EXT}. Above 150 volts, $r_{DS(ON)}$ is increasingly dominated by R_{BULK}. Table 1 gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(ON)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(ON)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{BULK} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and more resistive to support high voltages, the bulk component of resistance rapidly increases (see Figure 2) and begins to dominate the channel and external resistance. The $r_{DS(ON)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(ON)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(ON)}$ in Figure 2 holds only for a relatively small chip. Using a larger chip results in a lower value for $r_{DS(ON)}$ because a large chip has more cells (See Figure 3). A larger chip also increases MOSFET breakdown voltage capability.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(ON)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the original. Although the cost does not rise exponentially, it is substantially more than the original cost.

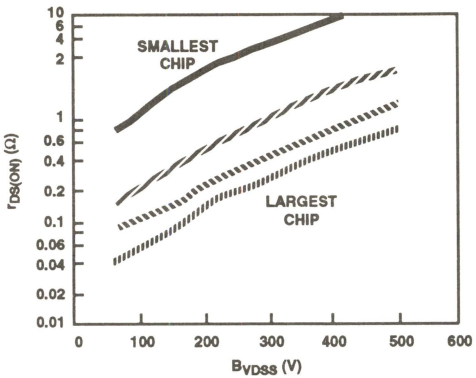


FIGURE 3. AS CHIP SIZE INCREASES, $r_{DS(ON)}$ DECREASES, & VOLTAGE HANDLING CAPABILITY INCREASES

Effects of Temperature

The high operating temperatures of bipolar transistors area frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slowdown as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Figure 4.

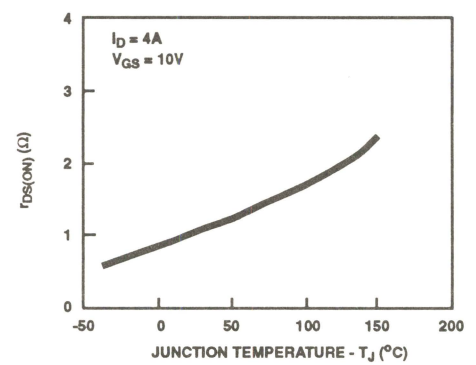


FIGURE 4. MOSFETs HAVE A POSITIVE TEMPERATURE COEFFICIENT OF RESISTANCE, WHICH GREATLY REDUCES THE POSSIBILITY OF THERMAL RUNAWAY AS TEMPERATURE INCREASES

The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Figure 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R, and capacitance, C. The capacitance, called C_{ISS} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

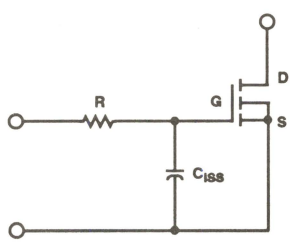


FIGURE 5. A MOSFETs SWITCHING SPEED IS DETERMINED BY ITS INPUT RESISTANCE R AND ITS INPUT CAPACITANCE C_{ISS}

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure (R in Figure 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFET in high-frequency (greater than 20MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from

datasheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20W/□. But whereas the total R value is not found on datasheets, the C value (C_{ISS}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{ISS} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1MHz to 10MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic, shown in Figure 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage (gs). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{GS} level required to operate a MOSFET, note, from Figure 6, that the device is not turned on (no drain current flows) unless V_{GS} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally V_{GS} for many types of DMOS devices is at least 2V. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Figure 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10V, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5V, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of l0V, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

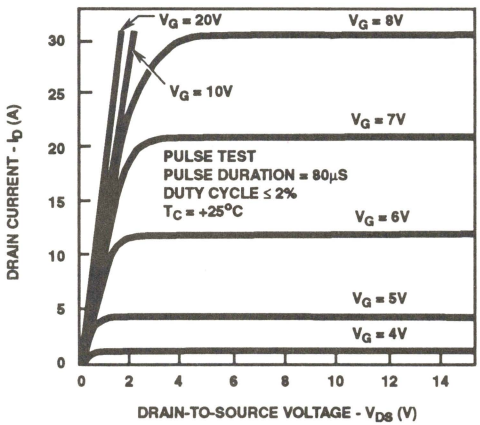


FIGURE 6. MOSFETs REQUIRE A HIGH INPUT VOLTAGE (AT LEAST 10V) IN ORDER TO DELIVER THEIR FULL RATED DRAIN CURRENT

Harris Semiconductor

APPNOTE

No. AN7254.2 April 1994

Harris Power MOSFETs

SWITCHING WAVEFORMS OF THE L²FET: A 5 VOLT GATE-DRIVE POWER MOSFET

Author: C. Frank Wheatley, Jr. and Harold R. Ronan, Jr.

The switching waveforms of a newly announced series of power MOSFET devices called Logic Level FETs (L^2FETs) and featuring a 5V gate drive are presented and contrasted with those of the more conventional 10V gate drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascade from a low voltage lateral MOS. The 2:1 advantage in rise and fall time and the 4:1 reduction in switching "dynamic $V_{(SAT)}$" dissipation with constant drive power of the L^2FET over the 10V MOSFET are demonstrated and discussed

Background

A new series of power MOSFET devices called Logic Level FETs, or L^2FETs, is compatible with the 5V power supply used for logic circuitry. L^2FETs retain the on resistance, drain current, and blocking voltage ratings of their 10V predecessors, but operate from a much less costly 5V supply.

The reduction in gate drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100nm to 50nm (500Å). Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, halving the insulator thickness halves the applied gate voltage without compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L^2FET over its 100nm predecessor, where gate drive power is the same for both devices. The "dynamic $V_{(SAT)}$" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded gate, depletion mode, vertical JFET driven in cascade by a grounded source, enhancement mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L^2FET Characteristics Compared to Standard Types - A Brief Review

Thirty-two different power MOSFETs of the L^2FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figures 1, 2, and 3, which are comparisons of the industry standard RFM10N15 with its Logic Level FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L^2FET product currently available is limited to n-channel devices handling 200V or less, with 15A ratings or less.)

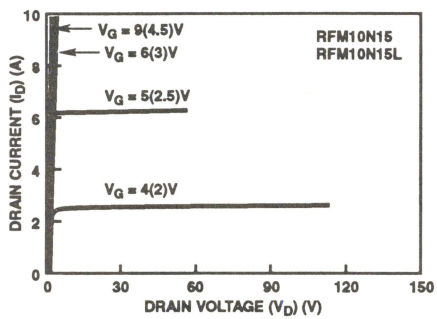


FIGURE 1. DRAIN CURRENT vs. DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES

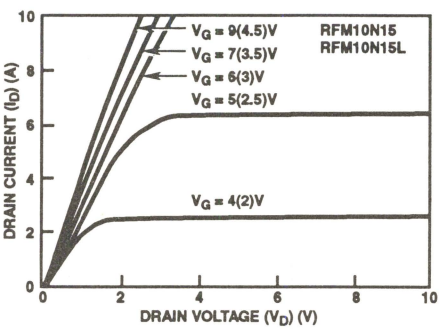


FIGURE 2. DRAIN CURRENT vs. LOW DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES DEMONSTRATING THAT R_{ON} HAS NOT BEEN SACRIFICED IN THE L^2FET

Figures 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L^2FET gate voltage is in parenthesis. The low drain voltage curves of Figure 2 demonstrate that RON has not been sacrificed in the L^2FET. Figure 3 is the transfer characteristic comparison

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for three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, L values are in parenthesis. It is evident from the curve that:

1. The threshold voltage is scaled down by a factor of two for the L^2FET.
2. The threshold voltage temperature coefficient in mV/°C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L^2FETs have similar relationships to their respective predecessors.

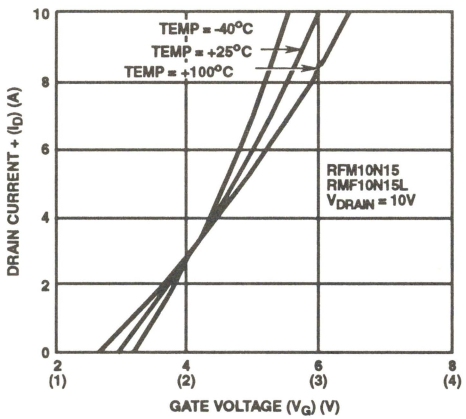


FIGURE 3. TRANSFER CHARACTERISTIC

Switching Waveforms with Conventional Drive

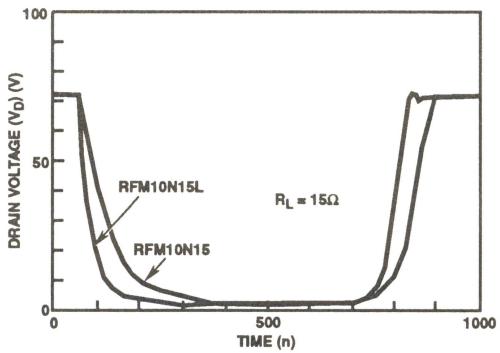
The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal". If the standard device is driven between zero and ten volts with an R_G of 25Ω, impedance transformation dictates that the L^2FET should be driven between zero and five volts with an R_G of $6^1/_4$ Ω, thereby transforming open circuit voltage and short circuit current by factors of 2 (or $^1/_2$). With these parameters, either drive system will supply a peak R_G, or generator dissipation, of one watt.

Figure 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5A, 75V resistive load line. The time scale is 100ns per division. The table under the graph compares on delay time, rise time, off delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input voltage and output voltage waveforms.

Note that:

1. The rise and fall times are not symmetrical
2. The L^2FET is faster
3. There is a "dynamic $V_{(SAT)}$" type of behavior
4. The "dynamic $V_{(SAT)}$" is of a lesser amplitude for the L^2FET

These observations are discussed below.



TYPE	GATE DRIVE	R_G (Ω)	$t_{D(ON)}$ (ns)	$t_{(RISE)}$ (ns)	$t_{D(OFF)}$ (ns)	$t_{(FALL)}$ (ns)
RFM10N15 (100nm)	0-10V	25	15	120	123	73
RFM10N15L (50nm)	0-5V	6.25	11	57	104	62

FIGURE 4. DRAIN VOLTAGE vs. TIME CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES

Switching Waveforms with Constant Current Drive

The power MOSFET is a current driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first order approximation to a constant current where the voltage compliance is determined by ground potential or the drive circuit power supply voltage. The on current may not equal the off current; this situation is addressed below.

Figure 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{G1} = I_{G2}$, with gate voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L^2FET receives less drive power or energy. The value for I_{G1} and I_{G2} was chosen as 5mA; the time scale is 1μs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic $V_{(SAT)}$" even at slow switching speeds.

4. The "dynamic $V_{(SAT)}$" curves are symmetrical during the low drain voltage portion of the turn on and turn off portion.
5. The "dynamic $V_{(SAT)}$" curves are lower in amplitude by a factor of approximately two for the L^2FET.

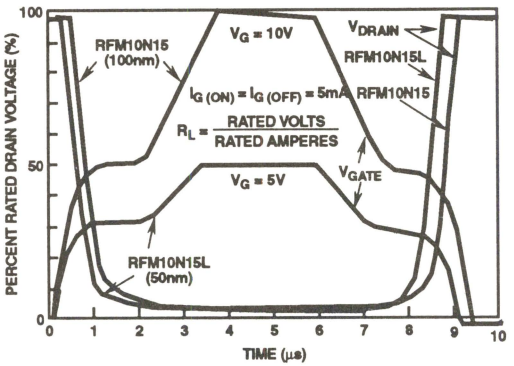


FIGURE 5. CHARACTERIZATION CURVES FOR REPRESENTATIVE DEVICES DRIVEN FROM A CURRENT GENERATOR

Large Signal Equivalent Circuit of the MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional power MOSFET must first be understood. Figure 6 shows a properly proportioned cross sectional view of the power MOSFET.

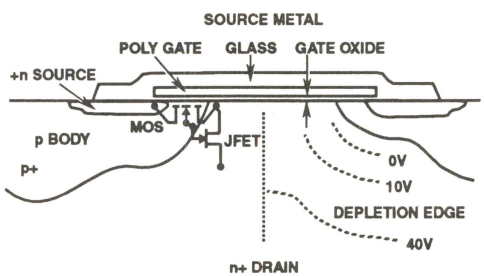


FIGURE 6. CROSS SECTION OF POWER MOSFET

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n+ region usually though of as being the MOSFET drain. This situation is shown in Figure 6, where the cross sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Figure 6. The right half indicates the edge of the depletion width for several drain voltages. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Figure 7. Note that the third quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

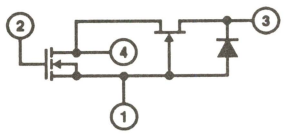


FIGURE 7. SCHEMATIC REPRESENTATION OF THE CROSS SECTION OF FIGURE 6

Interelectrode Capacitance

The equivalent circuit of Figure 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the small signal equivalent circuit of the MOS and JFET. Of course, the MOS and JFET small signal equivalent circuits are nonlinear functions of voltage and current and invariant with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three terminal characterization of this four node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reduces the power MOSFET to the capacitor network of Figure 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

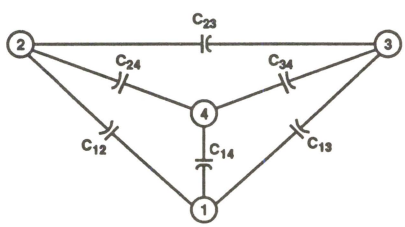


FIGURE 8. CAPACITOR NETWORK REPRESENTATION OF THE POWER MOSFET

When current does flow, node (4) of Figure 7 is a low impedance node due to the source follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate to Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Figure 6 shows that the gate to source capacitance (C_{12}) is that from the poly gate upward through the thick oxide to the source metal. In addition, there is a contribution from the poly gate to the n+ source through the thin gate oxide. Additionally a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate to Drain Capacitance, C_{23}

Capacitor C_{23} exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C_{23} exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate to Internal Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the middle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulation layer ceases to exist when the external drain voltage minus the IR drop through the n- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

Waveforms Expected from the Model

The following discussion relates the prior model discussion to the waveforms of Figure 5. The discussion begins with the gate voltage at +5V or +10V and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to I_D(max) and the drain voltage equals I_D(max) times R_{DS}(ON).

Gate Voltage Slope - t_{OFF} Delay

As time progresses, I_G = -5mA, which must flow through C_{12} + C_{23} + C_{24} of Figure 8 because the MOS and JFET are both heavily biased into conduction. Therefore, $dV_4/dt = dV_3/dt$ = nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_G/dt = I_G/(C_{12} = C_{24}) \quad (1)$$

Gate Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no longer flows from C_{12} during the constant gate voltage plateau.

Drain Voltage Shallow Slope

Since C_{23} is still zero, all gate current must flow from C_{24}. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Figure 7 must ramp at linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_D/dt = I_G/C_{24} \quad (2)$$

Again this curve will approximate a straight line.

Drain Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n- voltage directly beneath the gate oxide, and differs from the drain voltage by an amount nearly equal to $I_D r_{DS}$(on).)

Since the drain voltage is still fairly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_D/dt.

JFET Pinch Off Voltage - Drain Voltage Steep Slope

As the drain voltage approaches the pinch off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET sour-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain voltage waveform.

Gate Voltage Slope - $t_{(ON)}$ Delay

When the drain is totally off, most of the gate current flows from C_{12}. Again, this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_G/dt = I_G/C_{12} \quad (3)$$

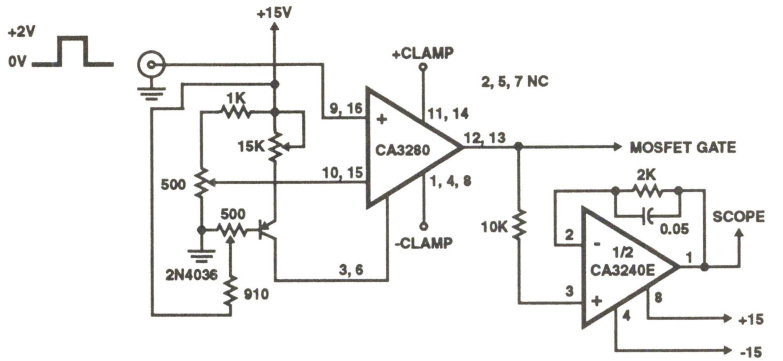


FIGURE 9. TEST CIRCUIT

New Switching Characterization for Power MOSFETs

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive circuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit - Drive

A test circuit is shown in Figure 9. The heart of this circuit is the Harris CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Figure 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximately 0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads parallel to the chips rather than wiring many sockets. However, this arrangement may require an increase in the bypass capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1mΩ or 10mΩ shunting impedance of the scope would load the high impedance circuitry associated with the MOSFET gate.

Testing Conditions

A pulse generator is set for 50µs on time duration and approximately 25ms repetition rate (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several µs exists at the +10V level. Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased to maximum rated value. The L^2FETs would be tested at +5V gate clamp.

Figure 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Figure 10(a) is the 3V signal to the CA3280. Figure 10(b) is the power MOSFET gate current. In this example, the amplitude is ±1mA with a third state of 0mA. Figure 10(c) displays the gate voltage and the drain voltage, 10V peak-to-peak and 150V peak-to-peak. Figure 10(d) is a piece wise linear approximation of Figure 10(c). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Figure 10 is 100µs full scale.

There are some features of the gate and drain voltage waveforms that should be noted. These features are consistent with the equivalent model discussion.

1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time. Exceptions will occur for very fast or very slow switching, and for nonsymetrical current drive. These exceptions are discussed in the following.

2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS}(on)$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

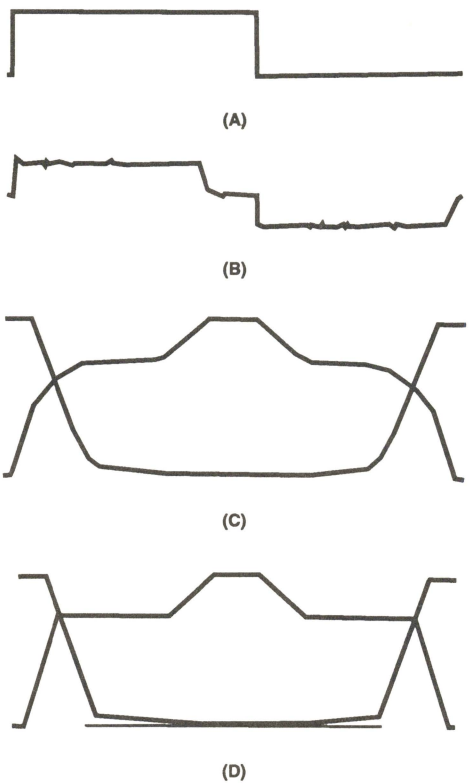


FIGURE 10. (A) 3V SIGNAL TO THE CA3280, (B) POWER MOSFET GATE CURRENT, (C) GATE AND DRAIN VOLTAGE, (D) PIECE WISE LINEAR APPROXIMATION OF 10(C)

Application of the Switching Data

Figure 11 is a family of curves similar to Figure 10(C), where the drain supply voltage is fixed at four values. Note that the ordinate is 10V full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_G) microseconds full scale, where I_G is the actual gate drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

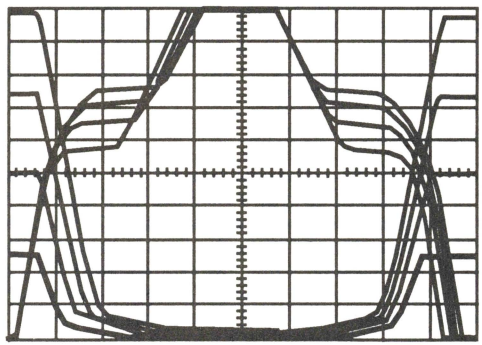


FIGURE 11. CURVES SIMILAR TO THOSE OF FIGURE 10(C) WITH DRAIN SUPPLY VOLTAGE FIXED AT FOUR VALUES

Symmetrical Current Drive

Waveforms of Figure 11 will scale in an inverse manner with gate current. Driving current was varied from ±200mA to ±2μA for the device of Figure 11. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Figure 12 and compared to the inverse scaling suggested by Figure 11.

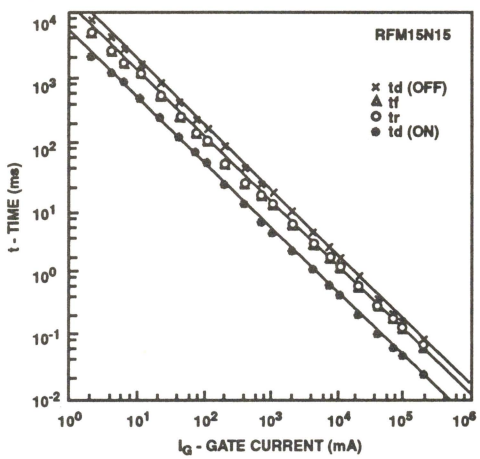


FIGURE 12. VARIOUS TIME MEASUREMENTS COMPARED TO THE INVERSE SCALING SUGGESTED BY FIGURE 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the

inverse scaling. This condition was not noted on Figure 12 for gate currents as low as ±2μA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. As a result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Figure 12, even though the gate current was increased to ±200mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piecewise linear methods will yield the gate current, which will permit the proper piecewise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Figure 11 dividing it into 10 equal voltage segments; for example, V_G = 0, 1, 2, . . . 9, 10V.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piecewise linear gate current for each time segment. I_{G1} = (10 - 0.5)/100 = 95mA, I_{G2} = (10 -1.5)/100 = 85mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Figure 11 corresponding to an average gate voltage of 9.5,8.5, . . . 1.5, 0.5 volts. Call these segments 11,12,... 19,20.
7. In that the pulse-generator voltage is now zero volts, calculate I_G as:
   I_{G11} = (0-9.5)/100 = -95mA, I_{G12} = (0-8.5)/100 = -85mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Figure 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Figure 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

Gate Voltage Propagation Effects

Most power MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage waveform applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figures 13(A), (B), and (C) show the increasing effect of gate voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Figure 13(C).

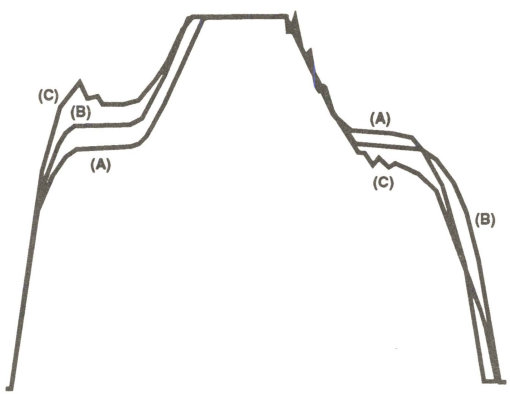


FIGURE 13. CURVES SHOWING THE INCREASING EFFECT OF GATE VOLTAGE PROPAGATION

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher R_{ON}).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield "breakthrough" devices unless used in combination.

Any of the previous methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of R_{ON} per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

References

1. "Power MOSFET Switching Waveforms - A New Insight," H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.
2. "Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed," E. Oxner, Proc. Powercon 9, April 1982.

Harris Semiconductor

APPNOTE

No. AN7326.1 April 1994

Harris Intelligent Power

APPLICATIONS OF THE CA3228E SPEED CONTROL SYSTEM

by W. Austin

The CA3228E Speed Control System is a monolithic integrated circuit originally designed for automotive cruise control systems; its block diagram is shown in Figure 1. The completeness and self-contained nature of the circuit can be appreciated by examination of the typical automotive application shown in Figure 2. Both I^2L logic and linear circuit design are combined to provide the primary functions, feature enhancements and safety backup necessary for a high-performance cruise control system. But its fully facilitated feedback system makes the CA3228E useful in a wider range of applications. The information provided in this Note will aid the user in applying the circuit to applications such as electric motor speed controls, engine speed controls, and rate controls for manufacturing systems. In fact, any powered system may be controlled with the CA3228E's accelerate or coast to a set speed adjustment and resume speed after braking (or safety stop) adjustment. Special features of the CA3228E include a single command line control and controlled PLL acceleration.

Overview

As shown in the detailed block diagram of the CA3228E in Figure 1, the primary function of the circuit interface to the logic control section is to provide a complement of capability in both linear and logic design. The command decode circuit

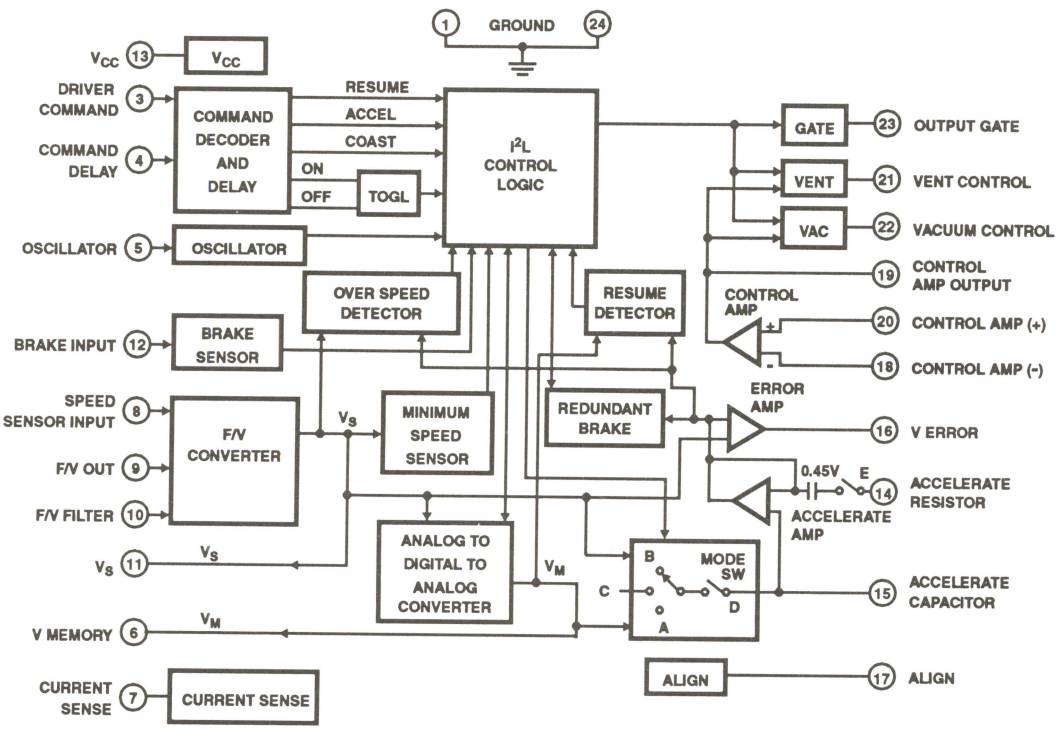


FIGURE 1. BLOCK DIAGRAM OF THE CA3228E SPEED CONTROL SYSTEM

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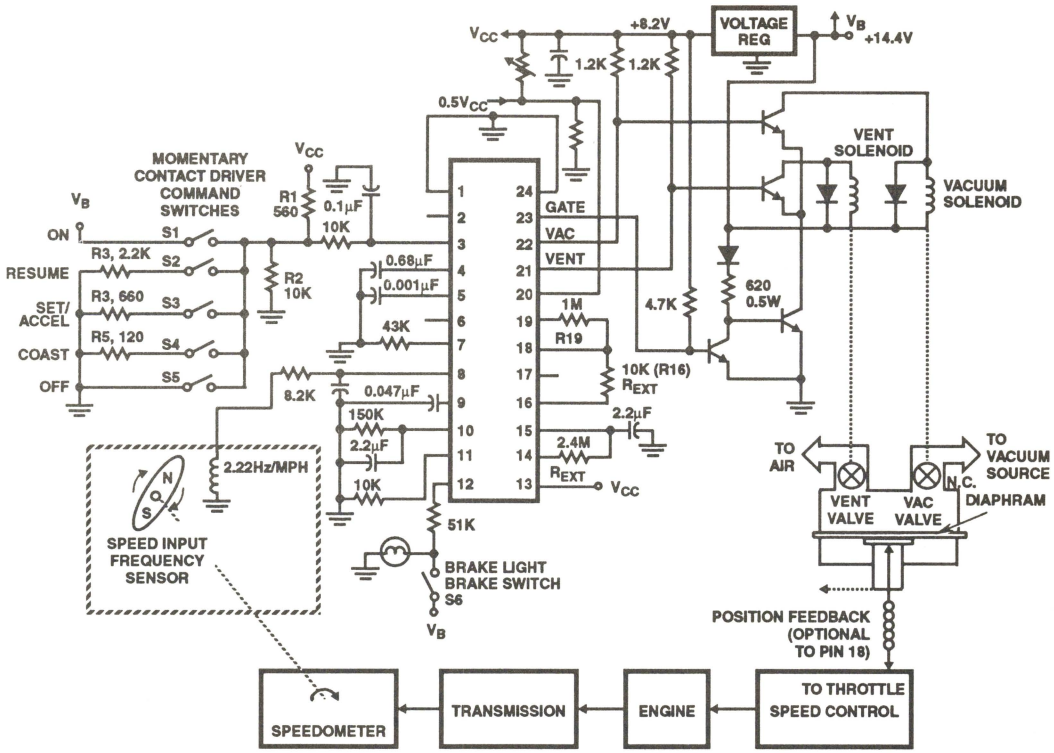


FIGURE 2. A TYPICAL APPLICATION OF THE CA3228E IN AN AUTOMOTIVE CRUISE CONTROL SYSTEM

determines which of five possible commands will be sent to the control logic. The frequency-to-voltage converter (F/V) accepts changing frequency signals and converts them to their linear representation in DC voltage.

An important feature of the circuit is a 9-bit A/D-D/A circuit, which stores a selected speed after the set/accel or coast command signal is sent to the command decoder. Within the constraints of speed-range and brake-sensing conditions, a mode switch activates an acceleration rate amplifier to maintain a cruise condition or to control a manual acceleration override condition. Any detected errors are amplified and routed to the control amplifier, which drives the output switching circuits; a built-in deadband eliminates overlap in the activation of the servo controls.

The A/D-D/A circuit consists of a 9-bit shift register which is clocked by an on-chip oscillator and current generators that sum the result of the stored bit information. The current is converted to voltage in a resistive load, and can be monitored at pin 6 as the V_M of the IC. The V_M output voltage is also sent to a memory update comparator where it is compared to the F/V output voltage, V_S. When a set/accel or coast command is finished and a return to idle is established (no switch contacts), the D/A clocks until $V_M = V_S$. The memory update comparator stops the clock when $V_M = V_S$, and the speed is stored in the bit register.

The broader prospects for use of the CA3228E are apparent if one considers all the electromechanical system possibilities that are adaptable. Some of these possibilities are:

- Automotive Cruise Control
- AC or DC Motor Speed Control
- Master/Slave Engine or Motor Speed Controls
- Manufacturing Conveyor Rate Control (With Safety/Overload Cutout)
- Oscillator Frequency Reset
- Wire/Ribbon Processing Rate Control
- Air or Fluid Rate Movement Control
- Air or Fluid Temperature Control

The characterization of the F/V converter circuit given below shows the many features of the CA3228E that permit a flexible interface between it and a variety of sensor conditions. Because of the many combinations of user input/output conditions that may be used for control, it is important to note that a single control wire provides the input for the five major commands (nonmetallic chassis requires a ground wire). This feature provides a cost savings along with design flexibility.

Command and Control Functions

The speed control functions and their descriptions are listed in the following table.

CONTROL	FUNCTION
OFF (Note 1)	Deactivates the device logic and erases memory. $V_3 \leq 0.094\ V_{CC}$
ON (Note 1)	Activates device logic and initiates a standby mode, $V_3 \geq 1.1\ V_{CC}$ or +100μA followed by $V_3 = 0.95\ V_{CC}$ (open switches).
SET/ACCEL	Momentary switch closure sets the current speed in memory. Acceleration continues at a constant rate when the switch is held closed. $V_3 = 0.54\ V_{CC}$. V_S must be greater than 1.5 V, the minimum speed lockout (MSLT), discussed below, which is approximately 25mph in the system of Figure 2.
COAST	Momentary switch closure sets the current speed in memory. When the switch is held closed, the servo disengages, causing the vehicle to slow-down. When the switch is released, the new speed is stored. During switch contact, $V_3 = 0.21\ V_{CC}$.
RESUME (Note 1)	Resumes a cruise condition if the speed is greater than MSLT, a speed has been stored after an on command, and the brake or redundant brake have not been activated. If the speed is greater than the stored memory speed, the coast function will continue until $V_S = V_M$. $V_3 = 0.76\ V_{CC}$.
Other control functions that directly affect the operating mode of command setting are:	
BRAKE	At approximately $0.55\ V_{CC}$ or more, the brake input, V_{12}, will place the system in standby, but a stored memory speed will be retained. A resume command will return the vehicle to cruise and the previous speed condition.
CLUTCH DISABLE	Same input as brake (for manual transmission).
MSLT (Minimum Speed Lockout)	Minimum Speed Lockout is a low-speed inhibit. This is an internal function that samples the F/V converter output V_S. For V_S approximately equal to $0.183\ V_{CC}$ or less, the set/accel, coast, and resume commands cannot be set. In the typical automotive application of Figure 2, MSLT is 25mph.
REDUNDANT BRAKE	If the error amplifier output voltage V_{16} drops below $0.42\ V_{CC}$, an internal comparator causes the system to go into the standby mode. This action assures that an excessive error in the servo loop will not cause an unsafe condition by providing an error speed dropout. In the application of Figure 2, the error speed is approximately 11mph.
COMMAND DELAY	To provide immunity to noise and short duration pulses, the set/accel, coast, and on and off switch input hold times are delay controlled to 50ms by a 0.68mF capacitor at pin 4. For each command, a current charge delay is used to counteract switch bounce and to enhance noise immunity. A delay of 330ms is used for the resume command.

NOTE:

1. This control function requires a momentary switch closure.

In addition to the braking and command delay safety features, a gate enable output is available at pin 23. The output at this pin remains low during normal operation of the accel, coast and cruise modes; however, it goes high for the brake, redundant brake, and low speed lockout (MSLT) commands, and during the high speed dropout condition of the resume mode. The normal applied circuit use of this feature is shown in Figure 2, where a low on the gate output at pin 23 permits the vent and vacuum drivers for the solenoid actuators to conduct through a saturated transistor common to the emitter of each driver. Should either the vacuum or vent driver transistor fail, the gate transistor would act as a safety backup, since it would be cut off and thereby mandate a standby condition.

Command Decoder Input Circuit

The command decoder input circuit is shown in Figure 3. Driver commands and their ranges of control are shown in Figure 4. Initially, the logic must be activated to an on and active standby state. This is done by setting the input emitter of Q38 at pin 3 to a higher voltage level than the V_{CC} supply line in the IC. The current should be safely limited by using a 10kΩ resistor in series with pin 3. A current of 100μA is more than sufficient to cause Q_{38} to conduct current to Q37, the transistor switch that activates the on state condition. A bias divider at pin 3 (shown in Figure 2) of 560Ω and 10kΩ establishes the command idle position after each momentary switch closure is completed.

When switch contact is made and the pin 3 bias levels are properly set, four comparators select the resume, accel, coast and off driver commands. An internal resistive divider is used to bias one input of each comparator, while the other input is biased from pin 3. As shown for the off comparator, in which I_{20} and I_{21} interface to the I^2L logic, each of the comparators drives the I^2L logic through switching transistor gates. The logic section of the IC determines all further control requirements from the state of the four comparators.

The control switching time is affected by the command delay circuit associated with pin 4 (Figure 1) and the charging time of the 0.68μF capacitor at pin 4. The 0.68μF capacitor sets command delays of 50ms, except for the resume command which is 330μs. The delay time is determined from two states of constant current drive to pin 3. Longer or shorter times may be set by changing the value of the pin 4 capacitor, but the ratio of other command delays to resume will remain the same. To calculate the capacitor value needed to change the time delay to the one desired, use the following equation:

$$V = It/C \text{ or } C = It/V$$

where V is voltage, I is current, C is capacitance, and t is time. Since V and I remain fixed, equation matching yields:

$$C1/C2 = t1/t2$$

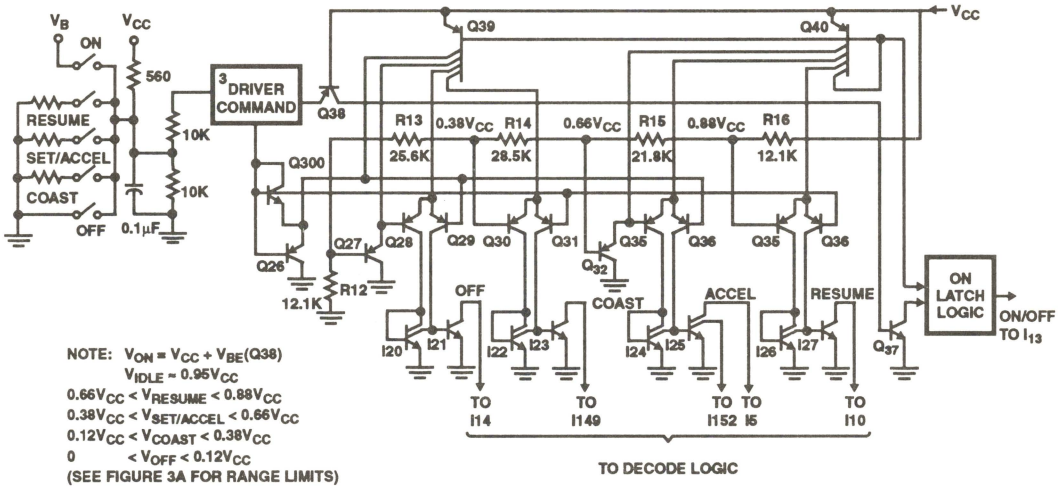


FIGURE 3. DRIVER COMMAND INPUT COMPARATOR CIRCUIT AND LOGIC OUTPUT TO COMMAND DECODE

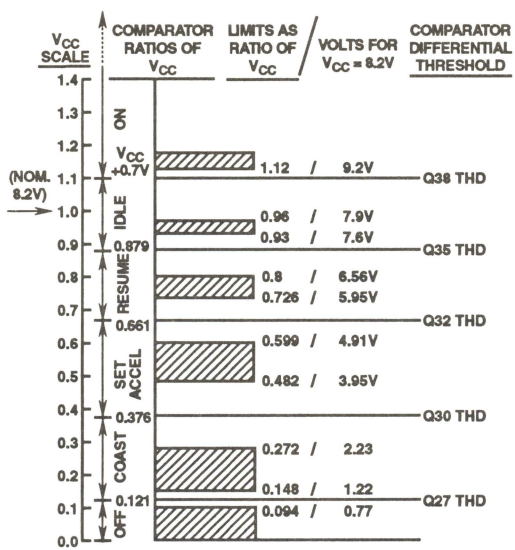


FIGURE 4. DRIVER COMMANDS AND THEIR RANGES OF CONTROL

Frequency-to-Voltage (F/V) Converter Operation

The schematic of Figure 5 shows the circuit of the F/V converter portion of the CA3228E. The input at pin 8 is normally the speed input from a speed sensor of the moving system. In normal use of the operating system, a frequency is applied at pin 8, which is a scale multiplier of the controlled system speed. For the circuit of Figure 2, the scale is 2.22Hz/mph and, with the components shown biasing the F/V converter, the conversion gain from pin 8 to pin 10 is typically 27mV/Hz. Under these conditions, the system performance parameters of the data sheet apply, including a normal speed-control range of 62 to 222Hz. In calibrating a normal range of F/V control for the V_S (pin 10) output, the frequency range in terms of voltage becomes 1.67 to 6V. Typical voltage range values of 1.5V minimum to 6.8V maximum are possible at the V_S output.

Figure 6 demonstrates the flexibility and range of design capability of the converter function by showing converter range possibilities for various values of C8 and C9; the capacitors are selected to accommodate a given range of input frequencies. The capacitor at pin 8 is chosen primarily as a filter to provide good noise immunity. Resistor R_8 and capacitor C8 provide both DC and AC overvoltage protection. The normal range of sensor input voltage is 3.5 V_{PP} minimum to 15 V_{PP} maximum.

As indicated by the capacitance versus frequency plot of Figure 6, the range of input frequencies may be changed; however, the minimum to maximum frequency ratio will always remain approximately the same. As an example, assume that it is desired to center the range of input frequencies at approximately 1000Hz. At this frequency, C9 should be approximately 0.005µF and C8 approximately 0.01µF. For these values, the minimum frequency at a V_S of 1.5V is 500Hz; the maximum frequency at a V_S of 6.8V is 2400Hz.

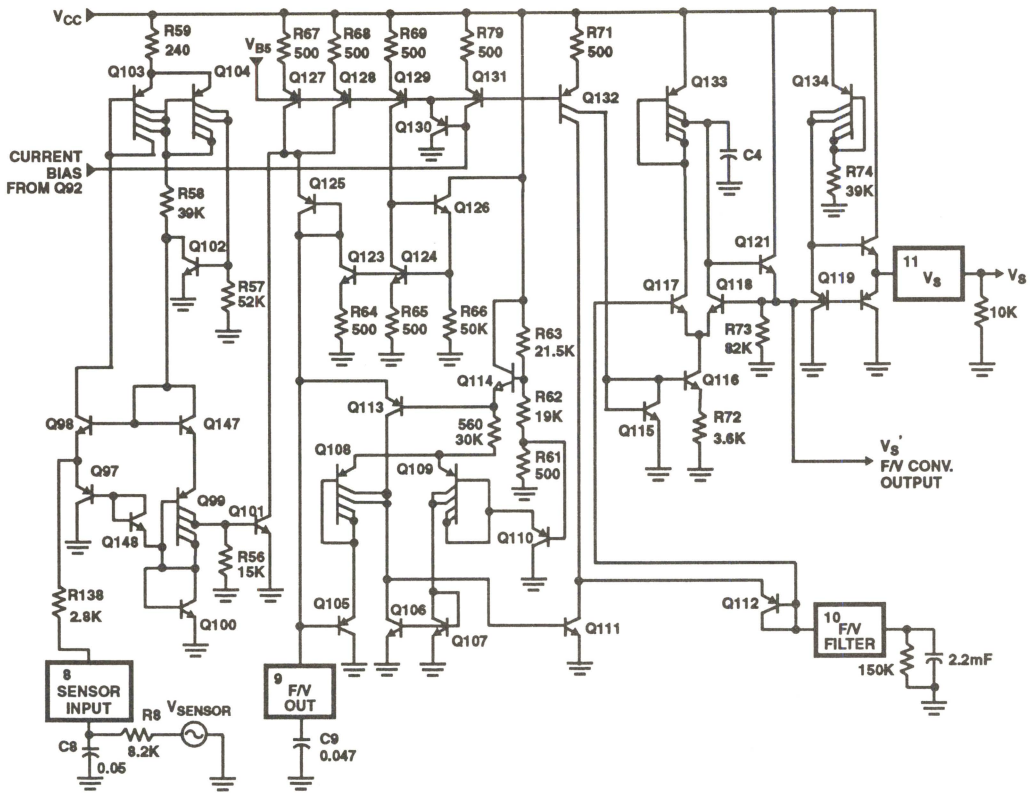


FIGURE 5. FREQUENCY TO VOLTAGE (F/V) CONVERTER CIRCUIT

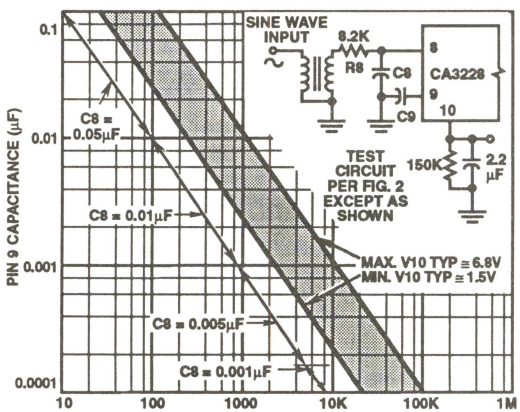


FIGURE 6. F/V CONVERTER RANGE EXTENSION WITH ADJUSTMENT OF C8 AND C9

It is possible to extend the frequency range of the F/V converter to frequencies as low as 10Hz and as high as 500kHz. However, the loop stability of the lower frequencies may be difficult to control. Higher values become very dependent on stray capacitance, causing some loss of output linearity where the internal circuit becomes bandwidth limited.

Input signal requirements at pin 8 are characterized by the voltage versus current characteristic of Figure 7. While the VI curve may appear to be complex, the drive requirement is explained simply by noting that the pin 8 input shown in Figure 5 is made through a 2.8kΩ resistor to the emitters of an n-p-n and a p-n-p transistor. When the signal input voltage polarity goes negative, Q98 conducts and changes the state of a latched current mirror (Q102, Q103, and Q104). The changing mode of the current source reflects back to the base of the input n-p-n transistor Q98, changing the DC level at pin 8. This change of state occurs when pin 8 is slightly negative (approximately 1 V_{BE}). The abrupt change to a positive voltage of approximately 2 V_{BE} is normal.

The requirements of this change of state have some influence on the design of the source input drive to pin 8. For the F/V converter input stage to switch properly, a current source drive such as an inductive pickup device or a transformer coupled signal source is preferred. In any case, it is important to note that the signal should swing negative to fully activate the change of state. It is also preferred that the input signal be nearly centered with respect to the voltage zero

crossing. The external series 8.2kΩ resistor at pin 8 must be used to limit peak currents, particularly when inductive pickup sensors are used. Inductively coupled circuits may produce transient pulses if any intermittent condition exists.

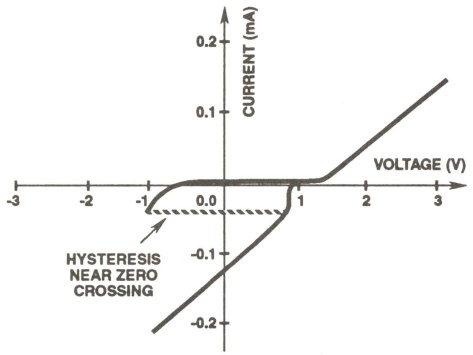


FIGURE 7. F/V CONVERTER INPUT CHARACTERISTIC PIN 8 VOLTAGE vs. CURRENT

As shown in the functional diagram of Figure 8, the second stage of the F/V converter is a pair of current generators that are used to produce both positive and negative ramp slopes when driven by the square-wave signal from the output of the first stage (at the collector of Q101). As shown in Figure 9, the capacitor at pin 9 is charged and discharged by the fixed current sources which develop a truncated ramp signal of approximately 4 V_{PP}. The ramping signal is applied to a window comparator with reference points of 0.482 V_{CC} at the emitter of Q113 and 0.012VCC at the base of Q105 (see Figure 5). When the ramp is in the transition range between these voltage levels, a high output pulse (from an equivalent 2 input NAND gate) drives the base of Q111. The comparator levels are determined from a resistor divider: R61, R62, and R63. The peak signal level is approximately 4V, while the minimum signal swing is nearly at ground level. The pulse width provided at the collector of Q111 is a function of the ramp transition time.

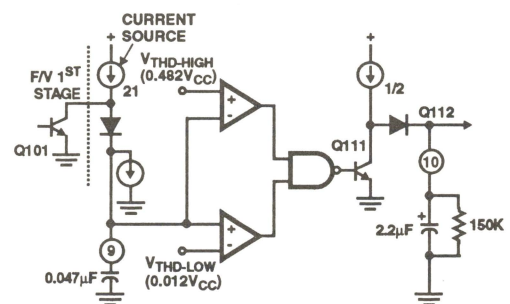


FIGURE 8. F/V CONVERTER COMPARATOR STAGE

Since a pulse of fixed width is generated on each positive and negative transition of the input signal at pin 8, it remains to integrate the pulses to produce a DC voltage proportional to the input frequency. The integration is accomplished in the RC filter circuit of pin 10. Diode Q112 rectifies the current-driven pulses developed at the collector of Q111.

Another important characteristic of the F/V converter is the absence of pulses from Q111 when no signal is present at pin 8. Diode Q112 remains reversed biased by any positive DC voltage applied to pin 10. Therefore, it is also possible to use a DC voltage signal input at pin 10 to directly control the servo feedback system. In many PLL control systems, a DC voltage signal is easily generated from position indicators. In the CA3228E, this capability provides the user with an alternative to some of the restrictions that apply to the use of the F/V converter, restrictions that may require frequency dividing to accommodate the desired frequency range and bandwidth limitations on the chip.

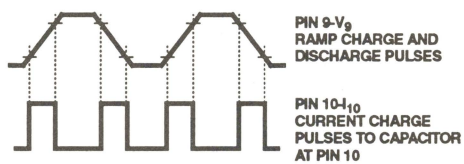


FIGURE 9. PIN 9 F/V OUTPUT AND F/V FILTER SIGNAL AT PIN 10

The range of the applied signal at pin 10 should be approximately 2V to 6V. The input impedance at pin 10 is quite high due to the source follower stage that follows the pin 10 input and drives Pin 11 plus the V_S' output to the A/D converter and mode switch circuits. Pin 11 is a sample test point for the F/V converter output, V_S. The V_S', signal is separately buffered and output to the A/D converter and mode switch circuits.

To provide a stable temperature characteristic for the F/V converter voltage, external control of the current-source generator has been provided. In the CA3228E, pin 7, Figure 10, represents a temperature-stable external sensitivity control point for the F/V converter output voltage V_S. The 43kΩ temperature-stable metal-film resistor used to bias pin 7 drives the F/V converter current sources. The current drive generated in the emitter of Q92 by this resistor provides a mirror-current bias to the F/V converter current-ramp circuits.

A/D Converter and Memory Update Comparator

The signal V_S', derived from the F/V converter output, Figure 5, and the D/A converter signal, V_M, are internally fed to the memory-update comparator circuit of Figure 11. The V_M signal may be monitored at pin 6. As noted in Figure 5, the V_S' signal is also fed to pin 11 through a buffer amplifier. The signal at pin 11 is the F/V converter output, V_S, and has a close tracking relation to V_S', when pin 11 is biased with a 10kΩ resistor to ground. In Figure 11, the V_M and V_S' signals drive buffer amplifiers Q276 and Q277, respectively. From Q274 and Q271 the V_S' signal is sent to the error amplifier, overspeed detector and mode switch. The V_M signal is sent to the mode switch via Q275 and Q269. The V_S' mode switch input (Figure 13) is at Q231 and the V_M input is at Q232. Transistors Q269 and Q271 also drive Q268 and Q270, the memory update comparator input transistors.

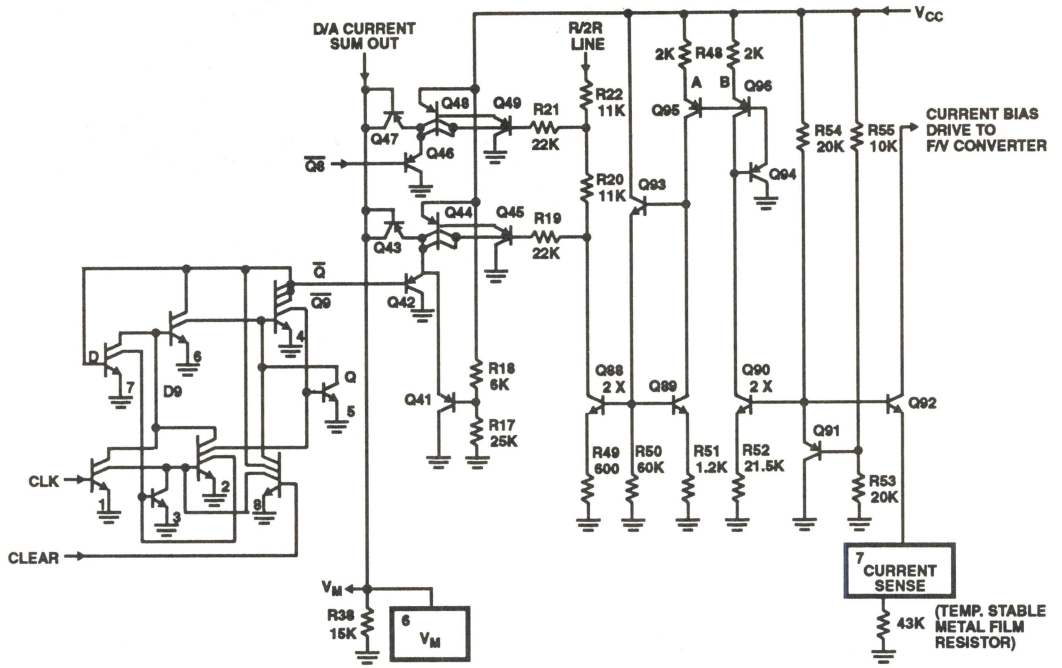


FIGURE 10. 1 OF 9 RIPPLE COUNTERS AND 2 OF 9 D/A CURRENT SUM OUTPUT CIRCUITS SHOWN WITH THE R/2R CURRENT SINK BIAS AND F/V CONVERTER CURRENT BIAS CIRCUIT

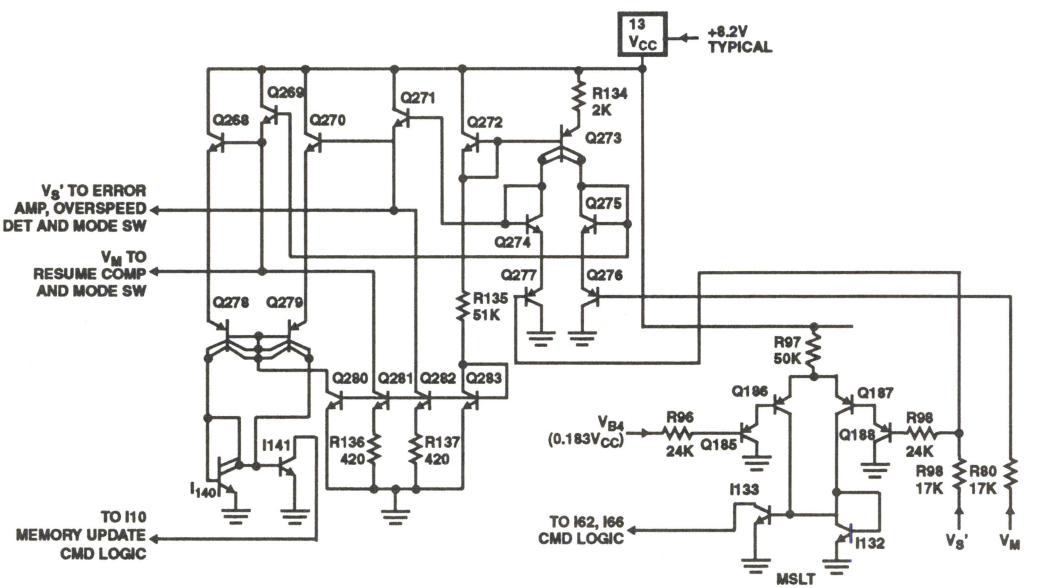


FIGURE 11. V_S' AND V_M BUFFERS WITH MEMORY UPDATE COMPARATOR AND MINIMUM SPEED LOCKOUT COMPARATOR (MSLT)

The block diagram of Figure 12 provides a broader perspective on the total operation of the D/A converter and stored memory operation by showing the signal flow by function. In Figure 12, the voltage developed by the F/V converter is V_S at the pin 11 monitor output, and is labeled as V_S, at the internal input to the memory update comparator. When, at a chosen speed, the accel/set or coast switch is depressed and then released, the command logic clears the register and initiates clocking in the ripple counter. Clocking continues and successively increases the D/A converter current output in increasing stair step increments until the V_M voltage resulting from the product of the current and the R38 resistor value is equal to V_S'.

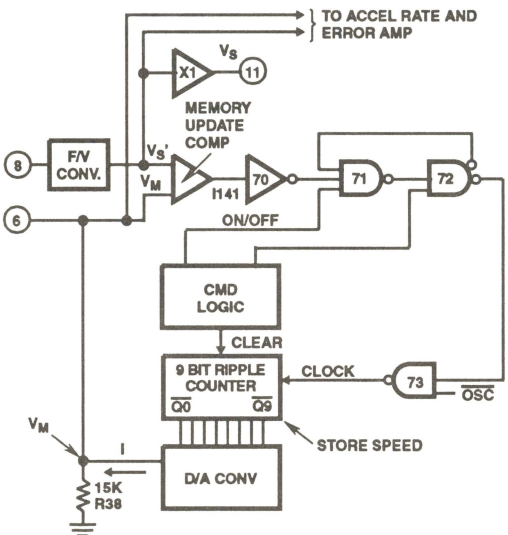


FIGURE 12. MEMORY UPDATE COMPARATOR WITH MEMORY AND D/A CIRCUITS

When $V_M = V_S'$, the memory update comparator changes state and sends a signal through output I141 to the logic circuit to stop the clocking of the 9-bit ripple counter. The stored bits in the ripple counter continue to bias the D/A converter to produce the memory set V_M speed reference. Any further changes in V_S', are compared to the V_M output of the D/A converter, which then provides the error signal for the servo control. (Refer to the Command and Control Functions section of this Note, above, for complete details of the command inputs that affect the stored speed setting.)

The circuit of Figure 10 shows a portion of the 9-bit ripple counter and the D/A circuit driven by the counter. Each cell of the 9-bit counter has a $\overline{Qx}$ output that drives its respective current source. When the counter is active, the summed outputs of the D/A converter driven current generators are present on the V_M line and at pin 6.

Mode Switch and Acceleration Control

The mode switch of Figure 13 is that portion of the CA3228E whose inputs for V_S' and V_M are Q231 and Q232, and whose output is through pin 15. Logic commands control the mode switch by controlling Q248, switch A; Q237, switch B; and Q250, switch D. When switch A is activated, Q248 is off, which allows Q232, Q240, Q241, and Q245 to conduct the V_M signal to pin 15 and the base of Q251. Similarly, V_S' is conducted to pin 15 via Q231, Q233, Q234 and Q244 when switch B (Q237 off) is activated.

In the accel mode, switch D is open, allowing the acceleration-rate amplifier to dictate a controlled rate of acceleration. A switch D open corresponds to an active high signal from I100, which causes Q250 to conduct, and which, in turn, causes Q243 to conduct. The Q243 output to Q242 is then at an emitter-base saturation level and Q242 is cut off, which prevents Q244 and Q245 from conducting V_S', or V_M to pin 15 and Q251.

Switch D is also open during resume ramp conditions. Note that V_S', and V_M are in tracking modes when Q250 is open and Q242 is conducting. The V_M tracking mode is the closed-loop cruise mode. The V_S', tracking mode applies to conditions other than cruise, accelerate, and resume. In the V_S' or V_M tracking modes, Q235 or Q246 supplies current to the base of Q242. The Q242 collector output supplies the current that charges the capacitor at pin 15.

The acceleration-rate amplifier controls a fixed rate of acceleration by providing an internal charging voltage and an external RC time constant at pins 14 and 15. When the acceleration circuit is active, Q135 is off and current source Q261 conducts current through Q266. Current-mirror circuits also control current through R132 and produce a fixed voltage offset in the signal path from pin 14 through Q266, R132, and Q263. In the active accelerate mode, an offset voltage is present at the bases of Q251 (pin 15) and Q257. The offset signal that is present at the base of Q257 is also the output of the acceleration rate unity gain source follower amplifier. The voltage generated across resistor R132 is approximately 0.45V, and is the charging voltage for the external resistor and capacitor. The typical values of the external R and C are 2.4MΩ and 2.2μF. Since the acceleration voltage that charges the external circuit is constant, linear approximations to the rate of change may be used. Using the equation:

$$V = It/C$$

$$V/t = I/C \cong 0.45/RC$$

Since V in the equations represents a fixed velocity-error voltage, V/t = 0.45/RC represents a fixed rate of acceleration. It is therefore possible to change the acceleration rate by adjusting the RC values. The desired rate of acceleration is based on system factors associated with the servo feedback loop. The values shown in this Note are for a typical automotive application. Since very low currents are used, the capacitor must also have a low leakage. For the conditions shown in Figure 2, charging current is 0.188μA.

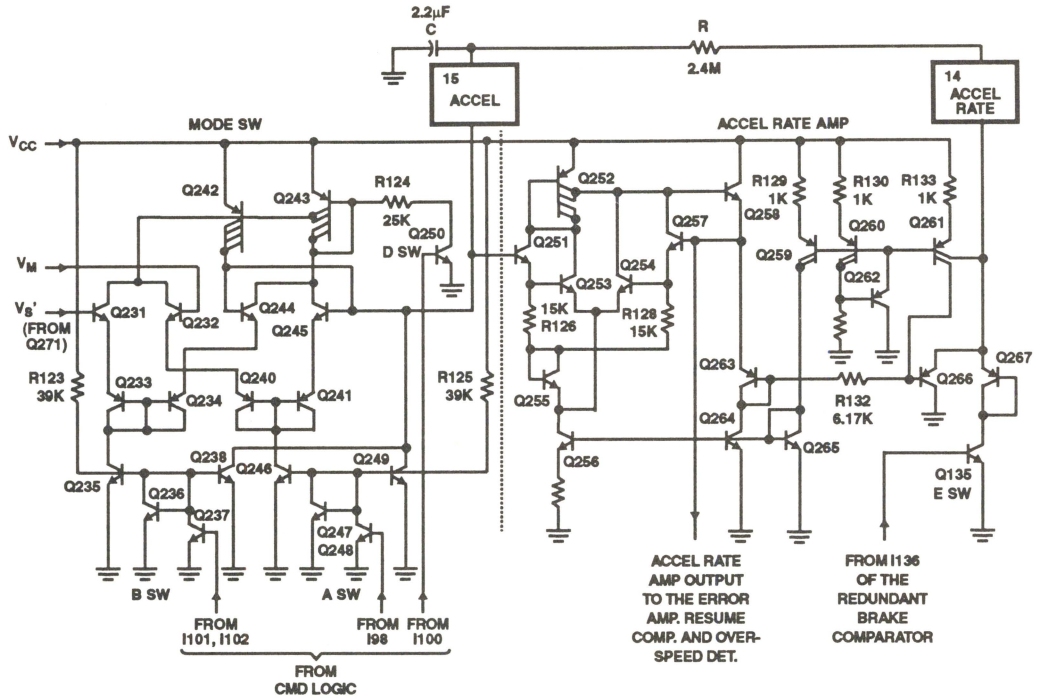


FIGURE 13. MODE SWITCH AND ACCELERATION-RATE AMPLIFIER CIRCUIT

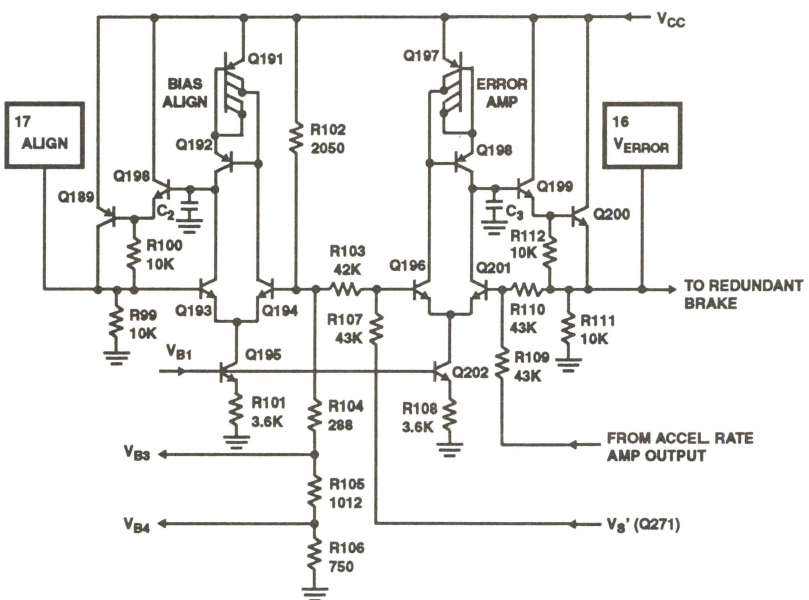


FIGURE 14. ERROR AMPLIFIER SHOWN WITH BIAS "ALIGN" SETUP CIRCUIT

Error Amplifier

The output signal of the acceleration rate amplifier is fed to the error amplifier, the overspeed detector, and the resume comparator. Under normal cruise conditions, the error amplifier continues to correct speed errors when V_S' deviates from V_M.

The error amplifier, Figure 14, is a part of the signal flow path of the feedback loop. The amplifier has an internal differential input and an output at pin 16. When the system is in a V_S' tracking mode, V_S' is present at both inputs. When the system is in a V_M tracking mode, the error signal is present at pin 16. The output signal of the error amplifier is externally coupled to the control amplifier at pin 18. Internally, the error amplifier output is fed to the redundant brake comparator. The error amplifier serves the error summing function of the servo loop and, as such, is a unity gain source follower.

The bias "align" function circuit is shown with the error amplifier circuit in Figure 14. The output at pin 17 is 0.5 V_{CC} and may be used for bias and setup. Current drain at pin 17 should not exceed 1mA.

Control Amplifier

The control amplifier shown in Figure 15 receives the signal from the error amplifier output at pin 16. Pin 18 is the negative input with respect to the control-amplifier output at pin 19, and pin 20 is the positive input with respect to the same output. The control amplifier may be regarded as a normal op amp whose gain is controlled with external feedback. However, the output signal is also internally coupled to the output vent, vacuum, and gate driver circuits. The open-loop gain, A_{OL}, of the control amplifier is typically 800. Figure 16 shows the control-amplifier bias configuration with pin 20 connected to an external divider at approximately 0.5V_{CC} and a variable feedback to pin 18. In the normal input circuit for pin 18, as noted in Figure 2, R16 and R19 are typically 10kΩ and 1MΩ, respectively.

Because the vent and vacuum driver amplifiers have a gain dependent controlled deadband, the feedback versus gain characteristic of the control amplifier is as shown in the curve of Figure 16. The curve follows the classic feedback gain equation and is approximately equal to R19/R16 for ratios less than 50. However, the approximation is less accurate for ratios in the 100 range where the error is 15%. The feedback versus gain characteristic of the application circuit of Figure 2 is typically centered at a ratio of 100. Figure 17 shows the deadband of the output vent and vacuum amplifiers as a function of the R19/R16 ratio; the output drive circuits are discussed in further detail in the following.

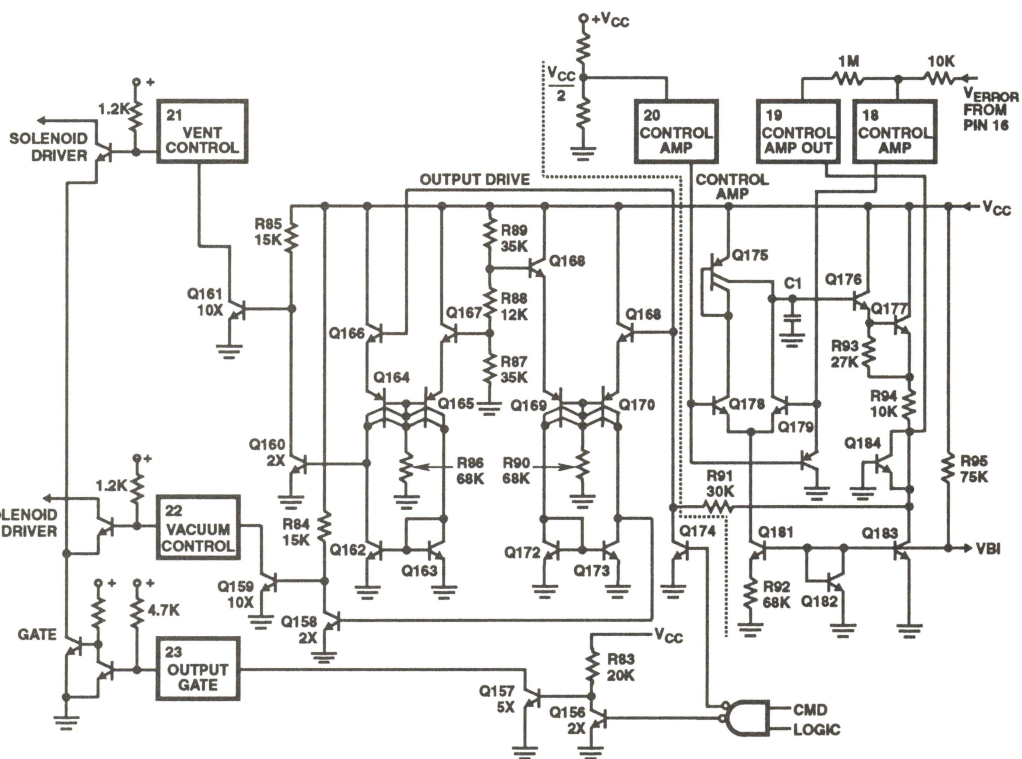


FIGURE 15. CONTROL AMPLIFIER AND OUTPUT DRIVERS

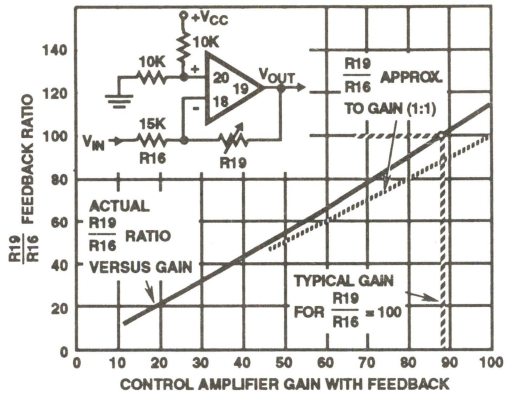


FIGURE 16. CA3228E FEEDBACK RATIO VERSUS CONTROL AMPLIFIER GAIN (WITH FEEDBACK)

Output Drive Circuits

The nomenclature of the output-drive circuits has been chosen to represent a normal vacuum-controlled actuator. Vacuum control of the actuator is intended to provide acceleration while vent control provides a relaxation or coast function. The output-drive circuits consist of amplifier drivers for the vent, vac (vacuum), and gate-output terminals at pins 21, 22, and 23, respectively, as shown in Figure 15.

A single input from the control amplifier controls the vacuum and vent outputs. The signal is passed through R91, a 30kΩ resistor, and the base of Q171 to a differential amplifier that controls the vacuum output. The base of Q171 is also common to the base of Q166, which is the differential-amplifier input that controls the vent output. The differential amplifiers for the vacuum and vent functions have reference inputs tied to a resistor divider composed of R87, R88, and R89.

The tap ratio for the Q168 input (comparator reference for the vacuum output) is at 57%. The tap ratio for the Q167 input (comparator reference for the vent output) is at 43%. When the control amplifier input is less than 0.43 V_{CC}, both vacuum and vent drivers are switched low or remain in a saturated on state. They remain on as long as the divider tap voltages are higher than the control amplifier input voltage. This situation defines a relaxed servo or coast mode.

When the control amplifier input voltage exceeds the 0.43 V_{CC} tap level, the Q166 differential input voltage forces the base of Q160 and the collector of Q161 at the vent out put to switch high. While the vent output is high and the vacuum output low, the system is in the deadband, which is the normal cruise mode. However, as the control-amplifier input voltage is further increased to the 0.57 V_{CC} tap level, both the vent and the vacuum outputs are switched high. The vacuum output switches to the high state when the base input of Q171 exceeds the 57% tap reference for Q168 and causes Q159 to switch off. When both the vent and vacuum outputs are high, the system is in a state of acceleration. As noted on Figure 2, the state of each mode is dependent on the external normally open (N.C.) and normally closed (N.C.) solenoid polarities.

The above action assumes that the gate output is low, permitting the external drive circuits of Figure 2 to function normally. The gate output remains low for acceleration, cruise, and coast functions. For brake, redundant brake, overspeed and minimum speed conditions, the gate output is high, which prevents acceleration and forces the system into a noncontrollable state. The gate output is forced high, and the vacuum and vent outputs low, by an internal logic switch, I103, that disables the output drivers.

The deadband of the output drive circuit is fixed by resistor ratio, but can be controlled through the gain of the control amplifier. It should be noted that measurement of the deadband or tap ratio points requires forcing of the drive voltage to the control amplifier and measuring of the voltage at pin 19 when the vacuum and vent outputs change state. The circuit of Figure 2 was used to generate the curve in Figure 17, which shows the variation of the deadband range when the gain of the control amplifier is changed by changing external feedback. The deadband range is shown in Figure 17 in a mV spread as a V_S reading at pin 11. As the control amplifier gain is made to approach unity, the deadband approaches the actual tap voltage separation of 1.19V when V_{CC} equals 8.2V.

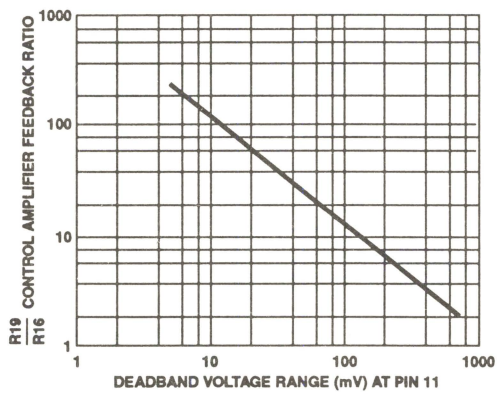


FIGURE 17. DEADBAND VOLTAGE RANGE IN OUTPUT CIRCUIT AS A FUNCTION OF CONTROL AMPLIFIER FEEDBACK RATIO (GAIN ADJUSTMENT) REFERENCED TO V_S AT PIN 11

Redundant Brake

When the speed-control system is in the cruise mode, the redundant brake comparator (shown in Figure 18) may become active if significant error voltage develops at the output of the error amplifier. Specifically, if loading or braking is causing the speed of the system to be reduced, the redundant brake comparator senses that the speed is falling off. When the error developed reaches a difference speed of 11mph, the redundant brake comparator switches logic gate I136, which causes the system to go to the standby mode. More generally, when the voltage at pin 16 drops below 42% of the V_{CC} supply voltage, I136 switches state. There is an additional output from the redundant brake through I135; this output remains high during cruise and acceleration modes. I136 inhibits the acceleration rate amplifier by controlling the E switch. (Also see Figure 11.)

The conditions that determine the operation of the brake and redundant brake can be determined from the acceleration and sensitivity factors discussed above. The sensitivity of the F/V converter is approximately 27mV/Hz. For the system of Figure 2, the system magnetic speed sensor ratio is 2.22Hz/mph. Multiplication of these factors yields a ratio of 59.94mV/mph. Dividing this ratio into the 450mV offset designed into the acceleration rate amplifier provides a result of 7.5mph. Comparison of this result to the 11mph error allowed before the redundant brake becomes effective indicates that there is a wide enough safety margin to prevent redundant braking during acceleration.

A special feature of the CA3228E prevents extraneous noise from switching the redundant brake output and causing the system to go into standby. This feature is provided by a 4-bit shift register that is used as a digital filter to clock all four outputs of the shift register to 1's before a 4-input AND gate can switch the logic to standby.

Brake Input Comparator

The brake input comparator, also shown in Figure 18, is a comparator amplifier driving an inverter logic gate (I142). When the brake input is greater than 0.55 V_{CC}, as determined by the resistor divider composed of R77 of 20kΩ and R75 of 24.5kΩ, the I142 gate output changes state. The brake input is normally connected through a current limiting resistor to the brake switch, and is in parallel with the brake light. The change of state at the output of the brake input comparator drives the command decoder which places the system in standby.

Minimum Speed Lockout

The minimum speed lockout (MSLT) comparator shown in Figure 11 senses the speed voltage V_S', and compares it to the output of a fixed resistor divider. When V_S' drops to less than 1.5V, the comparator switches, which sends a signal to the control logic that places the system in standby. If V_S' is initially less than 1.5V, the system cannot be set in the cruise mode. The divider ratio of $0.183V_{CC}$ is approximately 1.5 V for a normal V_{CC} of 8.2V. For a speed sensitivity factor of 59.94mV/mph, 1.5V is equivalent to 25mph.

Overspeed Detector and Resume Comparator

The associated functions of over speed detector and resume comparator are shown in Figure 19. From the normal condition, where a speed is set in memory and cruise is being maintained, it may be desired to increase speed and then return to the cruise mode. If the range of speed increase is large, it is best not to use the accel mode but to manually accelerate to the higher speed and then press the set/accel switch. An over speed detector comparator compares V_S' and V_M and controls the logic to assure a smooth transition.

During acceleration, V_S' is greater than V_M. When the set/accel command is given, the logic turns on Q250 (Figure 13) and the capacitor at pin 15 is rapidly charged. When the voltage at pin 15 is within 60mV of V_S', the over speed detector output is switched low. At that point, further V_S' correction is assumed by the acceleration-rate amplifier under fixed-rate conditions. The overspeed detector maintains the 60mV off-

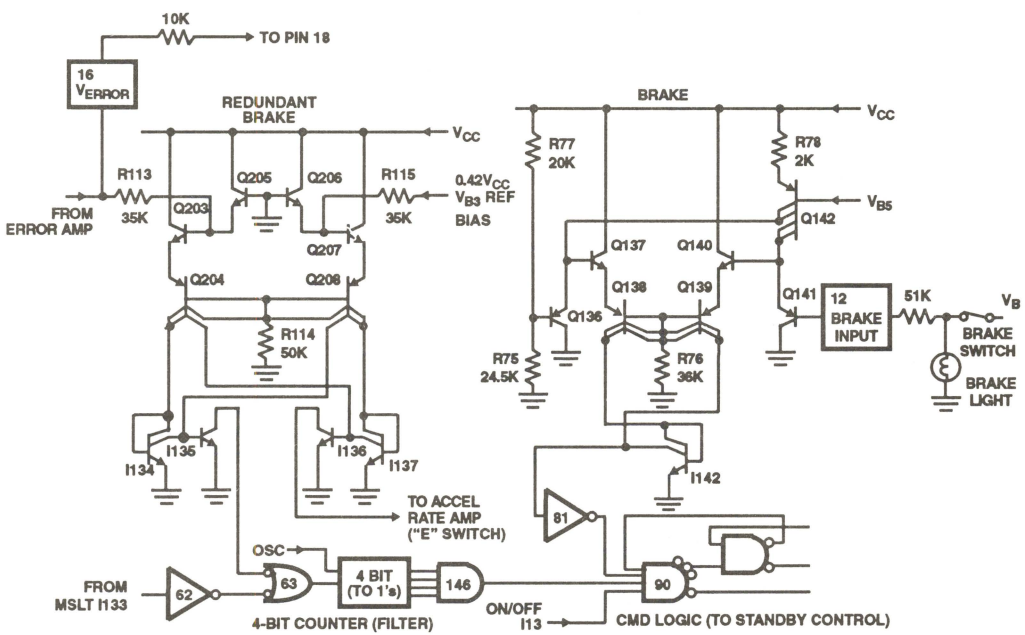


FIGURE 18. BRAKE AND REDUNDANT BRAKE

set along with a sufficient amount of hysteresis to assure noise immunity. When cruise conditions have been disrupted by braking action, and it is desired to return to cruise, the driver presses the switch for resume. The resume comparator samples V_S' and V_M and determines the fixed acceleration required for return to the speed previously stored in memory. An internal filter is used at the output of the comparator to prevent noise from resetting the comparator before V_S' reaches V_M.

Oscillator (Clock) Circuit

The circuit of Figure 20 shows the RC oscillator circuit used for internal clocking of the 9-bit ripple counter and the 4-bit counter that serves as a digital filter for the redundant brake. Various other elements of the command logic require oscillator control for the toggling of flip-flops. The oscillator frequency is an independent internal function on the chip, and has no relation to the frequency of the F/V converter input. A single capacitor at pin 5 determines the oscillator frequency. However, the fixed current source noted as V_{B5} also has an effect. The V_{B5} current source is derived from the same bias line that controls the F/V converter current sense drive from a 43kΩ resistor at pin 7. While the oscillator frequency may be changed by adjusting the resistor at pin 7, this adjustment will also change the F/V converter sensitivity. Since the voltage bias at pin 7 is approximately 5.5V, Q130 and Q131 are driven by 128µA through Q92 in the F/V converter (see Figure 5). The base bias line for Q131 is VB5, and is mirror connected to Q84 and Q85 in the oscillator. A charge current of 128µA goes to the 0.001µF capacitor at pin 5 from p-n-p transistor Q85. A 4x current mirror n-p-n transistor, Q86, discharges current at 512µA from the capacitor at pin 5. The resistor divider at the base of Q81 switches between 4.1V and 6.1V as I144 and Q85 are toggled on and off in the return feedback loop. With a charge current of 128µA and a discharge current of 512µA and using the equation:

$$t = VC/I$$

the clocking time, t, (and hence oscillator frequency) can be calculated using the 2V change for V, a 0.001µF capacitor value for C, and the charge and discharge currents for I. The result is 15.6 plus 3.9µs or a frequency of approximately 51kHz.

Operation and Performance

Table 1 defines the voltage values for the pins of the CA3228E IC. The annotations cover pins where conditions may be expected to vary. For further detail on the functions of the V_M and V_S voltages at pins 6 and 11, respectively, refer to the CA3228E data sheet.

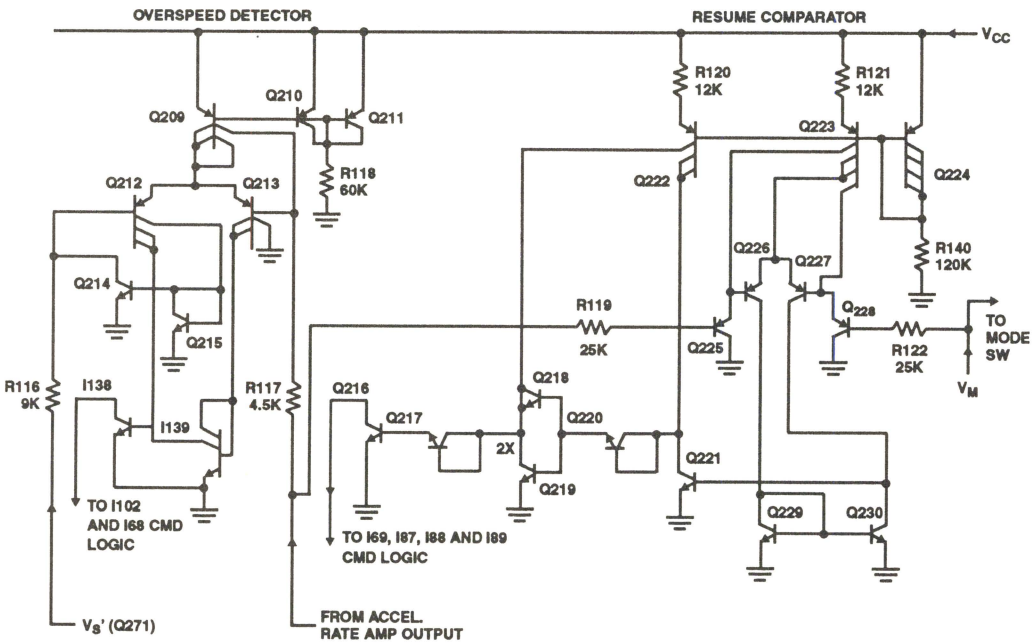


FIGURE 19. OVERSPEED DETECTOR AND RESUME COMPARATOR

TABLE 1. NORMAL CRUISE-MODE PIN VOLTAGES FOR THE CA3228E (NOTE 1)

PIN NO.	VOLTAGE	PIN NO.	VOLTAGE
1	Ground	13	8.2V Normal V_{CC} Supply Voltage
2	No Connection	14	4.55V
3	7.76V (Idle)	15	4.1V, 0.45 Less Than V_{15} in Accelerate Mode
4	0.01V	16	4.1V
5	5.2 V_{DC}, V_{AC} Sawtooth 4.1 to 6.1V	17	4.1V
6	1.5 to 6.5V, Speed Dependent (0V without Memory Set)	18	4.1V
7	5.45V	19	4.1V (Product of Error Voltage and Gain)
8	$\cong 0V_{DC}$, $\cong 2.5V_{AC}$	20	4.1V
9	4V Peak AC Signal	21	8.2V, Active Low
10	0V to 6.5V, sPeed Dependent, Equal to V_6 in Cruise Mode	22	0.06V, Active High
11	Same as V_{10}	23	0.025V
12	0.01V with Brake Switch Open	24	Ground

NOTE:

1. V_{CC} = 8.2V, speed set at 60mph (V_6 = 3.6V).

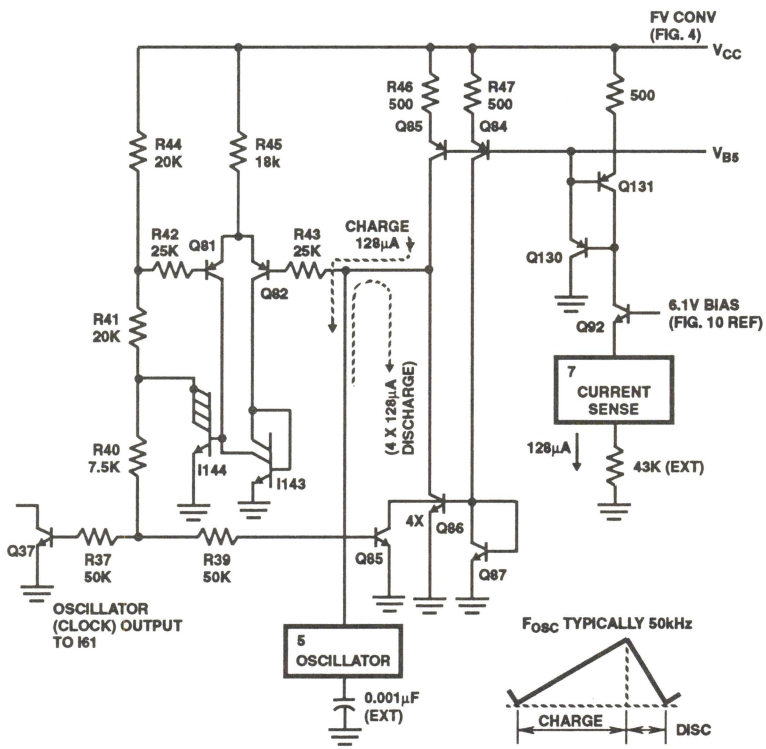


FIGURE 20. OSCILLATOR CIRCUIT USED FOR INTERNAL D/A CLOCK DRIVE

Note that the D/A converter cannot be set at low speeds and will remain at or near 0V until the frequency at pin 8 is near 50Hz (for the conditions of Figure 2). Dynamic signals are present at pins 5, 8, and 9. Speed dependent voltages are present at pins 6, 10, and 11. Error dependent signals have a notable effect on control amplifier output at pin 6 and the driver output pins 21 and 22. The command input at pin 3, the brake input at pin 12, and the gate output at pin 23 are mode dependent. The table does not reflect all of these changes since the conditions are noted only for a normal cruise setup at approximately 60mph. Again, the data sheet has further details on the various mode and state changes.

It is important to remember that the mode inputs are momentary touch switches except for the hold down condition of the accel and the coast switches. If pin 4 is monitored during the command input changes, it will be noted that delay switching times noted in the data sheet will be reflected at this pin.

Measures of the operating performance of the CA3228E are the wide power supply and temperature-operating ranges. The curve of Figure 21 shows the dynamic range of the power supply input V_{CC} at pin 13 over the temperature range of -40°C to +120°C. The normal V_{CC} specified is +8.2V ±0.8V or approximately 10% tolerance. The curves of Figure 21 also demonstrate a wide tolerance in the minimum to maximum range over which the device functions. A failure, as noted in the figure, is defined as a phase-locked-loop malfunction. Note that even with the wide range shown for power supply tolerance, it is still recommended that an external zener regulator or equivalent be used at the V_{CC} power supply input. Vehicular power supply conditions typically range from 9V to 16V, a range that exceeds the maximum range and rating for the operation of the CA3228E. While some applications may work at lower voltages than the recommended 7.4V minimum, operating conditions should not exceed the 9V power supply maximum rating.

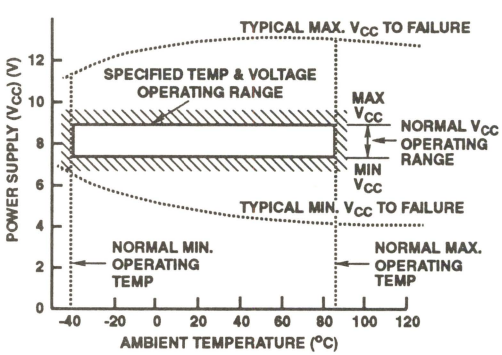


FIGURE 21. V_{CC} OPERATING RANGE OF THE CA3228E

Figure 22 shows another wide-range capability of the CA3228E when the temperature is varied. The V_S and V_M voltages are plotted versus temperature from -60°C to +100°C. Both the voltages for V_S and V_M are shown along with the equivalent speed condition for the typical application of Figure 2. For the 59.94mV/mph quoted above, the voltages of 4.3 to 4.5 are 72 to 75mph, respectively. It should be noted that Figure 22 is a measured curve from -55°C to +90°C with an equivalent 73.5 ±1.5mph error. Over the same range, the V_S and V_M readings typically tracked within 130mV while maintaining a cruise mode.

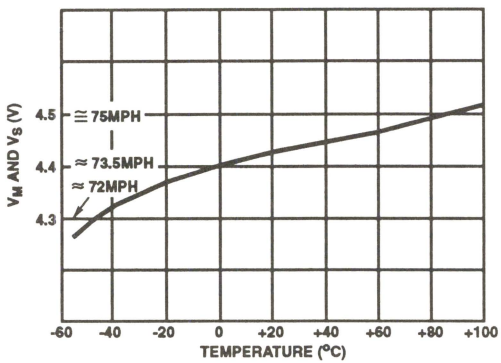


FIGURE 22. TYPICAL CHARACTERISTIC OF THE F/V CONVERTER OUTPUT, V_S, AND D/A OUTPUT, V_M, TRACKING vs TEMPERATURE IN THE CIRCUIT OF FIGURE 2

General Applications

A CD4046 CMOS VCO (voltage controlled oscillator) may be used in the external loop to drive the sensor input at pin 8. In the closed-loop circuit shown in Figure 23, the CA3228E will respond to the accelerate, cruise and coast conditions and provide the appropriate drive at the vacuum and vent outputs. From an idle mode after turn-on, the frequency may be adjusted by the 1MΩ potentiometer. The adjustable range of the potentiometer output to the VCO input at pin 9 is ground on the low end to V_{CC} on the high end. The 0.047µF capacitor between pins 6 and 7 and the 100kΩ resistor at pin 1 were chosen to accommodate a frequency range of 50 to 250Hz.

When a VCO frequency representing a given speed is set by the frequency control and applied to the sensor input at pin 8, the set value may be entered into the CA3228E D/A memory with the set/accel command. Changing the switch at pin 9 of the CD4046 to the loop position then closes the servo loop with the VCO set frequency retained in the D/A memory. The PLL of the CA3228E will maintain the frequency of the VCO, and any conditions that force the VCO off frequency will be corrected by cruise or resume mode control.

While the VCO closed-loop circuit was used to demonstrate the capability of the CA3228E, it is also apparent that many applications of the referenced circuit or variations of this circuit may exist.

Sketches of various application possibilities for the speed control system are shown in the functional diagrams of Figure 24. These applications have not been reduced to practice but are only suggested possible circuits. Since the MSLT and redundant brake affect the low end settings, a diode bias clamp of

1.6V should be used at pin 11 to keep V_S higher than the minimum speed lockout level. Pseudo DC voltage levels can be applied to pin 10 to set a V_S level for the D/A memory.

Further potential for use of the speed control system includes its combination with the CDP68HC05 series microprocessor control systems with added memory and D/A control.

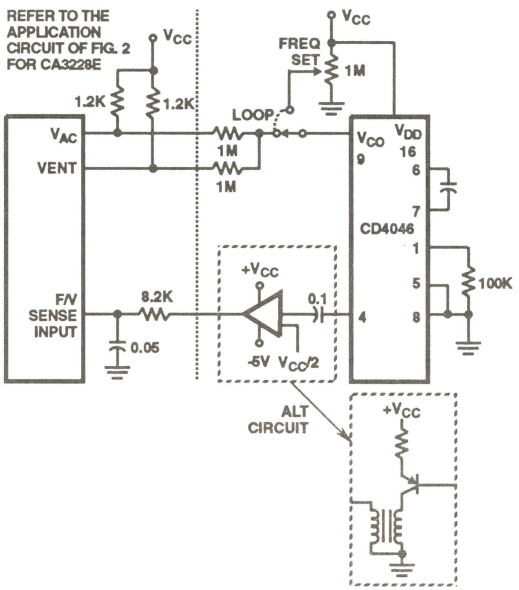


FIGURE 23. PLL OSCILLATOR FREQUENCY CONTROL CIRCUIT

References and Bibliography:

1. "CA3228E Speed Control System," Harris Data Sheet, File No. 1436.
2. "New Chips That Simplify Motor Control," L.J. Hadley, Machine Design, Feb. 12,1981.
3. "A Monolithic Speed-Control Micro-System For Automotive Applications," R.B. Jarret and W.D. Pace, ISSCC, 1978.

Acknowledgments

The author acknowledges the work of Gregory Kubak in engineering characterization, and T. DeShazo, R. Giordano, and A. Rodriques in design, development, and circuit information, and in editing support.

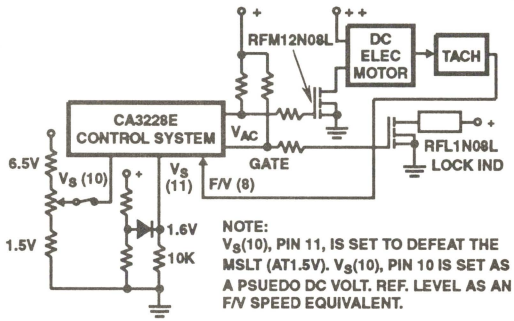


FIGURE 24A.

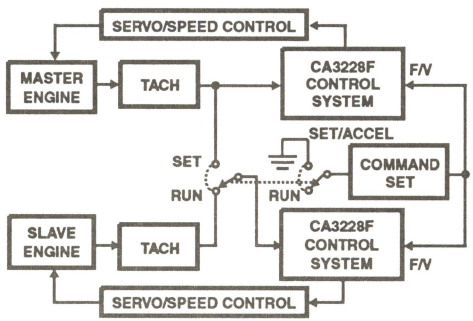


FIGURE 24B.

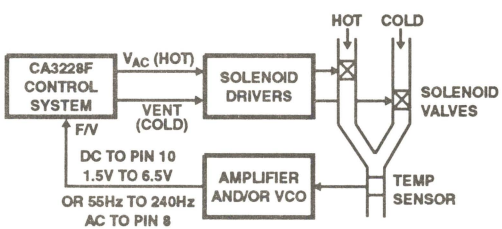


FIGURE 24C.

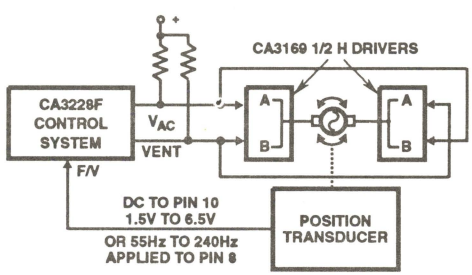


FIGURE 24D.

FIGURE 24. SUGGESTED APPLICATIONS OF THE CA3228E: A. DC MOTOR SPEED CONTROL, B. MASTER/SLAVE ENGINE SPEED CONTROL. SWITCH TO SET/ACCEL TO STORE MASTER SPEED IN SLAVE D/A MEMORY, THEN SWITCH TO "RUN". C. AIR OR FLUID TEMPERATURE CONTROL. (SEE A. FOR V_S SETUP CIRCUIT.) D. DC MOTOR POSITION CONTROLLER. (SEE A. FOR V_S SETUP CIRCUIT.)

Harris Semiconductor

APPNOTE

No. AN8614.1 April 1994

Harris Intelligent Power

THE CA1523 VARIABLE INTERVAL PULSE REGULATOR (VIPUR) FOR SWITCH MODE POWER SUPPLIES

Author: W. M. Austin

The CA1523, Variable Interval, Pulse Interval Regulator (VIPUR) is a monolithic integrated circuit designed for use in switch mode power supply (SMPS) systems. The advantages of both pulse interval modulation (PIM) and pulse width modulation (PWM) are combined in the VIPUR circuit. Figure 1 shows the block diagram and external circuit used in a typical CA1523 switching regulator circuit.

The special features of the CA1523, including a slow-start controlled power-up and mode sensitive logic control of the output pulse, provide several advantages in power supply applications. Intrinsic controls for adjustment of the pulse and frequency modulation range allow easy use of the CA1523 in a variety of SMPS systems, but especially those where line isolation is required.

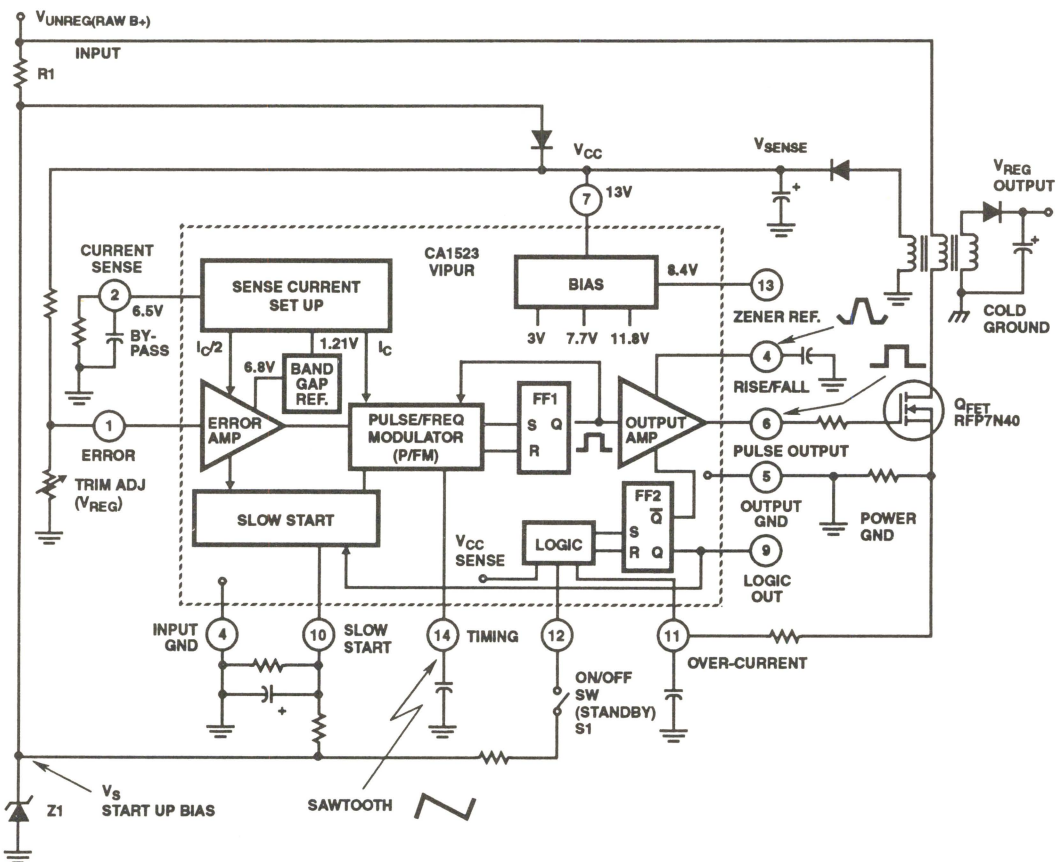
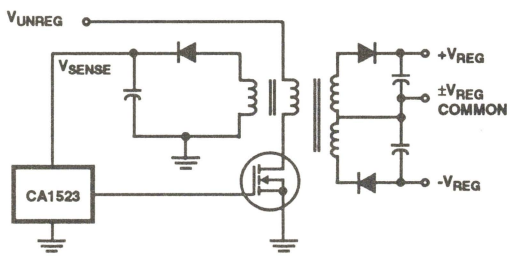


FIGURE 1. BLOCK DIAGRAM OF THE CA1523

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Systems that require line-isolated power supply voltages may be powered with the CA1523 regulator in a transformer flyback-converter system like the one shown in Figure 2(a). This system is particularly useful in meeting rigid safety standards when interfacing between workstation equipment or modular consumer audio and video instruments is required. Less stringent interface requirements may permit the use of regulators with a common ground for both the switching controller and power supply outputs; examples of these regulators are the flyback converter of Figure 2(b) or the buck converter regulator of Figure 2(c). However, the application of most interest is the line isolated type shown in Figure 2(a)



.FIGURE 2A. LINE ISOLATED FLYBACK CONVERTER

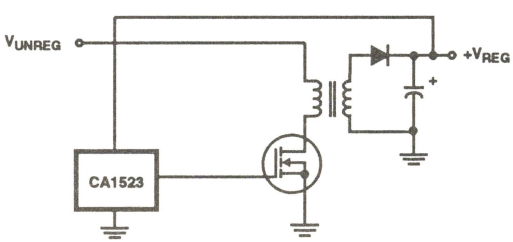


FIGURE 2B. NON-ISOLATED FLYBACK CONVERTER

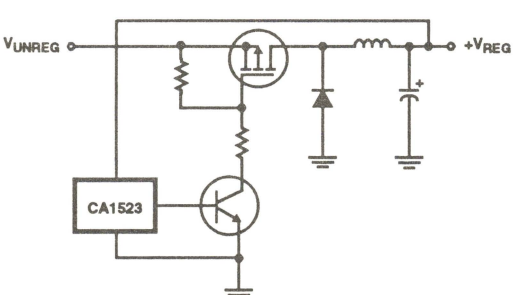


FIGURE 2C. BUCK CONVERTER REGULATOR

FIGURE 2. THE CA1523 IN SWITCH MODE POWER SUPPLY SYSTEMS

The PWM system is a popular mode of control in switching power supplies, as noted in the wide use of the CA1524. The counterpart of this mode of control, the PM system, was used extensively in the early period of switching power supply development. Both methods of control have their advantages and disadvantages. PWM offers effective control over a wide range of power supply loads. However, at the lower end of the load range, the PWM becomes limited because of the minimum pulse width, T_{ON}, required. In addition, the rise and fall time of the drive pulse of the power switching transistor must be slowed down to meet RFI and EMI requirements. On the other hand, the PIM can handle low loads better because the duty cycle is reduced by increasing the pulse interval. However, the low range of the operating frequency may cause filtering-related problems in audio or other sensitive instruments. Another problem with PIM at the low-frequency end is the related conversion losses.

The CA1523 is primarily a PIM controller with built-in PWM correction over a 2-to-1 pulse width range. For a frequency f and an associated period T, the pulse width reduces from a maximum width of T/2 (50% duty cycle), corresponding to the highest frequency at the maximum load limit, and approaches T/4 at the lowest frequency and minimum load.

The combination of both PIM and PWM control effectively compresses the operating frequency range over that of a pure PIM control for a given range of load. The combined CA1523 VIPUR advantages at minimum frequency include reduced losses and low ripple with improved efficiency and regulation. Pulse-widih correction done simultaneously with pulse-interval correction produces an inherent gain magnitude of approximately 2 at 50% duty cycle under high-load conditions. This feature helps in keeping the error-amplifier gain low, and improves stability without the addition of expensive external components.

Features of the CA1523

As shown in Figure 1, the output drive pulse of the CA1523 is modulated and mode-controlled by several system features:

1. The output drive pulse has a maximum continuous ±50mA capability into an 1800pF load.
2. The peak transient load is +300mA and -200mA for a maximum of 1µs.
3. The maximum pulse width can be controlled by choice of the timing capacitance at pin 14 and the current-sense resistance at pin 2.
4. The output-pulse rise and fall time can be controlled by choice of the rise/fall-time capacitor at pin 4.
5. The slow-start threshold of the pulse output is controlled by choice of the resistance at pin 2.
6. The output-pulse interval is rate controlled during power-up by the slow-start RC-charge time constant at pin 10.
7. Maximum output frequency is in excess of 200kHz, and is user controlled.

8. Output pulse interval and width corrections are maintained by the error voltage feedback to pin 1.
9. The standby on/off switch between pins 7 (V_{CC}) and 12 controls the output pulse. As an option, the on/off function may be controlled by logic-level switching at pin 12 or by line-isolated switching using an optical coupler.
10. Overcurrent shutdown may be controlled by using a sense resistor in the load circuit to shut down the output drive pulse.

Other Features of the CA1523 Include:

1. A substantial level of ESD (electrostatic discharge) protection designed into the interfacing pin terminals of the chip.
2. An 8.4V internal zener voltage reference for the on-chip bias circuits.
3. A 1.21V bandgap that provides a stable voltage reference for bias to the timing circuit and error amplifier.
4. NOR logic control of shutdown of the output pulse under fault conditions for low V_{CC}, on/off, and overcurrent. Pin 9 is a monitor or output indicator of a fault condition.
5. Availability in an economical 14 pin DIP package.

Control Structure of the CA1523

The CA1523 has five primary circuit functions:

1. Error amplification
2. Pulse/frequency modulation
3. Pulse driver/output amplification
4. Slow-start power-up control
5. System logic control

The block diagram of Figure 1 shows the interrelated functions of the circuit. When the system raw B+ is switched on, the slow-start function controls the pulse/frequency modulator, P/FM, until the voltage at pin 10 is greater than 7V.

Standby conditions then exist until switch S1 is closed. In the standby mode, the P/FM maintains a maximum frequency output with a 50% duty cycle. After switch S1 is turned on, the output amplifier is enabled and the P/FM response is a function of the error voltage at pin 1. The error amplifier accepts error-correction inputs and controls the pulse and frequency modulation. The P/FM output pulse is then amplified in the driver and output stage.

Figure 3 shows the timing-circuit schematic of the CA1523. For a given timing capacitance, C_T, the maximum frequency of the P/FM circuit is determined by the current-sense bias at pin 2. The current-sense level, I_S, is set by the fixed resistor at pin 2, R_S, which goes to ground. A resistor divider reference at the base of Q92 of differential amplifier Q91, Q92, is approximately $V_{CC}/2$. The differential amplifier feeds back, via Q17C, any error in the balance of Q91 and Q92, while holding the pin 2 voltage at the $V_{CC}/2$ reference level. The differential emitter current is supplied by Q93, and is determined by the bandgap bias voltage of 1.21V at the base of Q93.

The differential emitter current is approximately equal to the collector current of Q17C; the collector currents of Q17A and Q17B are current mirrors to the collector current of Q17C. The currents $I_C/2$ and I_C provide the P/FM charge and discharge timing, and are, respectively, the collector currents of Q17A and Q17B. The current ratio is $^1/_2$-to-1 to accommodate a 50% duty cycle at maximum frequency and load conditions. When start-up conditions exist, and the pin 1 error voltage is low, Q6 passes all of the $I_C/2$ current to Q11. Since Q11 and Q18 are current mirrors, the collector of Q18 discharges the timing capacitor, C_T, at pin 14. The state of the flip-flop, FF1, determines whether Q15 will conduct current I_C from Q17B into the timing capacitor.

When Q18 is discharging current from C_T at an $I_C/2$ rate, and Q15 is charging C_T at an I_C rate, the net charge current is $I_C/2$. This is an FF1 high state for the Q output, and Q16 is cut off while Q15 is conducting current I_C. The positive voltage ramp at pin 14 increases until the V_H comparator toggles at the 5V reference to the inverting input, resetting FF1, with the Q output going low. When Q is low, Q15 is cut off, and no charge current passes to C_T. Timing capacitor C_T is then discharged by Q18 at a maximum rate of $I_C/2$. The discharge ramp continues until the voltage at pin 14 reaches 2.5V, when the V_L comparator toggles the S input of FF1 to a high state. The cycle of charge/discharge to timing capacitor C_T is complete when the Q output of FF1 goes high in response to the high at the S input.

The above operation occurs when the error voltage is lower than the 6.8V differential input reference, a condition that allows the full $I_C/2$ discharge of C_T by the Q11 and Q18 current mirror. After being turned on from the line power source, the slow-start function shunts Q6 collector current through Q2. As a result, the Q11,Q18 current mirror initially receives little or no forward bias current, and C_T cannot be discharged. As the slow-start voltage increases, the current in Q2 decreases, allowing Q11 and Q18 to discharge C_T at an increasing rate. As long as the error voltage at pin 1 remains below the 6.8V reference level, the charge and discharge rate is at the 50% duty cycle condition.

In reference to the slow-start circuit of Figure 3, an increase of the slow-start bias on capacitor C2 at start-up exercises a decreasing degree of control over the discharge timing. If the current-sense adjustment at pin 2 is typically less than 100μA, there will be a full frequency range of slow-start control, and the range of increasing pulse width will be 2 to 1. Higher pin 2 bias currents will reduce the range of frequency control. The input to pin 10 drives the base of p-n-p transistor Q34. A 30kΩ emitter resistor, R22, is returned from Q34 to an internal 7.7V bias source. Transistors Q1 and Q2 mirror the Q34 collector current and shunt the Q6 collector current away from Q11, reducing the discharge current in the timing control circuit. As an example, with 4V at pin 10, there are approximately 3V across emitter resistor R22. This arrangement allows the discharge current to be controlled over a range of 100μA. A bias resistor in the range of 56kΩ to 68kΩ between pin 2 and ground is suggested for a full range of slow-start control. Higher levels of pin 2 sense current increase the $I_C/2$ current beyond the full range of the slow-start bias control at pin 10.

When a power-on condition has been established, slow-start completed, and S1 switched on, the CA1523 begins normal regulation through error-voltage control as follows. When S1 is switched on, maximum energy conversion occurs in the switched transformer. The supply voltage approaches normal regulation level, and the error voltage increases toward the 6.8V reference level. The error voltage is set by a resistive divider ratio determined from the rectified voltage of the transformer sense winding. The Q5, Q6, Q7, and Q8 differential controls the Q6 current to the Q11, Q18 current mirror, decreasing Q6 current as the error voltage increases. A portion of the $I_C/2$ current from Q17A is passed by Q6. This current controls the P/FM output pulse and maintains regulation at the desired level, as determined by adjustment of the divider at pin 1. Pulse output continues from FF1 during regulation, but at a reduced rate and with reduced pulse width. The Q output of FF1 is always high during the positive ramp at pin 14, a condition of maximum charge current to C_T. At minimum load, the pin 1 voltage increases, and the net charge current for the positive ramp is higher because Q18 is discharging less current. For example, if the error voltage at pin 1 is forcing half of the $I_C/2$ current to Q7, the Q6 current is $I_C/4$, and the net positive ramp charge current at pin 14 is:

$$I_C - I_C/4 = 3I_C/4$$

The net negative-ramp discharge current is then $I_C/4$. What had been a maximum charge and discharge rate of $I_C/2$ at start-up is now pulse-interval and pulse-width modulated to provide a 3 to 1 charge/discharge ratio.

To generalize, we can establish the range of error correction by assigning a k factor to the decimal portion of the Q17A collector current that is shifted from Q6 to Q7. Let k = 0 when V_1 (pin 1 voltage) is low and all Q17A current ($I_C/2$) flows through Q6 to discharge pin 14. k = 1 when all Q17A current is shifted to Q7 and there is no discharge current to pin 14. The maximum rate of charge and discharge is established by the sense current, I_S at pin 2; I_S is approximately $I_C/2$.

Since:

$$V = (1/C) \times \int i dt$$

For a constant rate of charge (or discharge) current:

$$V_H - V_L = I_{CHARGE} \text{ (or } I_{DISCHARGE}) \times (T_2 - T_1)/C.$$

And:

$$T_{ON(MAX)} = (V_H - V_L)C_T/I_S.$$

From Figure 3, the range of $(V_H - V_L)$ is approximately (5.0 - 2.5), or 2.5V, and I_S is approximately equal to $V_{CC}/2$ divided by R_S.

The above information is used to establish the pulse interval or system frequency. The frequency is the reciprocal of T_{ON}(charge) plus T_{OFF}(discharge). As V_1 increases, k increases. The positive ramp charge current to pin 14 and C_T is:

$$I_{CHARGE} = I_C - (I_C/2)(1 - k) = 2I_S - I_S(1 - k) = I_S(1 + k).$$

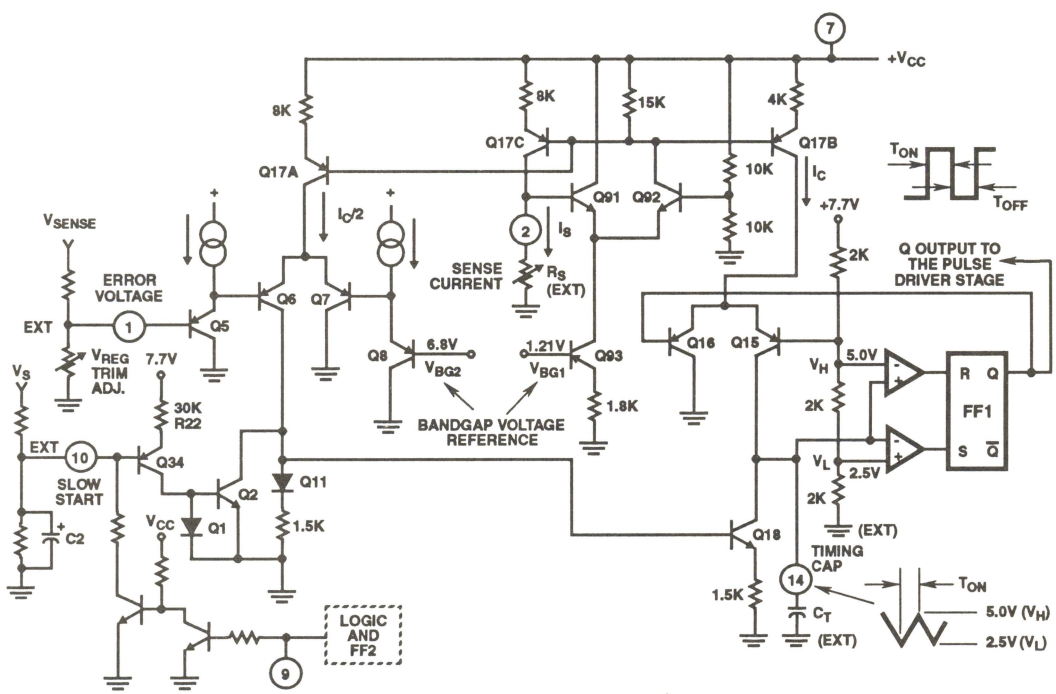


FIGURE 3. PULSE/FREQUENCY MODULATION AND TIMING CIRCUIT FOR THE CA1523

Since I_C is cut off during discharge:

$I_{DISCHARGE} = I_S(1 - k)$

Therefore, during charge:

$T_{ON} = [(V_H - V_L)C_T]/[I_S(1 + k)] = T_{ON}(max)/(1 + k)$

and, during discharge:

$T_{OFF} = [(V_H - V_L)C_T]/[I_S(1 - k)] = T_{ON}(max)/(1 - k)$

Note that T_{ON} approaches $T_{ON}(max)/2$ as k approaches 1. This is the condition of minimum power supply load. With the time conditions for T_{ON} and T_{OFF} established, the frequency, f, can be defined as:

$f = 1/(T_{ON} + T_{OFF}) = (1 - k^2)/2T_{ON}(Max)$

Since the maximum frequency occurs at k = 0:

$f_{MAX} = 1/2T_{ON}(Max)$ and

$f = f_{MAX}(1 - k^2) = (1 - k^2)/2T_{ON}(Max)$.

The duty cycle is $T_{ON}/(T_{ON} + T_{OFF})$ which, by substitution, is:

$D = (1 - k)/2$

Since k is the current split ratio of the input differential amplifier, the differential equation applies, that is:

$k \cong 1/(1 + e^{\Delta V/h})$

where e is the natural log value of 2.718, h is KT/q (≅26mV), and ΔV is V_1-V_{REF}. The equation for k is approximate, but provides a reasonably accurate transfer function for the CA1523 when output pulse width, frequency, and duty cycle may be calculated for given values of (V_1 - V_{REF}).

As k goes to 1, the frequency goes to zero, implying a no-load condition on the power supply. This is an improbable condition; however, the lowest system frequency is always determined by the minimum power supply load.

The timing circuit of the VIPUR is a stand-alone pulse generator in which the Q output of FF1 is amplified by the driver output circuit of Figure 4, subject to the logic control of transistor Q33 and the proper logic-state control for the slow start (SST), ON, V_{CC}, and overcurrent (OC) inputs shown in Figure 5.

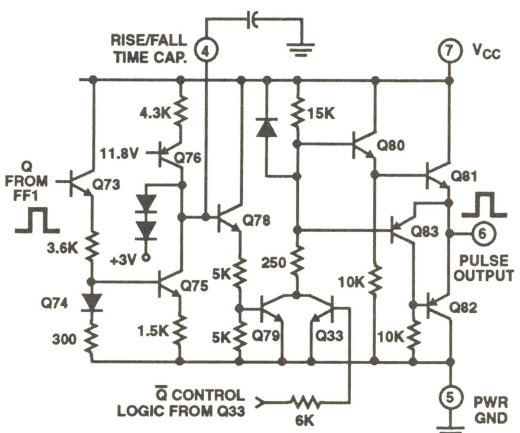


FIGURE 4. CA1523 DRIVER AND OUTPUT STAGE

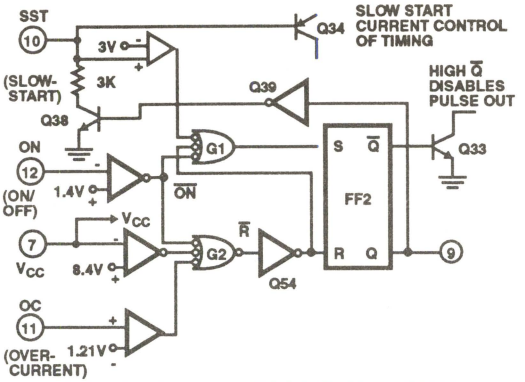


FIGURE 5. CA1523 LOGIC CONTROL DIAGRAM

The test circuit of Figure 6 demonstrates the pin 2 current sense (I_S) range using timing capacitance values of 100pF, 240pF, and 470pF. Figure 7 shows the frequency versus I_S current at pin 2. Figures 8 and 9 show the range of pin 6 pulse width and duty cycle. Since the curves of Figures 7, 8, and 9 were determined with V_1 at approximately 5.9V (much less than the 6.8V reference) maximum frequency conditions apply to all Figure 6 curves. With the rise/fall-time capacitance of 68pF at pin 4, the rise/fall delay will affect the duty cycle when the frequency is greater than 120kHz. Removing the pin 4 capacitance will extend the maximum frequency to well above 200kHz. However, use of the rise/fall-time delay function is important to the control of EMI and RFI. The optimum rise/fall capacitance value is chosen to assure a 50% duty cycle at the maximum frequency with a reasonable margin in design tolerance and, for the system requirements, to ensure compliance with EMI and RFI requirements.

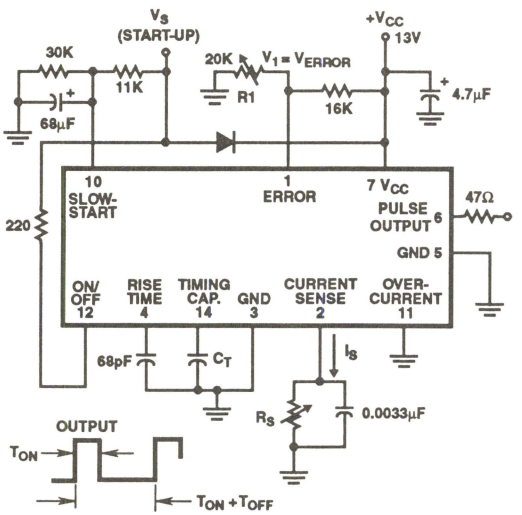


FIGURE 6. VARIABLE-INTERVAL SWITCHING-REGULATOR TEST CIRCUIT USED TO OBTAIN TIMING CURVES OF FIGURES 7, 8, AND 9

Where there are no external system restrictions on the operation of the CA1523, and the function is that of a pulse generator, very large values of capacitance may be used at pin 14 to achieve very low pulse frequencies. External resistor loading at pin 14 will contribute a nonlinear slope to the otherwise linear sawtooth there. This nonlinear contribution can also be noted in the waveform at pin 14 if the timing capacitor has less than 10MΩ leakage. Very low values of I_S are not recommended because the balance of charge and discharge currents is, to some degree, affected by base bias and junction leakage currents. As noted by the degradation of duty cycle balance in Figure 9, and for practical reasons, I_S should be greater than 20μA. The upper limit for I_S is determined by the maximum available collector current from Q17C, which is typically 350μA.

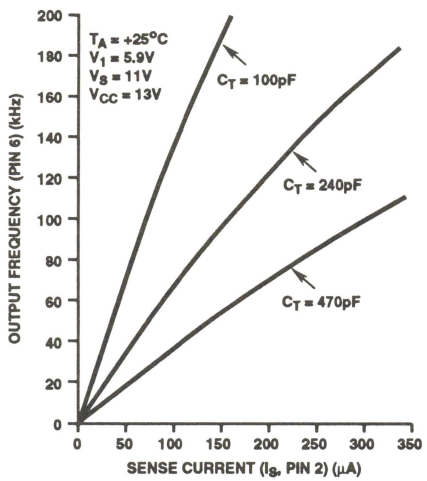


FIGURE 7. PULSE/FREQUENCY MODULATOR CHARACTERISTIC OF FREQUENCY vs. TIMING CAPACITOR C_T AND SENSE CURRENT I_S (T_A = +25°C, V_1 = 5.9V, V_S = 11V, V_{CC} = 13V.)

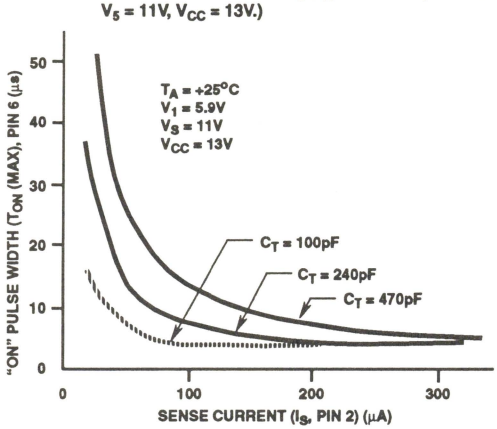


FIGURE 8. PULSE/FREQUENCY MODULATOR CHARACTERISTIC T_{ON}(MAX) OUTPUT PULSE WIDTH (PIN 6) vs. CURRENT SENSE (PIN 2). (T_A = 25°C, V_1 = 5.9V, V_S = 11V, V_{CC} = 13V.)

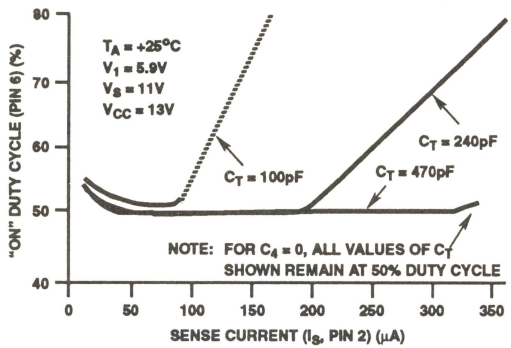


FIGURE 9. PULSE/FREQUENCY MODULATOR CHARACTERISTIC "ON" DUTY CYCLE (PIN 6) vs. CURRENT SENSE (PIN 2).

CA1523 Generated Waveforms And Delays

The signal waveforms of the CA1523 are shown in Figure 10, and are based on the test circuit of Figure 6, where R_S is adjusted for a maximum frequency of 100kHz. Because the sink and source current drivers of the timing capacitor, C_T, are constant current generators, the waveform at pin 14 is a very linear sawtooth. As noted in Figure 4, the waveform at pin 4 is derived from the Q75 sink and Q76 source drive currents, but is normally clipped at the top and bottom. The positive tip of the pin 4 signal is set by a positive clamp from two series diodes to an internal 3V bias source, providing a clamp level of approximately 4.5V. The bottom, or negative, truncation is the result of a current sink depletion of the charge on the rise/fall-time capacitor at pin 4. The degree of waveform clipping is determined by the maximum operating frequency and the value of the rise/fall time capacitor at pin 4.

In Figure 4, the rise, delay, and fall times of the input drive signal, Q, are controlled by the capacitance at pin 4, amplified, and output at pin 6. The Q input, a square wave output pulse from the timing generator (Figure 3), drives the rise/fall capacitor via the Q73 buffer and the Q74, Q75 current mirror. Rise time is determined by the Q76 constant current source. As such, the sink and source currents control the voltage at pin 4. Capacitance loading at pin 4 provides a controlled rise and fall delay time. With the 68pF capacitance shown in Figure 6, plus 10.5pF probe capacitance, the waveforms are as shown in Figure 10. A rise-time delay of 1.6μs is noted at the 2.1V point on the pin 4 waveform. The signal at pin 4 drives the base of Q78 and, through a resistor divider, Q79. Approximately 2.1V is required at pin 4 to switch Q79 and set the delay, which can be calculated from the rise time equation for constant currents. The source current from Q76 is approximately 100μA, and the delay, T_D, is:

$$T_D = VC/I = [(2.1V)(68 + 10.5pF)]/(100\mu A) = 1.6\mu s$$

If the rise time capacitor at pin 4 is too large, the peak voltage will be reduced below the positive clamp level. This condition will cause the on-time duty cycle at pin 6 to be increased. The rise time capacitor at pin 4 must be adjusted to restore the duty cycle to 50% at the maximum frequency

condition. When no external capacitor is used at pin 4, maximum operating frequencies in excess of 300kHz are possible. An example of the typical CA1523 pulse output capability at high frequency conditions is provided below.

Using the circuit conditions of Figure 6 with no pin 4 capacitor, I_S = 160μA, and C_T = 50pF, the pin 6 output pulse is:

$$t_R = 250ns$$

$$f_{(MAX)} = 312kHz$$

$$T_{ON}(Max) = 1.6\mu s$$

$$T_{ON}(Min) = 0.8\mu s$$

Additional delay in the pin 6 output drive pulse may result from the conditions of loading. The normal specifications for the CA1523 are given for a 68pF rise/fall-time capacitance at pin 4 and an 1800pF output capacitance loading to reflect typical drive requirements for a power-FET switch transistor. The rise and fall times for 1.8V and 10V thresholds at the V6 output are typically t_R = 600ns and t_F = 200ns.

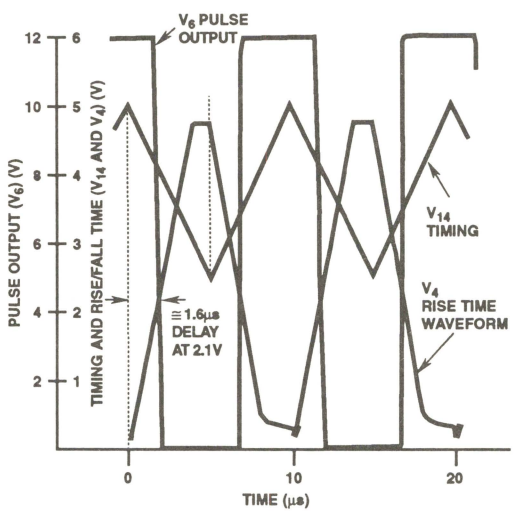


FIGURE 10. SIGNAL WAVEFORMS OF THE CIRCUIT OF FIGURE 4 (WITH 10.5pF TEST-PROBE LOADING). (C_T = 240pF, R_S APPROXIMATELY 39kΩ, $F_{(MAX)}$ = 200kHz.)

Application Circuits

TV Monitor Flyback Converter

Figure 11 shows a typical television receiver application of the CA1523. Line isolation permits use of the TV receiver as an RGB or composite-video DC-coupled monitor. In this system, the switching transformer isolates the power line from the signal circuits of the TV receiver. As shown in the block diagram of Figure 11, 120V_{AC} is connected through a fuse to the bridge rectifier and a step-down transformer, T2. The rectified output of the step-down transformer is used as a 16V standby power supply for the TV control module. The control module, in response to the user input control, switches Q2 on and off to control turn-on of the VIPUR regulator through the optoisolator. The bridge rectifier supplies a +150V raw B+ to the VIPUR start-up circuit and to the primary of the switching transformer, T1. After start-up, the run supply provides a regulated +V_{CC} for the CA1523 from the sense feedback circuit. In normal regulation, the VIPUR drives the Q1 power MOSFET, which switches the primary of T1. T1 converts regulated power to the cold 20V, 25V, and 150V levels required for the power supply outputs and the run-supply circuit.

Figure 12 explains the on/off operation of the switching power-supply portion of the converter application. The logic function maintains control of the on/off operation of the system. In the off state, the system remains in a standby mode as long as the 120V_{AC} is connected. Standby power is supplied via the start-up circuit, which consists of R2 and the 11V zener diode CR3. Continuous start-up bias is supplied to the +V_{CC} function at pin 7, the on/off input at pin 12 via the optoisolator, and the slow-start circuit at pin 10. The 11V source is connected to the pin 7 +V_{CC} function via the forward biased diode, CR13. The logic function inputs (as previously noted in Figure 5) are the B+ sense from pin 7, the slow-start function at pin 10, the on/off function at pin 12, and the overcurrent function at pin 11. The logic function responds to a voltage level for each input and, if the voltage range of a required input is not met, shuts down the output amplifier, so that no pulses appear at pin 6. After start-up, normal operation is resumed when the on/off input is greater than 2.5V, the peak overcurrent input is less than 1.2V, and the B+ sense has determined that +V_{CC} is greater than 8.4V. The slow-start function controls the gradual start-up of the pulse and frequency modulation functions such that a slow RC rise time at pin 10 is synonymous with a slow decrease of the pulse interval. As the pin 10 voltage increases, the slow-start allows a gradual increase of the I_C/2 discharge current. As the voltage at pin 10 increases from 3V to 7V, the full range of slow-start control over the P/FM changes from zero to maximum frequency. The RC time constant consisting of R1, C7, and R3 controls the slow-rise voltage at pin 10. The slow increase controls the power-up rate and limits the start-up dissipation in power MOSFET Q1.

The on/off function could be controlled by an insulated manual switch or a relay. However, the optoisolator has the advantage in that it can be remotely controlled with low standby power. The overcurrent shutdown voltage is sampled from the source terminal of the power MOSFET, Q1, to assure that peak currents in the transformer primary circuit will be fault-mode limited. When start-up is complete, the run B+ is greater than the start-up supply voltage from the 11V zener diode, and CR13 is reverse biased. The on/off and slow-start input circuits remain under the control of the 11V start-up source, but the VIPUR power supply is transferred to the well-regulated run B+ supply derived from the sense winding of the transformer.

Figure 13 shows the VIPUR switching-regulator output operation as it functions in a normal feedback mode. As explained above, the error amplifier at pin 1 is differentially compared to a 6.8V internal reference. The error amplifier supplies the correction signal for the P/FM. Pulse and frequency modulation is

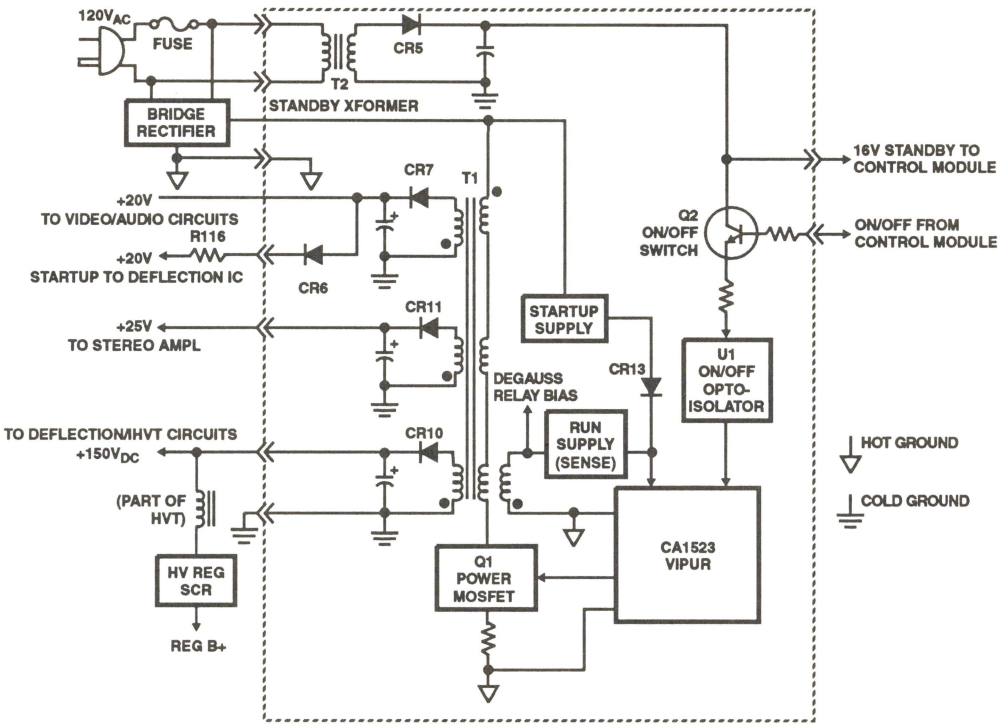


FIGURE 11. GENERAL TV MONITOR APPLICATION OF THE CA1523

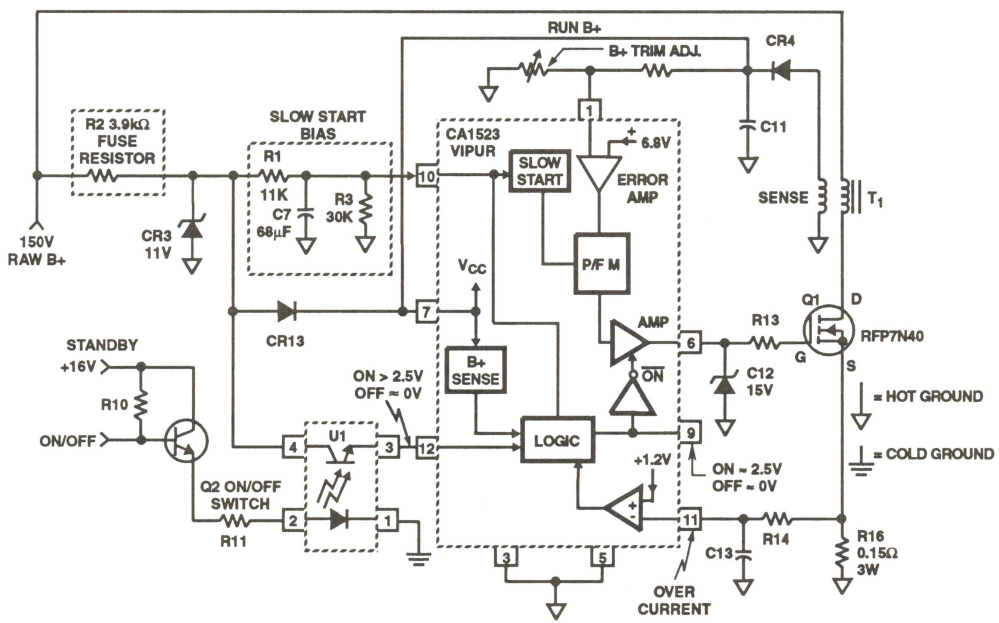


FIGURE 12. SWITCHING POWER SUPPLY ON/OFF OPERATION

controlled by timing-capacitor C15 and sense-current resistor R9. The output amplifier is controlled by the logic input; its rise time is controlled by capacitor C14. Zener-diode CR12 and resistor R13 are used to protect the gate of power MOSFET Q1. As Q1 switches the raw B+ current through the primary of the ferrite transformer, T1, power is supplied to the output windings and the sense winding. The pulse in the sense winding is rectified, and supplies run power to the CA1523 and error feedback to pin 1 through the resistor divider. The ratio of resistor R8 to the parallel trim resistors R4, R5, R6 and R7 sets the output voltage of the CA1523. The required output voltage of the regulator is determined by clipping resistors from the PC board.

A limited-range potentiometer adjustment may be used to control the regulator output, but this approach can be potentially dangerous if the high voltage of the CRT is not limited in some way. The fixed resistor-divider network is preferred for safety reasons. Because of the tight coupling of the transformer windings, the sense winding reflects the input-voltage changes and output-loading conditions. The preferred run B+ is 12V to 13V. The product of the resistor-divider ratio and the run B+ voltage should be, typically, 6.8V. When working with direct AC line power supplies, an isolation transformer must be used for hot AC line protection. Figure 14 joins together the circuits referenced in Figures 11, 12, and 13. The parts of the circuit connected to the "hot" line are identified at the center of the schematic. In addition to the circuitry discussed above, Figure 14 shows various chokes, bypass capacitors, and ferrite beads used in conjunction with the diode-rectifier filtering. These components are normally required to improve filtering and to reduce EMI and RFI.

CA1523 Buck Converter Switching Regulator

Figure 15 is the circuit schematic of a buck-type regulator useful in lower-voltage applications with a nominal raw B+ of 28V and an input tolerance range of 18V to 38V. This circuit has been chosen to illustrate some of the special capabilities of the VIPUR circuit; but, for the most part, these features are applicable to any other circuit controlled by the CA1523. The circuit of Figure 15 has special start-up features that minimize standby current in zener diode Z1 and make use of the internal zener diode for slow-start control. As shown, the error feedback voltage has been made adjustable over a typical range of 6.8V to 13.5V. The pulse frequency range is typically 25kHz to 75kHz, and the regulation at a nominal 12V output is typically 0.3%.

This circuit normally requires an output transformer only when it is desirable to isolate the output from the input. The pulse output of the CA1523 is inverted in a 2N2102 and used to drive an RFP8P10 p-channel enhancement mode power FET. The power FET is driven by the 2N2102 through a resistive divider that limits the maximum source-to-gate voltage. In the drain circuit of the power-FET output there is a shunt RUR-820 fast-switching catch diode followed by a filtering circuit comprising a 0.5mH choke and a 470µF capacitor.

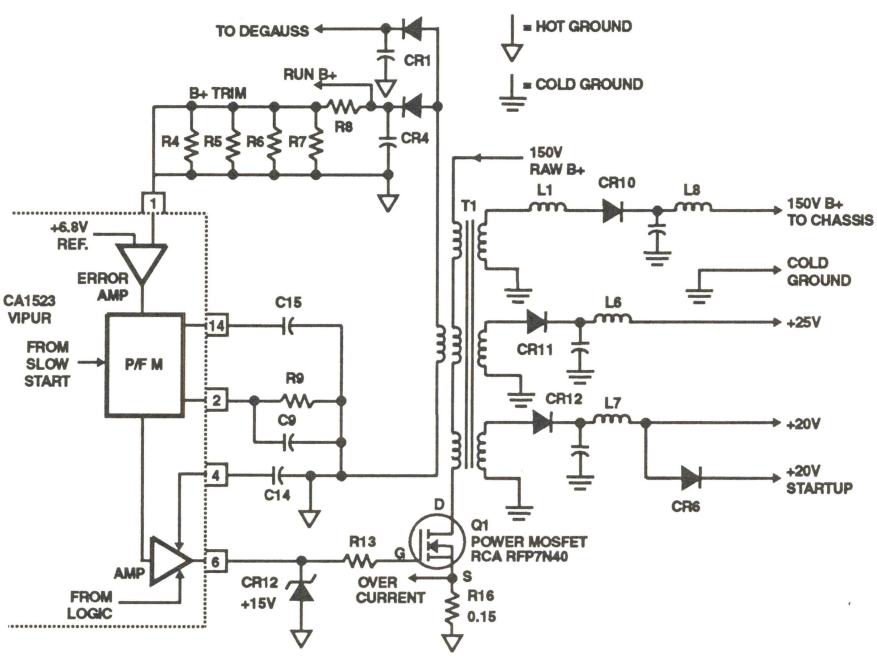


FIGURE 13. SWITCHING REGULATOR OUTPUT OPERATION

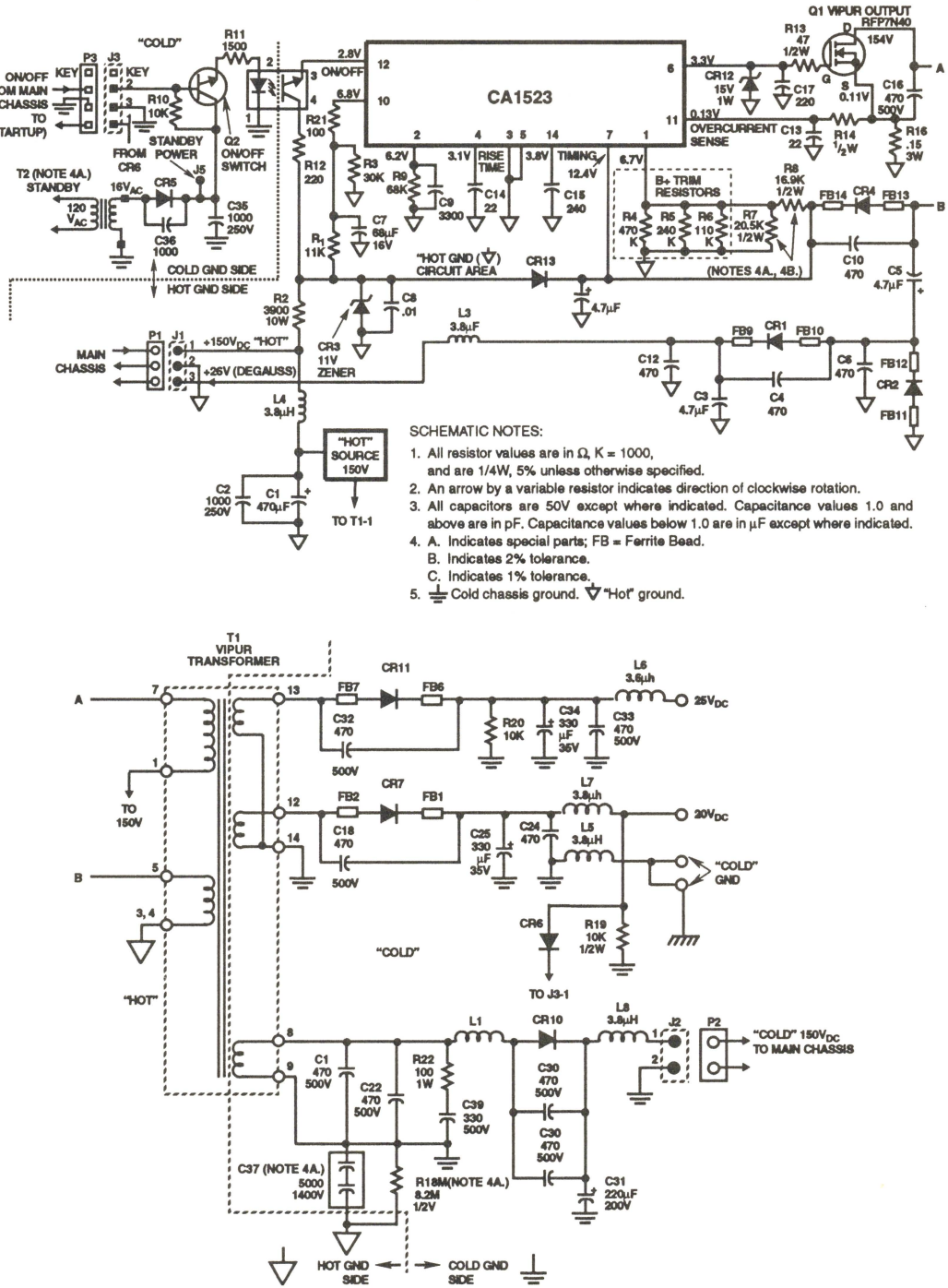


FIGURE 14. APPLICATION OF THE CA1523 VIPUR IN RCA CTC-130 TELEVISION CHASSIS POWER SUPPLY MODULE

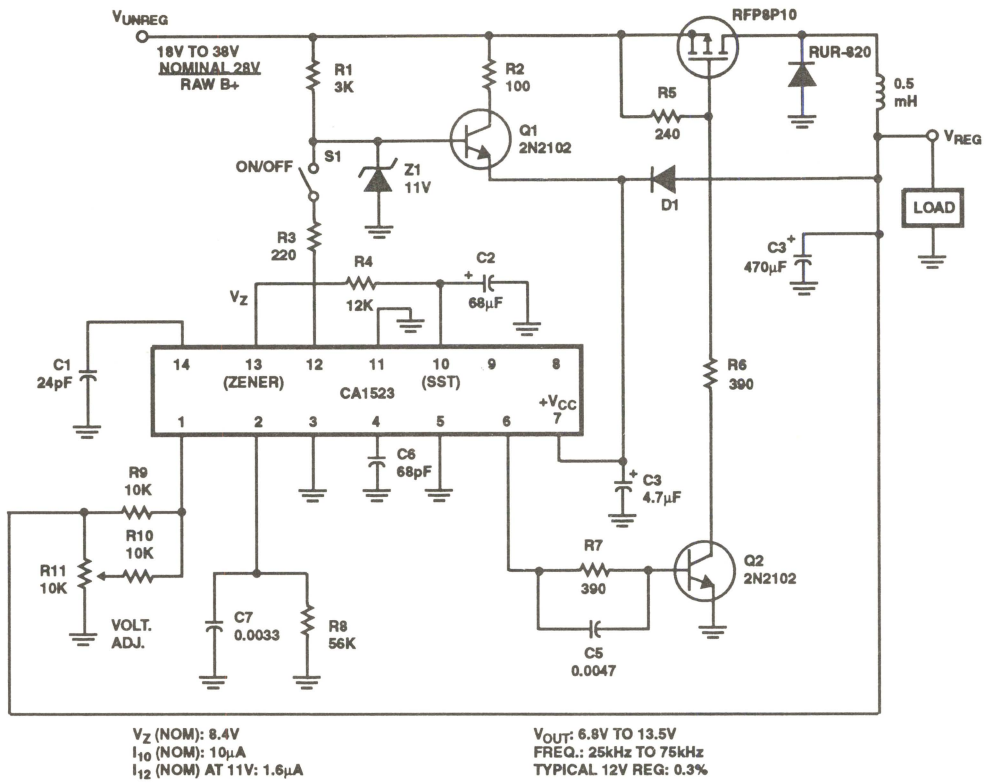


FIGURE 15. BUCK REGULATOR FEATURING ADJUSTABLE OUTPUT VOLTAGE AND SLOW START USING CA1523 ZENER

The raw B+ input may be a 28V battery source or the filtered output of a bridge rectifier supplied from a line isolated step-down transformer. The start-up components are substantially different from those shown in the transformer-isolated flyback-converter circuit, although, as noted, the start-up circuit shown here may be applied in either system. If the output voltage range of the regulator is chosen, as it is typically, to be 11V to 13V, transistor Q1 conducts only for a brief period after S1 is closed. The run B+ is supplied through diode D1 to $+V_{CC}$ at pin 7, and the emitter of Q1 is reverse biased after the power-up cycle is complete. This situation substantially reduces the continuous running dissipation of zener Z1 and resistor R1.

Even when the V_{REG} voltage is less than the zener voltage level, the base current to Q1 is a fraction of a milliampere in a normal run mode. However, more base current is required to charge C4 at line turn on. After start-up is complete and the standby on/off switch is closed, approximately 1.6mA of current is supplied to pin 12. Typically, less than 2mA are needed to sustain idle current to zener Z1. The difference in these losses for the circuit conditions shown in Figure 15 versus those shown in Figure 14 is approximately 2mA versus 35mA. A number of bias options are available for implementing the error-voltage feedback; most of the options are adaptable to either the buck regulator or the transformer flyback-converter system. Either system must feed back a sense return voltage of approximately 6.8V to pin 1. It is not required that the CA1523 be powered by the sense return voltage, but if it is, the voltage should be approximately 11V to 13V. The CA1523 will operate over a supply-voltage range of 9.5V to 15V.

The buck regulator circuit of Figure 15 shows an output voltage adjustment range ratio of 2 to 1. The adjustment range is from the typical 6.8V error-reference level to 2 times the error-reference level. If diode D1 is removed and Q1 used with zener Z1 to supply the run B+ for regulated $+V_{CC}$, higher levels of output can be set by reducing the divider ratio, R10 (R9 + R10). With a ratio of 3 to 1, the typical output voltage will be 3 times 6.8V or 20.4V. Of course, under this condition, the V_{UNREG} input voltage must be higher than 20.4V by the amount of the saturated voltage drop in the power FET. If the error input to pin 1 is directly connected to the V_{REG} output, the typical output voltage is 6.8V. V_{REG} output voltage levels less than 6.8V cause two concerns. First, the return resistor divider that sets the output voltage level must be referenced to a positive voltage greater than 6.8V. Although a concern, this condition is feasible. The second concern, that of using the 11V zener supply, is more serious. When the Z1 reference is used, a power-down condition may allow the V_{REG} output voltage to increase when zener voltage collapses. When that happens, pin 1 voltage will decrease and the error voltage will increase the pulse output drive, increasing V_{REG}. A proper choice of components can avoid the turn off output voltage peaking problem when the raw B+ collapses, and even extend the low voltage regulation range.

The circuit of Figure 16 shows the use of the internal zener diode at pin 13 as a reference for the return divider from the output V_{REG} voltage source. An optional adjustment method using the start-up zener, Z_1, is also shown. For the circuit of Figure 16, the range of this adjustment is 2V to 13V.

Using the CA1523 as a VCO Pulse Generator and Driver

The uses of the CA1523 VIPUR discussed above are application specific to a switch-mode controller for power supplies. Figure 17 shows the CA1523 as a general-purpose V_{CO} pulse generator and driver circuit with a minimum of external components. The V_{CO} control input is at the base of the external transistor Q1, which provides a linear current drive to the current sense, pin 2. For a given timing capacitance at pin 14, a 50% duty cycle pulse frequency at pin 6 is controlled by the pin 2 current. The frequency is linear, with the V_{CO} input to Q1. The pin 1 error voltage is biased low, but may be gated to provide synchronous burst control of the V_{CO} output. Some of the typical characteristics and features of this circuit are listed in Table 1. The drive capability of the pulse output from pin 6 has been noted to be as much as +50mA continuous for an 1800pF load. The internal zener bias and bandgap reference sources keep the frequency output very stable over a power-supply range of 10V to 15V.

TABLE 1. TYPICAL CHARACTERISTICS AND FEATURES OF VCO PULSE GENERATOR AND DRIVER CIRCUIT

CHARACTERISTIC	VALUE
V_{CC}	12V
V_{CC} Range	10V to 15V
I_{CC}	23mA
V_{CO} Input Range	1V to 4V
V_{CO} Sensitivity	53.3kHz/V
$f_{(MAX)}$	200kHz (for C14 = 240pF)
$f_{(MAX)}$	500kHz (C14 = Stray Capacitance)
V_O Output	11V
t_R	300ns (0V to 8V)
t_F	100ns (11V to 2V)

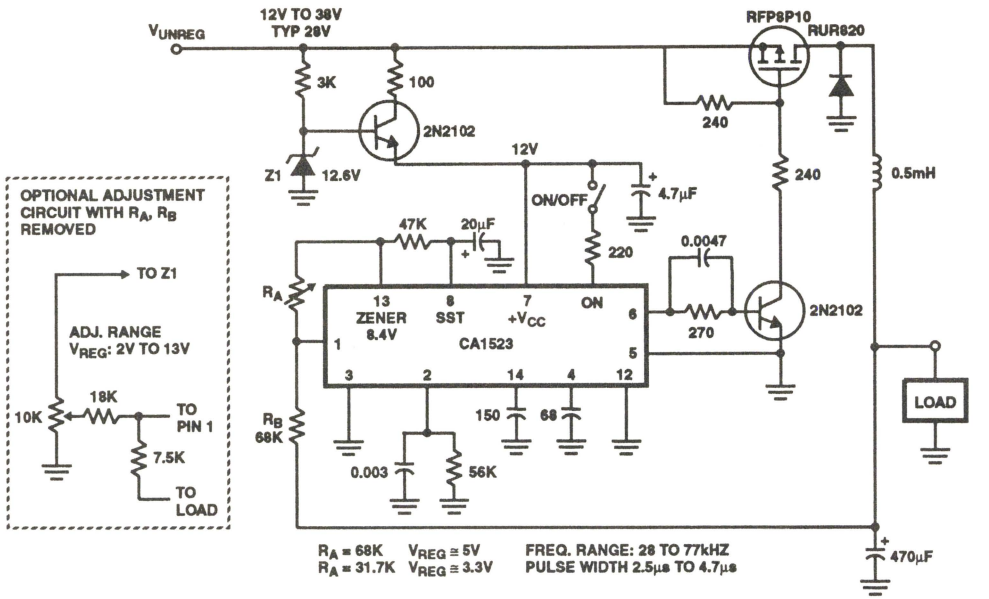


FIGURE 16. LOW VOLTAGE SUPPLY VARIATION IN THE BUCK CONVERTER CIRCUIT

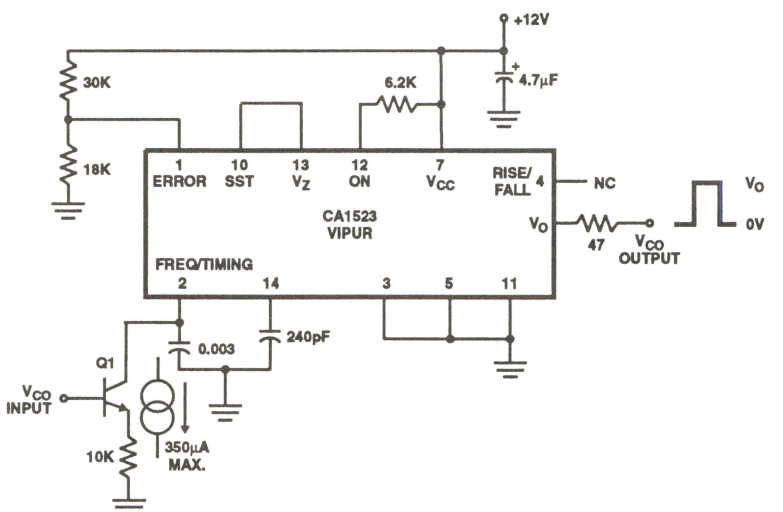


FIGURE 17. V_{CO} PULSE GENERATOR AND DRIVER CIRCUIT

Harris Semiconductor

APPNOTE

No. AN8829.2 April 1994

Harris Intelligent Power Products

SP600 AND SP601 AN HVIC MOSFET/IGT DRIVER FOR HALF-BRIDGE TOPOLOGIES

Author: Dean F. Henderson

The interfacing of low-level logic to power half-bridge configurations can be accomplished by an $500V_{DC}$ intelligent IC, the SP600 series driver, which is designed for up to $230V_{AC}$ line rectified operation. The primary function of the high voltage integrated circuit (HVIC) is to drive n-channel MOS gated power devices in totem pole configuration. Compatible with current-sensing MOSFETs/IGTs, this HVIC provides overcurrent shutdown, simultaneous conduction protection, and undervoltage lockout. Logic level inputs provide noise immune control of power element switching.

The SP600 has demonstrated high frequency (130kHz) operation as well as the ability to withstand high dv/dt. Its semicustom design flexibility makes it easily adaptable to a wide range of single and multiple phase applications. Other salient features of the device are described below.

Technology Overview

BiMOS structures are implemented in a junction-isolation process, known as "lateral charge control",[1] that supports high voltage laterally. By the use of this thin epi process, low voltage analog and digital circuitry can be combined monolithically with high voltage transistors. Low voltage circuits can be constructed to float up to $500V_{DC}$ with respect to the substrate. Additionally, $500V_{DC}$ NMOS and n-p-n transistors can also be fabricated.[2] Since this process conforms to mainstream low voltage IC manufacturing, it is cost effective.

Totem Pole Drivers

Historically, designers have been faced with awkward decisions regarding the upper-rail drive of bridge topologies. P-channel MOSFETs, while easy to drive, are more than twice as expensive as equivalent n-channel devices having the same rds(on). Economic barriers and product availability generally prohibit design beyond $200V_{DC}$. On the other hand, the driving of upper rail n-channel MOS gated devices requires a floating gate supply that must be 5 to $20V_{DC}$ greater than the upper rail link. While several discrete approaches for implementing this floating supply are known, the designer is burdened with additional components and potential dv/dt problems associated with voltage translation.

The SP600 series driver provides the economical solution as an intelligent totem pole n-channel driver. With the addition of as few as five, user defined, external, passive components (three if current detection isn't employed) a functional half-bridge driver can be built that has the following features:

- Creation and management of a $15V_{DC}$ upper-rail power supply
- Ability to interface and drive standard and current sensing n-channel MOSFETs/IGTs
- Shoot-through protection
- Overcurrent protection
- Undervoltage lockout
- CMOS logic-level input compatibility
- Semicustom flexibility through metal-mask changes
- Standard 22-pin DIP packaging

Theory of Operation

Figure 1 is the basic block diagram of the SP600. CMOS logic compatible input signals are filtered to ensure reliable operation when the device is subjected to noisy industrial environments. Digital commands at TOP and BOTTOM inputs cause the upper or lower drivers, respectively, to turn on or off. The $I_{TRIP\ SELECT}$ input provides a higher than nominal current limit on a pulse-by-pulse basis. The input signals are decoded to drive the appropriate output device. High voltage translation is provided by current mirror pulses used to communicate upward to the top gate driver to initiate turn on or off (I_{ON}/I_{OFF} pulses). These momentary pulses are captured by local latches to maintain the desired state. This feature minimizes power dissipation in the level shifter and provides added noise immunity as well. The bottom gate driver circuitry is similar. The floating bootstrap power supply is provided by low voltage capacitor C_F and high voltage diode D_F. Each time the V_{OUT} node goes low, C_F charges to roughly a diode drop less than V_{DD} ($15V_{DC}$). This situation prevails each time the lower output device is activated or, in the case of an inductive load, whenever the upper device is switched off and freewheeling load current forces the output node to a diode drop below ground. In either case, D_F is forward biased, allowing C_F to charge through the current limiting resistor R_{BS} to approximately V_{DD}. Noise dropping resistor R_{ND}, along with capacitor C_{DD}, provides localized filtering of the bias supply and bypasses bias supply series inductance facilitating fast and complete bootstrap refresh.

Each output device is protected on a pulse-by-pulse basis from overcurrent (OC) by sense resistor R_S, which is connected to 100mV comparators. This arrangement permits the designer to take advantage of nearly lossless current-sensing MOSFETs or IGTs.

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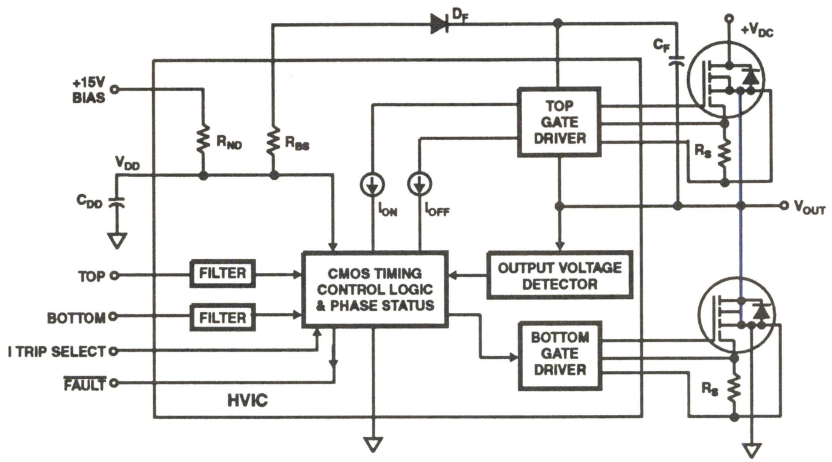


FIGURE 1. BLOCK DIAGRAM OF THE HVIC

Upon detection of any OC, the output is immediately disabled. In the case of the lower switch, a FAULT is directly detected and reported. Upper rail OC FAULTs are indirectly reported via the output voltage monitor when it detects an output state not in agreement with the commanded TOP input signal. With local OC detection and shutdown of the upper device, an inductive load will force V_{OUT} low due to freewheeling. This "out of status" detector recognizes a fault when V_{OUT} is typically less than $5.5V_{DC}$.

Logic and Timing

Figure 2 is a detailed functional circuit of the SP600. The filtered inputs, TOP, BOTTOM, and $I_{TRIP\ SELECT}$, ignore pulse widths less than typically 400ns to prevent false triggering. During the generation of I_{ON} and I_{OFF} pulses, the control logic ignores further changes in the input signal. For each I_{ON} pulse, an I_{OFF} pulse is simultaneously sent to the opposite driver, thus eliminating the possibility of spurious shoot

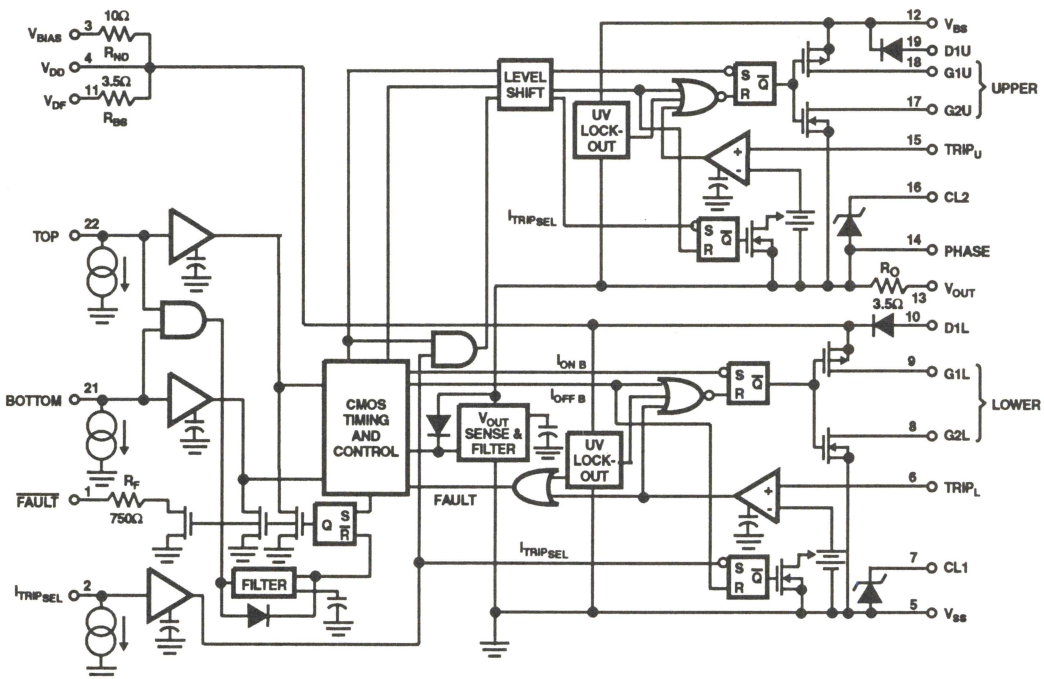


FIGURE 2. FUNCTIONAL DIAGRAM OF THE HVIC

through caused by high voltage, high-speed switching. These features aid in providing predictable operation of the floating upper rail driver section, which is capable of slewing over 10,000 volts per µs.

PHASE serves as a common reference for the floating bootstrap supply (V_{BS}) and all upper rail logic. V_{OUT}, for all practical purposes, is at the same potential as PHASE, being separated from it electrically by only a few Ω (R_O). This additional series output resistance helps to limit the peak current being drawn from the HVIC when an external lower flyback diode, undergoing forward recovery, forces V_{OUT} negative.

An automatic refresh algorithm is generated by the CMOS timing and control block to ensure that the bootstrap capacitor remains charged. As mentioned above, C_F is refreshed each time the V_{OUT} node swings to common. At power up, with zero voltage on C_F, there are two ways to refresh the bootstrap capacitor. The first is by initially commanding the bottom device to turn on, forcing V_{OUT} low. The second occurs when an automatic refresh is invoked if the TOP has been commanded on for longer than 200µs to 500µs. The logic momentarily ignores the inputs, and turns on the lower output (subsequent to an I_{OFF} TOP) for typically 2.0µs, charges C_F and finally restores control to the input commands. Automatic refresh is overridden at switching rates greater than 5kHz, the minimum refresh timer period.

A dual level current limit provision allows for a 30% higher current trip point (above nominal) on a pulse-by-pulse basis. A logic level 1 applied to $I_{TRIP\ SELECT}$ provides a boosted current limit suited for applications like uninterruptable power supplies (UPS), which may have occasional shifted peak power requirements. This feature may allow for a more optimally selected output device. Benefits of current boost have been demonstrated in an off-line PWM motor controller where $I_{TRIP\ SELECT}$ is momentarily applied to overcome the inertia associated with rotor start-up.[3]

Both outputs are disabled and a FAULT reported as a result of:

- Overcurrent
- V_{DD} (lower bias) and V_{BS} (upper bias) undervoltage
- V_{OUT}/PHASE out-of-status
- Simultaneously commanded TOP and BOTTOM input (outputs disabled, no FAULT reported)

The fault can be cleared by a logic 0 at both TOP and BOTTOM inputs for the required fault reset delay time of 3.4µs to 6.6µs.

Power Driver Section

The upper and lower driver output sections are nearly identical, Figure 3.[4] Separate sink and source transistors are separately bonded out for application specific designs requiring additional series gate impedance(s) for slower charge and discharge rates. This circuit property becomes particularly important with IGTs, where a minimum turn-off impedance of 100Ω may be required to ensure full SOA. Regardless of the switching element used, companion flyback diode characteristics may necessitate slower turn-on to reduce peak reverse recovery current by increasing the gate impedance by means of R_{CHARGE}.

A nominal 100mV_{DC} comparator provides overcurrent (OC) protection when used with either current sensing IGTs or MOSFETS. OC can also be implemented by using low impedance shunts with noncurrent sensing power output devices, Figure 4.

Clamp CL1 in Figure 4 provides overvoltage protection for current sensing structures during switching intervals, and protects the comparator from any voltage transients due to external lead inductances. To avoid nuisance OC trips caused by reverse recovery current during turn-on transitions, the comparator's output is blanked for approximately 3µs.

System Performance

The half-bridge test circuit in Figure 5 was built to demonstrate the SP600 as a high frequency driver of MOSFETs. The load is referenced to one-half the battery voltage, allowing bidirectional load current. This circuit characteristic emulates power configurations of half bridges with split supply or full bridges implemented with multiple HVICs.

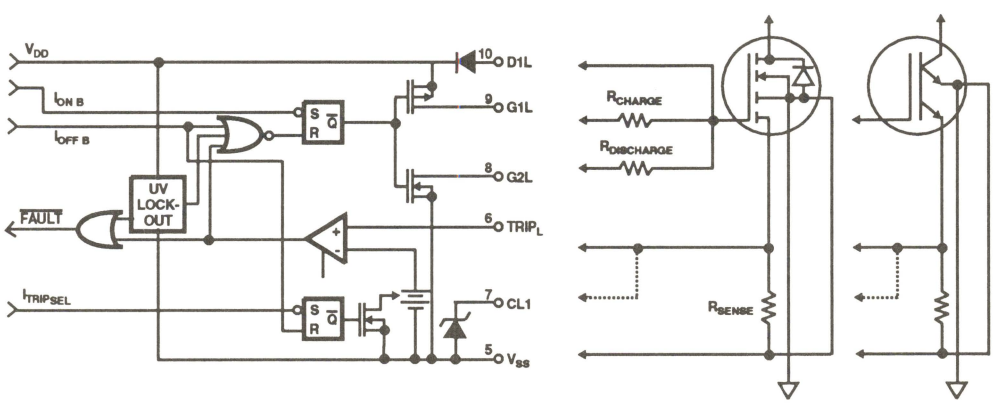


FIGURE 3. POWER-OUTPUT SECTION INTERFACING WITH CURRENT SENSING MOSFET OF IGT.

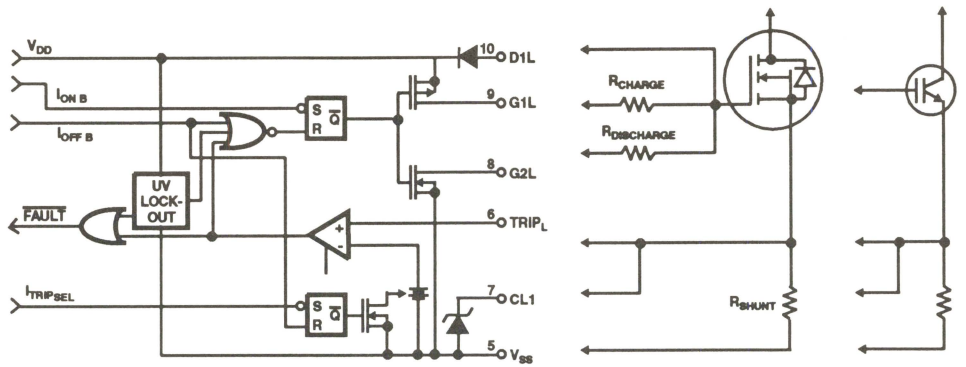


FIGURE 4. POWER OUTPUT SECTION INTERFACING WITH NONCURRENT SENSING MOSFET OR IGT.

For ultimate switching speed, no additional series gate impedances were used. Peak MOSFET gate charge and discharge current waveforms of 400 and 510mA$_{DC}$, respectively, were observed, Figure 6.

High frequency, high voltage operation requires that upper rail drive and level translator circuitry be immune to high dv/dt, as this section floats with respect to V_{OUT}/PHASE. Interjunction capacitance can dynamically inject displacement currents, raising havoc in circuit performance or even causing catastrophic failures, including the breakdown of voltage isolation tubs or latch-up in adjacent four layer structures.

At rail voltages of 200V$_{DC}$ to 400V$_{DC}$, rise and fall transitions of V_{OUT}/PHASE were measured in the 20ns to 35ns region.

The HVIC operated flawlessly while being subjected to output swings beyond 11,000V per µs. Figure 7 demonstrates the HVIC's ability to sustain such dv/dt when driving IRF820 devices.

IRF 842s were driven at 130kHz in this same half-bridge circuit, Figure 8. The ultimate switching speed of the SP600 series HVIC will depend on gate capacitance and the duty cycle limits dictated by the minimum I_{ON} and I_{OFF} times. A minimum I_{ON} time (1.6µs to 3.1µs) ensures time for refresh, while a minimum I_{OFF} time (1.3µs to 3.4µs) prevents simultaneous conduction by allowing for gate discharge prior to an opposite I_{ON} pulse. The same promising technology has been shown to operate a half-bridge resonant converter at frequencies up to 600kHz.[6]

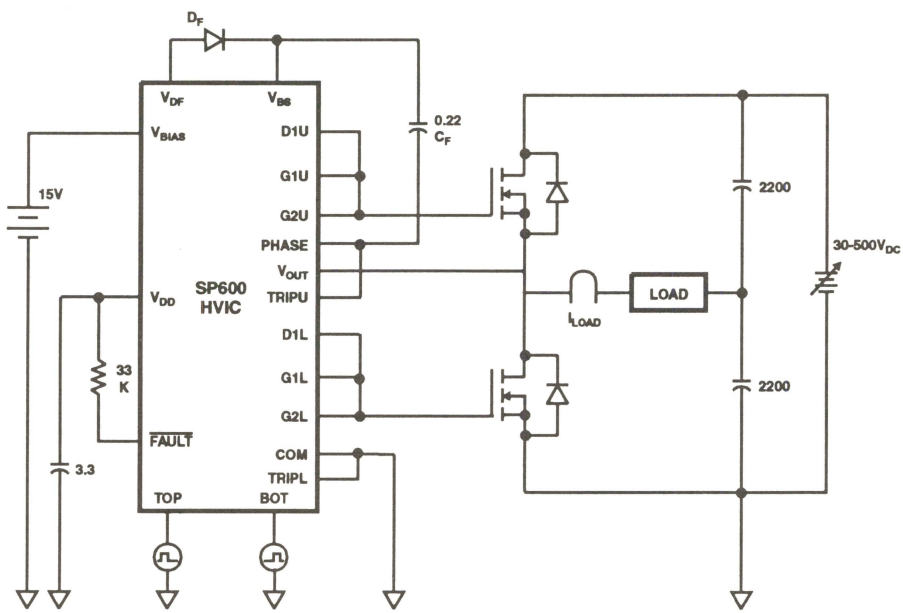
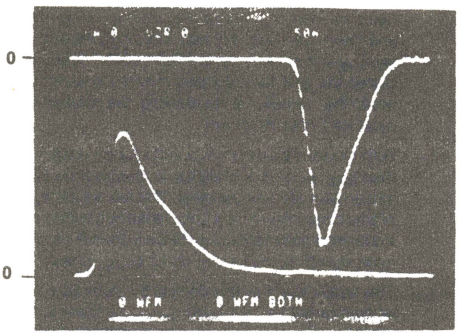
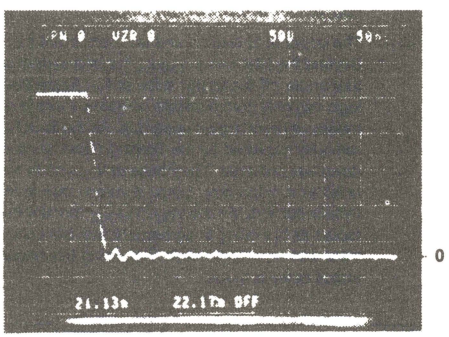


FIGURE 5. HALF-BRIDGE TEST CIRCUIT



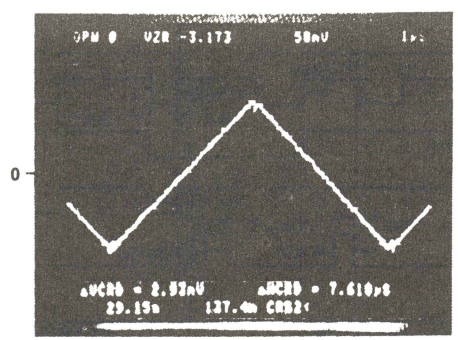
Top: Turn Off Vertical: 100mA/div
Bottom: Turn On Horizontal: 20ns/div

FIGURE 6. GATE-CURRENT WAVEFORMS DRIVING AN IRF820



Vertical: 50V/div
Horizontal: 50ns/div

FIGURE 7. V_{OUT} TRANSITION AT TURN ON OF LOWER IRF820



Vertical: 50V/div
Horizontal: 50ns/div

FIGURE 8. OUTPUT LOAD CURRENT AT 130kHz USING IRF842s

Semicustom Capability

The SP600 family can be customized by inexpensive, final metal mask alterations. Application specific designs are possible for variations in the following parameters:

- Minimum I_{ON}/I_{OFF} pulses
- OC trip response time
- Input signal conditioning filters
- OC trip level
- Inclusion of $R_{CHARGE/DISCHARGE}$
- $I_{TRIP\ SELECT}$ boost level
- FAULT reset timer

Other system related options include:

- Input protocol
- Automatic FAULT reset
- Ability to disable the automatic refresh algorithm

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3. J. G. Mansmann, et al, "ASIC Like HVIC for Interfacing to Half-Bridge Based Power Circuits," PESC March 88.
4. J. G. Mansmann, et al "A Flexible High Voltage Controller Core for Half "He" N-Channel Bridge Operation," MOTORCON proc, Sept '87, pp 194-205.
5. D. J. MacIntyre, "Motor Control Applications of Second Generation IGT Power Transistors," GE PESD Application Note 200.95.
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Appendix

Timing Waveforms (See page 6)

Although both SP600 and SP601 timing diagrams are shown the SP601 was chosen to provide further explanation.

$t_0 < t < t_1$ At t_0, with the enable high, the outputs are simultaneously commanded to switch from lower to upper which is also known as Bistate operation. After delay t_{OFFD}, the lower is turned off, followed by the uppers turned on. Dead time, $t_{D.T.}$, the difference between the lower off transition to the upper on transition is internally set. Since this timing sets the margin of safety for simultaneous conduction, it's the user's responsibility to ensure that proper external gate impedance is selected to ensure ample time for power transistor charging/discharging.

$t_1 < t < t_2$ The lower is turned on at t_1 and continues for a relatively long period, long enough that at t_2 an automatic refresh will be invoked.

$t_2 < t < t_3$ The HVIC has blinded itself to the logic inputs during this refresh mode. The upper is turned off, with its associated turn off delay, t_{OFFD}. After the fixed dead time, $t_{D.T.}$, the lower is briefly turned on, ton, providing a charge refresh path for the bootstrap capacitor, C_F. Once again the dead time is observed before turning the upper back on again and restoring control to the user inputs. This refresh cycle can be detected as a few µs wide pulse of lower MOSFET/ IGT current.

$t_3 < t < t_5$ The upper remains commanded on for a period of time less than t_{REF}. At t_4, the UP/$\overline{DOWN}$ time is brought low, commanding a lower turn on. Similar to the t_0-t_1 interval, the upper turns off after delay t_{OFFD} and the lower turns on after the dead time, $t_{D.T.}$

$t_5 < t < t_7$ The SP601 is disabled by the ENABLE line low at t_5. Previously conducting lower turns off after its delay, t_{OFFD}. Since the ENABLE line was previously brought low and neither output transistors are conducting, termed as three-state mode. The state of the output phase waveform remains unknown. At t_6, the ENABLE is once again pulled high. The lower turns on after delay, t_{ONDB}.

$t_7 < t < t_9$ At t_7, the SP601 is disabled and the UP/ DOWN line is toggled to the upper position. The lower turns off and the power devices go into a three-state mode. At t_8, upper turn on sequence begins. Since the auto one shot hasn't timed out yet, the turn on delay, t_{ONDB}, is relatively short.

$t_9 < t < t_{11}$ The chip shuts off as the ENABLE line is brought low at t_9, and is enabled again at t_{10} as the UP/DOWN line had remained high. Since the disable period was long and the refresh one shot had timed out, the turn on delay, t_{ONDT}, is slow. Keep in mind that the delay time includes the time for automatic refresh. In an attempt to not further complicate the drawing, the detailed refresh cycle isn't actually shown.

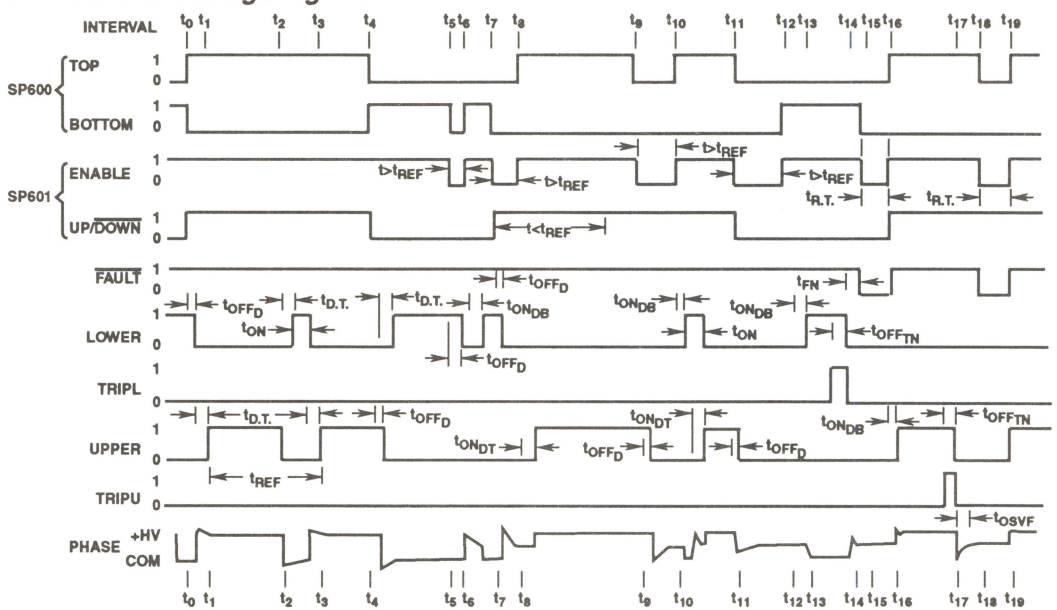
$t_{11} < t < t_{13}$ Both inputs are brought low at t_{11} for a duration longer than t_{REF}. At t_{13} the ENABLE is restored, initiating the turn on sequence for the lower. This follows a long period of time where the one shot had timed out, but in this case the lower is commanded on. Since it doesn't need the refresh algorithm, the turn on delay, t_{ONDB}, is fast.

$t_{11} < t < t_{13}$ This sequence of events depicts the detection of a lower overcurrent trip. Between t_{13}-t_{14}, the lower is on. Beyond the filter delay, t_{OFFTN}, the overcurrent trip shuts off the lower driver. A fraction of a µs later, t_{FN}, the flag report delay, FAULT goes low.

$t_{15} < t < t_{16}$
$t_{18} < t < t_{19}$ By holding both ENABLE and UP/DOWN lines low for the required fault filter reset time, $t_{R.T.}$, the fault is cleared.

$t_{16} < t < t_{17}$ The upper is turned on and an overcurrent trip begins. Beyond the filter delay, t_{OFFTN}, the overcurrent comparator shuts off the upper drive at t_{17}. Since the control logic can only communicate upwards, there is no direct means of reporting an upper trip. As the fault has been remotely captured by the floating upper section, shutdown has occurred. The Phase or V_{OUT} node will quickly fall to a diode drop below common due to inductive flyback current. Via the V_{OUT}/V_{PHASE} monitor this is detected as not being in agreement with the commanded input and reports the fault. Reporting this phase out of status delay is t_{OSVF}.

SP600 Series Timing Diagram



APPNOTE

No. AN9010.4 April 1994

Harris Intelligent Power

HIP2500 HIGH VOLTAGE ($500V_{DC}$) HALF-BRIDGE DRIVER IC

Author: George E. Danz

Introduction

The HIP2500 is an high voltage, high speed half-bridge driver for driving n-channel MOS gated power devices. The blocking voltage of the HIP2500 is 500VDC which provides the capability for application on most rectified 230VAC line. The HIP2500 uses the same proprietary technology which resulted in the first products in the HVIC (high voltage IC) family, the SP600/SP601 Half-Bridge Drivers.

The upper and lower drivers are junction-isolated from each other and controlled by independent input lines referenced to the system common. The HIP2500 offers a reliable, cost-effective means for driving high-side referenced n-channel power switches from ground referenced logic. Level-translation circuitry using optocouplers or, the more reliable, but often too expensive, transformer is not required. Highly integrated logic and drive circuitry minimizes propagation delays and allows higher switching frequencies and lower switching losses than would be attainable using more conventional techniques. Besides cost savings and performance increases, the HIP2500 simplifies and reduces the effort needed to design efficient MOS gated high and low side switch drivers.

The HIP2500 boasts high output drive capability (2A peak), while still employing the PMOS source and NMOS sink drivers which are also employed in the SP600 family. By removing the Overcurrent trip, automatic refresh and shoot-through protection features of the SP600 family, the simpler logic circuitry allows lower transport delays from input to output and operation at PWM frequencies as high as 500KHz. Gate rise and fall times are as low as 20ns into a 1000pF load.

While the burden of shoot-through protection now rests squarely with the user, the simplicity of precise user gate control allows the capability to drive double forward converters, a configuration popularly used in power supply, stepper motor and switched reluctance motor controls. Capacitor C_F, referred to as the "bootstrap capacitor," must always be fully pre-charged before turning on the upper switch. On power up, therefore, the lower switch should be turned on first, providing a charging path for C_F from V_{CC} through the bootstrap diode D_F and back to ground. Figure 1 and Figure 2 both show the bootstrap components.

An inductive load will often supply the current required to charge the bootstrap capacitor each time the upper switch is turned off. It does this through a lower flyback diode as shown in Figure 2, or the internal body diode of a lower MOSFET as shown in Figure 4. In the case of the buck converter, the load provides a path to pre-charge the bootstrap capacitor prior to turning on the high side switch.

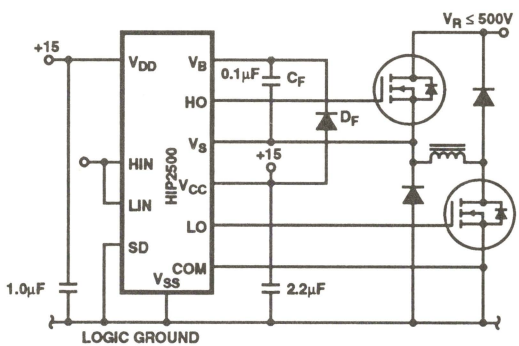


FIGURE 1. DOUBLE FORWARD CONVERTER SCHEMATIC

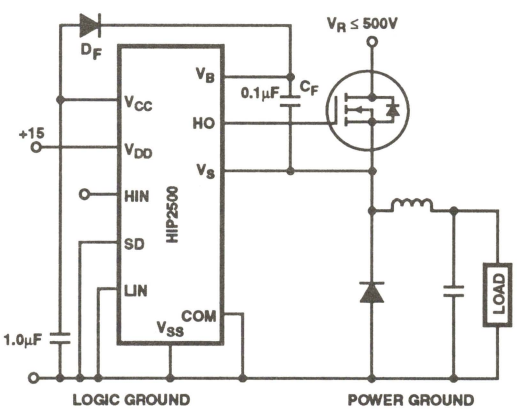


FIGURE 2. HIGH SIDE SWITCH OR "BUCK CONVERTERS"

11 APPLICATION NOTES

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Description of the HIP2500

The block diagram of the HIP2500 is shown in Figure 3. The HIP2500 contains both ground referenced and high voltage bus referenced (floating) gate drive circuits. With the exception of level-translation circuitry communicating between the upper driver circuit and the upper input control logic, the upper and lower driver and control circuits are nearly identical.

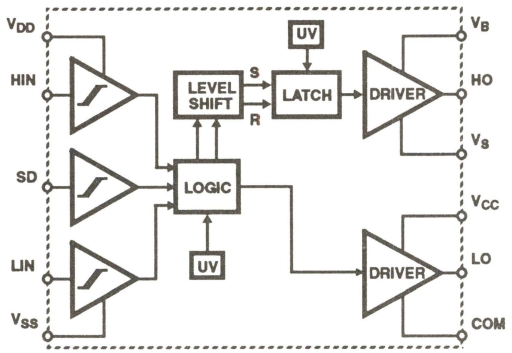


FIGURE 3. HIP2500 FUNCTIONAL BLOCK DIAGRAM

Input Logic

The input logic of the HIP2500 incorporates pull-down circuits which allow any of these inputs to be left open if they are not used. The pull-down current is approximately 12 micro-amps. As well as electrostatic input protection, the inputs are Schmitt-buffered and a level-translation circuit allows 5 volt logic inputs to communicate with the downstream logic which drives the gates of the power switches connected to the HIP2500. This logic is nominally biased between 12 and 15 volts. An extra benefit of the level-shifter is to provide input circuit noise immunity by continuing to function even though the V_{SS} terminal moves with respect to the COM terminal from about -2.0 volts to +VCC/2 volts. When attempting to lower the V_{SS} terminal more than -2.0 volts below COM, however, the HIP2500 will continue to function, but heavy substrate current flows. Therefore one should not attempt to deliberately shift the V_{SS} and COM terminals from each other.

The three inputs to the HIP2500; HIN, LIN and SD control the floating high side driver, the low side (ground referenced) driver and the "shutdown" functions, respectively, in accordance with the timing diagram in Figure 5. The HO and LO gate drive signals respond within a short (typically 400ns) propagation delay of their respective HIN and LIN signals. In half-bridges where deadtime is required to prevent conduction overlap or "shoot-through", the HIN and LIN input commands must be appropriately spaced by the user. For example in a typical half-bridge configuration such as in Figure 4, where the upper and lower switches are series connected between the high and low sides of the power bus, the user must ensure that one switch is completely off before turning on the other. If this precaution is not followed, conduction overlap will occur in both switches, usually leading to destruction of one or both power switches and possibly the HVIC. Occasionally, a few passive components added to delay switch turn-on without delaying turn-off can effectively control shoot-through (see the diode resistor parallel combination in Figure 4). As power levels and power switch devices become larger, active rather than passive techniques may be a more appropriate means for providing turn-on blanking of one switch while turning off the other.

Two independent latches provide a means to inhibit the HO and LO outputs from going high whenever a Shutdown pulse has occurred. Resetting of the latches is accomplished at the moment that the respective HIN and LIN signals go low, provided that the SD input is also low.

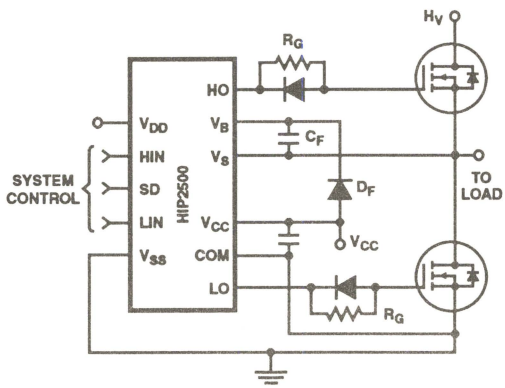


FIGURE 4. SIMPLIFIED SHOOT-THROUGH CONTROL

The timing diagram shown below will help to make operation of the input latch and shutdown logic more clear. The arrows

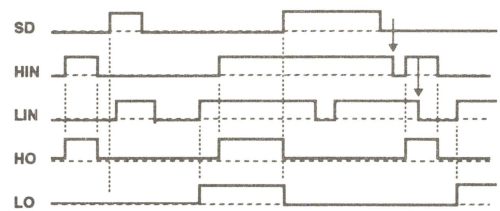


FIGURE 5. INPUT TIMING DIAGRAMS

show that at the instant the HIN and/or LIN inputs go low the shutdown latch is reset. Subsequent high signals on HIN or LIN will then be passed on to the edge logic and level-translation circuits before final processing by the output driver circuits.

Edge Logic

After the HIN and LIN input signals are squared up by the input logic, they are processed further by the Edge Logic. The purpose of the Edge Logic is to create short pulses to be further processed by the upper and lower output driver logic. There are two Edge circuits; one for the floating driver and one for the COM referenced driver.

Each Edge circuit has two inputs and two outputs. One output goes high coincident with a rising-edge signal from the input logic. The other output goes high coincident with a falling-edge signal from the input logic. Both outputs are short pulses which minimize the power dissipation of the Level-translation transistor. Although there is no lower level-translation transistor, the lower Edge circuit nonetheless helps provide the necessary symmetry between upper and lower switch delays. The second input to each Edge circuit comes from the lower Undervoltage (U/V) circuit. In the event of a lower undervoltage condition (i.e.: a low V_{CC}), the outputs of both upper and lower Edge circuits issue turnoff pulses.

Level-Translation

The upper Edge circuit issues turnon and turnoff pulses to the Level-Translation circuit. This circuit mainly consists of two high voltage npn transistors which conduct very narrow current pulses to the upper (floating) gate drive circuit.

Communication with the upper switch drive logic creates a potential for excessive power dissipation. By using only very short level-shift pulses from the V_{SS} referenced logic through the high voltage level-shift circuit to a latch in the upper switch driver, level-shifting power dissipation can be minimized. Two high voltage level-shift transistors are required to control the upper switch, one for turnon pulses and one for turnoff pulses. The level-shift current pulses are robust in order to provide noise discrimination, but are also very short so as to avoid significant power dissipation.

Driver Circuits

The driver circuits for the upper and lower gate drives are identical, except for the settings of the delay-matching circuits. Delay matching makes it easier to equalize the dead-time between upper and lower switch conduction periods. A secondary benefit of delay matching is to provide duty-cycle equalization of the input waveform and the output waveform at the V_S terminal. Delay-matching imbalance becomes more noticeable at high switching frequencies.

The HIP2500 uses p-channel mosfets in the output stage of the drivers for sourcing gate current to the power devices and is unique in its ability to drive the gates of the upper and lower switches to the full applied bias voltage. Similarly N-channel devices have been employed for sinking current from the gates of the power devices. This allows complete utilization of the supply voltage and power device gate voltage will be unaffected by changes in driver threshold voltage variations. The approach employed in the HIP2500 also avoids the additional power dissipated due to the threshold voltage drop associated with source-follower topologies. At high operating frequencies this can be significant.

The sink and source currents of the gate drivers are fully capable of supplying peak currents of at least 2.0A, which means that a power mosfet device with 3000pF gate source capacitance can be fully charged in 25ns. Discharge of the gate source capacitance will be slightly more rapid, since R_{DSon} of the sink driver is about 10% less than the source driver.

The high side driver section is built into an "isolation tub" which is capable of floating $+500V_{DC}$ above substrate potential with respect to power ground (COM pin 2). Pin 6 (V_S) is the common potential for the upper drive circuitry and is the most negative voltage within the floating tub. V_B (pin 5) is the positive rail within the floating tub and is usually 12 to 15 volts above V_S. The gate drive output, HO (pin 7) swings between V_S and V_B according to the state of the HIN input pin.

Under-Voltage Lockout

The HIP2500 is protected internally from insufficient bootstrap supply voltage (in the case of the upper floating driver) and insufficient bias supply voltage (in the case of the lower driver). Also the HIP2500 will not turn on either of the switches should the high voltage supply be brought up before the low voltage bias supply power.

As mentioned previously under Edge Logic, the lower undervoltage lockout blocks drive to both upper and lower power switches. The reason for turning off both switches when only the lower bias supply is below its U/V trip setpoint is that the upper bias supply is refreshed from the lower supply. Therefore the floating supply can never be any higher than the voltage on V_{CC}. The U/V latches are reset upon reestablishment of proper bias supply voltage level and a low transition of the LIN and/or HIN signals.

The upper logic circuit has a separate undervoltage circuit which controls only the gating of the upper (floating) switch. The switch is latched off upon occurrence of an undervoltage condition across the bootstrap capacitor. Latching is reset when the undervoltage condition goes away. A subsequent "on" pulse from the HIN terminal will turn on the upper switch. The HIN terminal must have previously gone low in order for the Edge circuit to issue an on pulse to the upper driver logic. Latching the drivers off in the event of an undervoltage condition eliminates the potential of entering a limit-cycle condition. To avoid U/V trip, the circuit designer must pick a value for bootstrap capacitance which supports the bias current requirements of the floating supply without tripping the under-voltage circuit. Guidance on choosing the bootstrap capacitor can be found under "Design Considerations" later in this note.

Design Considerations

The designer must deal with the following areas to successfully apply the HIP2500:

- Bias Supply Design
- Propagation Delay Issues
- Power Dissipation, Thermal Design

Bias Supply Design

The design of the HVIC bias supply is not particularly difficult. First establish the desired gate voltage for the power switch. For most MOSFETs and IGBTs there is a point at which increasing gate-to-source voltage yields no significant reduction in switch forward drop. Usually this occurs at about 8 to 9 volts. Avoid overcharging the gate of the power switch because the higher the gate voltage is the longer it takes to turn off the device. Also more charge must be transferred, which dissipates more power both in the HIP2500 and in the switch device. Finally, by increasing the time required to turn off the power MOS device, one increases the risk of "shoot-through". For all of the above reasons it is wise not to overcharge the gate of the power device.

Under-Voltage Requirements

The designer must pay attention to how low the Bias Supply voltage can go before causing the forward voltage drop of the power switch to increase dangerously. Generally, this voltage will be about 8 volts or less. The HIP2500 provides undervoltage protection at typically 9 volts, although the minimum trip value can be as low as 7.7 volts.

To reset the undervoltage circuit requires that the supply voltage exceed the trip level by at least 0.25 volts (the hysteresis of the U/V circuit). To again turn on a switch, a new edge signal must be generated by issuing a new high input on the desired input (HIN / LIN).

Lower Bias Supply Design

The lower bias supply design is simple, but must be clean and have low series resistance and inductance between the source and the VCC terminals. Also the common from the supply source to the COM terminal on the IC should be short and of low impedance. Usually it is sufficient to put a low ESR capacitor of a few microfarads directly from V_{CC} to COM. In any event, this capacitor must have sufficient charge to dump into the bootstrap capacitor whenever the VS (phase) terminal moves toward COM. This happens when the lower switch is on and usually whenever the upper switch has just been turned off. This will be explained in more detail under Bootstrap Circuit Design.

Another point to remember is that the voltage remaining on the bypass capacitor after dumping to the bootstrap capacitor should not cause the voltage on the bypass capacitor to drop below the Maximum undervoltage trip level. This level can be as high as 9.99 volts. Of course this assumes no current will come from the external bias supply during the refresh time. In practice, your supply will probably not be this soft and a good rule of thumb is to choose a bypass capacitor about 10 times larger than the bootstrap capacitance.

Bootstrap Circuit Design

The upper bias is maintained by the Bootstrap Capacitor between refresh cycles. A refresh cycle is defined as the time which elapses between conduction periods of the lower power switch and/or its body diode or flyback diode. Sometimes compromises on the size of the bootstrap capacitor must be made. For example, the capacitor should not be so large as to require an excessively long refresh period. Nor should it be so small that the voltage droops below the undervoltage trip point during the upper switch conduction period.

The largest factor in the amount of droop for frequencies above several KHz is the magnitude of charge required to charge the gate input capacitance of the driven switch to its final voltage. The charge lost by the bootstrap capacitor will be slightly larger than the charge acquired by the gate capacitance of the power switch as shown in (EQ. 1):

$$Q_G \approx (V_{BS1} - V_{BS2})\, C_{BS} \qquad \text{(EQ. 1)}$$

where:

V_{BS1} = C_{BS} voltage immediately after refresh
V_{BS2} = C_{BS} voltage immediately before refresh
C_{BS} = Bootstrap capacitance
Q_G = Turn-on Gate charge transferred

Figure 6 will help to understand the operation of the bootstrap circuit. The figure shows the refresh current paths which will charge the bootstrap capacitor to prepare it for driving the upper power switch. As previously stated, whenever the lower switch, its body diode or an external flyback diode conducts, the phase node (V_S) to which the load is connected, goes low toward the COM potential. The voltage at V_{CC} forces current through the bootstrap diode, the bootstrap capacitor and the lower switch/diode combination as shown by the arrows in Figure 6.

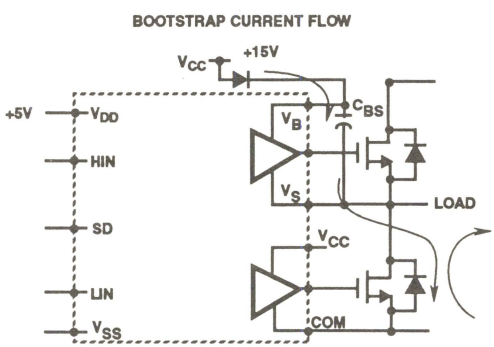


FIGURE 6. HVIC BOOTSTRAP CHARGING PATH

To charge the bootstrap capacitor quickly, without ringing or excessive overshoot, maintain a short, tight bootstrap refresh loop. This usually requires a low ESR decoupling capacitor located adjacent to HIP2500 from V_{CC} to COM and close positioning of the power switches to the HIP2500. The bootstrap capacitor and diode should also be located adjacent to the HIP2500 to aid in keeping this loop as short as possible, thereby minimizing the impedance of this loop.

To insure that the bootstrap capacitor voltage is maintained, it is usually necessary to turn on the lower switch each and every cycle of the PWM waveform. The duration of the refresh period should be long enough to guarantee that refreshing will be complete.

Relying on the lower freewheeling or body diode to provide refreshing without physically turning on the lower switch may fail to properly refresh the bootstrap capacitor under certain circumstances. This can happen when the load current is either zero or in a direction as to flow into the upper freewheel diode or body diode into the high voltage bus. Unless the lower power switch is turned on each cycle for the short refresh period, the bootstrap capacitor may not get refreshed. The conditions which can lead to this situation often occur in motor controls where the motor is coasting in one direction or the other at extremely light loads. Also controllers with a tendency to "over-modulate" can cause a refresh failure.

Users, anxious to get their circuit up and running quickly, will find that a ceramic bootstrap capacitor of approximately 0.1µF to 0.15µF will be sufficient to drive most small to medium size MOSFETs. The leadless surface-mount capacitors minimize series inductance and enhance rapid refreshing of this capacitor.

The bootstrap diode should be a small signal high voltage type capable of blocking full DC bus voltage plus the Vcc voltage. The recovery charge of the diode should be small so that when it recovers it will not appreciably discharge the bootstrap capacitor. Leakage current is usually not a concern, since the recovered charge of the diode will be much more significant than the leakage current over the PWM cycle. A 1000 volt signal diode, such as industry standard 1N5622, is preferable to a lower voltage diode, since its junction capacitance and recovered charge will be smaller. Also a higher voltage diode will have a low reverse leakage current when operated at half of its rated blocking voltage. Standard small signal diodes such as the 1N4000 series should be avoided. No rule of thumb will work in all situations, so it is usually better to take a more detailed look at all the factors which affect the bootstrap capacitor size.

The required value of capacitance depends on the Vcc voltage, the switching frequency, the HIP2500 high side supply current requirement, and the amount of equivalent gate capacitance or gate charge required to fully charge the gate. The gate charge requirement is generally included on most MOSFET data sheets. Figure 7 shows a curve for a Harris IRF450 MOSFET. By designing the bootstrap circuit to supply the total required gate charge shown on the MOSFET data sheet, the designer has included the effects of the Miller capacitance.

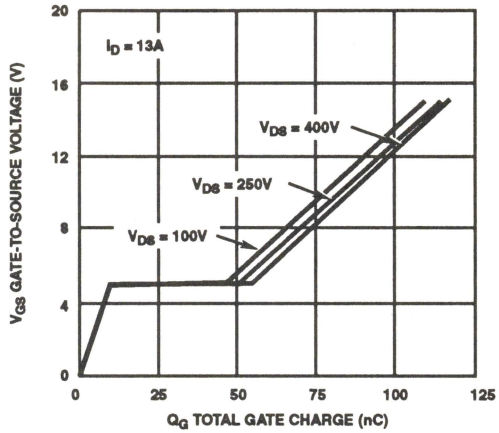


FIGURE 7. GATE CHARGE vs VOLTAGE

As previously mentioned, the layout of the bootstrap circuit should be compact so as to minimize the series inductance of the bootstrap circuit. Excessive inductance will interfere with rapidly charging the bootstrap capacitor during the time provided by the minimum off-time of the upper switch. The time allotted for turning off the upper switch is under full control of the circuit designer. However, maximum switching frequency and duty cycle requirements often forces the designer to live with "off-times" of less than 1 microsecond. As the allotted refresh time is forced lower and lower, the need for a short refresh loop becomes crucial.

A Real Example

A more exact sizing of the bootstrap capacitor than indicated by (EQ. 1) takes into account the upper bias supply current to the HIP2500 and leakage and recovery effects of the bootstrap diode. Obviously PWM frequency will affect the size requirement of the bootstrap capacitor too, so it would be valuable to include PWM frequency as well. If we define the following terms:

I_{DR} = Bootstrap diode reverse leakage current
I_{QBS} = Upper supply quiescent current
Q_{rr} = Bootstrap diode reverse recovered charge
Q_G = Turn-on Gate charge transferred
f_{PWM} = PWM operating frequency
V_{BS1} = C_{BS} voltage immediately after refresh
V_{BS2} = C_{BS} voltage immediately before refresh
C_{BS} = Bootstrap capacitance

then it will be possible to calculate a value for the bootstrap capacitor as shown in(EQ. 2):

$$C_{BS} = \frac{Q_G + Q_{rr} + \frac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \qquad \text{(EQ. 2)}$$

As an example, suppose we wish to drive an IRF450 to 15 volts allowing a droop of 0.5 volts over the PWM cycle (i.e.: V_{BS1}-V_{BS2}) with a 16 nano-coulomb recovery charge and a leakage current of 2 micro-amps for the bootstrap diode with a

maximum bias current, I_{QBS}, of 400 micro-amps. The gate charge, Q_G, of 120 nano-coulombs required to drive the IRF450 was read from the data sheet (see Figure 7). The desired PWM switching frequency will be 20KHz. Using (EQ. 2), one would need a bootstrap capacitance of at least 0.31 microfarads. Since 0.33 microfarads is the next larger standard capacitance available, a ceramic capacitor of this value will be chosen.

The length of the refresh time required to charge the bootstrap capacitor still needs to be evaluated. The refresh loop is comprised of the bootstrap capacitor, the bootstrap diode, stray circuit board resistance (the designer has laid out his circuit to minimize this and stray inductance) and the R_{DSON} of the power switch. The R_{DSON} of the IRF450 is approximately 0.3 ohms at 10 amps. To the above must be added the r_D of the bootstrap diode, which is about 1.1 ohms max. at 1.0 amp. Assuming another 0.1 ohm series resistance for the capacitor and circuit board traces, then a total resistance of about 1.5 ohms is in the bootstrap loop. The charge time constant of the bootstrap capacitor is the product of the loop resistance of 1.5 ohms and the bootstrap capacitance of 0.33 microfarads. This yields 0.5 seconds charging time constant. If 2 time constants are reserved for charging, then the bootstrap capacitor will only charge to about 86% of the V_{CC} supply. In 3 time constants it will charge to 95% of the V_{CC} supply. Keep in mind that the U/V circuit maximum trip level is 9.99 volts. This fact will impact the choice of capacitor and the allotted refresh time. If we assume 3 time constants are sufficient, then to drive the IRF450 to 15 volts would require a V_{CC} voltage of 15/95%, or 15.8 volts.

Propagation Delay Issues

The HIP2500 is designed to enhance rejection of noise from external circuits. Several filters and signal integrators are used to accomplish the noise rejection resulting in input to output propagation delays on the order of 400 nanoseconds. Much of the propagation delay associated with the upper switch is a result of the level-shift circuit. To better match the upper and lower propagation delays, additional delays were inserted in the lower circuit. Filter and matching circuits were designed to provide tracking of upper and lower propagation delays over temperature and bias voltage changes. In practice very good tracking is achievable, with the "on-delays" increasing approximately 150 nanoseconds over temperature and the "off-delays" increasing about 100 nanoseconds over temperature. Because the absolute propagation delays of the upper and lower circuits were not exactly matched, it is necessary to call attention to them so that the circuit designer can compensate for them.

The variation in propagation delays manifests itself in varying dead-times. Dead-time is defined as the time between the fall of one of the gate voltage waveforms and the rise of the other gate voltage waveform. The midpoints in the gate voltage waveforms are used to time the measurement. A 1000 picofarad load is used to simulate the "typical" power device gate-source load. It is possible, when turning off the upper and turning on the lower switch, to experience a slightly negative dead-time of less than 50 nanoseconds. The minimum dead-time experienced going the other way (turning off the lower and turning on the upper switch) is 95 nanoseconds. The best way to guarantee that proper dead-time always exists is to insure that the signals driving the LIN and HIN inputs of the HIP2500 always include dead-time. This will prevent shoot-through conduction and possible power device destruction. Dead-time can be enhanced by using the technique shown in Figure 4. With proper choice of series gate resistance, it may be possible to completely mask the effects of dead-time mismatch.

Power Dissipation and Thermal Design

The power dissipated in the HIP2500 can be lumped into static and dynamic losses. The static losses are limited to bias current losses for the upper and lower sections of the IC. The lower bias current, I_{QCC}, is typically 1.5 mA at +25°C. The upper bias current, I_{QBS}, is typically 300µA. At 15 volts bias, the total power dissipation is less than 30 milli-watts. Since I_{QDD} is typically only 100 pico-amps, the losses associated with this bias current is insignificant.

The switching losses are those losses associated with turning on and off the upper and lower power devices. These are the significant losses within the HIP2500. The switching losses can be further broken down into the following components:

- Low Voltage Gate Drive Charge Transfer
- High Voltage Level-Shifter
- High Voltage Tub-Capacitance Charge Transfer

The low voltage gate drive charge transfer power loss is the most significant of the 3 loss components above. (EQ. 3) describes the power loss attributable to the upper and lower switch gate charge transfer as a function of bias supply, V_{CC}, switching frequency, f_{PWM}, gate charge, Q_G, and the HIP2500 internal CMOS charge transfer losses, $Q_{internal}$, of the driver stages. Unless the gate charge of the power device is very small, $Q_{internal}$ is not very significant.

$$P_{SWLO} = 2f_{PWM}\left(Q_G + Q_{INTERNAL}\right)V_{CC} \quad \text{(EQ. 3)}$$

The high voltage level-shifter power dissipation, EQ. 4, is much more difficult to analyze. The reason that this equation is hard to solve is that the level-shift current pulses, i_{on} and i_{off}, and the phase voltage, v_{shift}, are all functions of time and the phase voltage moves in response to power switch turnon and turnoff, which is also dependent on the power MOSFET or IGBT used. The i_{on} pulse, for example, may come and go before any movement in the phase voltage is evident and therefore dissipate very little energy. The phase voltage usually will be a maximum when the i_{off} pulse comes, so the off pulse may dissipate quite a bit of energy.

$$P_{SHIFT} = \frac{1}{T}\int_0^T \left(i_{ON} + i_{OFF}\right)v_{SHIFT}\,dt \quad \text{(EQ. 4)}$$

Finally, the tub capacitance power dissipation can be calculated from EQ. 5. The "tub" is the p-n junction which isolates all of the circuitry associated with the high side driver from all

of the low side circuits. The calculation is a charge transfer energy calculation very similar to that used for the gate charge transfer, except that the charge is much smaller and the voltage, v_{shift}, much larger. This capacitance unfortunately varies with voltage and it is difficult to measure. The tub capacitance charge transfer losses are shared between resistances both internal and external to the HIP2500. A conservative approach, however, assumes all of the losses are dissipated within the HIP2500.

$$P_{TUB} = C_{TUB} V^2_{SHIFT} f_{PWM} \quad \text{(EQ. 5)}$$

Power Dissipation The Easy Way

Fortunately there is a much easier method available for measuring power dissipation and none of the above equations ever need to be evaluated. Very simple lab equipment can be used to obtain the measurements and simple calculations can be used to obtain accurate results.

The simple method for evaluating power dissipation breaks down the total power dissipation problem into high voltage power dissipation and low voltage power dissipation.

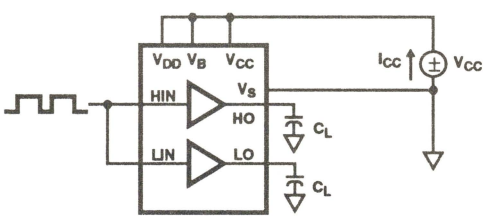


FIGURE 8. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

Low Voltage Power Dissipation

The low voltage power dissipation includes low voltage leakage and switching losses associated with gating both of the power switches. It also includes the CMOS switching losses associated with both driver stages. As shown in Figure 8, the upper and lower bias supplies are tied together and supplied by bias voltage V_{CC}, while capacitors C_L are tied to both of the HIP2500 outputs. Both inputs are then pulsed at the frequency of interest and the average current, I_{CC} is measured. The total low voltage power dissipation is then simply the product of I_{CC} and V_{CC} as shown in EQ. 6 below:

$$P_{LV} = V_{CC} I_{CC} \quad \text{(EQ. 6)}$$

Plotting the results of EQ. 6 as a function of switching frequency and the load capacitance of each of the power switches yields a family of curves for the low voltage power dissipation of the HIP2500 as shown in Figure 9.

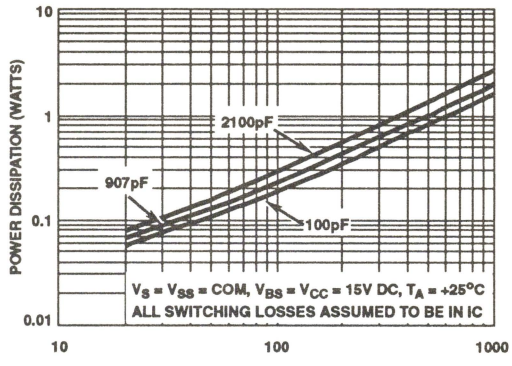


FIGURE 9. LOW VOLTAGE POWER DISSIPATION vs FREQUENCY

If the quiescent bias current and CMOS switching losses are subtracted from the above power calculation, what is left is the power required to drive the gate-source capacitance of the power switches. The power required from V_{CC} to drive the gates can also be calculated by EQ. 7, where C_G is the combined equivalent gate capacitance of both power switches. Half of this power is dissipated in the combined source resistance of the driver and any external resistance in the source circuit and the other half of the power is dissipated in the sinking circuit, including any external resistance in the sinking path.

$$P_G = V^2_{CC} C_G f_{PWM} \quad \text{(EQ. 7)}$$

High Voltage Power Dissipation

The high voltage power dissipation component includes the losses associated with the level-shifter and the tub charge transfer power losses. This component is not affected by the size of the power device being switched. Figure 9 shows the test circuit which is used to measure the high voltage level-shifter and high voltage leakage power losses.

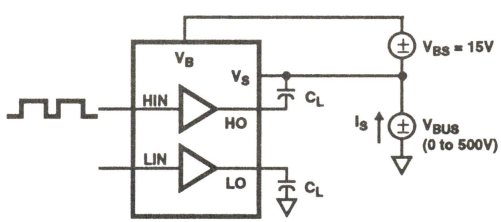


FIGURE 10. HIGH VOLTAGE POWER DISSIPATION TEST CIRCUIT

By measuring I_S and V_{BUS} and calculating the product of these measurements, one can obtain the value for total high voltage power loss for the HIP2500. The value derived will include both reverse leakage power due to the isolation tub and two level-shift events. Both the turnon level-shift and the turnoff level-shift events are included. The high voltage power dissipation will increase directly with both switching frequency and bus voltage level as shown in Figure 11.

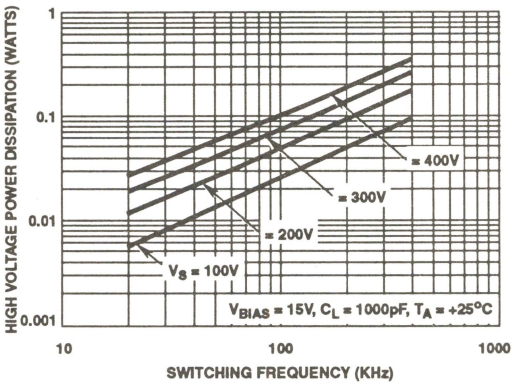


FIGURE 11. HIGH VOLTAGE POWER DISSIPATION vs SWITCHING FREQUENCY

Layout Issues

While a lot of effort was spent in designing the HIP2500 to be immune to noise, poor layout can cause problems.

Particular attention should be paid to keeping the distance between the HIP2500 and the power switches as short as possible. If your design is experiencing any of these effects, it may be helpful to first look at the possible causes in the table: Layout Problems and Effects.

Layout Problems and Effects

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance can cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead (V_S) causing V_S to ring excessively below the COM terminal causing possible malfunction of the HIP2500 due to excessive charge being pulled out of the substrate.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing Miller Effect when an opposing switch is being rapidly turned on.
Floating VSS with respect to COM. These should be tied together.	Can cause drive pulses to disappear or excessive current flow between V_{SS} and COM.

Quick Help Table

To aid in locating possible solutions to problems which can occur in applying the HIP2500 and similar high voltage IC gate-drivers, the following table is included.

General Problems and Effects

PROBLEM	EFFECT
Low V_{DD} and V_{BS}	Low supply voltages can cause U/V lockout and blocking of gate drive.
High V_{DD} and V_{BS}	Causes wasted bias supply power due to overcharging the gates of the external switches and can result in reduced reliability due to decreased voltage margin to Max. bias voltage rating and increased operating temperature of the IC.
C_F too small	Insufficient charge to drive external power devices and/or possible U/V lockout can occur.
C_F too large	The bootstrap capacitor may not charge sufficiently to overcome U/V lockout level and gate drive never occurs. Either decrease C_F or increase the refresh time allotted to charge C_F
R_{GATE} too big	R_{GATE} x C_F time constant too long causing excessive power device switching losses. Also R_{GATE} too big may fail to hold gate low when the opposing power device turns on, tending to either turn on the device prematurely or slow desired turn-off, due to the Miller Effect. May need to bypass R_{GATE} with an anti-parallel signal diode.
R_{GATE} too small	R_{GATE} too small tends to reduce effective dead time and increase shoot-through tendency. Also switching dv/dt increases EMI.
Negative or insufficient dead-time	Can cause external power devices and the IC to fail, possibly destroying circuit board traces also. This also tends to severely reduce "refresh" time (see C_F too large, above).
HIP2500 IC gets too hot	Trying to drive too large an external power device. Reduce the switching frequency, the high voltage bus or find a power device with a lower equivalent gate capacitance. You may also be able to increase air flow over the IC and/or add heat-sinking.
Unexplained arcing in vicinity of pins 3, 4 and 5 of IC	Poorly cleaned, dirty or improper attention to strike and creepage distances for the bus voltage level being used may cause this damage or similar damage between traces going to these points.

Harris Semiconductor

APPNOTE

No. AN9105.1 May 1992

Harris Intelligent Power

HVIC/IGBT HALF-BRIDGE CONVERTER EVALUATION CIRCUIT

Author: George Danz

The HVIC high voltage integrated circuit is designed to drive n-channel IGBTs or MOSFETs in a half-bridge configuration up to $500V_{DC}$. Power supply and motor control inverters can be configured for voltages up to $230V_{AC}$ using the HVIC, IGBTs and a few other components.

A few precautions should be taken in using the circuit. Lead lengths between the external power circuit (including gate and pilot leads), the 15V bypass capacitor (C_{DD}), the bootstrap diode (D_F) and capacitor (C_F) and the HVIC should be minimized.

The basic components required to evaluate the features of the SP601 are shown in the simplified schematic. The recommended load is largely resistive so that the largest current component will flow through the IGBTs, IGT1 and IGT2.

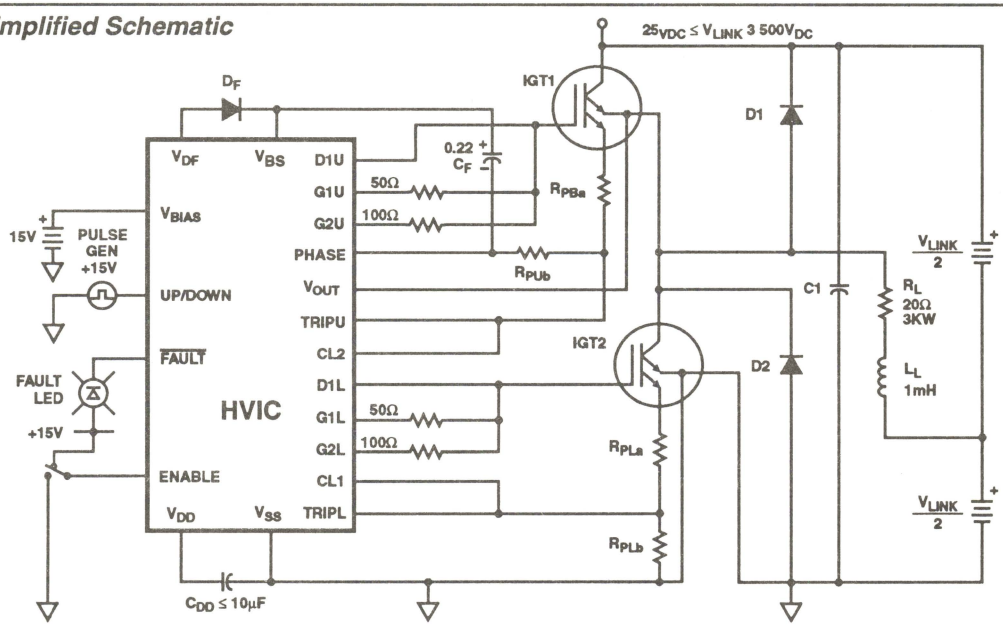
The flyback diodes, D1 and D2, rated 8A, will carry a much smaller flyback current component. A small amount of load inductance will cause the switching waveforms to simulate the conditions which would normally be observed with motor or transformer loads, while limiting the current carried by the lower rated flyback diodes in this circuit.

The values for R_{PUa}, R_{PUb}, etc., have been chosen to result in overcurrent trip at approximately 25Apk. At this level of current, heat sinking for the IGTs and flyback diodes is required. The series resistance of the upper and lower pilot resistor dividers would be approximately 1KΩ; the divider ratio should cause 0.1V at the tap at the desired trip current.

When first energizing your evaluation circuit, begin with a reduced bus voltage of about $20V_{DC}$ to $30V_{DC}$ to verify proper circuit operation before proceeding to higher voltages.

More specific information can be found in File Number 2428 and File Number 2429 Half-Bridge $500V_{DC}$ Driver data sheets and in the Application Note, AN-8829.1.

Simplified Schematic



HVIC - Harris Part # SP601 (Formerly GS601) | D1, 2 - Harris Part # RUR860 | R_{PUa}, R_{PLa} - 910Ω, 1.8W | C1 - 0.1µF, $600V_{DC}$

IGT1, 2 - Harris Part # HGTA24N60D1C | D_F - Harris Part # A114M | R_{PUb}, R_{PLb} - 68Ω, 1.8W | R_L - 20Ω, 3KW 13 -50

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APPNOTE

No. AN9201.1 April 1994

Harris Intelligent Power

PROTECTION CIRCUITS FOR QUAD AND OCTAL LOW SIDE POWER DRIVERS

by Wayne Austin

Overview

Normally, the defined requirements for a Quad or Octal Driver are very much affected by the type of protection circuits used on the chip. Fault protection for an open or shorted load is an interactive function, making it important in the decision process of specifying the proper IC for an application. The various types of on-chip features may include protection for over-current, over-voltage and over-temperature. The response action to a fault condition may be either limiting or shutdown. Shutdown methods may include hysteresis and may require a logic reset. On-chip clamp diodes provide current steering to an external zener diode clamp as over-voltage protection from inductive switching pulses. Internal Zener diodes are also used to limit the output voltage on the output driver of the IC. In addition, fault detection is available with diagnostic feedback, including serial bus (SPI) control. All of the protection features noted are represented in the Table 1 listing of Quad and Octal Low Side Drivers:

TABLE 1. QUAD & OCTAL LOW SIDE POWER DRIVERS

TYPE	DESCRIPTION	KEY FEATURES
CA3242	Quad Gated Inverting Power Dr.	Over-Current Latch-Off, Fast Fault Shut-Down, Output Protection Diodes
CA3262	Quad Gated Inverting Power Dr.	Over-Current Limiting, Over-Temperature Limiting, Output Protection Diodes
CA3262A	Quad Gated Inverting Power Dr.	Same as CA3262 plus +125°C Max. T_A Range.
CA3272 and CA3272A	Quad Gated Inverting Power Dr. with Fault Mode Diag. Flag Output	Over-Current and Temp. Limiting, Fault Flag Output, +125°C Max. T_A Range. CA3272A has improved Fault Flag Output Drive Capability.
CA3282	Octal Driver with SPI Logic Control	Over-Current and Over-Voltage Fault Mode Protection with Fault Mode Feedback/ Control with -40°C to +125°C Max. T_A Range.
CA3292A	Quad Gated Inverting Power Dr. with Fault Mode Diag. Flag Output	Similar to CA3272A with added Internal Over-Voltage Output Clamp.
HIP0080 and HIP0081	1A and 2A Quad Gated Inverting Power Drs. with Multi-mode Diag. Feedback	Over-Current (Latch-Off), Over-Temperature (Gates-Off), Open Load and Output Ground Short Detection, Over-Voltage Internal Output Clamp Diodes, Fault Mode Feedback/Control and -40°C to +125°C Max. T_A Range.

While the CA3282 Octal Driver is quite different from the quad drivers, it is included here because it is used in similar applications. The CA3282, HIP0080 and HIP0081 feature Power BiMOS with MOSFET Output Drivers for higher current and voltage capability. Because of the additional dissipation associated with these drivers, the CA3282 and HIP0081 are provided in a 15 pin SIP power package. The other Quad Drivers are available in the 16 pin DIP and/or 28 lead PLCC packages which have special construction for improved heat dissipation. All of these Low Side Switches generally share a common characteristic of 5V input CMOS or TTL logic level control.

The Quad and Octal Power Drivers include a wide variation of choice in selecting a device type. The available types are listed in TABLE 1 which also highlights the key parameters for most applications. By-type, the protection features of the Quad and Octal Drivers are listed in the table and are explained in the following detail of this IC Application Note to assist the user in making an intelligent device selection for the application of interest.

CA3242 Quad Power Driver

In normal use, the supply voltage is applied through a load to an NPN open collector output of the CA3242 quad driver. The functional block diagram is shown in Figure 1. The maximum current rating of 1A does not distinguish between average and peak. Each output is independently protected and latches "OFF" when the load current exceeds the latch-off threshold in the "ON" state. The CA3242E feature of short circuit protection is a responsive high-speed shutdown of the output drive to a shorted load. Under worse-case shorted load conditions, the supply voltage is applied direct to the output device. The latch-off threshold is typically 1.3V ($I_{SC}R_{ON}$), where R_{ON} is the saturated "ON" resistance of the output. The CA3242 latches "OFF" at a typical short circuit current of 1.2A with 25µs nominal delay. The ENABLE or the IN pin of the latch-tripped channel must be toggled to reset the latch.

To better understand the mechanism of protection when the CA3242 is subjected to a shorting condition, Figure 2 illustrates that part of the Figure 1 noted as the "PROT" functional block. When an over-load current is applied to an output driver, the V_{SAT} increases to a threshold level set in a

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TABLE 2. QUAD AND OCTAL DRIVER FEATURES

	CA3242	CA3262	CA3262A	CA3272 CA3272A	CA3292A	HIP0080	HIP0081	CA3282 (OCTAL DR.)
Max. Output Voltage, No Load	50V	60V	60V	60V	32V Typ. (Clamp)	36V Typ. (Clamp)	80V Typ. (Clamp)	32V Typ. (Clamp)
Max. Output Load Current	0.6A	0.7A	0.7A	0.6A	0.6A	1A	2A	1A
Max. V_{SAT} Output Voltage Max. R_{ON} Output Resistance	0.8V at 0.6A	0.6V at 0.6A	0.5V at 0.6A	0.4V at 0.5A	0.4V at 0.5A	1.0Ω at 0.5A	0.5Ω at 1A	1Ω at 0.5A
Max. Load Switching Voltage, $V_{CE(SUS)}$ or V_{CLAMP} Limited	35V	40V	40V	40V	28V	27V	73V	30V
Typical Output Current Limiting and/or Shutdown Protection	1.4A (Latches Off)	1.6A	1.3A	1.2A	1.2A	1.8A (Latches Off)	3.5A (Latches Off)	1.5A (Latches Off)
Output Thermal Limiting and/or Shutdown Protection (Temp. T_J)	None	155°C (Limits)	155°C (Limits)	165°C (15°C hys.)	165°C (15°C hys.)	150°C (15°C hys.)	150°C (15°C hys.)	None
Over-Voltage Protection	Current Steering Clamp Diode			None	Zener Diode Feedback Clamp			
Fault Diagnostics	No			Fault Flag		Fault Mode Flag and Feedback		
Temp. Range, -40°C to __°C	105°C	85°C	125°C					
Packages: 16 DIP Pwr WEB (θ_{JA}) 28 PLCC Pwr WEB (PC Bd, θ_{JA}) 15 SIP (Tab H.S., θ_{JC})	40°C/W	40°C/W	40°C/W 30°C/W	30°C/W	30°C/W	30°C/W	3°C/W	3°C/W

comparator circuit. The comparator outputs a switching signal to the protection latch and the input drive is "latched-off". The input may be reset with an INPUT or ENABLE toggle, or by and ON-OFF toggle of the power supply to the control circuits.

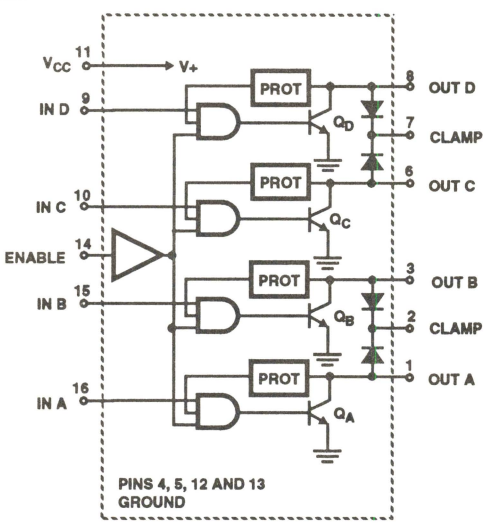


FIGURE 1. CA3242 FUNCTIONAL BLOCK DIAGRAM

Proper application will protect the CA3242E during turn-off under shorted load conditions. Observations of wide ranging conditions have been done to test the shutdown behavior and has revealed several pitfalls that should be addressed to assure safe shutdown. One should be aware that a forced short circuit test condition may be considerably more severe than a normal application shorted load. In either case, two problems arise that affect the severity of the overload during shutdown. These are:

1. A shorted load is inductive and causes the generation of voltage spikes, exposing the output device to at least 2 times the value of the V+ supply voltage.
2. Lack of bypassing can provoke severe oscillations during the delay period before shutdown is complete. This is typically less than 25µs.

The result of this oscillation with an inductive load is to alternately stress the output device in both a forward and reverse direction at rates as high as 1mHz, lasting until shutdown occurs. This problem is compounded in some applications when 2 or more devices are used in parallel to increase drive output. In this case, a short may now draw twice the current of one driver which, in turn, results in almost twice the unclamped voltage spike developed across each output transistor.

To suppress oscillations during shutdown requires some attention to the use of adequate bypassing of both the +5V V_{CC} supply and the battery or output supply voltage. Bypassing the output supply will minimize both the transient oscillations and the voltage spike effects of lead inductance.

Then, the shorted output is stressed in the forward bias mode with the shorted current determined by voltage source, duration of short, line resistance and the resistance of the saturated output. In a practical application, the load and any potential short may occur in a remote location. As such, bypassing the output supply may not be practical. Bypassing the +5V supply with a 0.1µF capacitor closely wired to pins 11 and 12 of the CA3242E constitutes adequate bypassing of the +5V supply.

Because voltage spikes are normal to the application, a 30V zener "clamp" diode is needed to limit the device output voltage spikes to less than the maximum rating of 35V. The zener clamp diode protection should be closely wired to pins of the output divide in order to avoid any delay in the voltage clamping action. Alternatively, the on-chip diodes may be used in a free wheeling mode by connecting the CLAMP pins to the supply voltage if it does not exceed 30V during transients. Zener diode clamp protection is preferred over the power supply clamp option, primarily because the power supply may be subject to large transient changes.

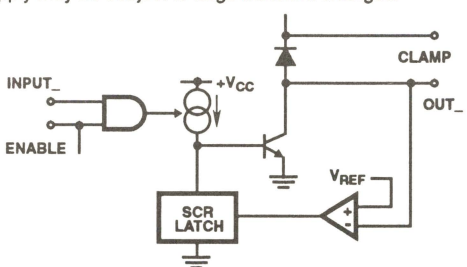


FIGURE 2. CA3242 FUNCTIONAL DIAGRAM FOR EACH OUTPUT CHANNEL SHOWN WITH PROTECTION CIRCUIT

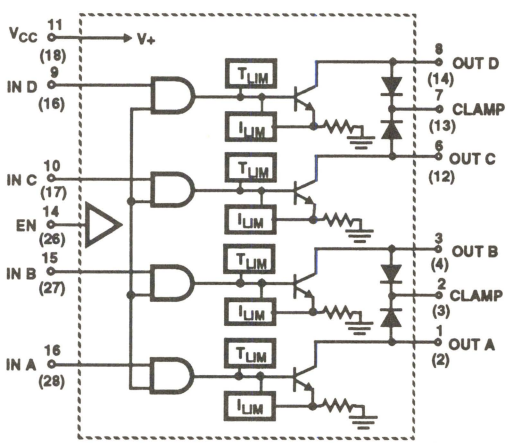
CA3262 and CA3262A Quad Power Drivers

The CA3262 is a quad-gated inverting low-side driver capable of switching 700mA load currents (at +25°C) in each output without interaction between the outputs. Shown in Figure 3, each output is independently protected with overcurrent limiting and over temperature limiting features. If an output load is shorted, the remaining three outputs function normally unless the junction temperature of their output device exceeds the over temperature limiting threshold of +155°C (typical). Current limiting prevents the output current from exceeding a value determined by the design (1.2A typical), independent of the load condition. The power dissipation of the shorted output driver is equal to the product of the limiting value of current and the applied output collector voltage. If this value causes the junction temperature to exceed +155°C (typical), the base drive to the output transistor, and thereby it's collector current, is reduced until the resulting power dissipation is equal to that value which maintains the junction temperature at the thermal limit value. The current which flows in the output transistor in a short circuit mode is therefore a function of the ambient temperature, the thermal resistance of the package in the application, the total power dissipated in the package. If the short is removed, normal operation resumes automatically.

In order to clamp high voltage pulses which may be generated by switching inductive energy in the load circuit, zener diodes with a value not greater than 30V should be connected to the CLAMP pins. On-chip diodes are connected from each output to one of the two CLAMP pins and are intended for use as steering diodes to provide a path for the clamped pulse current to a CLAMP pin; allowing the use of one zener diode to clamp all outputs. Alternatively, the on-chip diodes may be used in a free-wheeling mode by connecting the CLAMP pins to the supply voltage if it does not exceed 30V during transients. Zener diode clamp protection is preferred over the power supply clamp option, primarily because the power supply voltage may be subject to large transient changes. Note that the rate of change of the output current during switching is very fast. Therefore, even small values of inductance (such as the inductance of several meters of wire) in the load circuit can generate voltage spikes of considerable amplitude on the output terminals and may require clamping to prevent damage.

The CA3262A is a lower V_{SAT} version of the CA3262 and is rated for +125°C ambient temperature applications. The CA3262 is limited to about +100°C (data sheet rating at +85°C) ambient temperatures. Otherwise, the protection features described here apply to both versions. Figure 3 shows a functional block diagram for the CA3262 and CA3262A. Each type has independent current limiting and thermal limiting protection for each output driver. The maximum current rating of each output is typically greater than 1.2A. However, this is not a users choice rating, the current limiting may range from 0.7A to as high as 2A.

Typical applications of the CA3242 and CA3262 quad drivers with the recommended method for use of the current steering diodes is shown in the circuit of Figure 4. Where inductive loads are not used, the protective diodes need not be externally connected. However, the user should be alert to the potential for stored energy in long wire connections to the load circuits.



PINS 4, 5, 12 AND 13 GROUND (PACKAGE E)
PINS 5-11 AND 19-25 GROUND (PACKAGE Q)
PIN #'S IN PARENTHESIS APPLY TO PACKAGE Q

FIGURE 3. CA3262 AND CA3262A FUNCTIONAL BLOCK DIAGRAM

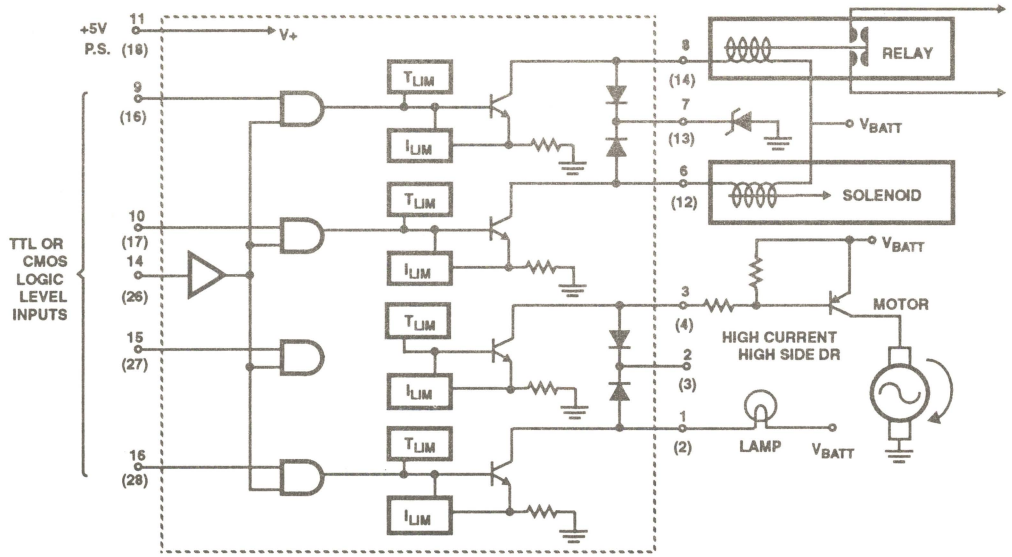


FIGURE 4. TYPICAL APPLICATION CIRCUIT FOR THE CA3262 AND CA3262A QUAD POWER DRIVERS WITH PROTECTION DIODES EXTERNALLY CONNECTED TO A ZENER CLAMP DIODE FOR INDUCTIVE LOAD PROTECTION.

The CA3262 and CA3262A will typically survive when shorted if the output supply voltage is less than 18V. This potential for failure is flagged in the data sheet as a note under the Electrical Characteristics table. It takes a few milliseconds to shutdown when the output is short circuited. During shutdown the dissipation may be excessive and is primarily determined by I_{SC} which is the limiting current. The short-circuit current will be limited but the voltage that the shorted output sees may approach V_{SUPPLY}. Not considering transient effects, the worst case dissipation would be $P_D = (V_{SUPPLY})x(I_{SC})$. Normally, a shorted solenoid or relay will have a few ohms of impedance which should prevent catastrophic IC failure in 12V automotive applications. A typical value for I_{SC} is 1.3A. R_{ON} is the saturated collector resistance of the output transistor with a typical value of 1Ω. V_{SUPPLY} is normally 9V to 16V in automotive applications. The thermal shutdown could be made faster but the circuit would not be able to effectively drive lamps which have a very low resistance in a cold start-up. Lamp drive capability is a common application use for the CA3262 and CA3262A.

CA3272 and CA3292 Quad Power Drivers with Fault Mode Flag

The CA3272 and CA3292 are quad-gated inverting low-side power drivers with a fault diagnostic flag output. They are rated for +125°C ambient temperature applications and have current limiting and thermal shutdown. As shown in Figure 5, they differ from the CA3262A by not having output clamp diodes but do have the diagnostic short-circuit flag outputs. Each output driver is capable of switching 400mA load currents at +125°C ambient without interaction between the outputs. Current limiting functions in the same manner as the CA3262 with a typical limit value of 1.2A. The current limiting range is set for 0.6A to 1.6A. While the thermal shutdown characteristics differ from the CA3262 by having hysteresis, the same precaution applies for potential damage from high transient dissipation during thermal shutdown. The CA3272Q, CA3272AQ and CA3292AQ Quad Driver are provided in the 28 pin web-leadframe PLCC package. This package has slightly lower thermal resistance than the 16 lead DIP package with a web leadframe.

The FAULT DETECTOR circuit of the CA3272, CA3272A and CA3292A is shown in Figure 6 as an equivalent logic block diagram. Channel A is one of 4 power switching functions displayed in the diagram. Transistor Q_A is the protected power transistor switch that drives the "OUT A" terminal. The FAULT DETECTOR block illustrates the logic functions associated with FAULT DETECTION. The ENABLE input is common to each of the 4 power switches and also disables the FAULT output when it is low. From the "IN A" input to the "OUT A" output, the switch condition is inverting (NAND). When IN is high, OUT is low. The FAULT DETECTOR senses the IN and OUT states and switches Q_F "ON" if a fault is detected. Transistor Q_F activates a sink current source to pull-down the FAULT pin to a 0 (low) state when the fault is detected. Both shorted and open load conditions are detected.

The CA3292A is equivalent to the CA3272A except that it has internal clamp diodes on the outputs to handle inductive switching pulses from the output load. The CA3272A and CA3292A have significantly higher I_{OL} FAULT output drive than the CA3272. Expanded functional block diagram detail of the fault logic is similar to that of the CA3272 as shown in Figure 6. The structure of each CA3292A output, shown in Figure 6B, includes a zener diode from collector-to-base of the output transistor. This is a different form of protection than the CA3242 or CA3262 which have current steering clamp diodes on each output, paired to one of two "CLAMP"

output pins. The CA3292A output transistor will turn-on at the clamp voltage threshold which is typically 32V and the output transistor will dump the pulse energy through the output driver to ground.

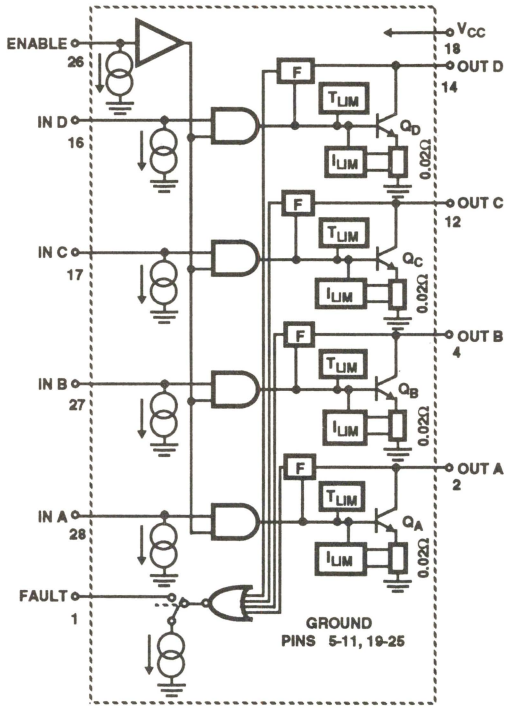


FIGURE 5. CA3272 AND CA3272A FUNCTIONAL BLOCK DIAGRAM

Each of the outputs are independently protected with over-current limiting and over-temperature shutdown with thermal hysteresis. If an output is shorted, the remaining outputs function normally unless the temperature rise of the other output devices can be made to exceed their shutdown temperature of +165°C (typical). When the junction temperature of a driver exceeds the +165°C thermal shutdown value, that output is turned off. When and output is shutdown, the resulting decrease in power dissipation allows the junction temperature to decrease. When the junction temperature decreases by approximately 15°C, the output is turned on. The output will continue to turn on and off for as long as the shorted condition exists or until shutdown by the input logic. The resulting frequency and duty cycle of the output current flow is determined by the ambient temperature, the thermal resistance of the package in the application, the total power dissipation in the package. Since each output is independently protected, the frequency and duty cycle of the current flow into multiple shorted outputs will not be related in time. Long lead lengths in the load circuit may lead to oscillatory behavior if more than two output loads are shorted.

A diagnostic flag indicates when an output is shorted. This information can be used as input to a microprocessor or dedicated logic circuit to provide a fast switch-off when a short occurs and also to determine by sequence action, which output is shorted. A fault condition in any output load will cause the FAULT output to switch to a logic "low". Added detail of the fault logic is shown in Figure 6A. Since a fault condition will be indicated during switching, use of an appropriate size capacitor to filter the FAULT output is recommended (see data sheet). This will prevent the FAULT output voltage from reaching a logic level "0" within the maximum switching time. The FAULT detection circuitry compares the state of the input and the state of the output. The output is considered to be in a high state if the voltage exceeds the typical FAULT threshold reference voltage, V_{THD} of 4V. If the output voltage is less

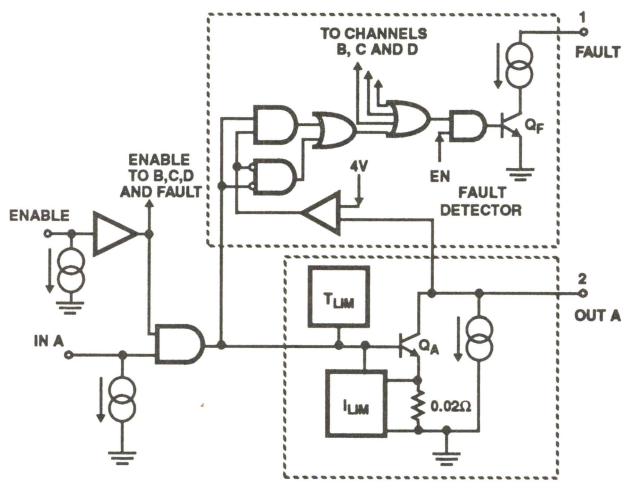


FIGURE 6A. FAULT DETECTOR SHOWN WITH THE CA3272 AND CA3272A OUTPUT STAGE

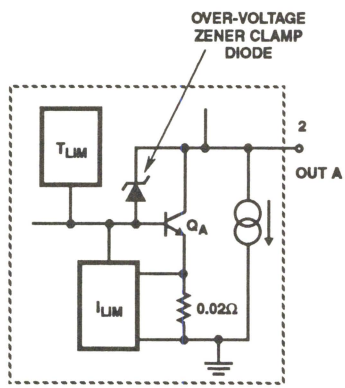


FIGURE 6B. CA3292A OUTPUT STAGE WITH CLAMP DIODE

FIGURE 6. FAULT DETECTION FUNCTIONAL BLOCK DIAGRAM OF THE CA3272, CA3272A AND CA3292A

than V_{THD}, the output is considered to be in a low state. For example, if the input is high and the output is less than V_{THD}, a normal "ON" condition exists and the FAULT output is high. If the input is high and the output is greater than V_{THD}, a shorted load condition is indicated and the FAULT output is low. When the input is low and the output is greater than V_{THD}, a normal "OFF" condition is indicated and the FAULT output is high. If the input is low and the output is less than V_{THD}, an open load condition exists and the FAULT output is low. The FAULT output is disabled when the ENABLE input logic level is low.

To detect an open load, each output has an internal low-level current sink which acts as a pull-down under open load fault conditions and is always active. The magnitude of this current plus any leakage associated with the output transistor will always be less than 100µA. (The data sheet specification for I_{CEX} includes this internal low-level sink current). The output load resistance must be chosen such that the voltage at the output will not be less than V_{THD} when the I_{CEX} sink current flows through it under worse case conditions with minimum supply voltage. For example, assume a 6.5V minimum driver output supply voltage, a maximum FAULT threshold reference voltage of V_{THD} = 5.5V and an output current sink of I_{CEX} = 100µA. Calculate the maximum load resistance that will not result in a FAULT output low state when the output is OFF.

$$R_{LOAD}(max) = [V_{SUPPLY}(min) - V_{THD}(max)] / I_{CEX}(max)$$

$$R_{LOAD}(max) = (6.5V - 5.5V) / 100\mu A = 10k\Omega$$

Since the CA3272 and CA3272A do not have on-chip diodes to clamp voltage spikes which may be generated during inductive switching of the load circuit, external zener diodes (30V or less) should be connected between the output terminal and ground. Only those outputs used to switch inductive loads require this protection. Note that since the rate of change of output current is very high, even small values of inductance can generate voltage spikes of considerable amplitude on the output terminals which may require clamping. External free-wheeling diodes returned to the supply voltage are generally not acceptable as inductive clamps if the supply voltage exceeds 30V during transients.

CA3282 Octal Power BiMOS Driver with SPI Bus

The CA3282 is a logic controlled Power Driver with a Serial Peripheral Interface (SPI). The chip is fabricated in a Power BiMOS process with high voltage and current drive capability. A functional block diagram is shown in Figure 5. There is an extensive amount of logic circuitry to provide individual diagnostic feedback; including which output may be shorted. Each of the open collector output drivers has individual protection for overcurrent and overvoltage; and, each output has separate output latch control. The current limiting of the CA3282 is set for a range of 1A to 2A (1A min.). In the normal ON state, each output driver is in a saturated low state. Comparators in the diagnostic circuit monitor the drain of the output drivers to determine if an out-of-saturation condition exists. If a comparator senses a voltage higher than the threshold trip level of 3V typical, the latch control circuit is reset (unlatched) and the respective output driver is shutdown. The on-chip current limiting protection is independent of the diagnostic feedback loop. If an over-current condition exists, the condition may be sustained unless the diagnostic circuit senses a fault condition. Open-load faults may be detected with a diagnostic check of the output in the off state. A 150µA typical internal current sink pull-down forces the output low when it would otherwise be high.

Maximum current ratings allow all eight outputs to be turned on to a level of 0.5A. This is allowed because the CA3282 chip is packaged in 15 pin SIP power package with 3°C/W typical junction-to-case thermal resistance, allowing high dissipation capability in ambient temperatures up to 125°C. The CA3282 output driver structure consists of a MOSFET with a zener diode feedback from the drain to gate, forming an overvoltage clamp structure for protection from voltage spikes generated when switching inductive loads. The pulse energy is shunted to ground through the MOSFET output driver.

The CA3282 protection features support many application requirements. A typical application circuit is shown in Figure 8. Where inductive loads are used, no external diode is needed to shunt the load coil turn-off pulse. However, it is important to adhere to the maximum peak current ratings for currents that can flow in the output devices. The output drivers are turned-on by an internal zener feedback for over-

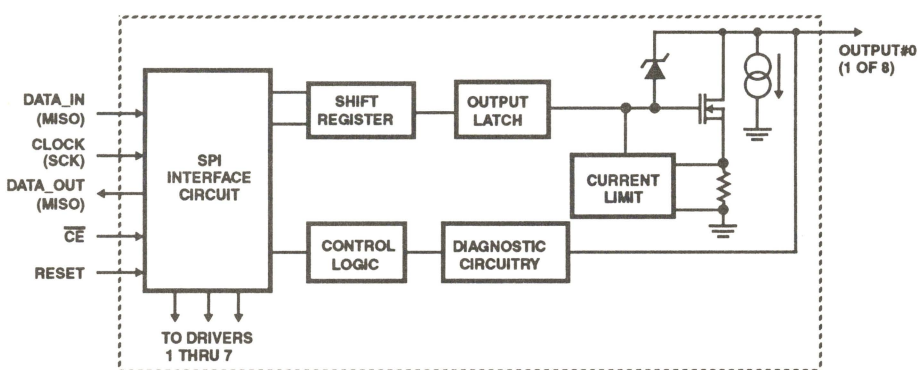


FIGURE 7. CA3282 BLOCK DIAGRAM FOR ONE OF EIGHT DRIVER STAGES

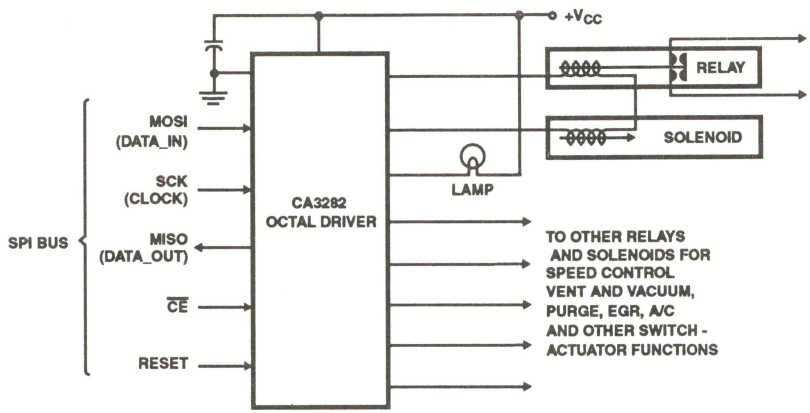
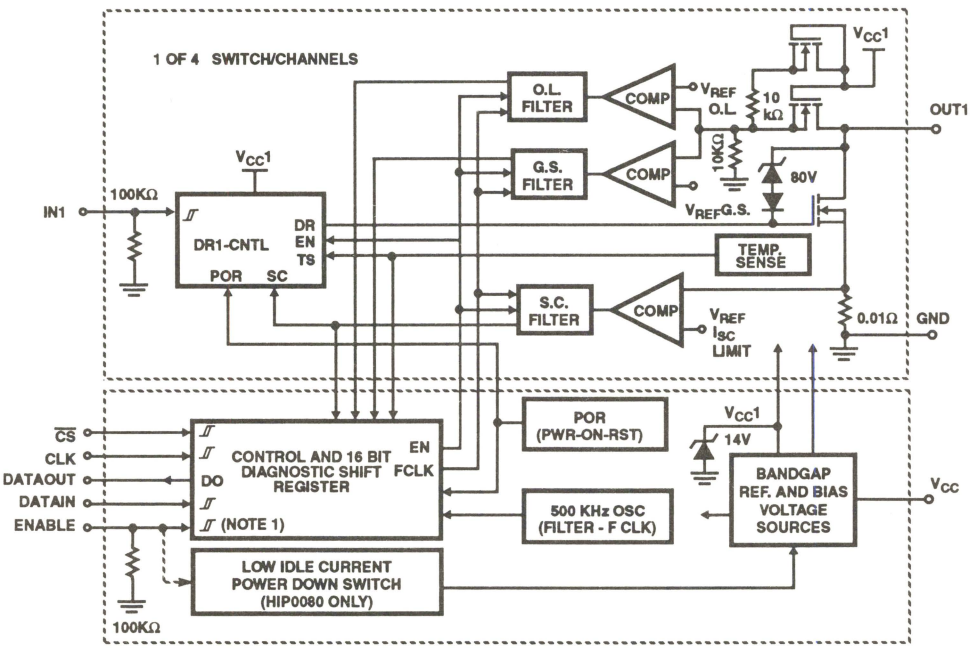


FIGURE 8. CA3282 TYPICAL APPLICATION CIRCUIT WITH SPI BUS CONTROL



NOTE:

1. HIP0080 - no enable hysteresis.

FIGURE 9. EQUIVALENT FUNCTION BLOCK DIAGRAM OF THE HIP0080 AND HIP0081

voltage clamp protection of each output. The circuit of Figure 8 illustrates an automotive application where a CDP68HC05 microprocessor or equivalent controls the SPI bus and determines what action if any will happen when a fault is detected. In this way the CA3282 is designed to support a variety of applications such as industrial controls. Due to the high cold starting current of lamp loads, it is not advisable to switch-on more than one lamp load at a time. Included in the many features of the CA3282 is a very low logic supply current to support the needs for low stand-by current drain.

HIP0080 and HIP0081 Quad Power MOSFET Drivers with Serial Diagnostic Interface

The HIP0080 and HIP0081 are low side power switches fabricated in a Power BiMOS process technology. They can typically sustain higher voltage and current capability than Power Bipolar ICs. Except for package and pinout differences, both circuits are functionally similar as shown in the functional block diagram of Figure 9. The HIP0080 and HIP0081 are designed to sustain 1A and 2A respectively of DC output current drive. The output drivers are voltage rated up to the clamp level set by drain-to-gate zener diodes and typically clamp at 80V for the HIP0081 and 36V for the HIP0080. A 15 pin SIP power package is used to achieve maximum capability for the HIP0081 while the HIP0080 is available in the 28 pin PLCC web lead frame package.

The diagnostic monitoring and feedback process of the HIP0080 and HIP0081 is different from the CA3282. Each output device is independently toggled on or off through a driver interface circuit that is, in part, controlled by over-current and over-temperature diagnostic feedback. The conditions on each output device are monitored to sense over-current, over-temperature, open-load and output-ground shorting. Four separate bits for each of the four outputs are loaded into a 16 bit serial diagnostic register. The diagnostic information is accessed with a low on the chip select pin and the clock input. Both DATA IN and DATA OUT pins are available to allow cascade operation. The first bit in the data readout is a fault error flag which is high if any one of the following 16 bits indicate a fault condition. When chips are cascaded, the error flags are cascaded and a fault condition is immediately evident if there is a fault on any chip. Although, all bits must be read to determine where, if any, the fault condition exists. While the diagnostic interface for data gathering purposes is quite different than the CA3282, the drive control and diagnostic feedback is SPI Bus compatible.

Another part of the diagnostic feedback circuits provides for digital delay filtering to prevent short transient over-current and output voltage readings from loading the diagnostic register with false data. Each output is sensed with a window comparator to determine whether the output is high, low or centered. A resistor divider consisting of two 10KΩ resistors sets a reference voltage level for the window comparator. When a centered reading is detected with the driver output off, the centered reading is sensed as a no load condition on the output. If the window comparator senses a low reading when the driver output is off, the result is interpreted as a short to ground. The results are passed through a digital delay filter and are transmitted to the diagnostic shift register. The over-current sense level is read from a metal source-to-ground resistance in each output by a comparator that senses the voltage as a current. When an over-current level is detected, the result is sent through a digital delay filter to the diagnostic shift register and also toggles a latch circuit in the drive control which cuts-off drive to the output stage. Where a shorted condition exists, the short must be removed and the input toggled off and on to reset normal operation. If an over-temperature condition is sensed, the feedback result is fed directly back to the input control stage to gate-off drive to the output stage while also loading the diagnostic shift register. Normal chip operation may resume when the chip is sufficiently cooled. There is a typical 15°C hysteresis shift intended by design to provide a cooling cutoff period.

Summary

While this information on the protective structures of the Quad & Octal Power Drivers should be helpful, it must also be recognized that the design of the application circuit should be consistent with performance requirements. Generally, the data sheets define parameters in terms of each separate switch. Although the data sheets do not specify parallel switch ratings and limits, the switches may be used in parallel to increase current drive capability. Also, there are a number of design considerations that will impact the continuing performance and reliability of the IC. The protective features of the Quad and Octal Drivers discussed here provide substantial system application protection by reducing the potential for catastrophic failure. To provide the user with a better in-sight into the device on-chip functions, the function block diagrams with their respective protection features have been included here. Additional detail can be found in the data sheet for each type.

References

1. CA3262, CA3272 distributed Automotive Brochures provided a document titled "Quad Power Drivers", No. BR-002. (Stress Data)
2. CA3262 - PCIM June 1988 article titled "Current and Temperature Limiting Protect Power Switch Driver Outputs" which has shutdown timing information to show the independent action of shutdown plus other application detail.

For reference, the data sheet file numbers are listed by type as follows:

TYPE	NO.	TYPE	NO.
CA3242	1561.2	CA3282	2767.4
CA3262, CA3262A	1836.3	CA3292A	2223.3
CA3272, CA3272A	2223.3	HIP0080, HIP0081	3018.2

Acknowledgments

The material presented here has been written by Wayne Austin, Harris Intelligent Power Product Applications of the Harris Automotive Design Center, Somerville, NJ with contributions from Tom DeShazo, Lou Pennisi, Bob Kumbatovic and Paul Dackow.

Harris Semiconductor

APPNOTE

No. AN9208 April 1994

Harris Intelligent Power

HIGH FREQUENCY POWER CONVERTERS

Authors: Rudy Severns, Springtime Enterprises
Hal Wittlinger, Harris Semiconductor

Introduction

Computers and telecom equipment are steadily becoming more complex, providing ever higher levels of performance. Simultaneously, the selling price for this equipment is being driven ever lower by market competition. Integral to all of this equipment is a power conversion system which converts the incoming unregulated power from the utility, or other source, to the multiple regulated voltages required by the equipment. In present designs the power subsystem constitutes a significant part of the equipment cost and volume.

The development of a unique power converter(s) for each new system is a substantial cost item in the equipment development. Frequently the equipment will have a variety of configurations with differing power requirements. To save development cost only a single design is often used to cover a range of loads. The result is that many users have to pay for capability not needed in their particular configuration.

One means to reduce power subsystem over capacity and cost is to use a distributed power system where the power processing functions are distributed within the system and more power processing capacity is added as required when more capability is installed. A typical distributed system will have a central power processor which converts the raw input power into a regulated DC bus. The central power processor is relatively simple but it does provide for line isolation and the safety requirements for the system. The central processor may be modular to allow for power scaling as the loads change. Each board or group of boards within the equipment has a small power processor which converts the DC bus to the voltages required by that particular section of the equipment. In general these board level converters are quite simple and efficient. Frequently no DC isolation is required at the board level which further simplifies the converters.

The use of multiple small power converters allows a custom system to be designed using high volume, low cost, standardized modules. In a complex system there can be substantial cost savings.

Board space is always at a premium and the localized power converters take up space. In general height is severely constrained and the power converter has a low profile geometry which tends to increase the board area required. In order to minimize the area required, the switching frequency (fs) of the converter is pushed as high as possible. The latest generation of systems [1] use converters with fs in the low MHz.

In addition to minimizing board area there are other requirements placed on these converters. [2] The components must be small enough for automated insertion and be low cost. All of this has to be achieved without seriously reducing conversion efficiency. Poor efficiency would increase the size and cost of the input converter and create thermal problems within the unit.

Overall these "simple" converters represent a significant design challenge.

Converter Circuits For MHz Switching

Many possible circuit topologies exist which could be used. They fall into three general categories: switchmode, resonant and quasi-resonant. At the power levels typical of board mounted converters (1 to 100W) single switch topologies are usually preferred for their lower cost. Examples of typical single switch, PWM converters are shown in Figure 1. A comparison of the switch, diode and capacitor voltages for these circuits is given in Table 1. In general circuits with the switch referenced to the ground node are preferred to simplify the switch drive circuits. The boost, Cuk and SEPIC circuits are non-isolated circuits with ground referenced switches. The flyback and forward converters provide isolation as well as multiple outputs with a single, ground referenced switch. The price paid for using an isolating transformer is higher cost and the increasing difficulty of designing a high performance transformer as the frequency is raised. The simpler non-isolated topologies are usually preferred in a distributed system unless there are compelling reasons to provide isolation.

TABLE 1. COMPONENT VOLTAGE STRESS FOR VARIOUS TOPOLOGIES

CIRCUIT	V_{SWITCH}	V_{DIODE}	$V_{COUPLING}$
Buck	V_I	V_I	N/A
Forward	$V_I/(1-D)$	$V_O/(1-D)$	N/A
Boost	V_O	V_O	N/A
Flyback	$V_I/(1-D)$	V_O/D	N/A
Buck-Boost	$V_I + V_O$	$V_I + V_O$	N/A
SEPIC	$V_I + V_O$	$V_I + V_O$	V_I
Cuk	$V_I + V_O$	$V_I + V_O$	$V_I + V_O$

NOTE: V_I = Input Voltage, V_O = Output Voltage, D = Duty Cycle

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The boost, Cuk and SEPIC circuits each have different characteristics. The boost has a non-pulsating input current and a pulsating output current. It can only make voltages higher than the input bus. The Cuk converter has non-pulsating input and output currents and it can generate voltages either greater or less than the input voltage. The non-isolated Cuk converter inverts the sign of the input voltage. For the normal case of a positive DC bus, the Cuk converter will only produce negative voltages. The SEPIC converter is non-inverting and can generate voltages either above or below the input. The input current is non-pulsating but the output current is pulsating. Non-pulsating input and output currents are desirable to minimize EMI and reduce the need for additional filter elements.

The circuits in Figure 1 are considered "conventional" in that they have been widely used for many years. These topologies have first order input to output voltage transfer functions $M = V_O/V_I$, such as D, 1/(1-D) or D/(1-D). Recent work by Maksimovic [3, 4, 5] has shown that single switch quadratic and even higher order topologies exist. Three circuit examples are given in Figure 2. Quadratic circuits are particularly useful when large input to output voltage ratios are needed or a large variation in input voltage is present.

When implemented with discrete components the high frequency performance of switchmode circuits is limited by the parasitic inductance and capacitance normally present. This is due to the very fast voltage and current transitions required for efficient power conversion. One way to get

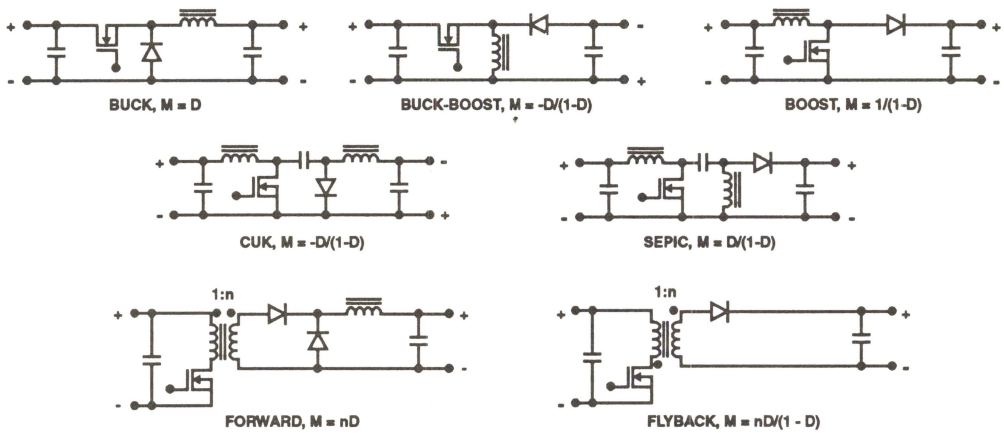


FIGURE 1. CONVERTER CIRCUITS, $M = V_O/V_I$

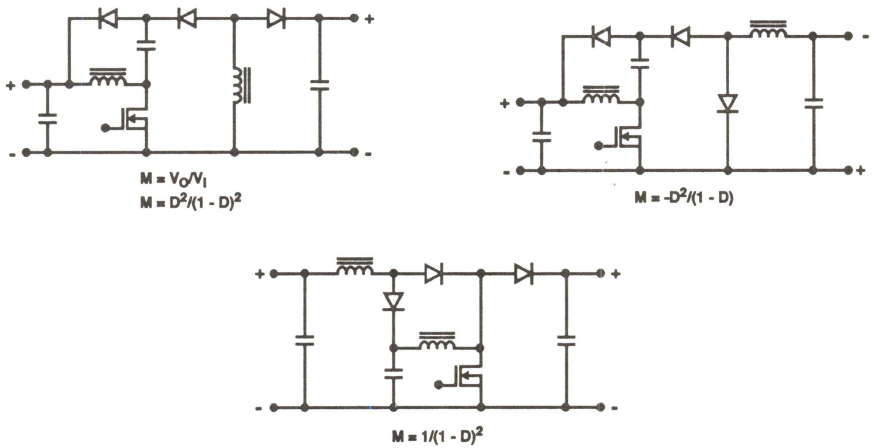


FIGURE 2. QUADRATIC CONVERTERS

around these problems is to modify the circuit such that it exploits the parasitic elements as part of normal operation. A boost version of a zero voltage switching quasi-resonant converter (ZVS-QRC) is shown in Figure 3. This is a typical example of this class of circuit. Many others exist [6, 7, 8, 9] and most switchmode topologies can be implemented as ZVS-QRC. This circuit operates quasi-resonant; i.e. during a portion of the switching cycle the waveforms are sinusoidal like a resonant converter and during other portions of the switching cycle the waveforms are essentially straight line segments like a non-resonant switchmode converter.

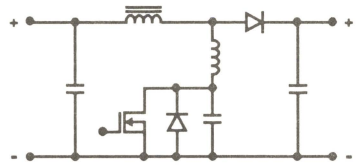
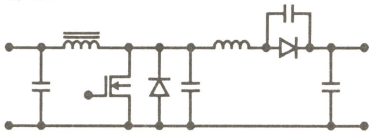


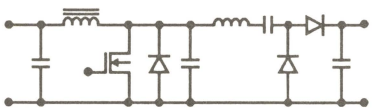
FIGURE 3. ZVS-QRC BOOST CONVERTER

The primary advantage of this topology is that the switch turns on and off while the voltage across the switch is zero. This translates to essentially zero switching loss and very low stress during switching transitions. The inherent junction capacitance of the switch is utilized as an active component as well as the series package inductance. This enables the switch to operate efficiently at very high frequencies (10MHz+). A price has to be paid for this performance. The converter can only be controlled by varying frequencies (fs). This is a relatively simple control scheme to implement but sometimes leads to EMI problems, particularly if the range of variation of fs is large. If fixed frequency operation is desired another switch must be added to the circuit. An additional disadvantage is that the switch voltage will be much higher than the input or output voltages. Peak switch voltages of 3 to 5 times the input voltage are typical. There are also restrictions on the acceptable load ranges and the switching frequency range can be large under some conditions.

Some improvement in performance can be obtained by operating the converter in a ZVS-multiresonant mode [10, 11]. Two examples are given in Figure 4. In this topology both the switch and the diode operate with low switching stress. This circuit does however, still have many of the disadvantages of the ZVS-QRC.



ZVS-MRC BOOST



CLASS E

FIGURE 4. MULTI-RESONANT CONVERTERS

Because of their disadvantages this family of converters is not usually employed until the operating frequency is so high that more conventional approaches cannot be used.

Many resonant converters can also be used for very high fs but in general they require more than a single switch and are not normally advantageous for low power levels (<100W).

Using Switchmode Circuits at MHz Frequencies

One of the primary motivations for developing resonant and quasi-resonant topologies has been to overcome the problems associated with switchmode converters when they are operated with high fs. While these approaches have been helpful, in general some price must be paid. This often takes the form of higher conduction losses, higher voltage stress, more numerous and larger components, loss of PWM control and limited load and input voltage ranges.

If the problems associated with high frequency operation can be overcome then switchmode circuits are advantageous. The limitations of switchmode converters for MHz operation stem primary from the difficulty of switching rapidly enough and the effect of parasitic components on the circuit behavior. An example of the parasitics present in a typical power stage is shown in Figure 5.

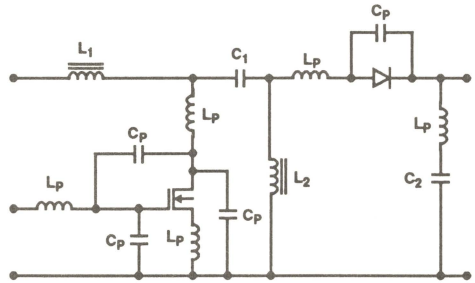


FIGURE 5. TYPICAL PARASITIC COMPONENTS

MOSFETs are inherently fast switching devices. If the input capacitance can be charged quickly enough they are capable of sub-nanosecond switching. However, in discrete or even hybrid circuits, the parasitic inductance in the gate and source connections limits the charge rate, increasing the switching transition time. The parasitic inductance and capacitance associated with the drain circuit causes voltage and current ringing which can over stress the switch and associated components, increase the switching loss and create VHF radiated and conducted EMI.

For power levels typically used in distributed power systems, a power IC manufactured with the Harris PASIC [12] (Power Applications Specific Integrated Circuit) process is an excellent way to minimize the parasitic elements that limit circuit performance and increase the level of integration. Other advantages of the PASIC technology is that the IC design can provide on-chip temperature monitoring and high speed, on-chip, current sensing. Moreover, on chip gate drivers help reduce and confine gate drive current and parasitic capacitance associated with external power transistors. Because the switch and its drive circuitry can be integrated

onto a very small area, nanosecond switching times are readily achieved. For volume production the IC has the advantage of much smaller size and lower cost than discrete equivalents.

Some external power components will still be needed, but they can be arranged to minimize parasitics. In the SEPIC converter shown in Figure 5, C_1 would be a chip ceramic capacitor and D_1 would be a surface mounted Schottky diode. Both of these components would be placed immediately adjacent to the IC. Efficient and economical 1MHz designs using this concept are presently in volume production.

It is possible to have floating or "high side" switches in the PASIC process for use with the buck topology shown in Figure 1. However, by using the SEPIC topology, the power DMOS transistor source may be returned to ground. This results in much simplified and efficient gate driving circuits. Moreover, a shorted or open power transistor is not detrimental to the load in the SEPIC topology. Because of the load coupling capacitor and the switch being returned to ground in the SEPIC topology, a shorted or open power transistor will not place the full high voltage input voltage on the load as in the buck topology. Besides the SEPIC topology, there is a host of topologies that may be implemented with a grounded source device, among them is the boost, forward, flyback, Cuk, and quadratic topologies.

The SEPIC Converter

The boost, Cuk, flyback and forward converters are well known to power supply designers and information on their design is widely available [13, 14 and 15]. The SEPIC topology has however, not been widely used. The following information is provided to familiarize designers with this circuit and its characteristics.

The name SEPIC is an acronym for Single-Ended Primary Inductance Converter. The circuit was first developed at AT&T Bell laboratories [16] in the mid 1970s. The intent of the developers was to create a new topology with properties not available in contemporary topologies. Of particular interest is the ability to buck or boost the input voltage without inverting voltage polarity.

A typical SEPIC circuit is shown in Figure 6A. This circuit has three dynamic energy storage elements, L_1, L_2 and C_1. The behavior of any switchmode circuit is strongly dependent on the continuity of the currents in the inductors and the voltages on the capacitors. A number of different operating modes are possible depending whether the inductor currents and capacitor voltages are continuous or discontinuous. As shown in Table 2, there are six possible inductor current operating modes. The -C entries are for conditions where one inductor current goes to zero before the other causing that inductor current to reverse direction. The inductor current is still continuous but the circuit behavior is different. The -D entries are for conditions where one inductor current goes negative and then a state exists where the two inductor currents are constant. The modes shown in Table 2 assume the voltage on C_1 is constant (small ripple). An additional set of modes is possible if the voltage on C_1 is discontinuous.

While all modes are possible, the usual operating mode is to have the voltage on C_1 continuous and either both L_1 and L_2 in continuous conduction or both L_1 and L_2 in discontinuous conduction. These two modes will be the only ones for which the circuit behavior will be derived in this applications note and will be referred to as the CCM and DCM modes, respectively. There is a brief discussion of four other modes which may be encountered.

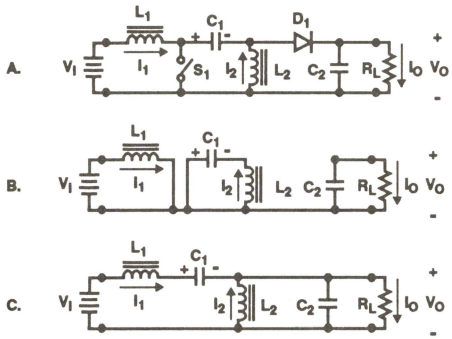


FIGURE 6. SEPIC CONVERTER

Table 2. SEPIC Operating Modes (C_1 and C_2 have small ripple)

INDUCTOR	CONDUCTION MODE					
L_1	D	C	C	-C	C	-D
L_2	D	C	-C	C	-D	C

CCM Circuit Operation

For this analysis it is assumed that both C_1 and C_2 are sufficiently large that the voltage ripple across them is small. By tracing the DC path from V_I through C_1, L_1, L_2 and back to V_I we see that $V_{C1} = V_I$. By inspection it can be seen that $V_{C2} = V_O$.

When S_1 is on, D_1 is off and when S_1 is off, D_1 is on. This means there are two circuit states during each switching cycle. The two states are shown in Figures 6B and 6C.

When S_1 is closed, L_1 is directly across V_I and I_1 is increasing. Energy is being stored in L_1. C_1 is connected across L_2 and I_2 is increasing. The energy in C_1 is being transferred to L_2. I_O is being maintained by C_2.

When S_1 is opened, the energy in L_1 is discharged into C_1 and C_2. The energy in L_2 is discharged into C_2. For CCM operation some energy remains in L_1 and L_2 (I_1 and $I_2 \neq 0$). At the end of the switching sequence S_1 is again closed and the cycle repeated.

To make the following discussion easier to follow, the details of the circuit analysis have been omitted. The equation derivations can be found in the appendix.

The ratio of the output voltage to the input voltage and the duty cycle are defined as:

$$M \equiv \frac{V_O}{V_I} \qquad \text{Equation 1}$$

$$D \equiv \frac{t_{ON}}{T} \qquad \text{Equation 2}$$

Where t_{ON} is the on time of S_1 and T = 1/fs, the switching period.

D as a function of M is:

$$D = \frac{M}{M+1} \qquad \text{Equation 3}$$

And M as a function of D is:

$$M = \frac{D}{1-D} \qquad \text{Equation 4}$$

A graph of Equation 4 is given in Figure 7 with comparisons to the buck, boost, Cuk and buck-boost converters. The large signal input-to-output voltage ratio for the SEPIC is identical to the Cuk and buck boost circuits except that there is no polarity inversion. V_O may be either less than or greater than V_I depending on D.

TABLE 3. SEPIC CCM VOLTAGES AND CURRENTS

M	V_O/V_I
D	$\frac{M}{M+1}$
M	$\frac{D}{1-D}$
$(I_1)_{RMS}$	MI_O
V_{L1}	V_O, M ≥ 1 and V_O/M, M ≤ 1
V_{S1}	$\left[\frac{M+1}{M}\right]V_O = V_O + V_I$
$(I_{S1})_{AVG}$	MI_O
$(I_{S1})_{RMS}$	$I_O\sqrt{M^2+M}$
V_{C1}	$V_O/M = V_I$
$(I_{C1})_{RMS}$	$I_O\sqrt{M}$
V_{L2}	V_O, M ≥ 1 and $V_O/M = V_I$, M ≤ 1
$(I_2)_{RMS}$	I_O
V_{D1}	$\left[\frac{M+1}{M}\right]V_O = V_O + V_I$
$(I_{D1})_{AVG}$	I_O
$(I_{D1})_{RMS}$	$I_O\sqrt{M+1}$
V_{C2}	V_O
$(I_{C2})_{RMS}$	$I_O\sqrt{M}$

Expressions for the voltages and currents in other circuit elements as a function of M, V_O and I_O are given in Table 3. Note that the expressions for the peak value for V_{L1} and V_{L2} depend on whether M > 1 or M < 1. The expressions in Table 3 assume that L_1 and L_2 are large with only small current ripple. For the case where the inductors are operating close the CCM-DCM boundary, the current waveforms will be triangular rather than rectangular and the RMS values will be approximately 15% higher.

The boundary between CCM and DCM modes will depend on several variables. For a given load resistance ($R_L=V_O/I_O$), fs and M, the values for the critical inductances of L_1 and L_2 are:

$$L_{1C} = \left[\frac{1}{2fs\,(M^2+M)}\right]R_L \qquad \text{Equation 5}$$

$$L_{2C} = \left[\frac{1}{2fs\,(M+1)}\right]R_L \qquad \text{Equation 6}$$

If the inductor values are higher than critical, then the converter will operate in CCM. If the values for the inductors are less than critical then the converter will operate in DCM.

The ratio of L_{2C} to L_{1C} is:

$$\frac{L_{2C}}{L_{1C}} = M \qquad \text{Equation 7}$$

A very important point here is that the currents in L_1 and L_2 go to zero simultaneously only if L_2/L_1 = M! If V_O is held constant and V_I is varied then the CCM-DCM transition will occur at some other point and will involve an intermediate mode.

In distributed power systems V_I is the DC bus and is normally relatively well regulated so the M varies only over a small range. In that type of an application, a smooth transition from both inductors in CCM to both in DCM will be possible. If L_2/L_1 does not equal M then the circuit behavior will be quite different.

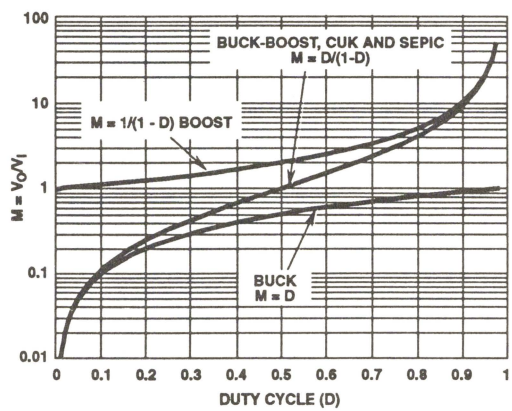


FIGURE 7. VOLTAGE TRANSFER AS FUNCTION OF DUTY CYCLE FOR VARIOUS TOPOLOGIES

If I_2 reaches zero before I_1, D_1 will still be conducting because of the current in L_1. This means there will be a voltage across L_2 which reverses I_2. This leads to two additional operating modes. Current waveforms for the case where $I_1(T) > -I_2(T)$ are shown in Figure 8. This mode corresponds to the C, -C state in Table 2. Figure 9 shows the waveforms for the case where $I_1 = -I_2$ at $t < T$. In this mode, when $I_1 = -I_2$, D_1 drops out of conduction and a new operating state is introduced as shown. During this state (t_2 to T) the inductor currents are constant (ideally) because the voltage across C_1 cancels the input voltage. The conduction mode shown in Figure 8 is a continuous conduction mode but different from the continuous conduction mode where the current is unidirectional in both inductors. In the mode shown in Figure 9 the inductor currents are continuous but because of the period of time where di/dt = 0 (t_2 to T) the circuit will operate in a discontinuous mode. This mode corresponds to the C, -D mode in Table 2.

Both of these modes, C, -C and C, -D, have different characteristics from those mentioned in the previous discussion of continuous mode operation. The conditions where the current in L_1 reaches zero before the current in L_2 will be similar.

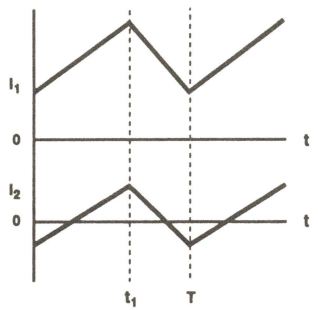


FIGURE 8. INDUCTOR CURRENTS FOR $I_1 > -I_2$ AT $t = T$

CCM Circuit Example

The following numerical example is provided to give a feeling for the component sizes and stresses in a typical application for the SEPIC converter.

Let:

$V_I = 35V$
$V_O = 12V$
$P_O = 50W$
fs = 1MHz

From this it can be seen that:

$I_O = 4.2A$
$R_L = 2.88\Omega$
M = 0.34

From Equations 5 and 6:

$L_{1C} = 3.2\mu H$
$L_{2C} = 1.1\mu H$

To operate well within CCM and minimize the RMS currents let:

$L_1 = 5\mu H$
$L_2 = 1.7\mu H$

These inductors could be a single layer, wound on small powdered iron or NiZn ferrite cores. From the equations in Table 3:

$V_{S1} = 47V$
$(I_{S1})_{RMS} = 2.8A$ RMS

A MOSFET with $BV_{DSS} = 60V$ would be appropriate for S_1.

$V_{D1} = 47V$
$(I_{D1})_{AVG} = 4.2A$

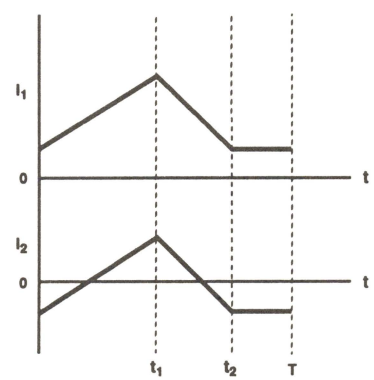
A 60V Schottky diode could be used for D_1.

$V_{C1} = 35V$
$(I_{C1})_{RMS} = 2.4A$ RMS

For C_1 a 50V, 0.47 to 1µF, multilayer, ceramic chip capacitor would be appropriate.

$V_{C2} = 12V$
$(I_{C2})_{RMS} = 2.4A$ RMS

For C_2 a 25V, 1µF, ceramic chip capacitor would be appropriate.



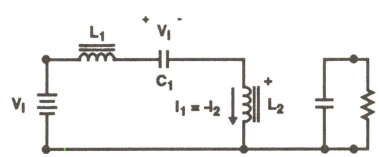


FIGURE 9. INDUCTOR CURRENTS AT $I_1 = I_2$ FOR $t < T$

DCM Circuit Operation

The following discussion assumes that $L_2/L_1 = M$ and that both inductors go into discontinuous conduction simultaneously.

Operation in the DCM mode adds an additional circuit state as shown in Figure 10. At t = 0, the point at which S_1 is turned on, I_1 and $I_2 = 0$. The current in both inductors will rise until S_1 turns off (Figure 10A). At that point the energy in the inductors is discharged into the output (Figure 10B). When the inductor currents reach zero, D_1 stops conducting and the final state is assumed (Figure 10C). No current flows in the inductors because the voltage on C_1 cancels V_I.

The expressions for D and M are:

$$D = \sqrt{2\tau_L\left[\frac{M^3}{M+1}\right]} \qquad \text{Equation 8}$$

Where:

$$\tau_L = \frac{fsL_1}{R_L} \qquad \text{Equation 9}$$

Equation 8 is only valid for D < 1. This sets an upper limit on τ_L of:

$$(\tau_L)_{MAX} = \frac{M+1}{2M^3} \qquad \text{Equation 10}$$

Values of τ_L greater than this limit mean that the converter is operating in CCM for the particular value of M.

Graphs of Equation 8 is given in Figures 11 and 12. These graphs illustrate the effect of varying load on the output voltage for M > 1 and M < 1.

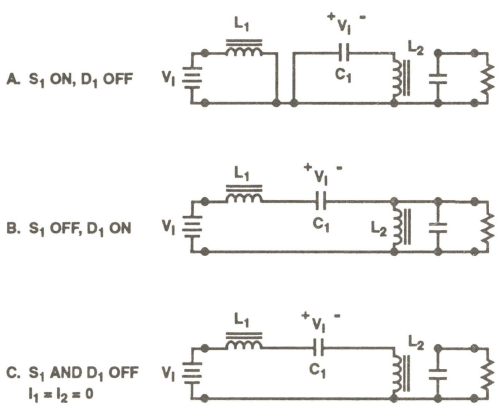


FIGURE 10. SEPIC DCM CIRCUIT STATES $L_2/L_1 = M$

Coupled Inductor Operation

Referring to Figure 6, when S_1 is closed, the voltage across both L_1 and L_2 is equal to V_I. From Figure 6B it can be seen that for the remainder of the switching cycle the voltage across L_1 and L_2 is equal to V_O. Because these two voltages are equal and in phase, L_1 and L_2 may be integrated into a single magnetic structure with only one magnetic path, this is referred to as a coupled inductor. A coupled inductor version of the SEPIC topology [14] is shown in Figure 13. This topology has several advantages. The leakage inductance of the coupled inductor can be arranged to effect zero current ripple on the input with finite value of L. Because the turns ratio between the windings is 1:1, there cannot be two different values for L_1 and L_2. This does not lead to multiple modes however. Because they are wound on a common core, both windings are either conducting or not depending on whether there is energy in the core or not. The circuit operates either CCM or DCM.

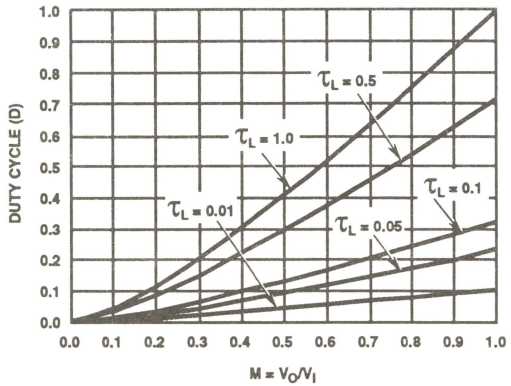


FIGURE 11. SEPIC CONVERTER IN THE DCM MODE FOR A FAMILY OF LOAD PARAMETERS, τ, WITH THE VOLTAGE TRANSFER RATIO, M < 1

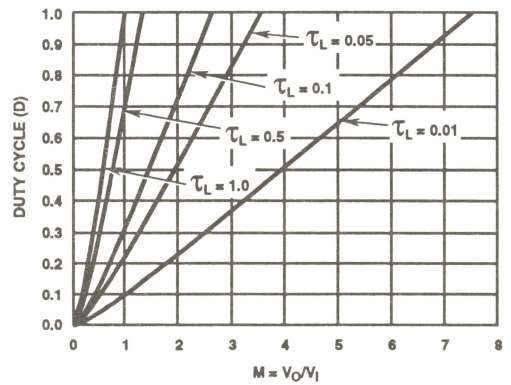


FIGURE 12. SEPIC CONVERTER IN THE DCM MODE FOR A FAMILY OF LOAD PARAMETERS, τ, WITH THE VOLTAGE TRANSFER RATIO, M < 8

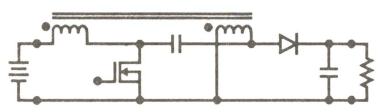


FIGURE 13. COUPLED INDUCTOR SEPIC

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Appendix

SEPIC Equation Derivations for CCM and DCM Operation CCM Operation

The following calculations are referenced to Figure 6.

For C_1 and C_2 large: $V_{C1} = V_I$ and $V_{C2} = V_O$

When S_1 is closed: $V_{L1} = V_{L2} = V_I$

When S_1 is open: $V_{L1} = V_{L2} = -V_O$

By conservation of flux in the inductors:

$$V_I t_{ON} = V_O (T - t_{ON}) \quad \text{(A1)}$$

For $D = t_{ON}/T$ and $M = V_O/V_I$ Equation A1 reduces to:

$$M = D/(1 - D) \quad \text{(A2)}$$

Equation A2 can be inverted:

$$D = M/(M + 1) \quad \text{(A3)}$$

Assuming that L_1 and L_2 are sufficiently large that the current ripple is small and substituting A3

$$I_O = (I_1 + I_2)(1 - D) = (I_1 + I_2)(1/(M + 1)) \quad \text{(A4)}$$

For Power In = Power Out: (A5)

$$V_I I_1 = V_O I_O,\ M = V_O/V_I = I_1/I_O$$

Combining Equations A4 and A5:

$$I_2 = I_O \quad \text{(A6)}$$

S_1 Voltage and Current

For S_1 open:

$$V_{S1} = V_{C1} + V_O = V_I + V_O \quad \text{(A7)}$$

Restating in terms of M and V_O:

$$V_{S1} = (1 + 1/M)V_O \quad \text{(A8)}$$

For S_1 closed:

$$(I_{S1})_{RMS} = (I_1 + I_2)\sqrt{D} \quad \text{(A9)}$$

Which reduces to:

$$(I_{S1})_{RMS} = I_O\sqrt{(M + M^2)} \quad \text{(A10)}$$

D1 Voltage and Current

By inspection:

$$(I_{D1})_{AVG} = I_O \quad \text{(A11)}$$

When S_1 is closed:

$$V_{D1} = V_I + V_O = (1 + 1/M)V_O \quad \text{(A12)}$$

Note the switch and diode have the same peak voltage.

Inductor Currents

$$(I_1)_{RMS} = I_1 = MI_O \quad \text{(A13)}$$

$$(I_2)_{RMS} = I_O \quad \text{(A14)}$$

This assumes small current ripple. If smaller inductors are used such that the inductor currents are nearly triangular (near the DCM-CCM boundary) the RMS current values will be approximately 15% higher.

Capacitor Currents

$$(I_{C1})_{RMS} = \sqrt{I_1^2(1-D)+I_2^2} \quad \text{(A15)}$$

Which reduces to: $(I_{C1})_{RMS} = I_O\sqrt{M}$ (A16)

$$(I_{C2})_{RMS} = \sqrt{I_O^2 D + (I_1 + I_2 - I_O)^2} \quad \text{(A17)}$$

Which reduces to: $(I_{C2})_{RMS} = I_O\sqrt{M}$ (A18)

Values for the Critical Inductances of L_1 and L_2

For a given current, the critical inductance is the value for the inductor that allows the current to just reach zero at the end of the switching cycle. This is a special case of CCM.

L_1 Critical

The input current will be triangular. I_{1P} = peak value of the current:

$I_{1P} = 2I_{1AVG} = 2MI_O$ (A19)

$I_{1P} = V_I t_{ON}/L1$ (A20)

$t_{ON} = DT$ (A21)

$fs = 1/T$ (A22)

Combining Equations A19 - A22:

$L_{1C} = [1/2fsM(M + 1)]R_L$ (A23)

A similar calculation for L_2 yields:

$L_{2C} = R_L/(2fs(M + 1))$ (A24)

DCM Analysis

For this analysis it will be assumed that:

$L_{2O}/L_{1C} = M$ (A25)

This means I_1 and I_2 go to zero simultaneously. The circuit states shown in Figure 10 will be used for this analysis.

$t_1 = t_{ON}$ = on time of S_1

t_2 = the current fall time in the inductors

From conservation of flux in L_1 and L_2:

$V_I t_1 = V_O t_2$ (A26)

From conservation of charge in C_1 (A27)

$I_{1AVG} t_2 = I_{2AVG} t_1$

From conservation of power: (A28)

$V_I I_{1AVG} = V_O I_O$

Derivation of Expressions for M and D

$I_{1P} = V_I t_1/L_1$ (A29)

$$I_{1AVG} = I_{1P}\left[\frac{t_1 + t_2}{2T}\right] \quad \text{(A30)}$$

Combining Equation A27 through A30:

$$D = \sqrt{\left[\frac{2fsL_1}{R_L}\right]\left[\frac{M^3}{M+1}\right]} \quad \text{(A31)}$$

A SPICE-2 SUBCIRCUIT REPRESENTATION FOR POWER MOSFETs, USING EMPIRICAL METHODS

Author: C. Frank Wheatley Jr., and Harold R. Ronan, Jr.

Abstract

An accurate power-MOSFET model is not widely available for CAD circuit simulation. This work provides a subcircuit model which is compatible with SPICE-2 software and MOSFET terminal measurements. SPICE-2 is the circuit simulation package of choice for this work because of its universal availability, despite its inherent limitations. These limitations are circumvented through circuit means.

This effort models power-MOSFET terminal behavior consistent with SPICE-2 limitations; hence it will differ from the physical model as suggested by Wheatley, et al[1], Ronan et al[2] and others. We feel we have advanced prior efforts[3] particularly in areas of third-quadrant operations, avalanche-mode simulation, switching waveforms and diode recovery waveforms.

Discussion

The subcircuit shown in Figure 1 is described in Table 1. All passive circuit elements are constants. The very-high-gain JFET is used to simulate the dual-slope drain voltage vs time switching curve common to the power MOSFET.[1,2]

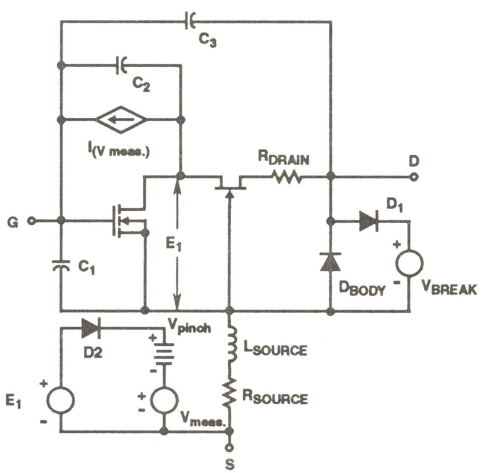


FIGURE 1. SPICE-2 SUBCIRCUIT FOR POWER MOSFET SIMULATION.

NOTE: If the JFET source voltage, E_1, is very low relative to its V_{PINCH} voltage, the JFET is in a highly conductive state, tightly coupling C_2 to the JFET drain. However, as the voltage E_1 approaches V_{PINCH}, the JFET operates in a constant-current mode, thereby permitting a much faster drain slew rate, which is determined primarily by C_3.

If E_1 exceeds V_{PINCH}, errors will exist in the turn-on waveforms. The C_2 discharge current-controlled current source remedies this situation in conjunction with the subcircuit containing D_2. The D_2 ideality factor was set at 0.03 to assure that E_1 minus V_{PINCH} does not exceed several millivolts.

The body diode cannot be properly modeled by the JFET gate-drain diode, hence D_{BODY}. Conditions of Table 1 assure that most third-quadrant current flow is via D_{BODY}. Avalanche breakdown is more accurately modeled by the clamp circuit containing D_1.

Table 1 in combination with Figures 2, 3, 4 and 5 provides the required empirical inputs. Table 2 lists the preferred algorithm for parameter extraction.

TABLE 1. EMPIRICAL INPUTS

MOSFET	Enhancement mode; W = L = 1µm; K_P (Figure 2); V_{TO} (Figure 2); C's = 0; I_{DSO} = IE -12
JFET	Depletion mode; areas factor = 1; B = 100K_P (Figure 2); V_{TO} = V_{PINCH} (Figure 5); C's = diode lifetime = R_{SERIES} = 0; diode ideality factor = 1.0, I_{DSO} = IE -20
BODY DIODE	I_S from Figure 4; Ideality Factor = 1.0; R from Figure 4 (must be very much greater than R_D); C (from C_{OSS}); lifetime = best fit to T_{RR}
D_1	I_S = arbitrary; C = lifetime = 0; ideality factor = best low-current fit; R = best high-current fit
D_2	I_S = 1E -8; C = lifetime = R = 0; ideality factor = 0.03
R_S	Figure 2.
R_{DRAIN}	Figure 3.
L_S	Approximately (5L) ln (4 L/d) nH; L and d are source wire inches.
V_{PINCH}	V_{TO} of JFET.
V_{BRK}	Avalanche voltage.
C_1	From Figure 5.
C_2	Maximum from Figure 5.
C_3	Minimum from Figure 5.

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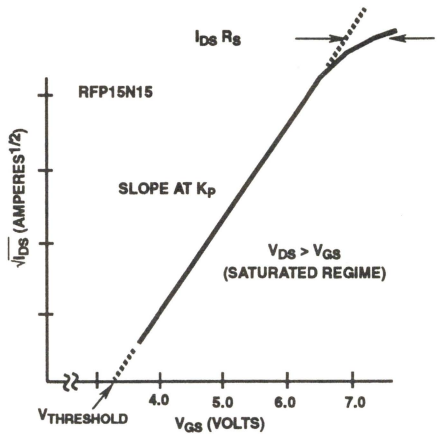


FIGURE 2. SQUARE ROOT OF DRAIN CURRENT vs GATE VOLTAGE DEFINES $V_{THRESHOLD}$, K_P, AND R_S.

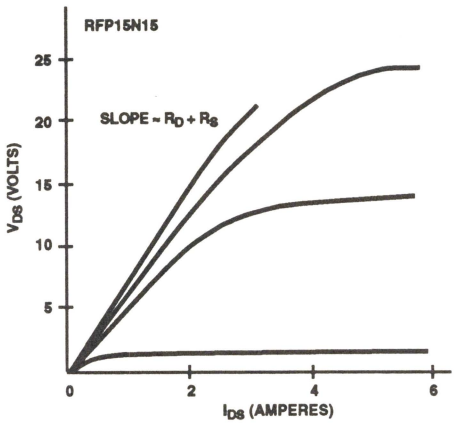


FIGURE 3. DRAIN CURRENT vs DRAIN VOLTAGE WITH CONSTANT GATE VOLTAGE DEFINES "ON" RESISTANCE.

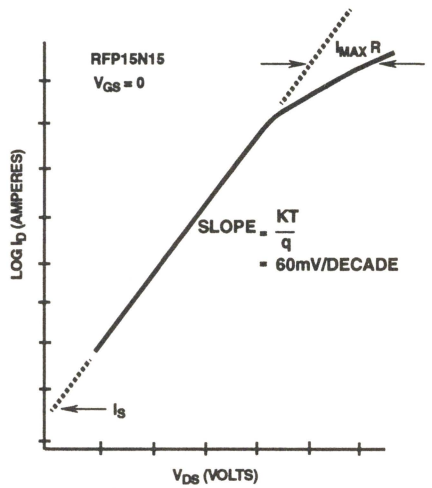


FIGURE 4. THIRD-QUADRANT OPERATION DEFINES I_S AND R OF DIODE D_{BODY}.

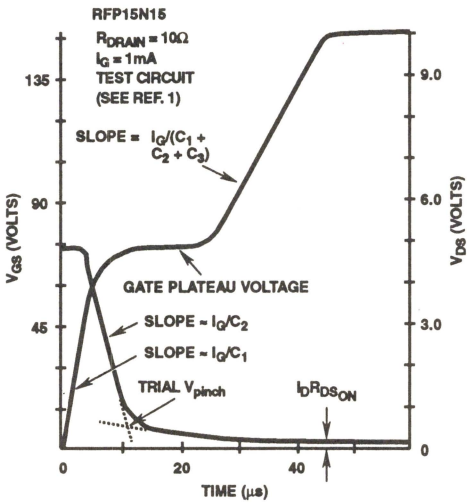


FIGURE 5. DRAIN AND GATE VOLTAGE vs TIME DETERMINE C_1, C_2, C_3 AND V_{PINCH}.

TABLE 2. PREFERRED ALGORITHM FOR PARAMETER EXTRACTION

1. Determine K_P of lateral MOS
2. Determine V_{TH} of lateral MOS
3. Determine C_1
4. Determine $C_1 + C_2 + C_3$
5. Determine R_{DS}
6. Assign B of JFET = 100 x K_P of lateral MOS
7. Use trial V_{PINCH}
8. Use C_2 (Maximum), C_3 (Minumum) are curve-fit C's
9. Adjust V_{PINCH} to fix gate voltage plateau

Results

Figure 6 and Figure 7 compare measured static data to calculated transfer curves and output curves. Calculated static-output curves are shown in Figure 8 and Figure 9 for third-quadrant range, including avalanche.

Calculated switching data is compared to measured switching curves[1,2] in Figure 10 and Figure 11. Calculated body-diode recovery curves are shown in Figure 12.

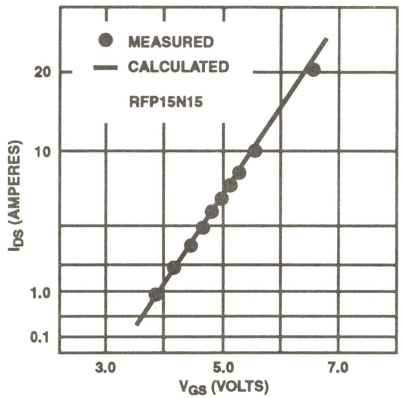


FIGURE 6. DRAIN CURRENT vs GATE VOLTAGE (NOTE SQUARE ROOT SCALE) - MEASURED CURVE vs CALCULATED POINTS.

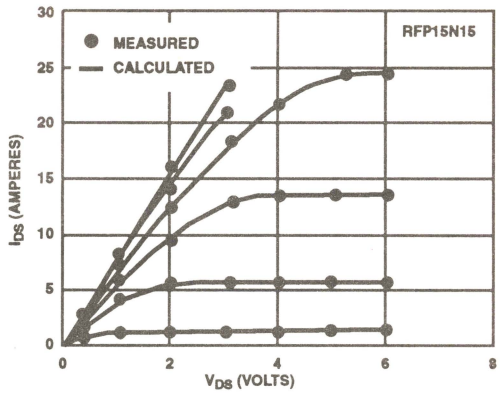


FIGURE 7. DRAIN CURRENT vs DRAIN VOLTAGE FOR CONSTANT VALUES OF GATE VOLTAGE - MEASURED CURVES vs CALCULATED POINTS.

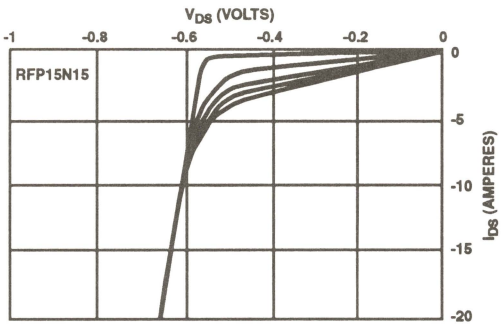


FIGURE 8. THIRD-QUADRANT DRAIN CURRENT vs DRAIN VOLTAGE WITH CONSTANT POSITIVE GATE VOLTAGE (CALCULATED).

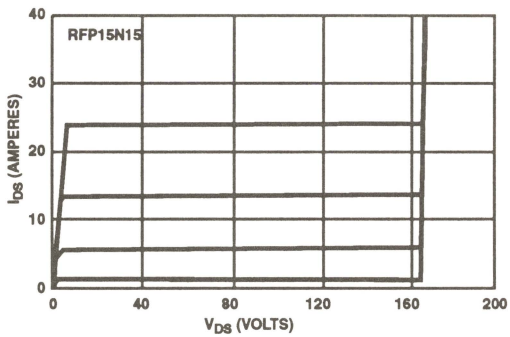


FIGURE 9. FIRST-QUADRANT DRAIN CURRENT vs DRAIN VOLTAGE, V_{GS} = CONSTANT. NOTE AVALANCHE BREAKDOWN (CALCULATED).

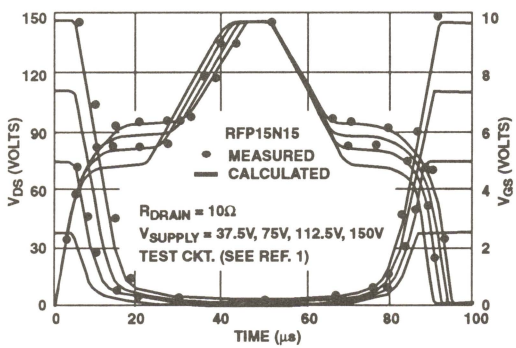


FIGURE 10. DRAIN AND GATE VOLTAGE vsTIME FOR CONSTANT GATE CIRCUIT - MEASURED CURVES vs CALCULATED POINTS.

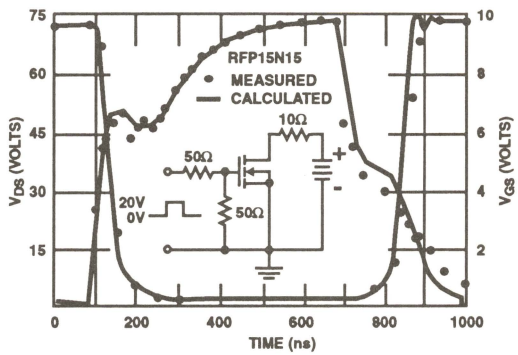


FIGURE 11. DRAIN AND GATE VOLTAGE vs TIME FOR STANDARD SWITCHING CIRCUIT - MEASURED CURVES vs CALCULATED POINTS.

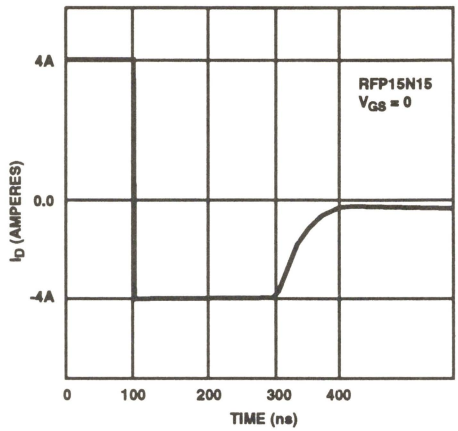


FIGURE 12. THIRD-QUADRANT DIODE-RECOVERY-TIM CURVE (CALCULATED).

Conclusion

An equivalent-circuit model for power-MOSFETs, that is suitable for use with the SPICE CAD program, has been demonstrated. The model is compatible with all versions of SPICE presently available without modification to the program's internal code. The model addresses static and dynamic behavior of first and third-quadrant operation, including avalanche breakdown, and is empirical in nature; all necessary input parameters may be inferred from data sheets or simple terminal measurements.

Excellent agreement has been obtained between measured and simulated results.

References

1. Wheatley Jr., C. F. and Ronan Jr., H. R., "Switching Waveforms of the L2FET: A 5-Volt Gate-Drive Power MOSFET," Power Electronic Specialists Conference Record, June 1984, p. 238

2. Ronan Jr., H. R. and Wheatley Jr., C. F., "Power MOSFET Switching Waveforms: A New Insight," Proceedings of Powercon II, April 1984, p. C-3

3. Nienhaus, H. A., Bowers, J. C., and Herren Jr., P. C., "A High Power MOSFET Computer Model," Power Conversion International, January 1982, p 65

No. AN9212.1 April 1994

HIP5060 FAMILY OF CURRENT MODE CONTROL ICs ENHANCE 1MHz REGULATOR PERFORMANCE

Authors: Robert G. Hodgins and Hal Wittlinger

Abstract

The trend towards distributed power grows and so does the demand for compact, efficient, high frequency, low EMI power supplies[1]. This application note addresses this need by showing an example of how an 80W, 1MHz supply can be implemented with a single, current controlled PWM power IC that contains both a DMOS power transistor and a sophisticated control loop that protects both the IC and the load from a variety of load and fault conditions. SEPIC (Single-Ended Primary Inductance Converter) supply topology is shown. This topology has the advantage of AC coupling the load, with the accrued load protection not usually found in typical "buck" types of topologies. Techniques that are required to obtain high efficiency, high frequency power supplies are discussed. Methods of achieving low EMI at 1MHz are also addressed.

Introduction

Power control is expanding and moving with newer approaches that provide the designer with even more challenges. Distributed power is becoming the answer for systems where local faults will not necessarily shut down an entire system. This application note describes a family of ICs for distributed power. They were jointly designed by IBM and Harris Semiconductor. IBM chose this advanced system approach for their new series of personal computers. This approach is in contrast to the common practice of using just one central power supply in these types of computers. Economies in terms of cooling requirements with the consequential elimination of large cooling fans and associated noise provided added incentive[2]. Figure 1 shows the basic approach to a distributed power system, and Figure 2 shows a schematic diagram of the device in a 5.1V supply application.

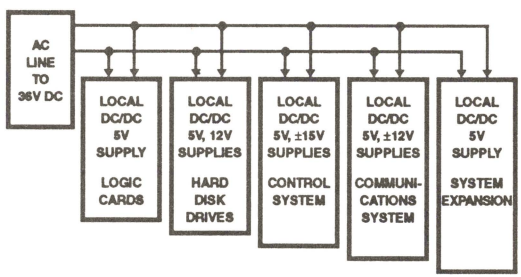


FIGURE 1. AN EXAMPLE OF A DISTRIBUTED POWER SYSTEM

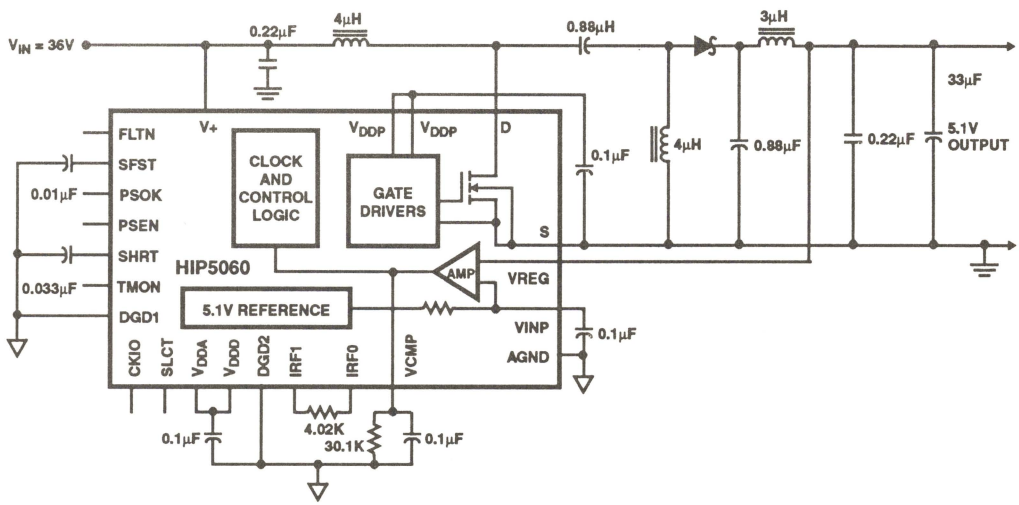


FIGURE 2. SCHEMATIC DIAGRAM OF THE HIP5060 IN A 5.1V SUPPLY

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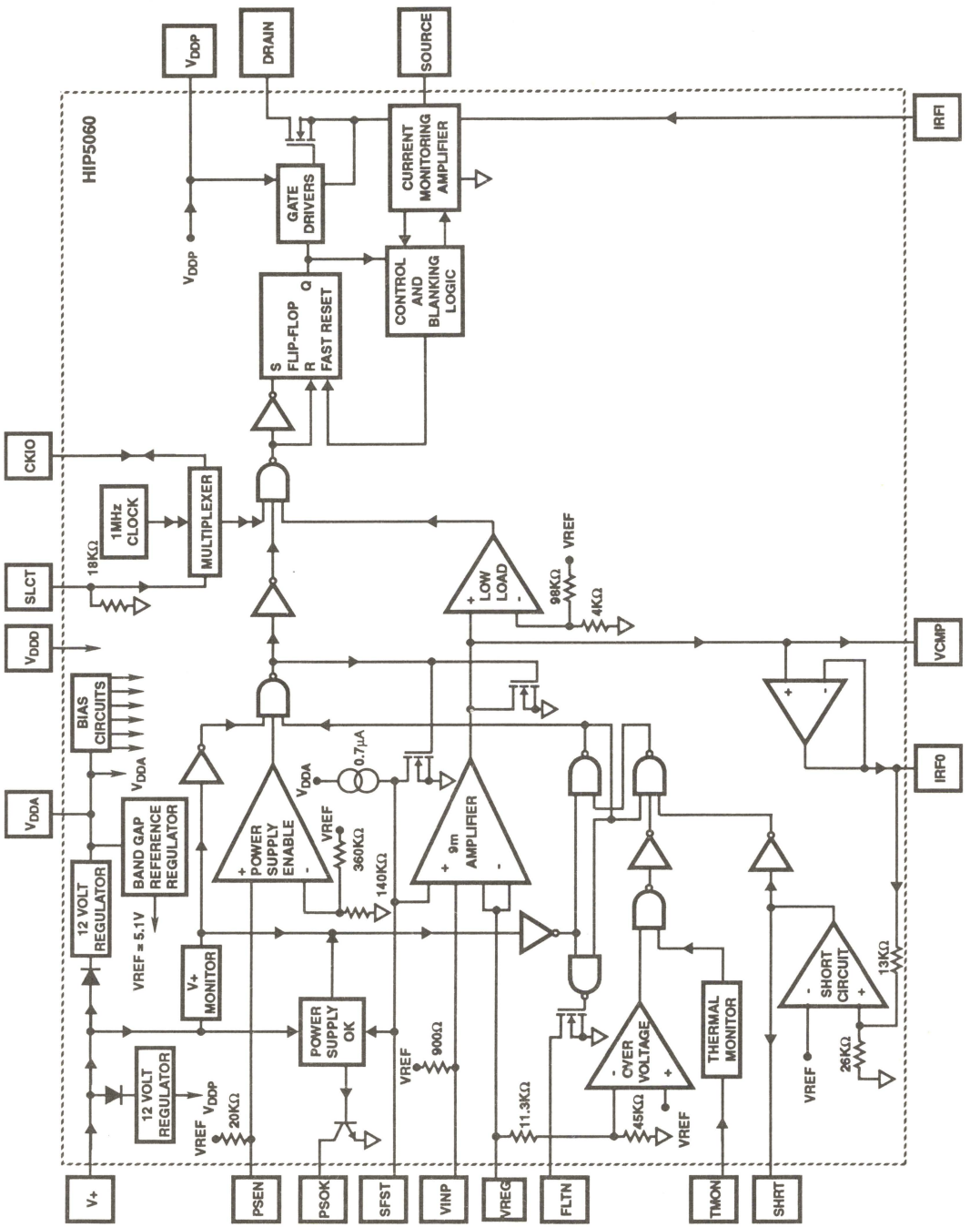


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM OF THE HIP5060, 1MHz CURRENT CONTROLLER REGULATOR IC

Input voltage comes from a 36V supply which can range from 22V to 45V, depending upon line and load conditions. A SEPIC topology[3 & 4] was chosen because it lends itself to the power DMOS transistor available in the PASIC process [5 & 6]. Moreover, this topology also affords excellent load protection. Because of AC coupling to the load, a faulted IC will not place full input bus voltage on the load as in the case of most "buck" configurations.

AC coupling suggests that this configuration is also suitable for stacking of power supplies, or providing a voltage at another level, such as a 7V supply added to or stacked on to a 5V supply to provide a 12V output. Lower power outputs may be obtained from the two inductors used in the SEPIC configuration. This is very convenient for generating negative bias supplies from the positive supply. Secondary outputs, however, cannot have feedback control for precise regulation. Making the second inductor a transformer allows secondary unregulated output with a regulated supply, e.g. +12V at 250mA with a regulated +5.1V at 10A output.

Basic Circuit Operation

Figure 3 shows the functional block diagram of the IC, while Figure 4 shows a functional diagram of the major control loop. A 5.1V reference is provided to the non-inverting input of the transconductance error amplifier via a decoupling resistor that serves two purposes. First it allows the reference input to be AC bypassed and secondly, it provides a means of introducing lower reference voltages such as 3.3V. A MOS-input voltage follower buffers the high output impedance of the 30mA/V transconductance error amplifier. The interface connection between the two stages is brought out for gain and frequency compensation of the regulator loop.

The MOS-input voltage follower buffer provides a low impedance driver for the external current scaling resistor shown on the Basic Control Circuit diagram, Figure 4. Scaling factors within the current monitoring and control circuit are such that there are approximately 4.5A per mA of current through this resistor. This signal is the reference for the current sense amplifier located within the Current Monitoring Amplifier block on the diagram. This reference current level is compared with the current feedback from the DMOS transistor. The DMOS transistor is allowed to remain on until the peak current reaches the level set by the reference current times the current gain. The "ON" time incrementally increases in response to demand for greater load current, then stabilizes at a value determined by input-to-output voltage ratio. To insure accurate sampling after the initial transients due to gate charge and discharge current, a blanking signal is provided that allows only observation of the feedback current pulse. Internal circuitry limits the duty cycle to 50%. A fast reset input to the flip-flop allows 30ns current loop response time that permits rapid tracking of load variations to output current transients.

Protection Circuitry

Performance within the above referenced feedback loop closely follows the typical current controlled switching regulator. There are additional circuits within the IC that monitor the performance of the regulator and feedback loop that protect the IC and the load from unusual load and environmental conditions.

Low Load or Under Current

When the error voltage (VCMP) drops below the Low-Load comparator threshold voltage, indicating a load current condition below the minimum controllable level, switching stops.

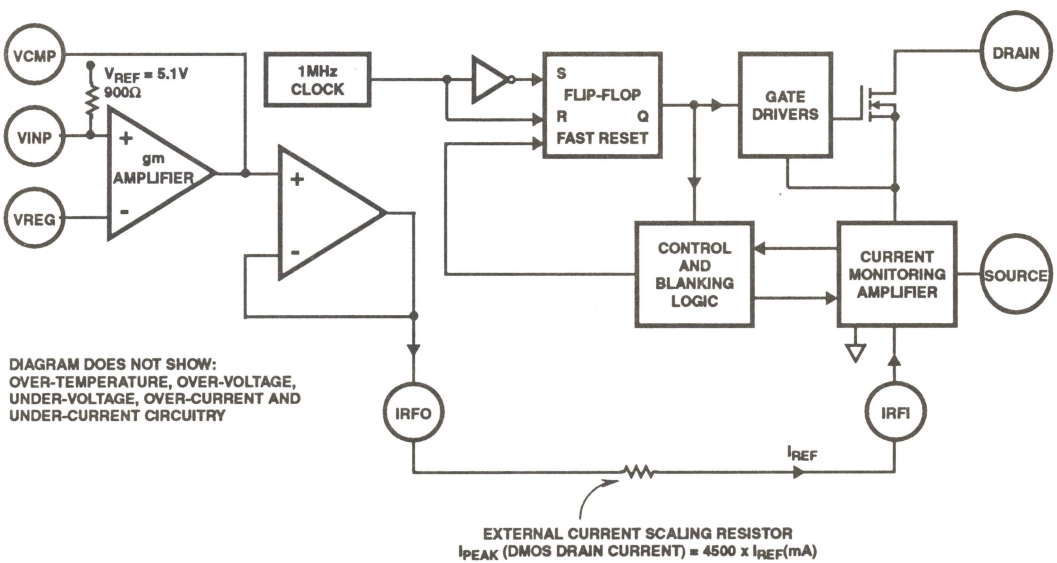


FIGURE 4. BASIC CONTROL CIRCUIT

As the output voltage decays below the reference voltage, 1MHz switching starts again. The resulting burst mode maintains the required regulator voltage under very light load conditions.

Short Circuit Current, Over-Voltage and Over-Temperature

Just as important to satisfactory performance is operation at the other extreme condition - high current. As the output voltage of the error amplifier approaches full scale, implying excessive output current, another threshold detector, labeled Short Circuit on the diagram is activated. While its output is high, an external capacitor connected to the SHRT terminal is charged. When this capacitor voltage exceeds 6V, the fault latch is set and the regulator is shut down. Thus the choice of capacitor value sets the limit on the tolerable over-current duration.

Output over-voltage protection is provided by a circuit that monitors the feedback error voltage to the error amplifier. This is a most important aspect of this regulator in terms of protecting logic circuits from dangerous over-voltage. Output from the Over-Voltage comparator will also trigger the fault latch.

Also coupled to this fault latch is an over-temperature monitoring circuit that triggers the latch when chip temperature rises above a nominal +120°C.

The input supply bus must be lowered below 15V to reset the fault latch. The status of the fault latch is signaled by the open NMOS drain, FLTN terminal. In addition, FLTN is low when the input bus is too low. The FLTN may be wire OR'd to other supplies in systems employing supervisory functions.

Input Voltage Protection

A V+ Monitor circuit controls the input level that initiates the start-up sequence and also the shutdown operation. A rising nominal supply voltage of 25V is needed to initiate the supply start-up sequence and a falling voltage of approximately 15V will cause shutdown.

Soft Start Circuit

During start-up, a current of 0.7μA is available to an external timing capacitor via the SFST terminal. The rising soft start voltage is applied to a third input of the error amplifier to bypass the internal 5.1V reference. This slowly rising reference prevents excessive start-up currents and component stresses.

Power Supply OK

To provide external system monitors and controllers with an indication of the condition of the supply, an output is available via an open collector NPN transistor. This circuit provides a logic signal indicating a valid supply after a time equal to twice the soft start time.

Power Supply Enable

External on-off control of the power supply is provided by the Power Supply Enable comparator through the PSEN terminal. This TTL compatible input is returned to 5.1V through an internal 20KΩ pull-up resistor. Returning this terminal low or to ground will disable the regulator and the clock output.

Clock Control

An internal 1MHz clock is provided on the chip. External clocks may be used to synchronize other switching supplies to the same operating frequency. When the SLCT terminal remains open, an internal 18KΩ resistor returns this input to ground. Under this condition, the clock is available on the CKIO terminal. Returning this input to a logical "1" will then disable the internal clock and allow the introduction of an external clock into the CKIO terminal.

Performance

Figure 5 shows an oscilloscope photograph of power DMOS drain voltage in a 5.1V supply with a 5A load with a 37V input supply bus. NOTE: the rise and fall times of less than 4ns. A complete cycle is shown in Figure 6.

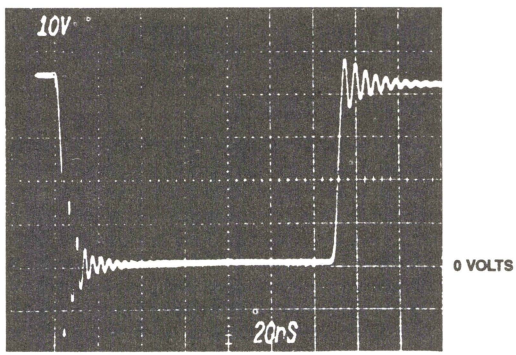


FIGURE 5. DMOS TRANSISTOR DRAIN VOLTAGE DURING CONDUCTION.

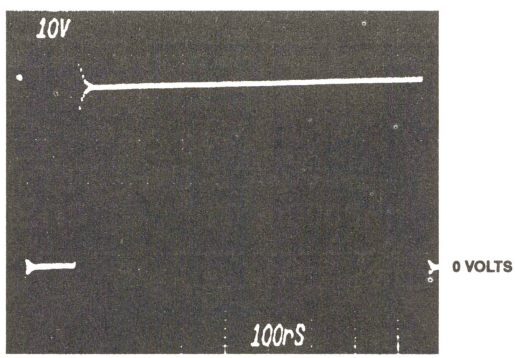


FIGURE 6. DMOS DRAIN VOLTAGE FOR COMPLETE CYCLE.

HIP5062 and HIP5063 Complement the Product Line

Two other ICs are available that complement the product line. Table 1 gives a summary of all three devices currently available. The dual HIP5062 is intended for use in applications such as dual 5V and 12V power supply. Figure 7 shows a block diagram of this device. It should be noted that the clock signal is configured to alternately drive each output

TABLE 1. HIP5060, HIP5062, AND HIP5063 CAPSULE COMPARISON

DEVICE	SINGLE POWER MOSFET	DUAL POWER MOSFETs	POWER MOSFETs (V-I)	ICs OPERATING VOLTAGE	SUPPLY CURRENT AT	VOLTAGE	CURRENT LOOP RESPONSE TIME	MOSFET OUTPUT CURRENT GAIN	ERROR AMPLIFIER TRANSCONDUCTANCE	REFERENCE VOLTAGE	THERMO-TRIP TEMPERATURE	INTERNAL CLOCK FREQUENCY
HIP5060	√		60V, 10A	27V to 45V	19.5mA	36V	30ns	4.5A/mA	30mS	5.1V	120°C	1MHz or External
HIP5062		√	60V, 5A	26V to 42V	24.7mA	36V	30ns	2.6A/mA	30mS	5.1V	120°C	1MHz or External
HIP5063	√		60V, 10A	10V to 45V	14mA	12V	30ns	4.5A/mA	N/A	External	120°C	External

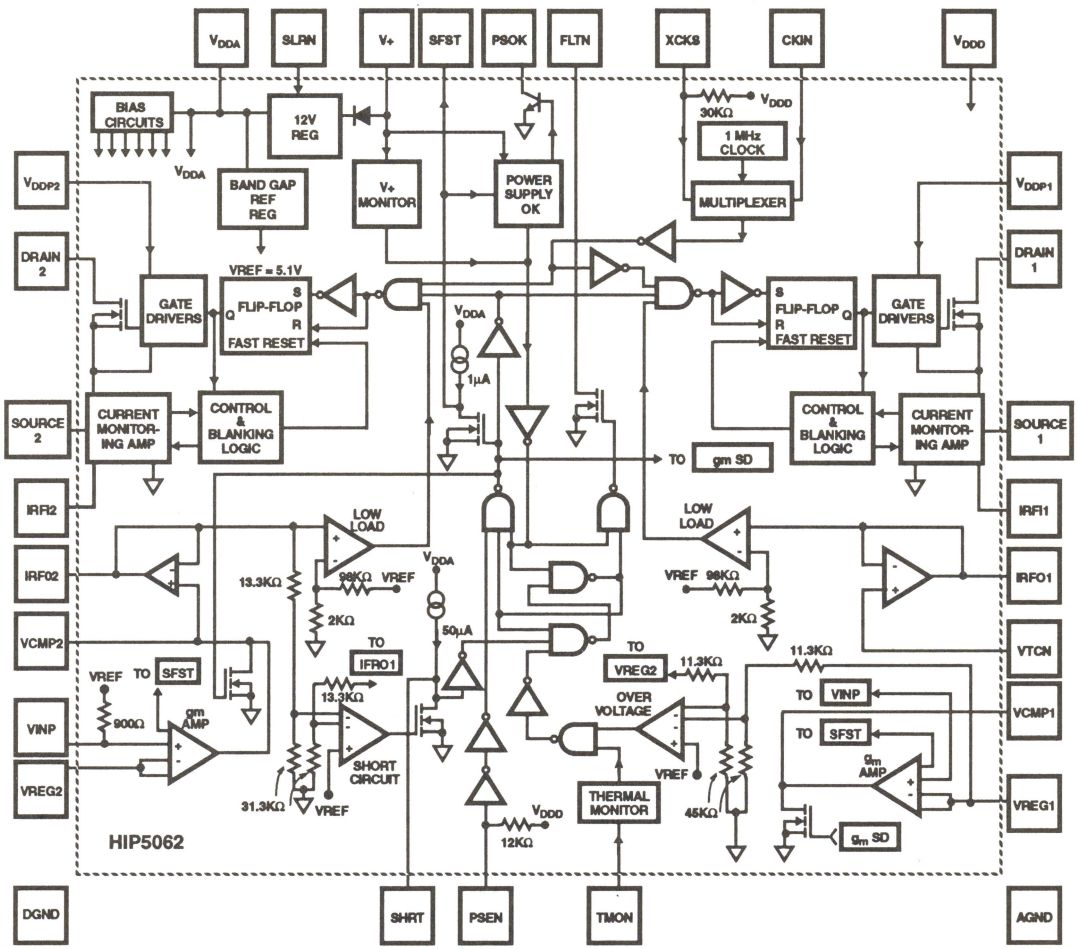


FIGURE 7. FUNCTIONAL BLOCK DIAGRAM OF THE HIP5062

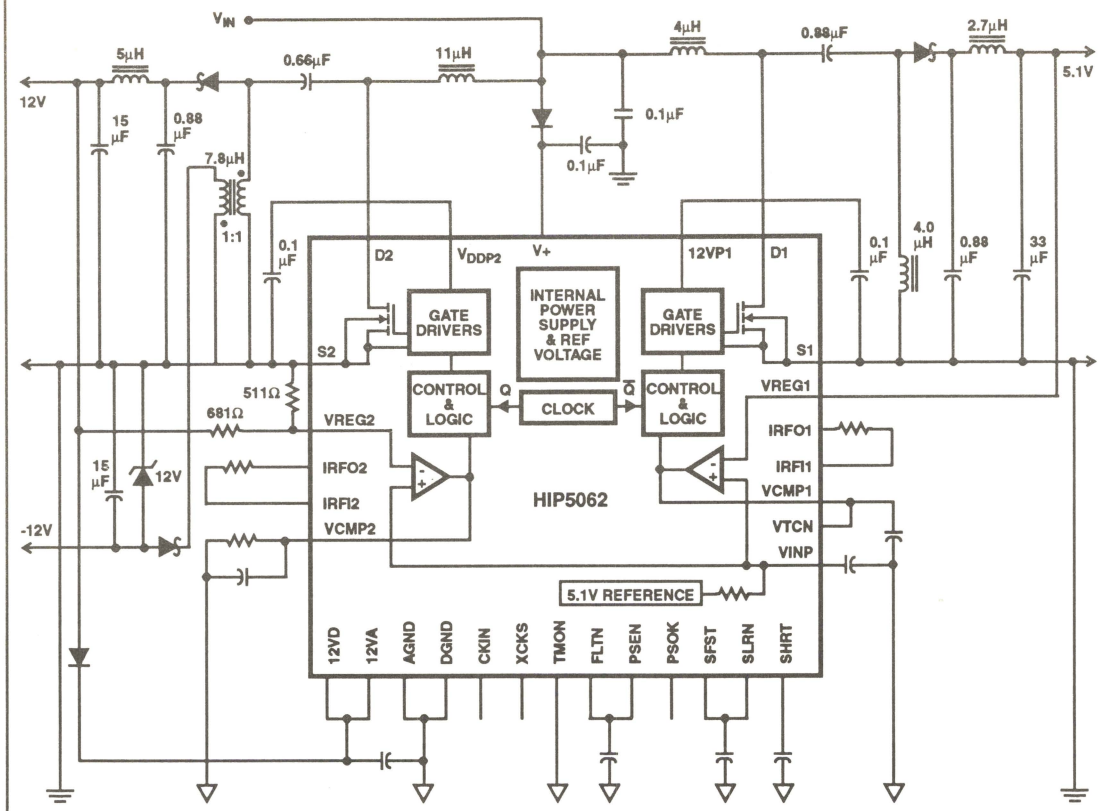


FIGURE 8. SCHEMATIC DIAGRAM OF THE HIP5062 IN A TRIPLE OUTPUT POWER SUPPLY

stage to minimize large asymmetrical transient currents. From the 12V output, a low current, -12V output may be derived as shown in Figure 8.

The HIP5063, shown in block diagram of Figure 9, is the most flexible of these devices. It is intended to be used in conjunction with either of the other two devices as an added power MOSFET with thermal monitoring and the basic current control circuitry. Its application can range from power supply functions to power amplifiers for both audio and servo amplifier. An external op amp is used to provide the error amplifier function. This allows the designer to optimize the control loop for transient response in these varied applications.

Successful 1MHz Operation and EMI

Aside from an on-chip, high-speed, high-power DMOS transistor, external circuit techniques play the most important role in the realization of excellent performance at higher frequencies. Parasitic inductance must be minimized. This is achieved at the chip level with 8 drain leads. Inductance at this point can lead to extremely large transient voltages at the MOS drain and reduction in supply efficiency. A secondary benefit to parallel contacts is the reduced resistive losses. Voltage drops in the source terminal degenerate the performance in several ways. To minimize some of these effects, 8 source leads are provided, again reducing lead inductance and resistance. Resistance and inductance in this lead would allow large voltages to be developed from the MOS source to ground. This can result in an effective loss of gate drive signal which appears as a loss of transconductance and an increase of r_{DS} (on). Voltage drop across the device is also increased with resulting reduction in efficiency.

Another consideration is bypassing. High peak gate currents exist around the output stage and the gate driver. On this chip additional terminals are brought out to permit bypassing of the positive supply voltage of the gate driver stage, returning the current directly back to the DMOS source terminal. Internally, the gate drive stage is returned to the DMOS source.

Surface mount capacitors are used to minimize lead inductance. Four 0.22µF capacitors are used in the drain connection to reduce series inductance. All components including the inductors are surface mounted. These techniques that are so essential to excellent high frequency performance also help to minimize both radiated and conducted noise. Short leads and low profile due to surface mounting and a large ground plane all contribute to efficiency and minimal interference.

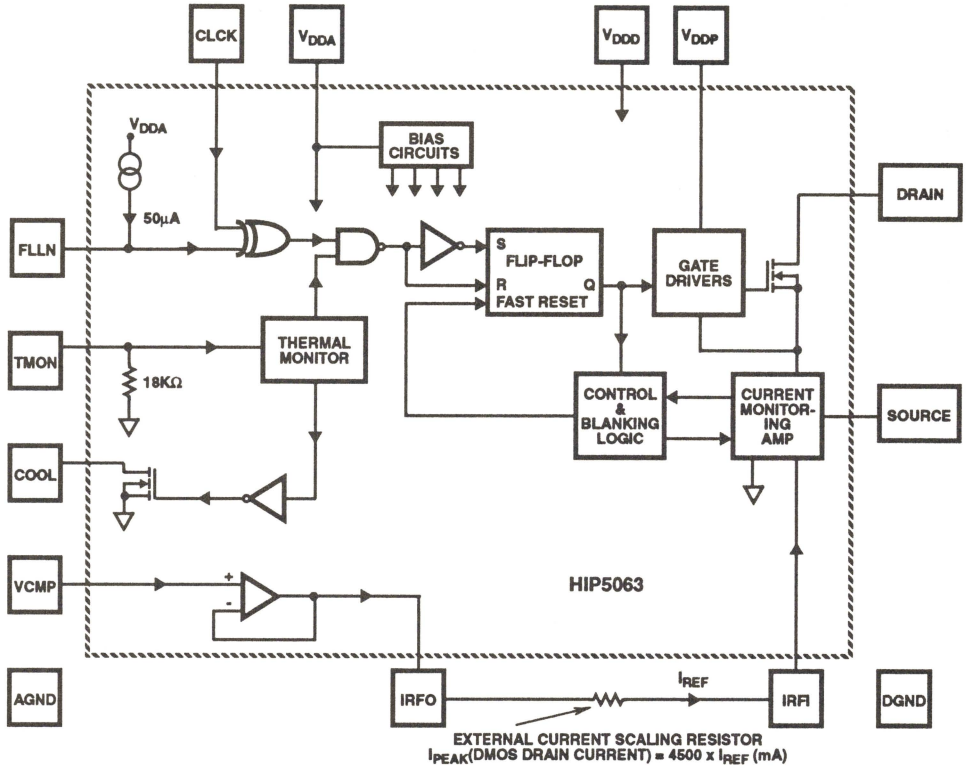


FIGURE 9. FUNCTIONAL BLOCK DIAGRAM OF THE HIP5063

Conclusions

A family of new 1MHz, current controlled switching regulators has been described that have many features that make these devices especially attractive to distributed power systems for both large main frame systems and the ever expanding consumer and industrial markets.

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Harris Semiconductor

APPNOTE

No. AN9217.1 April 1994

Harris Intelligent Power

HIGH CURRENT OFF LINE POWER SUPPLY

Author: Don LaFontaine

Introduction

Design Engineers are constantly pushed to reduce the space and cost of the power supply in their systems. For supplies between 2W and 6W that can operate over the world wide range of input voltage and frequency the options were flyback switching power supply or a high voltage linear regulator. The typical transformer supply requires AC voltage sensing and active tap switching, which is not common practice.

The flyback switching power supply is the most efficient, but is costly, complex and requires special EMI filters for suppression. The high voltage linear regulator is simple in design, cheap, but not practical at this power level. The transformer supply offers isolation and better efficiency but is limited to a small range of input voltage and frequency, is bulky, costly, and can be acoustically noisy.

An alternative solution is to configure the HV-2405E as a control chip to drive a MOSFET. This solution is not as efficient as the switching or transformer supplies and does not provide isolation, but is a low cost, compact (no transformer) 2W to 6W power supply accepting the world wide range of input voltage and frequency.

Features

- Low Cost Direct AC to DC Conversion
- Operates from 30VAC to 280VAC Line 50Hz/60Hz
- Output Current from 0mA to 250mA
- Output Short Circuit Protection
- Adjustable DC Output Voltage 5VDC to 24VDC†

  †Output Voltages up to 35V Possible

Applications

- Fan Power Supply
- Subfractional Horsepower Motor Drives
- Power Supply for Simple Industrial/Commercial/Consumer Equipment Controls

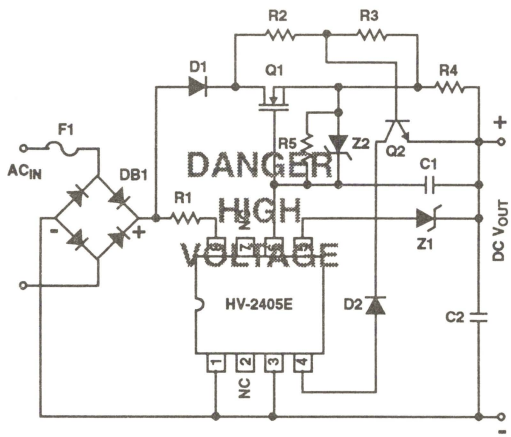
CAUTION: This product does not provide isolation from AC line.

Overview

When configured as a control chip for a power MOSFET, the HV-2405E provides AC to DC conversion over the world wide range of input voltage and frequency. The circuit shown below delivers an output voltage of 5 volts DC to 24 volts DC with output current from 0mA to 250mA. The output voltage can be extended to 35V for input voltages of $120V_{RMS}$ and output currents up to 150mA (see section titled "Output Voltage >24V").

The intent of this application note is to offer a cost effective solution at the expense of efficiency. The Harris IRF830 MOSFET was selected because of its relative low cost, low Ron and current handling capabilities. Improvements to the circuit performance illustrated in this application note can be made by selecting a larger MOSFET (i.e. Harris IRF840).

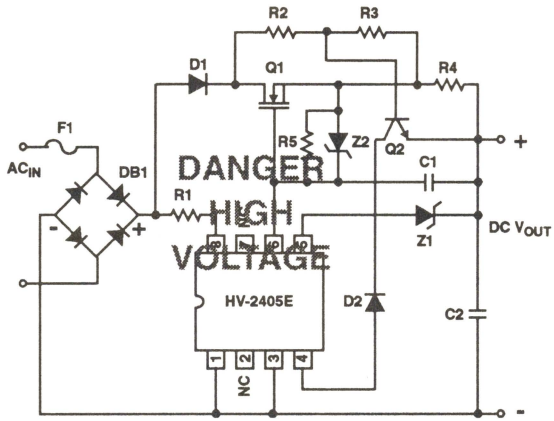
This circuit provides protection for the MOSFET by monitoring both its voltage and current with a resistor network. This network disables the HV-2405E, through its inhibit pin, when a predetermined voltage or current is exceeded.



HIGH CURRENT APPLICATION CIRCUIT

The optimum values of the resistors in the protection circuit (R2, R3, R4) are dependent upon the input voltage and output current. Thirteen circuit solutions are presented along

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COMPONENT LIST †DETERMINED BY APPLICATION			
Q1	IRF830	R3	†
Q2	2N2222	R4	†
D1	1N4007	R5	10KΩ, 1/4W
D2	1N914	C1	†0.022µF, 50V
Z1	†	C2	†100µF, 50V
Z2	15V	DB1	DB1M Bridge
R1	1KΩ, 1/2W	F1	†2A, 250VAC Fuse
R2	510KΩ, 1/4W		

FIGURE 1. HIGH CURRENT APPLICATION CIRCUIT

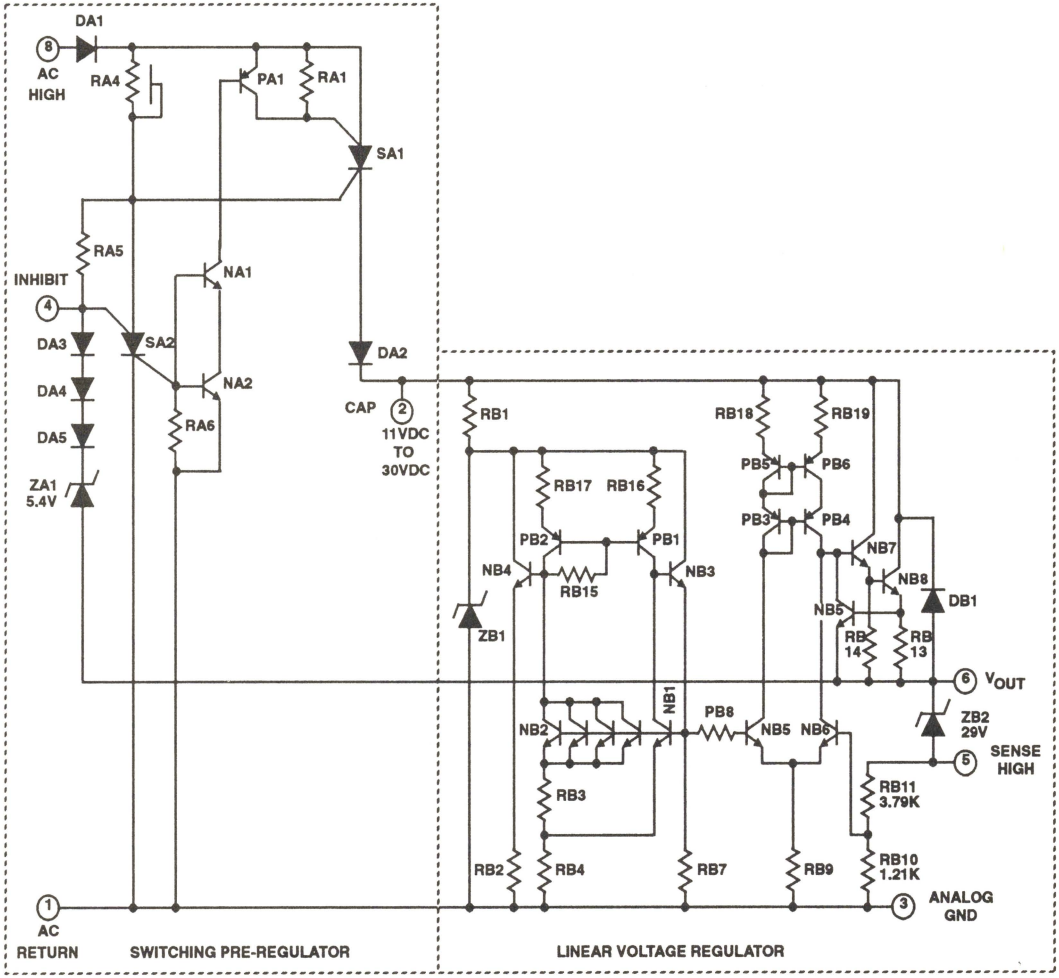


FIGURE 2. HV-2405E SCHEMATIC

with the MOSFET Power Dissipation and Circuit Efficiency; 5 for the World Wide Supply (V_{IN} = 30V_{RMS} to 280V_{RMS}, Table 2), 5 for the 120V_{RMS} Supply (V_{IN} = 30V_{RMS} to 120V_{RMS}, Table 3) and 3 for the 35 Volt output Supply (V_{IN} = 30V_{RMS} to 120V_{RMS}, Table4).

Circuit Description of the High Current Circuit

Figure 1 shows the schematic of the High Current Circuit. To understand the circuits operation first look at the operation of the HV-2405E as a control chip. The basic operation of the HV-2405E can be broken down into two functional sections (see Figure 2): (1) Switching Pre-Regulator and (2) Linear Voltage Regulator.

The Pre-Regulator takes energy from an incoming AC line to bias-up the Linear Voltage Regulator. The Linear Voltage Regulator performs two functions. The first is to supply a reference voltage at pin 5 that is temperature independent and the second is to supply an output voltage on pin 6 that is adjustable from 5 volts to 24 volts. To obtain higher output voltages see section titled "Output Voltages >24 volts". The output voltage is adjusted from 5V to 24V by placing a Zener diode (Z1) between pin 5 and the output capacitor (C2). The 5V reference is generated by the band-gap circuitry ensuring that pin 5 will sink 1mA through 5kΩ of resistance (RB10 + RB11).

The Linear Voltage Regulator provides gate drive to an external power MOSFET (Q1) that charge pumps the output capacitor. Gate drive to Q1 occurs when current flows into pin 8 and out of pin 6. The switching Pre-Regulator turns off when current is pulled out of pin 4 (anode gate of SA2). When SA2 turns ON, SA1 turns OFF and the gate drive to Q1 stops until the next half cycle on AC high. The gate to source Zener diode (Z2) ensures that the maximum V_{GS} is not exceeded.

SA1 is turned OFF when either of the following two conditions exist:

(1) **Under Normal Operation**. Feedback from the linear voltage regulator results in current flowing out of SA2's anode gate and through the zener diode stack (ZA1, DA3, DA4, DA5) when the output capacitor reaches full charge.

(2) **Under Fault Conditions** (i.e. Q2 gated on because power dissipation limit exceeded). Current flows out of SA2's anode gate and through the 2N2222 (NOTE; Pin 4 is higher than pin 5 or pin 6).

Output voltage regulation is achieved when the output voltage at pin 5 exceeds the reference voltage. This causes more current to flow through NB6, which in turn decreases the drive to the output darling pair (NB7, NB8), causing an increase in the already increasing voltage on pin 2, resulting in turning ON SA2 and turning OFF SA1.

In this application the HV-2505E only has to supply gate drive to the power MOSFET. This enables the value of the input series resistor R1 to be 1kΩ.

Typical waveforms of the MOSFET are illustrated in Figures 3 and 4 with output currents of 50mA and 250mA respectively. From these waveforms it can be seen that the circuit supplies large current spikes (8A to 11.5A) to the output capacitor for a short period of time (120µs-300µs). The current spikes are supplied to the output capacitor while the input voltage is only a little larger than the desired output voltage. This technique makes the efficiency higher than for an equivalent linear regulator.

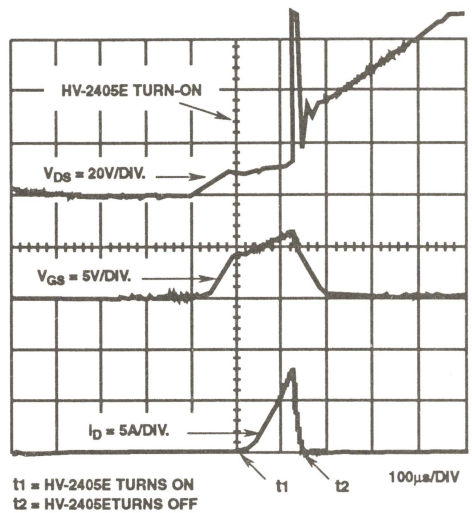


FIGURE 3. TYPICAL WAVEFORMS OF THE MOSFET (I_{OUT} = 50mA)

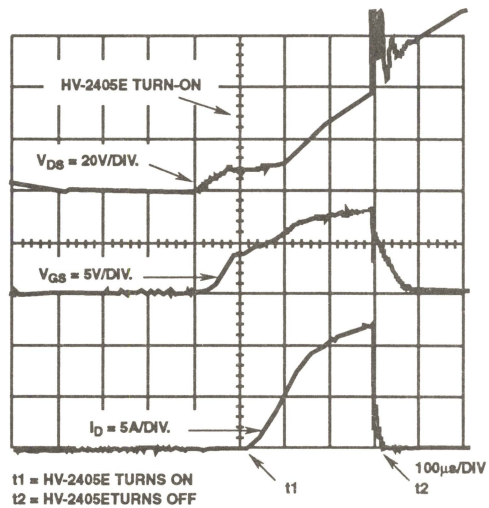


FIGURE 4. TYPICAL WAVEFORMS OF THE MOSFET (I_{OUT} = 250mA)

MOSFET/IGBT Protection Circuit

The circuitry shown in Figure 5 protects the MOSFET during fault conditions by limiting its maximum power dissipation. Under normal operating conditions the protection circuit is off. Three 1/4 watt resistors (R2, R3, R4), a diode (D2), and a transistor (Q1) form the protection circuit. Resistors R2 and R3 monitor the drain to source voltage and resistor R4 the drain current. When a predetermined voltage/current combination is exceeded the MOSFET is turned off via the HV-2405E's inhibit pin.

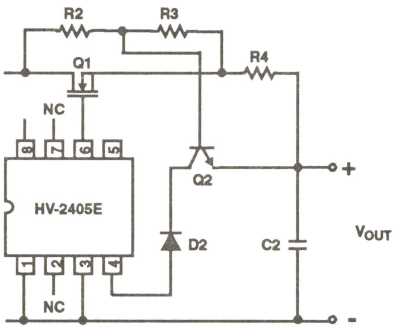


FIGURE 5.

Determining R2, R3 and R4

Optimization of the resistor values for minimizing Q1 power during fault conditions is dependent upon the input voltage and output current. Table 1 (A, B) gives the peak drain current (I_D) and the peak drain to source voltage (V_{DS}) for the Harris IRF830 in this application for $240V_{RMS}$ and $120V_{RMS}$ respectively during normal operating conditions.

TABLE 1A. WORLD WIDE SUPPLY (V_{IN} = $30V_{RMS}$ to $280V_{RMS}$)

I_{OUT}	V_{DS} (PEAK)	I_{DRAIN} (PEAK)
50mA	15V	7.60A
100mA	20V	11.00A
150mA	31V	11.00A
200mA	37V	11.25A
250mA	44V	11.50A

TABLE 1B. $120V_{RMS}$ SUPPLY (V_{IN} = $30V_{RMS}$ TO $120V_{RMS}$)

I_{OUT}	V_{DS} (PEAK)	I_{DRAIN} (PEAK)
50mA	12.5V	6.00A
100mA	15.0V	9.00A
150mA	18.0V	9.30A
200mA	24.0V	9.50A
250mA	27.0V	10.00A

The resistance values of R2, R3 and R4 for the circuit solutions presented in this application note were determined from the V_{DS} and I_D values in Table 1. A maximum peak power load line for the MOSFET is determined by doubling both the I_D peak and V_{DS} values and setting the voltage drop across R3 (EQ 1) and the Voltage drop across R4 (EQ 2) equal to $1V_{BE}$. One Be across R3 or R4 limits the MOSFET's power by turning on the 2N2222. A graphical representation of this load line is presented in Figure 6.

The protection circuit will remain off for any combination of V_{DS} and I_D below the load line, including the maximum power dissipation from which the line was derived.

$$Vbe = \frac{R3}{R2+R3} \cdot (2V_{DS(max)}) \qquad \text{(EQ1)}$$

$$Vbe = (2) \cdot (R4) \cdot (I_D) \qquad \text{(EQ2)}$$

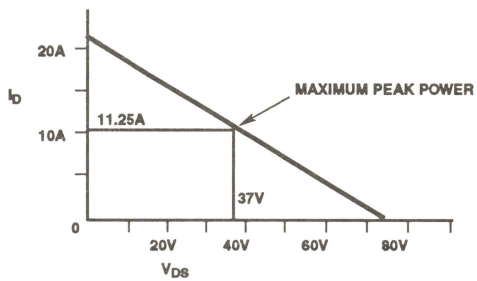


FIGURE 6.

Example:

Assume: I_{OUT} = 200mA, $V_{IN} = 264V_{RMS}$

From Table 1(A): V_{DS} = 37V, I_D = 11.25A

Figure 6 shows the maximum power load line for an output current of 200mA with $V_{IN} = 264V_{RMS}$.

To limit the maximum V_{DS} voltage to <74V (twice that of Table 1) select the values of R2 and R3 so that with 74V across them, there is a 0.6V potential drop across R3.

Assume R2 = 510kΩ

$$0.6 = \frac{R3}{510k+R3}(74) \qquad \text{(EQ3)}$$

$$R3 = \frac{(0.6)\ (510k)}{74-0.6} \qquad \text{(EQ4)}$$

R3 = 4.16kΩ

To limit the maximum I_D current to <22.5A select the value of R4 so that with 22.5A there is a 0.6V potential drop across R4. (NOTE: Although we've designed the circuit for a maximum of 22.5A, theory predicts that V_{DS} would equal 0 volts

and therefore no power dissipation. Once again the maximum power dissipation would be in the middle of our I_D and V_{DS} ranges.

$$0.6 = (22.5A)(R4) \quad \text{(EQ5)}$$

$$\therefore R4 = 0.026\Omega$$

The combination of voltage drops across R3 and R4 determine the trigger point of the protection circuit. The recommended resistor values of R3 in Tables 2 and 3 are higher than predicted by the above calculation at the lower output currents. This is because the value of R4 was set to 0.02Ω decreasing its sensitivity at lower output currents. (NOTE; R4's calculated resistance is closer to 0.02Ω at the higher currents.) R3's value was increased to maintain the same trip point.

Tables 2 and 3 give the recommended resistor values for both the World Wide Supply and the $120V_{RMS}$ supply. Also presented in both tables are the circuits MOSFET Pd, Peak drain current and circuit efficiency under normal operation as well as the MOSFET Pd under short circuit conditions. The peak power is several hundred watts but because the MOSFET is on for such a short period of time the average power is only a few watts. Reference Figures 9-12 for average power dissipation of the MOSFET.

TABLE 2. WORLDWIDE SUPPLY (V_{IN} = $30V_{RMS}$ TO $280V_{RMS}$)

Input Frequency = 60Hz, V_{OUT} = 24V
Input Voltage = $240V_{RMS}$ (NOTE: Reduce the Value of R3 for V_{IN} > 264)

				NORMAL OPERATION			OUTPUT SHORTED‡	
I_{OUT} (mA)	R2 (Ω)	R3 (Ω)	R4 (Ω)	MOSFET Pd (IRF830) *	PEAK I_{DRAIN}	CIRCUIT EFFICIENCY†	I_{SC} (mA)	MOSFET Pd (IRF830)
50	510k	7.5k	0.03	0.99W	7.60A	60.5%	57.4	4.49W
100	510k	9.0k	0.02	2.19W	11.00A	47.9%	153.0	8.93W
150	510k	7.0k	0.02	3.51W	11.00A	40.1%	212.0	11.35W
200	510k	4.7k	0.02	5.46W	11.25A	38.6%	350.0	15.16W
250	510k	3.9k	0.02	7.15W	11.50A	34.2%	420.0	17.74W

TABLE 3. $120V_{RMS}$ SUPPLY (V_{IN} = $30V_{RMS}$ TO $120V_{RMS}$)

Input Frequency = 60Hz, V_{OUT} = 24V Input Voltage = $120V_{RMS}$

				NORMAL OPERATION			OUTPUT SHORTED‡	
I_{OUT} (mA)	R2 (Ω)	R3 (Ω)	R4 (Ω)	MOSFET Pd (IRF830) *	PEAK I_{DRAIN}	CIRCUIT EFFICIENCY†	I_{SC} (mA)	MOSFET Pd (IRF830)
50	510k	6.0k	0.06	0.85W	6.0A	66.5%	94	2.13W
100	510k	13.0k	0.02	1.88W	9.0A	57.3%	155	5.28W
150	510k	10.0k	0.02	2.89W	9.3A	49.8%	245	8.47W
200	510k	6.8k	0.02	4.05W	9.5A	48.9%	422	14.13W
250	510k	5.6k	0.02	5.25W	10.0A	44.8%	530	17.83W

* Reference Figures 9, 10, 11 and 12 for complete MOSFET Power Dissipation for 24V 60Hz, 24V 50Hz, 5V 50Hz and 5V 60Hz operation vs. Output Current

† Reference Figures 13, 14, 15 and 16 for complete Circuit Efficiency for 24V 60Hz, 24V 50Hz, 5V 50Hz and 5V 60Hz operation vs. Input Voltage.

‡ See Fold-Back Current Limiting Section to reduce power dissipation in MOSFET.

Fold-Back Current Limiting

Fold-back current limiting is a well known method of reducing power dissipation and nuisance fuse blowing under short circuit conditions. This can be realized by adding a fraction of the output voltage to the base of Q2 in the protection circuit. By connecting a resistor (R_F) (Figure 6A) from the base of Q2 to ground, an output-sensing voltage divider consisting of R4, R3, and R_F produces a voltage that offsets the current sense (IR4) and SOA voltage (IR2 + IR3) so that a higher MOSFET current is required to turn on Q2 at full output voltage than that required at zero output voltage (i.e. short circuit). Therefore, at short circuit, the maximum available current is determined by the voltage divider R2, R3 (for V_{DS}) and the current sense resistor R4. Under normal output conditions, the available output current is increased by the magnitude of the offset voltage produced by the output sensing voltage divider, and foldback is achieved.

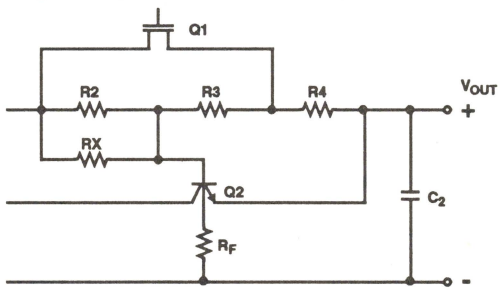


FIGURE 6A.

A measure of the degree of foldback is a ratio of the output current at short circuit to the maximum current available at normal output voltage, and ideally would range between zero and 1 (assuming that the I-V characteristics of the supply were perfectly square). This ratio is determined by the magnitude of the offset voltage introduced at the base of Q2. A practical range would be between 0.5 and 0.8, depending on the type of load. Too much foldback (<0.5) will produce a soft-start response into a large capacitive load, or no-start into an incandescent, or constant current load.

The addition of foldback into the Q2 circuit requires a review of the values of the V_{DS} sense resistors R2, R3, and peak current sense resistor R4. For example, the effect of adding a value of R_F to produce a foldback ratio of 0.8, will introduce an offset voltage that will require a higher V_{DS} to turn on Q2. At normal output voltage, this has the effect of moving the load line (Figure 6) to the right, increasing the stress on the MOSFET. To compensate, equations 1 and 2 must be modified to include the offset voltage in the calculation of the resistors R2, R3 and R4. At short circuit the offset voltage disappears, moving the load line back to the left (in the direction of less stress on the MOSFET).

One way to compensate for the addition of R_F is to place a resistor Rx in parallel with R2. The value is chosen to provide a compensating current equal to the current through R_F. Therefore:

$$\frac{V_{OUT}}{R_F} = \frac{V_{DS(PEAK)}}{R_X}$$

From Table 1 the V_{DS} for the output current desired allows the value of the R_X compensating resistor to be calculated. Thus, foldback is added without changing the MOSFET protection load line under normal output conditions. Under short circuit conditions, the line will shift to the left in an amount proportional to the current through R_F.

Determining R2, R3 and R4 for a Different MOSFET

The first step is to determine the worse case peak V_{DS} and peak I_D values for the power MOSFET in this application. Worse case V_{DS} and I_D values occur when the AC input voltage, input frequency, output current and output voltage are all at their maximum values for the application (i.e. 264V_{RMS}, 60Hz, 250mA and 24V).

CAUTION: Reference section titled "General Precautions" before making the following measurements.

NOTE: A DC meter only provides the average voltage, not the peak and therefore not suitable for the following measurements.

Measurement of the peak V_{DS}, as shown in Figures 3 and 4, requires an oscilloscope with isolated inputs. This allows the measurement to be taken directly across the MOSFET.

Measurement of the peak I_D, also shown in Figures 3 and 4, requires a non-contact current probe that measures the drain current only (cathode side of D1 is a good connection point).

The above measurements will allow the values of R2, R3 and R4 to be sized such that under normal operating conditions the protection circuit is off (see following section on verification of resistor values).

Determining the MOSFET power dissipation or circuit efficiency requires an oscilloscope with isolated inputs and a waveform processing capabilities to calculate the area of the complex waveforms. The analysis for this application note used the Gould 2608 Digital Storage Oscilloscope.

Verification of Correct R2, R3 and R4 Values

It is important to verify that the protection circuit is off under normal operating conditions.

Monitor the output voltage with an oscilloscope to ensure that the peak voltage is not dropping when the output current is greater than that required by the application. If the peak voltage decreases before I_{OUT} (max) is reached, then the

value of R4 is too large. Once again, a DC meter will only give the average output voltage and will not give any indication that the peak output voltage is dropping.

Once the value of R4 is set, the value of R3 is verified by setting the output current to $I_{OUT(max)}$ and monitoring the output voltage with a scope (assuming R2 is selected). While monitoring the peak output voltage change R3's resistance value above that calculated. Select the next lower standard value that doesn't cause the output peak voltage to drop.

Output Short Circuit Protection

Output short circuit protection is provided by sensing the output current through resistor R4. Under shorted output conditions Q2 is turned on. This results in turning off the HV-2405E sooner in the cycle via the inhibit pin. Maximum power dissipation in the MOSFET is during output short circuit conditions. This should be considered when choosing the heat sink.

Wave Shaping for EMI

EMI can be a problem for switch mode power supplies due to the fast turn off times of the switch. The faster the di/dt the higher the harmonic content of the signal fed back into the power line. By wave shaping the input current pulse through the power MOSFET the size of the EMI filter can be reduced and in some cases is not required at all. (See Figure 7A).

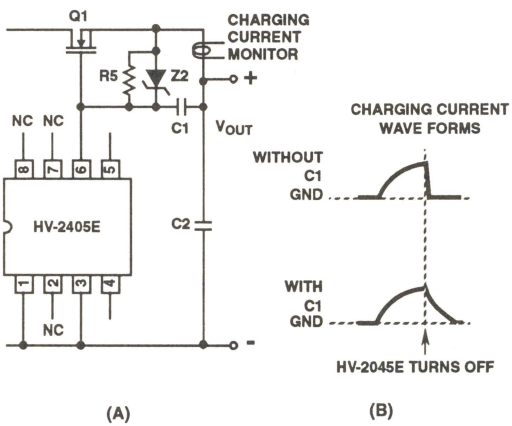


FIGURE 7.

Capacitor C1 is used to slowly turn off the power MOSFET once the HV-2405E has turned off. This is illustrated in Figures 3 and 4, notice that the V_{GS} voltage starts ramping down after t_2. The rate of this turn off is a function of the RC time constant between R5 and C1. Figure 7B shows a graphical representation of the input current pulse w/wo C1. Empirical tests have shown that longer RC time constants result in lower EMI noise at a cost of higher power dissipation in the MOSFET. The optimum RC time constant is a function of the input line voltage and output current and determined on an application by application basis. R5 also prevents charge pumping of the gate during transient noise spikes.

Setting the Output Voltage

The circuit shown in Figure 1 provides a regulated 5V to 24V DC and is set by adjusting the value of Z1. The output voltage of the HV-2405E (pin 6) is set by feedback from the sense pin (pin5). The output will rise to the voltage necessary to keep the sense pin at 5V. The output voltage is equal to the Zener voltage (V_{Z1}) plus the 5V on the sense pin. For a 5V output, the sense pin would be tied directly to the output. The output peak voltage has the accuracy and tolerance of both the Zener diode and the band-gap of the HV-2405E. The maximum value for VZ1 is 20V due to maximum output voltage rating of the HV-2405E. This circuit regulates the peak output capacitor voltage. The minimum output voltage is determined from the output capacitor size and the load current.

Output Voltages >24V

The output voltage can be extended to 35V for input voltages of $120V_{RMS}$ and output currents up to 150mA by placing another zener diode between pins 1 and 3 to GND, as illustrated in Figure 8.

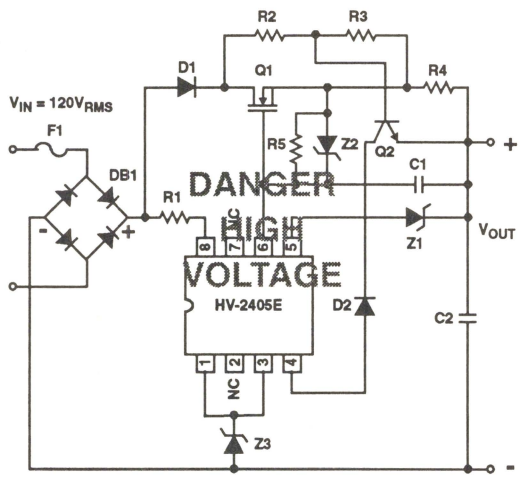


FIGURE 8. OUTPUT VOLTAGE UP TO 35V

Table 4A gives the recommended resistor values for output voltages up to 35V. Table 4B gives the MOSFET Pd, Peak drain current and circuits efficiency under normal operation as well as the MOSFET Pd under short circuit conditions for output voltages of 24V, 30V and 35V.

TABLE 4A. 35 VOLT OUTPUT SUPPLY (V_{IN} = 30V_{RMS} TO 120V_{RMS})

RESISTOR VALUES FOR INCREASED OUTPUT VOLTAGE UP TO 35V			
I_{OUT}	R2(Ω)	R3(Ω)	R4(Ω)
50mA	510k	6.0k	0.06
100mA	510k	9.0k	0.02
150mA	510k	7.5k	0.02

TABLE 4B. 35 VOLT OUTPUT SUPPLY (V_{IN} = 30V_{RMS} TO 120V_{RMS})

Input Frequency = 60Hz, Input Voltage = 120V_{RMS}

			NORMAL OPERATION			OUTPUT SHORTED‡	
	I_{OUT} (mA)	V_{OUT} (V)	MOSFET Pd (IRF830)	PEAK I_{DRAIN}	CIRCUIT EFFICIENCY	I_{SC} (mA)	MOSFET Pd (IRF830)
V_{OUT} = 24V Z_3 = 0V Z_1 = 20V	50	24.09	0.63W	6.5A	56.8%	84.9	1.26W
	100	23.76	1.35W	9.0A	56.7%	222.0	4.05W
	150	23.45	2.44W	10.0A	50.0%	300.0	6.19W
V_{OUT} = 30V Z_3 = 6.8V Z_1 = 20V	50	30.65	0.71W	6.5A	59.6%	117.0	1.44W
	100	30.33	1.50W	9.0A	59.4%	235.0	4.27W
	150	30.02	2.59W	10.0A	59.3%	308.0	6.27W
V_{OUT} = 35V Z_3 = 12V Z_1 = 20V	50	35.79	0.69W	6.5A	65.9%	680.0	11.47W
	100	35.48	1.44W	9.0A	65.0%	600.0	14.62W
	150	35.17	2.44W	10.0A	65.3%	640.0	17.30W

‡ See Fold-Back Current Limiting Section to reduce power dissipation in MOSFET.

Component List (†Determined by Application)

Fuse

Opens the connection to the power line should the system fail.

Value: = †, 2AG

Bridge Rectifier

DB1M or 4 diodes similar to 1N4007. Reduces power dissipation in the MOSFET by reducing the peak current for a given output load.

R1 Source Resistor

R1 limits the input current into the HV-2405E.

Value: = 1kΩ

D1 Blocking Diode

D1 prevents current flow back into the input of the HV-2405E through the MOSFET. This helps to reduce the total power in the MOSFET.

D2 Blocking Diode

D2 prevents overstress of the 2N2222 base collector junction. Without it current would flow through the HV-2405E when SA2 turns on, which over time could degrade the performance of the 2N2222.

Q1 Power Transistor

Q1 must have sufficient heat sink to dissipate the power. Reference Figures 7 through 10 for MOSFET (IRF830) power dissipation vs. input voltage and output current.

Recommendation = IRF830 or equivalent.

Q2 MOSFET/IGBT Power Limiting Transistor

Q2 is a Bipolar Transistor that turns off the HV-2405E when a predetermined ID or VDS limit is exceeded.

Recommended transistor = 2N2222 or equivalent.

R2,R3,R4 Power limiting Resistors

R2, R3, R4 set the maximum Power dissipation in the MOSFET/IGBT.

Values = †, 1/4W

R5 Input Current Wave Shaping Resistor

R5 is used to provide an RC time constant to wave shape the input current. R5 also removes charge off the gate during initial start-up.

Value = 10kΩ

Z1 Output Voltage Adjust

Z1 is used to set the output voltage above the 5 volt reference on pin 5 (see section titled "setting the output voltage" for more information).

Value = †, 1/2W

Z2 Gate to Source Voltage Clamp

Z2 protects the Power Transistor's gate to source from being overstressed.

Value = 15V, 1/2W

Z3 Output Voltage Adjust > 24V (See Figure 8)

Z3 is used to set the output voltage above 24V.

Value = †, <12V.

C1 Input Current Wave Shaping Capacitor

C1 is used to provide an RC time constant to wave shape the input current.

C2 Output Storage Capacitor

C2 is charged twice each line cycle by the Power Transistor. Value = †, 1000µF.

General Precautions

Instrumentation Effects:

Background: Input to output parasitic exist in most test equipment power supplies. The inter-winding capacitance of the transformer may result in substantial current flow (mA) from the equipment ground wire to the AC and DC ground of the HV-2405E. This current can induce instability in the inhibit circuit of the HV-2405E resulting in erratic operation.

Recommendations for Evaluation of the HV-2405E in the Lab:

a) The use of battery powered DVM's and scopes will eliminate ground loops.

b) When connecting test equipment, locate grounds as close to pin 1 as possible.

c) Current measurements on the AC side of the HV-2405E (Pin 8, 1 and 2) should be made with a non-contact current probe.

If AC powered test equipment is used, then the use of an isolated plug is recommended. The isolated plug eliminates any voltage difference between earth ground and AC ground. However, even though the earth ground is disconnected, ground loop currents can still flow through transformer of the test equipment. Ground loops can be minimized by connecting the test equipment ground probe as close to pin 1 as possible.

CAUTION: Dangerous voltages may appear on exposed metal surfaces of AC powered test equipment.

AC Source Effects:

Background: Laboratory AC sources (such as VARIACs, step-up transformers etc.) contain large inductances that can generate damaging high voltage transients any time they are switched on or off. Switch arcing can further aggravate the effects of source inductance.

Recommendation: Adequate protection means (such as MOV, avalanche diode, surgector, etc.) may be needed to clamp transients to within the ±500V input limit of the HV-2405E.

Preset VARIAC output voltage before applying power to part.

IRF830 MOSFET Power Dissipation vs Input Voltage and Output Current

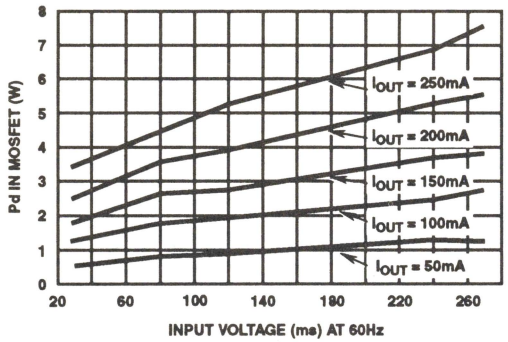


FIGURE 9. MOSFET POWER DISSIPATION 5V

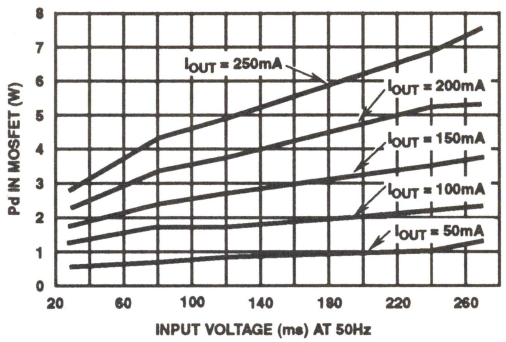


FIGURE 10. MOSFET POWER DISSIPATION 5V

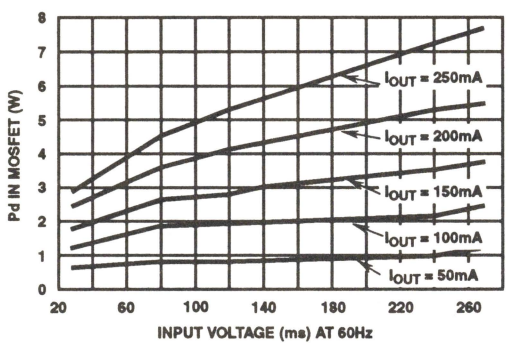


FIGURE 11. MOSFET POWER DISSIPATION 24V

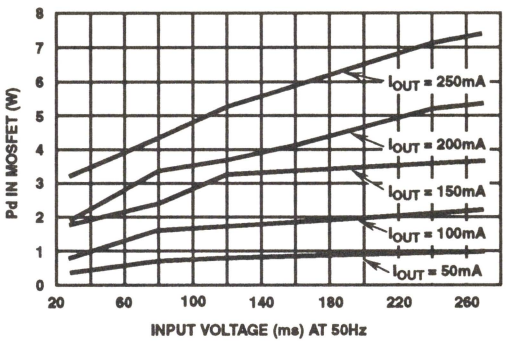


FIGURE 12. MOSFET POWER DISSIPATION 24V

Efficiency of High Current Circuit vs Input Voltage and Output Current

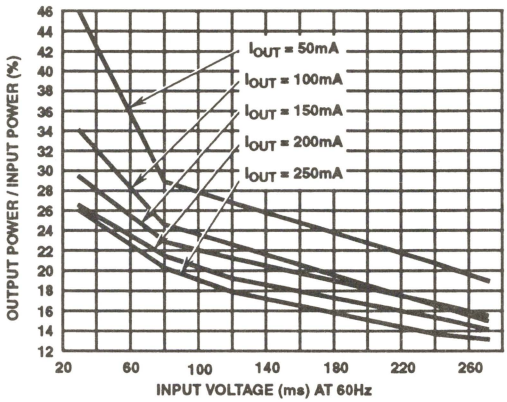


FIGURE 13. EFFICIENCY OF HV-2405E HIGH CURRENT CIRCUIT 5V

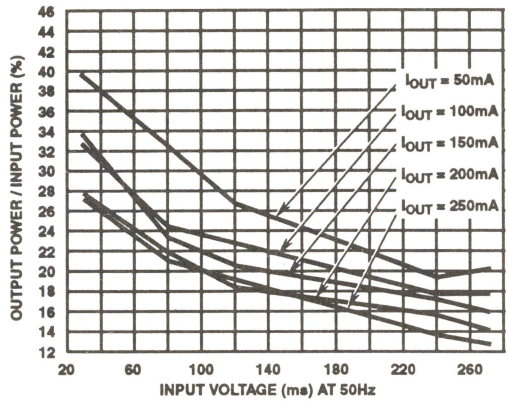


FIGURE 14. EFFICIENCY OF HV-2405E HIGH CURRENT CIRCUIT 5V

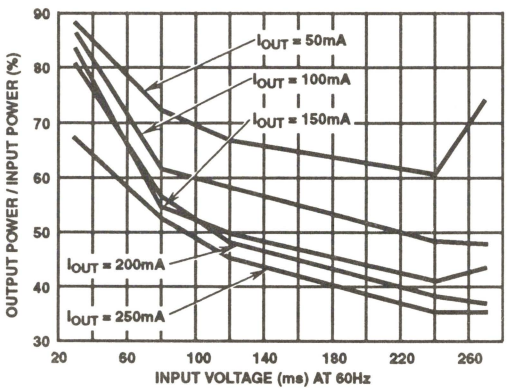


FIGURE 15. EFFICIENCY OF HV-2405E HIGH CURRENT CIRCUIT 24V

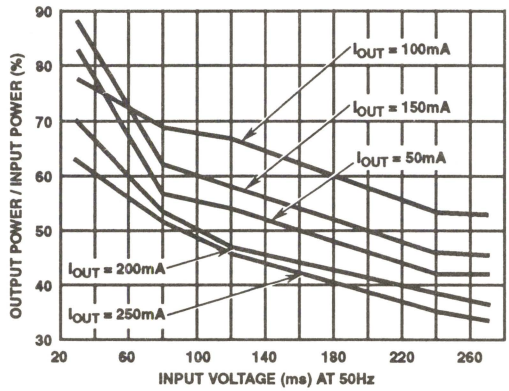


FIGURE 16. EFFICIENCY OF HV-2405E HIGH CURRENT CIRCUIT 24V

Footnotes

The circuit in Figure 1 is an improvement over a previous application note AN9101 (March 1991). The advantages of this circuit over that illustrated in AN9101 are:

1) Better output short circuit protection scheme. Protection circuit enables the designer to tailor the circuit for a given power dissipation in the power MOSFET by monitoring the MOSFET's voltage and current during operation.

2) Better output voltage regulation. By connecting the ground of the HV-2405E to AC return the band-gap circuitry of the HV-2405E provides a temperature independent reference voltage that regulates the output voltage.

3) Better performance to EMI (conducted interference). By wave shaping the input current pulse through the power MOSFET during turn off, the circuit can be tailored to pass EMI 0871 class "B" testing.

Harris Semiconductor

APPNOTE

No. AN9301 April 1994

Harris Intelligent Power

HIGH CURRENT LOGIC LEVEL MOSFET DRIVER

Author: John Prentice

Introduction

Although the HV400 was designed as an interface between a pulse transformer and a power MOSFET, there are applications for high current MOSFET gate drive controlled by standard logic. This application note provides a method of interfacing the HV400 to logic signals. It also reviews the input control requirements of the HV400. The data sheet for the HV400 may be found in the "Intelligent Power IC's" data book DB304.

HV400 Circuit Schematic

The HV400 schematic is shown in Figure 1. There are separate outputs for sinking and sourcing current. When the input goes low, resistor R3 provides base drive for Q2. An SCR is used to sink large currents. Transistor Q2 triggers SCR1 at both the anode and cathode gates. This triggering sequence begins as soon as D4 becomes reverse biased; the triggering delay time is then independent of the input fall time. Resistor R4 provides a base discharge path for Q1. Diode D6 increases the input hysteresis to reduce the chances that ringing at the input or output will trigger the SCR. Resistors R1 and R2 remove excess stored charge from the SCR and also help prevent false triggering. Diode D5 clamps the input low voltage.

A high input turns on Q1. Diodes D2 and D3, along with D1, prevent Q1 from saturating. Diode D1 also provides a means of passing charge from the input to the supply.

HV400 Input Characteristics

The HV400 is a non inverting current buffer. Pin 2 is the input control pin. For the output to be high, the input must also be high. This requires at least 12mA since R3 is approximately 1250Ω. Additional input current is required for the base current of Q1. The input driver should be capable of sourcing 200mA for a few hundred nanoseconds to achieve a 3A output current pulse but much less is required for smaller output currents due to the change in transistor gain with current and voltage. The input voltage should be 2V higher than the desired output voltage.

To set the output into the low state, the input voltage must drop 1V below the output. This can be accomplished by terminating the pin 2 input current since R3 acts as a pull-down resistor. The input voltage should be no more than 2V above pins 4 and 5 to make sure that Q1 will not turn back on.

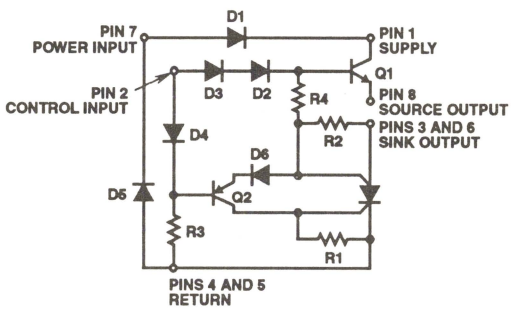


FIGURE 1. MOSFET DRIVER SCHEMATIC

Once the output is triggered low, it will remain low until the current into the output, pins 3 and 6, drops below 10mA and the SCR unlatches. The input must not go positive until the SCR unlatches and has had time to recover its voltage blocking capability defined by the "minimum off time" specification.

Logic Level Input

There are many instances where the control signal is a logic level referenced to the source of the MOSFET, i.e. logic ground and the source are at nearly the same potential. For example, forward, flyback and push-pull switch mode power supplies use power MOSFET's with grounded sources.

The Harris ICL7667 is a dual MOSFET driver that converts TTL/CMOS level signals into the higher voltages required for gate drives. The combination HV400 and ICL7667 results in a low cost, high output current, logic level input MOSFET driver. The circuit schematic is shown in Figure 2. One of the ICL7667 outputs becomes the input for the HV400 and the other is connected in parallel with the HV400 output. Since the ICL7667 is a CMOS product, its outputs swing rail-to-rail. Based on the HV400 input requirements, it should be apparent that a low impedance, high voltage (i.e. 15V) CMOS output is ideal for driving the HV400 input.

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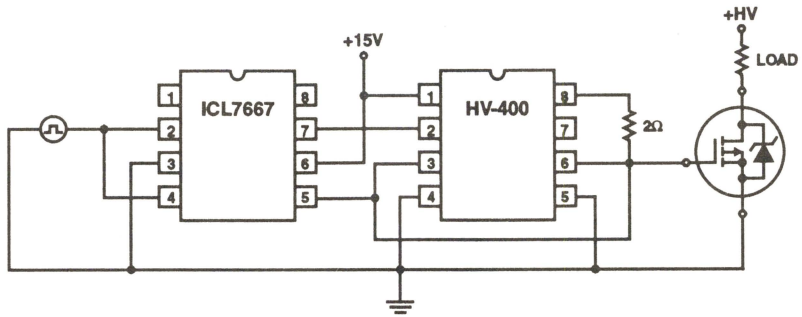


FIGURE 2. LOGIC LEVEL CIRCUIT

The result of combining one channel of the ICL7667 with the output of the HV400 is an improved driver with the voltage swing of a CMOS part and the large peak currents available from BiPolar. During switching transitions, the HV400 provides most of the sinking/sourcing current until the output is within 2V of the supply or ground. When the output is low, the ICL7667 continues to discharge the power MOSFET gate to ground after the HV400 SCR unlatches. It also provides a low impedance path to ground to keep the power MOSFET off in the presence of drain coupled noise or gate leakage currents. When the output is high, the ICL7667 continues to charge the MOSFET gate to the supply voltage minimizing MOSFET "on" resistance. Since most power MOSFET gate energy is dissipated in the HV400, the ICL7667 operates cooler minimizing the switching and delay times. The maximum supply voltage is 15V limited by the ICL7667.

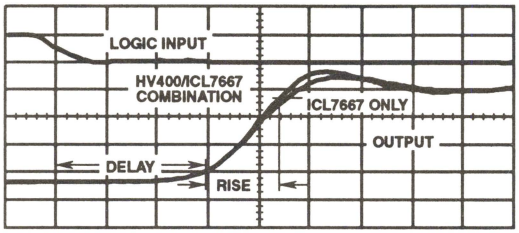
The following figures illustrate the performance of the HV400/ICL7667 combination. Figures 3 and 4 show the response with a 1nF capacitive load. Included for comparison is the response of the ICL7667 by itself. The low-to-high transition (Figure 3) has a 30nS delay and a 15nS rise time. The high-to-low transition (Figure 4) has a 10nS delay and a 14nS fall time. The HV-400 reduces the rise and fall times by only a few nanoseconds.

Figures 5 and 6 are for the same conditions except the load has been increased to 5nF. Here, the HV400 reduces the rise time to about 50% of that of the ICL7667 alone and the fall time is about 25%. The delay times are unchanged.

Figures 7 and 8 show the ICL7667/HV400 combination driving a 20nF load. From the dv/dt measurements, the peak source current is about $3^1/_3$A and the peak sink current is about 8A.

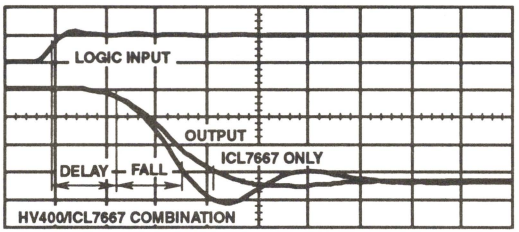
Summary

A simple circuit combination of the HV400 and an ICL7667 MOSFET drivers results in a logic compatible driver with large drive current capacity.



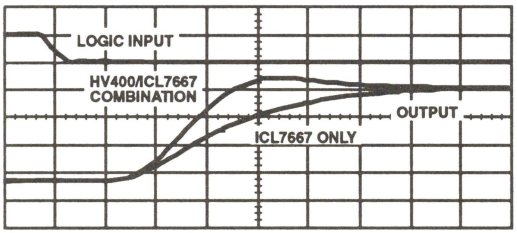
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 10.0ns/div
C_L = 1nF

FIGURE 3



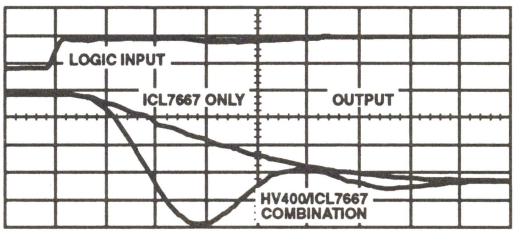
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 10.0ns/div
C_L = 1nF

FIGURE 4



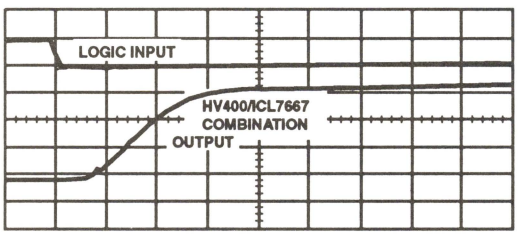
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 20.0ns/div
C_L = 5nF

FIGURE 5



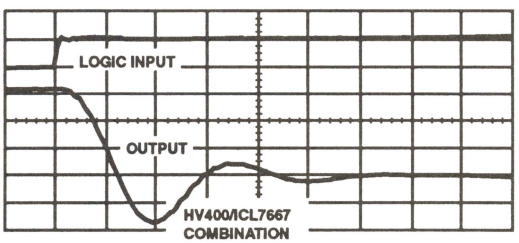
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 20.0ns/div
C_L = 5nF

FIGURE 6



NOTE:
Ch. 1 = 5.000V/div
Ch. 2 = 5.000V/div
Timebase = 50.0ns/div
C_L = 20nF

FIGURE 7



NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 50.0ns/div
C_L = 20nF

FIGURE 8

Harris Semiconductor

APPNOTE

No. AN9302.1 April 1994

Harris Intelligent Power

CA3277 DUAL 5V REGULATOR CIRCUIT APPLICATIONS

Author: John C. Rice

Introduction

The CA3277 dual 5V regulator was designed to perform reliably in harsh Automotive and Industrial environments where reverse voltages and unclamped inductive loads are commonly present. The primary 5V regulator OUT1 is generally used to power a microprocessor and backup CMOS memory. For systems requiring low power operation, the auxiliary 5V regulator, OUT2 can be disabled by applying a logic low signal to the ENABLE pin. Both regulators are capable of supplying up to 100mA at 5V and are internally protected against over-voltage, over-current and over-temperature conditions. This Application Note explores the basic structure of the CA3277 and presents several examples on applying the unique features of this device.

General Discussion

The exceptionally low dropout voltage and low quiescent current (500µA typical) makes the CA3277 a perfect choice in systems requiring 5V regulation from a battery supply. Figure 1 illustrates many of the CA3277 features. A bandgap reference is used to establish a temperature compensated reference for the internal over-current, over-temperature and over-voltage protection circuitry. An open collector reset pin is available for systems requiring a programmable, time delay reset during power supply transitions.

To enhance input noise immunity, the Ignition and Data Comparators were designed with 200mV of input hysteresis. Both comparators provide a means for translating digital information from the battery voltage to a 5V logic level. The

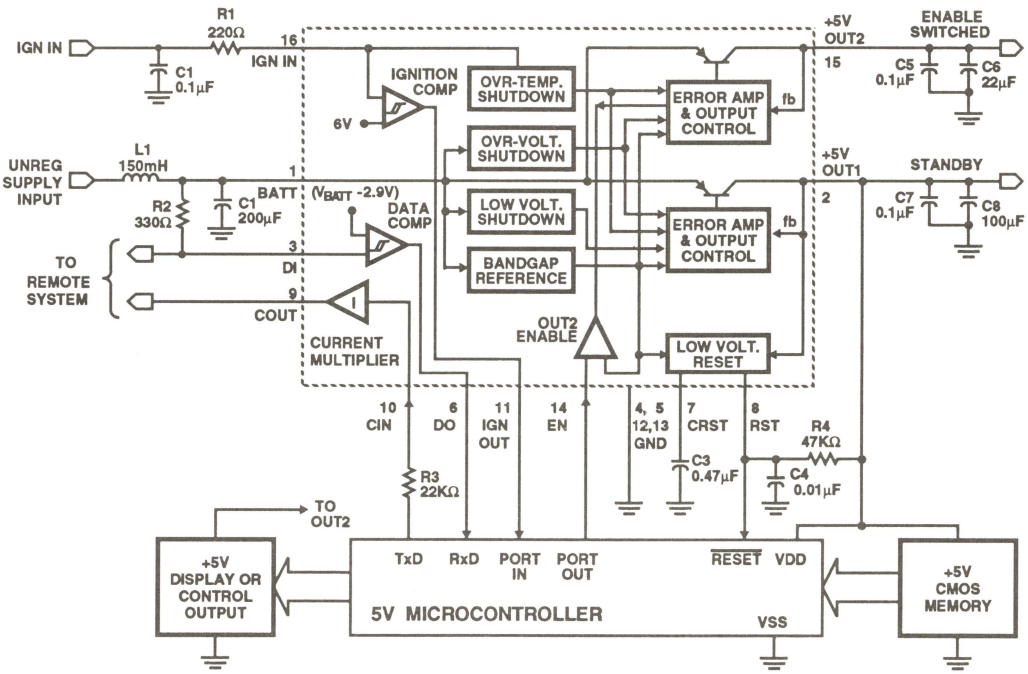


FIGURE 1. TYPICAL APPLICATION OF THE CA3277 USING THE SERIAL DATA BUFFERS

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Data Comparator Input pin, DI and the Current Output pin, COUT were originally designed to facilitate current loop, serial communication with a remote system. Serial data is processed through the CA3277 and interfaces to a microcontroller at the Data Output, DO and Current Input, CIN pins. The CA3277 Current Multiplier can also be used wherever a programmable constant current sink is needed.

The input LC filter illustrated in Figure 1 may not be necessary, but is recommended in harsh automotive and industrial environments where high speed, current transients could be present. Proper application of the CA3277 provides for a wide range of positive and negative transient voltage immunity (See Data sheet).

The CA3277 is packaged in a 16 pin power DIP enhancing its ability to dissipate heat well above standard DIP packages. It will maintain the device junction temperature below 150°C while dissipating 1.5W at 60°C. To maintain FULL load regulation and stability, a minimum of 22µF should be used on each output. The required output capacitance may vary depending on the application load and system temperature range. The effective capacitance of many electrolytic capacitors quickly diminishes at low temperatures. Therefore, in systems where temperatures are expected to be below -25°C, solid tantalum capacitors should be used.

Remote System Communications

The application circuit in Figure 2 illustrates how the CA3277 Ignition Comparator and Current Multiplier Output pins (IGN IN and COUT) can be used to communicate with a remote system. The primary advantage of this communication scheme is that digital information is transferred between systems using battery level voltage. This mechanization helps reduce EMI susceptibility on the 5V µP supply.

As a simple illustration, circuitry was added to the REMOTE system to sense a low voltage on OUT2. Once OUT2 goes below the threshold set by potentiometer P1, a fault is latched by the D flip-flop. The Ignition Comparator of the CA3277 translates the battery level fault signal into a 5V logic level. Once the fault is detected, the µP can attempt to reset the D flip-flop by sinking current from the CIN pin. The CIN pin is referenced to OUT1 and current into this pin is multiplied by 100 at the COUT pin. A pull-up on the COUT pin to battery converts the CA3277 current multiplier into a TTL-to-CMOS digital level translator.

Low Voltage Reset Function

Two pins on the CA3277 are dedicated to a Low Voltage Reset control function. The circuit for the Reset control is shown in Figure 3. When the supply voltage input level to BATT drops below the regulation threshold, the 5V OUT1 regulator voltage tracks the input from 5V down to ~3.5V before dropping out. The Reset circuit senses the falling OUT1 voltage level to initiate the Reset flag for the microcontroller.

The Reset circuit will provide a bandgap controlled delay, generated from an internal 10µA constant current source to pin 7 (CRST) to charge the external reset capacitor, C_{RST}. The RST Output, pin 8 is held low as long as the voltage on the reset capacitor, $V_{CAP}(t) < 3.08$. (This corresponds to less than 4.2V at OUT1) The voltage on C_{RST} is given by:

$$V_{CAP}(t) = \frac{1}{C} \times \int_0^t i(t)\,dt$$

Where the value of i(t) is a constant current source and is equal to10µA, then:

$$V_{CAP}(t) = \frac{10\,(\mu A) \times t_{RST}}{C_{RST}}$$

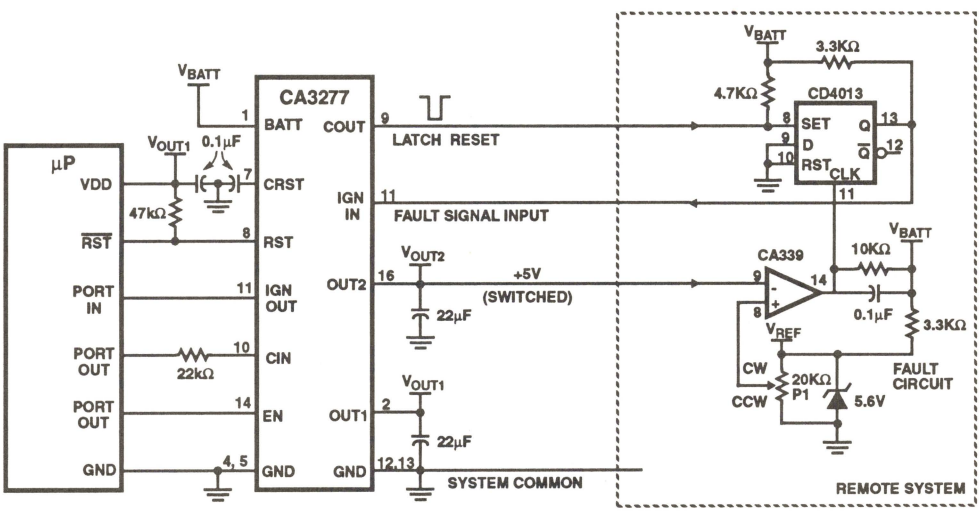


FIGURE 2. REMOTE SINGLE BIT COMMUNICATION AND LOGIC LEVEL TRANSLATION

Solving the above equation for C_{RST} when $V_{CAP}(t) = 3.08V$ yields an expression that can be used to calculate the value of the external capacitor for a desired reset time. Where t_{RST} is in milliseconds, the solution for C_{RST} in μF is:

$$C_{RST}(\mu F) = \frac{t_{RST}(ms)}{308}$$

Example: For a 150ms reset pulse, the capacitor value in μF would be:

$$C_{RST} = \frac{150(ms)}{308} = 0.48\mu F$$

Reset as a Stable Constant Current Source

When not otherwise committed to use, the 10μA constant current source from the C_{RST}, pin 7 output can be used as illustrated in Figure 4 to form a non-inverting current-to-current multiplier. The circuit is connected as a unity-gain buffer which forces the voltage drop, $I_{IN} \times R1$ across R2. The output current equals the sum of the input current and the current flowing through R1.

i.e.: $$I_{OUT} = I_{IN} \times (1 + \frac{R1}{R2})$$

The compliant voltage range of the 10μA current source is limited on the high side by saturation of the PNP transistor, Q_C, shown in Figure 3. On the low side, the FLAG/SW Reset Comparator input may source upto 1μA of current when the input is less than 3.08V. The most stable load voltage range for the C_{RST} constant current source is 4V to (V_{BATT} - 2V).

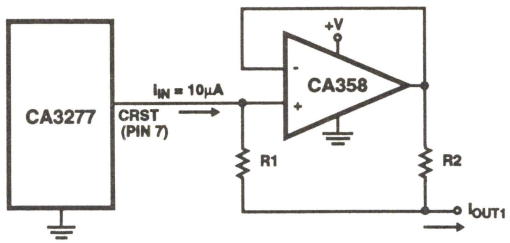


FIGURE 4. CURRENT-TO-CURRENT MULITPLIER

Current Multiplier

The Current Multiplier circuit of the CA3277 is shown in Figure 5A. The CIN pin is a current controlled input and the COUT pin is a 100 times current amplified output. As such, the Current Multiplier is available if a programmable current sink is required. Figure 5B illustrates the linearity of the current gain across temperature. For 10mA of output current, referenced to 25°C, the current gain variation is plotted over the -40 to 85°C ambient temperature range. The current gain is typically 100 times and is defined as the output current, I_{COUT} divided by the input current, I_{CIN}. (Figure 5C) Notice that some nonlinearity does exist when the input current, I_{CIN}, is below 30μA.

The external components of Figure 5A illustrate a simple test circuit the reader can use to verify that the current gain linearity will meet a particular application need. Adjust P1 such that I_{CIN} is within the recommended current range of $30\mu A < I_{CIN} < 300\mu A$. The calculation for output voltage across the 1KΩ resistor should be approximately

$$V_{COUT} = V_{BATT} - (I_{CIN} \times 100) \times 1K\Omega.$$

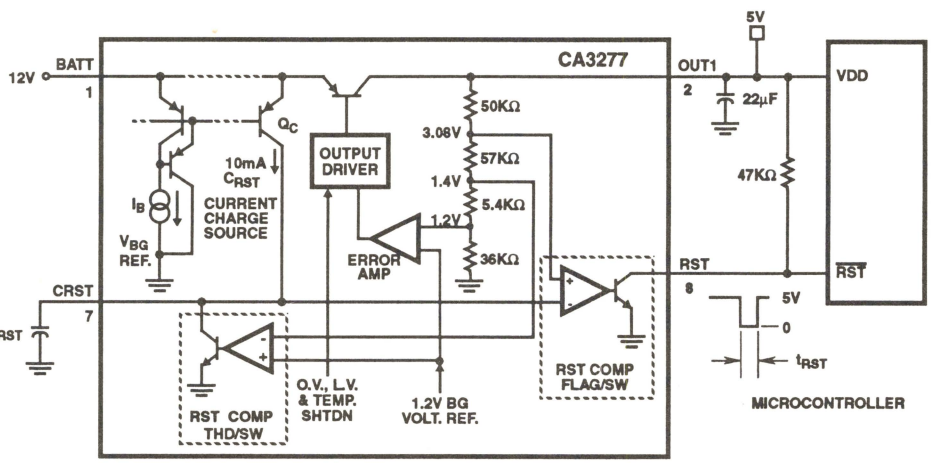


FIGURE 3. LOW VOLTAGE RESET CIRCUITRY

The output stage can be driven to current levels exceeding 30mA. To minimize dissipation, the no-signal state should be a condition of zero input bias current.

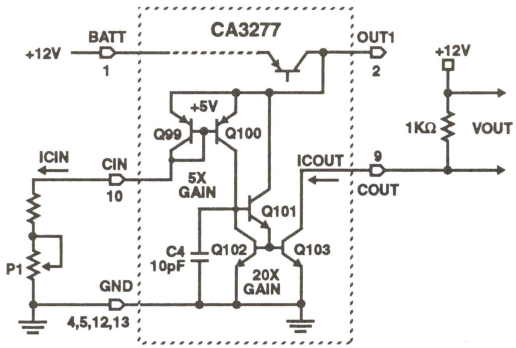


FIGURE 5A. CURRENT GAIN LINEARITY TEST CIRCUIT SHOWN WITH THE CA3277 CURRENT MULTIPLIER

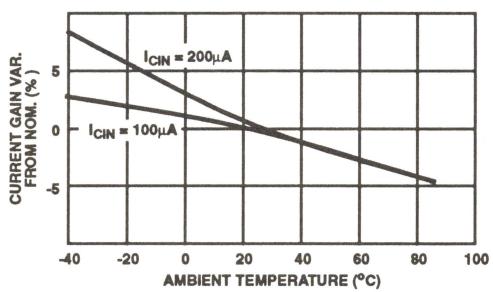


FIGURE 5B. CURRENT MULTIPLIER CURRENT GAIN vs TEMPERATURE CHARACTERISTIC

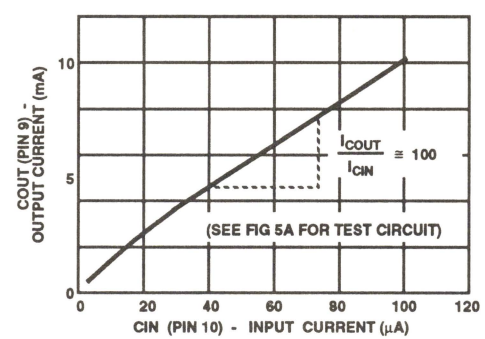


FIGURE 5C. CURRENT GAIN CHARACTERISTIC OF THE CA3277 CURRENT MULTIPLIER

Low Battery Fault Indicator - Current Multiplier Application

The Current Multiplier can be used with the Data Comparator to provide a Low Battery feedback signal to the microprocessor. Figure 6 illustrates the interface between the CA3277 and the microprocessor. As previously discussed, the CIN input is internally connected to the base and collector (diode connection) of a PNP transistor; the Emitter being tied to OUT1. (See the internal Current Multiplier Schematic of Figure 5A)

To use the Current Multiplier as a Low Battery detector, simply reverse bias the CIN input to a higher voltage than the turn-on threshold. A practical condition is to make $V_{CIN} = V_{OUT1}$ which provides the equivalent of one diode drop as a threshold margin when the battery is new. As the battery voltage decreases over the battery life, so will V_{CIN}; until the CIN input voltage is below V_{OUT1} by ~0.7V. This will forward bias the diode connected PNP, turning on the Current Multiplier and driving the Current Output pin low.

Note: The voltage drop, V_{be} ~ 0.7V of the diode connected PNP has the same temperature dependence as a normal junction diode, decreasing as the chip temperature rises.

The LED in Figure 6 will serve as a visual indicator of a low battery condition. The Data Comparator can be used to provide feedback to the Microprocessor. Buffer the COUT pin by tying it to the Data Comparator input. The Data Out pin can then be directly connected to the Microprocessor port input or interrupt pin. Recall that the Data Comparator has 200mV of input hysteresis which helps reduce the risk of noise on this Microprocessor input.

Note: OUT2 must be enabled if the Data Comparator is used.

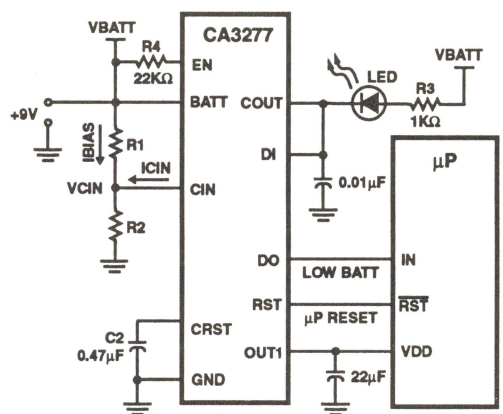


FIGURE 6. EXAMPLE OF A LOW BATTERY FAULT INDICATOR CIRCUIT

Example:

When the 9V battery, illustrated in Figure 6, is new:

$$V_{BATT} = 9V \text{ and } V_{OUT1} = 5V \text{ (Typical)}$$

For a low battery threshold voltage margin of one diode voltage drop where $V_{be} = 0.7V$; and V_{CIN} is the voltage at the R1 and R2 resistor divider junction,

Let $V_{CIN} = V_{OUT1}$

The CIN input does not begin to source current until

$$V_{CIN} \leq V_{OUT1} - V_{be}$$

The voltage divider equation for the V_{CIN} voltage is:

EQ1: $$V_{CIN} = V_{BATT} \times \left(\frac{R2}{R1+R2}\right)$$

To keep the idle current drain (I_{BIAS}) as low as possible on the battery,

Let $100\mu A \leq I_{BIAS} \leq 200\mu A$

The circuit equation for I_{BIAS} current while $I_{CIN} = 0$ is:

EQ2: $$I_{BIAS} = \left(\frac{V_{BATT}}{R1+R2}\right)$$

Solving EQ1 and EQ2 and using $V_{CIN} = V_{OUT1} = 5V$; $I_{BIAS} = 100\mu A$ and $V_{BATT} = 9V$, we can calculate the values of R1 and R2 as follows:

To solve for R2:

$$R2 = \frac{V_{CIN}}{I_{BIAS}} = \frac{5V}{100\mu A} = 50K\Omega$$

To solve for R1:

$$R1 = \frac{V_{BATT}}{I_{BIAS}} - R2 = \frac{9V}{100\mu A} - 50K\Omega = 40K\Omega$$

Standard values of 51KΩ and 39KΩ should provide a V_{CIN} divider value of 5.1V. The range of V_{OUT1} is specified as 4.75 to 5.25V and the threshold for turn-on of V_{CIN} is $V_{OUT1} - V_{be}$; where V_{be} is approximately ~0.6V±0.1V volts over the full temperature range. This defines the V_{BATT} range for a low battery LED indicator output, given worse case conditions. Using EQ1 and substituting $V_{CIN} = V_{OUT1} - V_{be}$; we have:

$$V_{BATT} = (V_{CIN} + V_{be}) \times \left(\frac{R1+R2}{R2}\right)$$

The extreme variations for the given conditions result in a low battery indicator V_{BATT} range from 7V to 8.2V.

Using the Current Mult. and Data Comp. in a Full Duplex Signal Transmission

Current loop, data transfer between equipment can be accomplished via one of three ways; Simplex, Half Duplex or Full Duplex. The CA3277 was originally designed to accommodate full duplex, point to point communication between electronic modules within an automobile. Full duplex communication provides for simultaneous, bidirectional data flow from a local transmitter to a remote receiver.

The CA3277 Current Multiplier and Data Comparator can be used to transmit serial data as illustrated in Figure 7. The Data Comparator is internally referenced to (V_{BATT} - 2.9V) and is used to translate the battery voltage data to a microprocessor compatible 5V signal. Also, note that OUT2 must be enabled for proper operation of the Data Comparator. The loop current is controlled by R1 and R2 and is given by

$$I_{LOOP} = \frac{(V_{OUT1} - V_{be} - V_{OL})}{R_{IN}}$$

where R_{IN} is the R1 or R2 value. As previously noted, the V_{be} value is 0.7V and V_{OL} is the Output Low specification for the microprocessor.

Using $V_{OUT1} = 5V$ and $V_{OL} = 0.3V$:

$$I_{LOOP} = \frac{400}{R_{IN}}$$

Current flows from the pull-up resistors R3 and R4 to the transmitting system ground. Either a microprocessor SCI port (Serial Communication Interface) or an input/output port

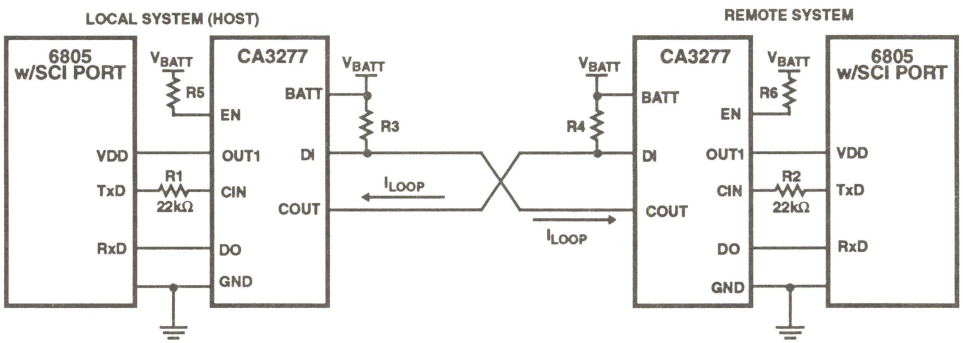


FIGURE 7. USING THE CA3277 FOR FULL DUPLEX SIGNAL TRANSMISSION

can be used to transmit and receive data. A data rate of 9600 baud should be easily attainable in most applications and could potentially be much higher where line impedances are low and a twisted pair, shielded cable is used. The shield should be tied to the system with the lowest source ground impedance.

Using the Current Mult. In Transducer Applications

A transducer responds to the state of a measured quantity such as temperature, light, pressure, etc. and converts this state into a convenient electrical or mechanical quantity. These devices are often used to measure process variables in closed loop systems and can be located hundreds of feet from the system controller. Signal integrity can be compromised if the necessary precautions are not taken in transmitting low-level and nonlinear signals. The measurement of an impedance signal such as a photoconductive or resistive sensing element can be accomplished using the CA3277 Current Multiplier. Figure 8 illustrates a typical circuit configuration where the loop current is given by:

$$I_{LOOP} = \frac{V_{OUT1} - 0.7V - V_{ZENER}}{R_S + R_B}$$

Select R_B such that the loop current is within the CA3277 and transducer current specifications and also insensitive to variations in line impedance (i.e. $R_B >> R_{LINE}$).

Temperature measurement with a thermistor represents a typical application. The nonlinear, resistance-vs-temperature characteristic of a thermistor makes it particularly useful when a large resistance change is needed over a narrow range of temperature. Because of this exponential relation to temperature, the excitation current through the thermistor must be kept to a minimum. Recall that the CA3277 Current Multiplier has a current gain of 100. This will help to minimize the required excitation current and potential errors associated with self heating. A two wire, twisted pair cable with shield should be used to minimize capacitive and normal-mode inductive pickup.

Finding the best static bias point is a common problem in sensor pickup circuits. A sensor's voltage-current characteristic may dictate the need to fix the range of bias current or voltage. This may include the need to add various types of zener diodes and/or diode-resistor circuit configurations. A typical example would be to lower the operating voltage on the sensor to shift the current versus voltage output range. This may be effectively accomplished by adding a zener diode in series with the sensor, as shown for the example of Figure 8.

Programmable Voltage Reference

Many of today's popular microcontrollers like the 68HC05 and 68HC11 have multi-channel analog-to-digital converters (ADC). The microcontrollers provide two reference pins for the conversion of the input signal, V_{REF}(High) and V_{REF}(Low). If the full scale input signal is much less than the reference voltage, the accuracy of the conversion may be compromised. Absolute accuracy can be maximized by using a stable voltage reference that is close to the maximum expected input voltage. The CA3277 lends itself nicely to applications that need a programmable voltage reference. Figure 9 illustrates a possible configuration for setting the reference voltage for a microcontroller ADC. While a resistor divider from OUT1 or OUT2 could be used to establish a stable and accurate reference voltage for V_{REF}(High), it is possible to program an output port from the microprocessor to enable the reference voltage as illustrated in Figure 9. The R_{IN} value selected and adjusted is switched ON to fix the value of reference voltage, V_{REF}. By this method, the battery current drain and dissipation in R_{EXT} is limited in duration to the conversion period. The I_{CIN} equation includes a V_{OL} term; however, this should be less than 0.1V for the normal range of I_{CIN} currents. With added R_{IN} values returned to separate Port Out controls, different values of V_{REF}(High) can be programmed as needed.

The OUT2 (Enabled) supply is used as the voltage source for this application. The input bias current of V_{REF} is typically much less than 1.0µA. Where $V_{REF} = V_{REF}$(High) and I_{COUT} is much greater than I_{REF}, we can assume that the output current is given by

$$\text{EQ1:} \qquad I_{COUT} = \frac{(V_{OUT2} - V_{REF})}{R_{EXT}} = 100 \times I_{CIN}$$

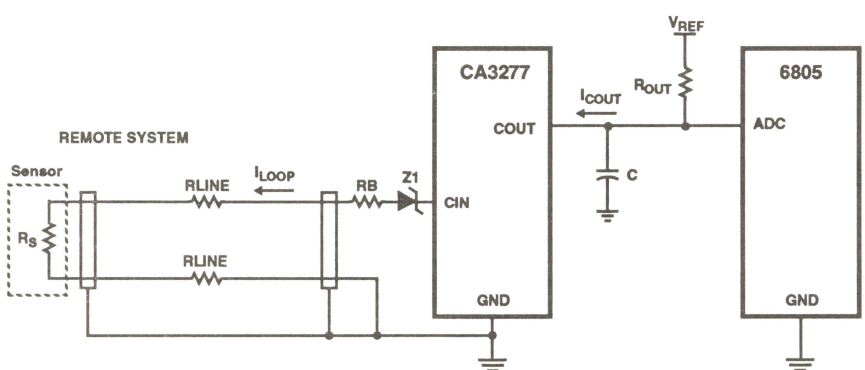


FIGURE 8. ANALOG SIGNAL TRANSMISSION USING THE CA3277 CURRENT MULTIPLIER

The input current equation is given by

$$\text{EQ2:} \qquad I_{CIN} = \frac{5V - V_{be} - V_{OL}}{R_{IN}} = \frac{4.2}{R_{IN}}$$

Combining EQ1 and EQ2 we have:

$$\text{EQ3:} \qquad \frac{R_{EXT}}{R_{IN}} = \frac{(V_{OUT2} - V_{REF})}{420}$$

Where V_{REF} is the desired value for a given ADC input voltage.

Example:

A particular application requires 1.5V reference to accommodate a maximum input voltage of 1.0V. Solve for the external resistor, R_{EXT} and R_{IN}, required to obtain a 1.5V voltage reference for the microcontroller ADC of Figure 9.

Select R_{EXT} such that I_{COUT} = 3.5mA (For a stable Reference voltage). Then from EQ1:

$$R_{EXT} = \left(\frac{V_{OUT2} - V_{REF}}{I_{COUT}}\right) = \frac{3.5V}{3.5mA} = 1K\Omega$$

And $$I_{CIN} = \frac{I_{COUT}}{100} = \frac{3.5mA}{100} = 35\mu A$$

Then, from equation EQ2:

$$R_{IN} = \frac{4.2}{I_{CIN}} = \frac{4.2}{35\mu A} = 120K\Omega$$

An Evaluation PC Circuit Board

For the purposes of bench evaluation, the circuit of Figure 10A with the single layer PC Board layout shown in Figure 10B is suggested as a point of reference for layout recommendations. As shown in the Data Sheet, the output current of each 5V regulator is conservatively rated based on free air heat transfer and a maximum ambient of 85°C. For a given output current and ambient temperature condition the objective is to maintain the IC junction temperature, T_J below the 150°C maximum temperature rating. If the Watt Input to the IC is greater than the conducted plus radiated Watt Output, the chip temperature will continue to increase. The goal is to achieve a balance of Watt Input and Watt Output with the junction temperature of the chip less than or equal to the maximum junction temperature rating.

One approach is to maximize the ground plane under the IC package. Internally, the CA3277 chip rests on the mounting pad of a copper lead frame. The mounting pad is internally connected to the ICs four inner ground pins. The lead frame is designed to maximize thermal conductivity from the IC junction to the IC case (pins 4, 5, 12 & 13) and is rated at θ_{jc} = 14°C/W. The temperature difference between the IC case and the ambient temperature will determine to a large extent the output current capability of each regulator. By increasing the ground plane area under the IC as illustrated in Figure 10B, heat transfer from the IC case is enhanced. The area closest to the IC pins is most significant in attempting to improve the thermal conductivity and output current capability. The layout of Figure 10B is recommended as an economical compromise with good packing density and good layout for heat conduction. Consider the difference in thermal

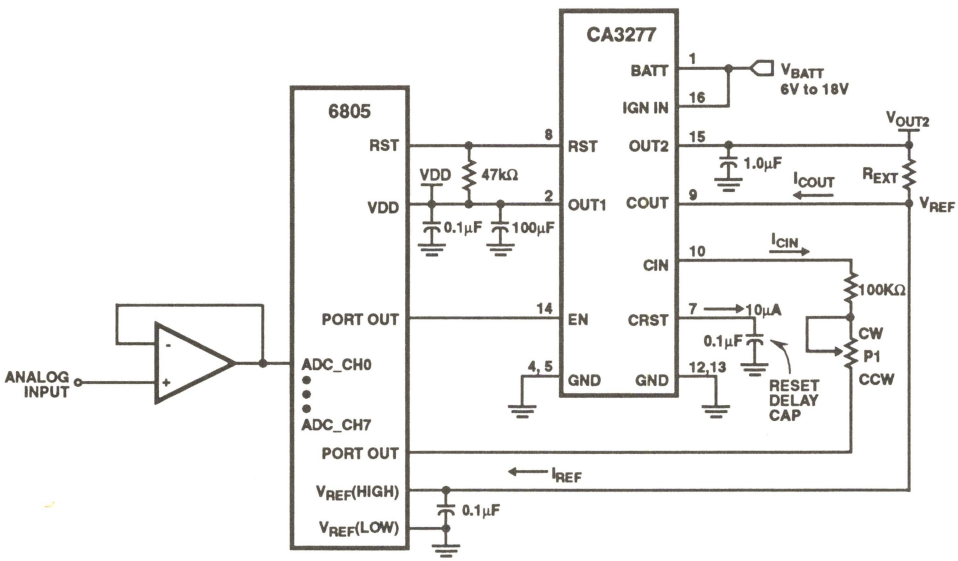


FIGURE 9. PROGRAMMABLE VOLTAGE REFERENCE FOR MICROPROCESSOR APPLICATIONS

conductivity between θ_{JC} = 14°C/W and θ_{JA} = 60°C/W (given as data sheet ratings). Adding ground plane area will help reduce θ_{JA} and enhance output current capability. If the CA3277 resides on a multilayer PC Board, be sure to connect the four ground pins to the inner ground plane. Note: Thermal relief pads are commonly used to enhance solderability. This technique however will reduce the effectiveness of the ground plane as a heat sink. See the CA3277 data sheet for a more detailed discussion on power dissipation.

Example:

Calculate the maximum power dissipation with an ambient temperature of 40°C in free air. Assume the Current Multiplier is not used and no ground plane area is available on the PC Board.I

EQ1: $T_J = T_{AMB} + (P_D \times \theta_{JA}) < 150\ °C$

EQ2: $150 = 40 + (P_{D(MAX)} \times 60)$

Solving EQ1 and EQ2, we have $P_{D(MAX)} = 1.83W$.

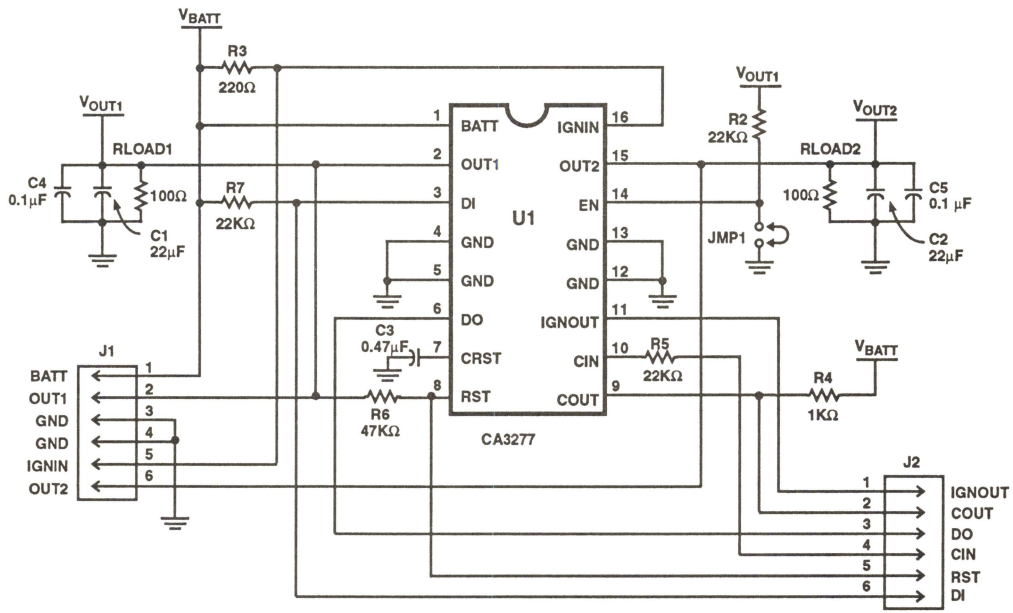


FIGURE 10A. CA3277 EVALUATION PC BOARD

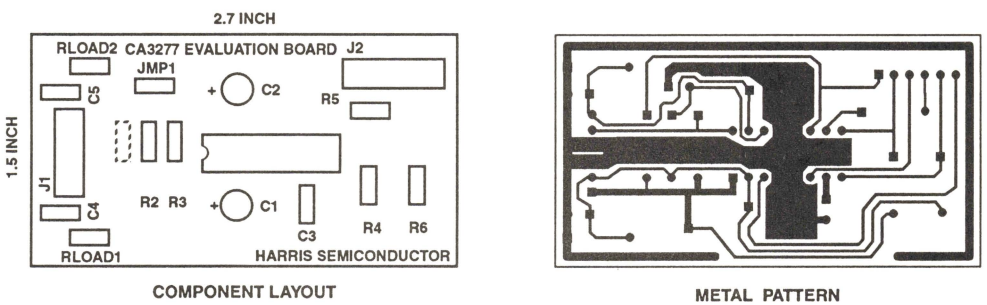


FIGURE 10B. LAYOUT OF CA3277 PC BOARD

Defintion Of Terms

Dropout Voltage: The minimum, differential voltage between the input and output that will maintain output regulation. It is typically load dependent.

Quiescent Current: The input current that does not support the load. Current that flows through the regulator ground lead.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Load Regulation: The change in output voltage for a change in load current at a constant chip temperature.

Acknowledgements

CA3277 Product information and Application Support supplied by W.Austin, Application Engineering, Somerville, NJ

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Harris Semiconductor

APPNOTE

No. AN9304.3 April 1994

Harris Intelligent Power

ESD AND TRANSIENT PROTECTION USING THE SP720

Author: Wayne Austin

The need for transient protection in integrated circuits is driven by the quest for improved reliability at lower cost. The primary efforts for improvement are generally directed toward the lowest possible incidence of over-voltage related stresses. While electrical over-stress (EOS) is always a potential cause for failure; a discipline of proper handling, grounding and attention to environmental causes can reduce EOS causes for failure to a very low level. However, the nature of hostile environments cannot always be predicted. Electrostatic Discharge (ESD) in some measure, is always present and the best possible ESD interface protection may still be insufficient. As the technology of solid state progresses, the occurrence of ESD related IC failures is not uncommon. There is a continuing tendency for both ESD and EOS failures, due in part, to the smaller geometries of today's VLSI circuits.

The solid state industry has generally acknowledged a standard for the level of capability in LSI designs of ±2000V for the Human Body Model where the defined capacitance is 100pF and the series resistance is 1500Ω. However, this level of protection may not be adequate in many applications and can be difficult to achieve in some VLSI technologies. Normal precautions against ESD in the environment of broad based manufacturing are often inadequate. The need for a more rugged IC interface protection will continue to be an established goal.

Historically, it should be recognized that early IC development began to address the ESD problem when standards for handling precautions did not exist. High energy discharges were a common phenomena associated with monitor and picture tube (CRT) applications and could damage or destroy a solid state device without direct contact. It was recognized that all efforts to safe-guard sensitive devices were not totally sufficient. Small geometry signal processing circuits continued to sustain varying levels of damage through induced circulating currents and direct or indirect exposure in handling. These energy levels could be substantially higher than the current standard referenced in Mil-Std-3015.7; also referred to as the Human Body Model.

The recognized need for improved ESD protection was first precipitated under harsh handling conditions; particularly in applications that interfaced to human contact or from the interaction of mechanical parts in motion. The popular features of component and modular electronic equipment have continued to generate susceptibility to IC damage while in continuing use. These market items include computers and peripherals, telecommunication equipment and consumer electronic systems. While some IC's may only see the need for ESD protection while in manufacturing assembly or during service in the field, the most common cause for ESD failures can still be related to a human contact. Moreover, educational efforts have improved today's manufacturing environment substantially reduce failures that relate to the mechanical handling. The ESD failure causes that relate to mechanical handling now have a test standard referred to as a Machine Model which relates to the source of the generated energy.

While the electrical model for an energy source is generally accepted as a capacitor with stored charge and a series resistance to represent the charge flow impedance, the best means to handle the high energy discharge is not so clearly evident. The circuit of Figure 1 illustrates the basic concept that is applied as a method of ESD testing for the Human Body Model. The ESD energy source is shown as a charged capacitor C_D and series connected, source impedance, resistor R_D. The point of contact or energy discharge is shown, for test purposes, as a switch external to the IC. A protection structure is often included on an IC to prevent damage from an ESD energy source. To properly protect the circuit on the IC the on-chip switch, S_S, is closed when a discharge is sensed and shunts the discharge energy through a low impedance resistor (R_S) to ground. It is imperative that the resistance of the discharge path be as low as practical to limit dissipation in the protection structure. It is not essential that the ground be the chip substrate or the package frame. The energy may be shunted via the shortest path external to the chip to an AC or DC ground.

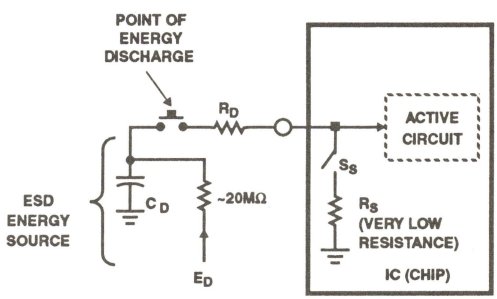


FIGURE 1. ESD TEST FOR AN ON-CHIP PROTECTION CIRCUIT USING THE MIL-STD-883, METHOD 3015.7 (HUMAN BODY MODEL)

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This conceptual method has been used in many IC designs employing a wide variation of structures, depending the IC technology and degree of protection needed. The switch, S_S is generally a threshold sensitive turn-ON at some voltage level above or below the normal signal range; however, it must be within the a safe operating range of the device being protected. The resistance, R_S is shown as the inherent series resistance of the protection structure when it is discharging (dumping) the ESD energy. In its simplest forms, the protection structures may be diodes and zeners, where the sensing threshold is the forward turn-ON or zener threshold of the device. The inherent resistance becomes the bulk resistance of the diode structure when it is conducting. Successful examples of two such protection structures that have been used to protect sensitive inputs to MOS devices are shown in Figure 2. The back-to-back zener structure shown for the dual-gate MOSFET was employed in the 3N - dual gate MOS devices before IC technology was firmly established. The series poly and stacked diode structure used to shunt ESD energy followed several variations for use in CMOS technology and was employ in the CD74HC/HCT - High Speed CMOS family of logic devices. This CMOS protection structure is capable of meeting the 2000V requirements of Mil-Std-883, Method 3015.7; where the R_D in Figure 1 is 1500Ω and C_D is 100pF.

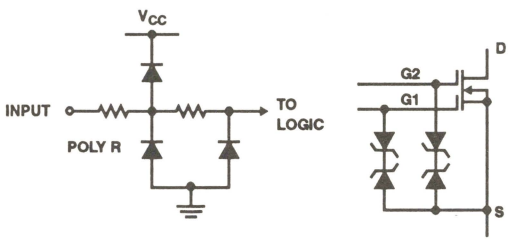


FIGURE 2. ESD AND TRANSIENT PROTECTION EFFECTIVELY USED IN MOS AND CMOS DEVICES

Due to greater emphasis on Reliability under harsh application conditions, more ruggedized protection structure have been developed. A variety of circuit configurations have been evaluated and applied to use in production circuits. A limited introduction to this work was published in various papers by L. Avery (See Bibliography). To provide the best protection possible within economic constraints, it was determined that SCR latching structures could provide very fast turn-ON, a low forward on resistance and a reliable threshold of switching. Both positive and negative protection structures were readily adapted to bipolar technology. Other defining aspects of the protection network included the capability to be self-protecting to a much higher level than the signal input line being protected. Ideally, when a protection circuit is not otherwise needed, it should have no significant loading effect on the operating circuit. As such, it should have very little shunt capacitance and require minimal series resistance to be added to the signal line of the active circuit. Also, where minimal capacitance loading is essential for a fast turn-ON speed, the need for a simpler structure is indicated.

The switching arrangement for a basic and simple protection structure is shown in Figure 3. Each high side and low side protection structure (R_S and S_S) is an embedded device, taking advantage of the P substrate and epitaxial N material used in bipolar technology. Each cell contains an SCR with a series dropping resistor to sense an over-voltage turn-ON condition and trip the SCR (Switch S_S) into latch. The ON-resistance (R_S) of the latched SCR is much lower than R_D and, depending on the polarity of the ESD voltage, dumps energy from the input signal line through the positive or negative switch to ground. The return to ground for either ESD polarity is not limited by voltage supply definition, but may be to positive or negative supply lines, if this suits the needs of the application. When the energy is dissipated and forward current no longer flows, the SCR automatically turns-OFF.

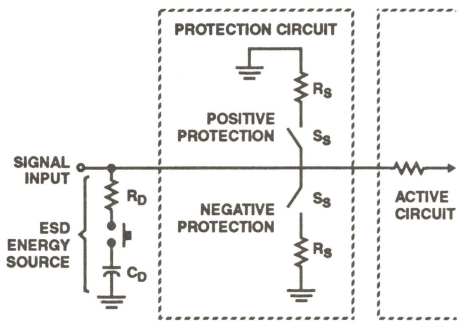


FIGURE 3. ESD AND TRANSIENT PROTECTION CIRCUIT

Figure 4 shows the diagram of a positive and negative cell protection circuit as it applies to the SP720. The PNP and NPN transistor pairs are used as the equivalent SCR structures. Protection in this structure allows forward turn-ON to go marginally above the +V supply to turn-ON the high-side SCR or marginally below the -V supply to turn-ON the low-side SCR. The signal line to the active device is protected in both directions and does not add series impedance to the signal input line. A shunt resistance is used to forward bias the PNP device for turn-ON but is not directly connected to the signal line. As an on-chip protection cell, this structure may be next to the input pad of the active circuit; which is the best location for a protection device. However, for many applications, the technology of the active chip may not be compatible to structures of the type indicated in Figure 4. This is particularly true in the high speed CMOS where the substrates are commonly N type and connected to the positive supply of the chip. The protection cell structure shown in Figure 4 is not required to be on the active chip because it does not sense series input current to the active device. The sense mechanism is voltage threshold referenced to the V+ and V- bias voltages.

The cell structure of the SCR pair of Figure 4 are shown in the layout sketch and profile cutouts of Figure 5. It should be noted that the layout and profiles shown here are equivalent structures intended for tutorial information. The structures are shown on opposite sides of the 'IN" chip bonding pad, as is the case for the SP720. As needed for a preferred layout, the structures are adjacent to the pad and as close to the

positive and negative supply lines as possible. The common and best choice for effective layout is to provide a ground ring (V-) around the chip and to layout with minimum distance paths to the positive supply (V+). In the SP720 the V- line is common to the substrate and frame ground of the IC.

The equivalent circuit diagram of the SP720 is shown in Figure 6. Each switch element is an equivalent SCR structure where 14 positive and negative pairs as shown in Figure 4 are provided on a single chip. Each positive switching structure has a threshold reference to the V+ terminal, plus one V_{BE} (based-to-emitter voltage equal to one diode

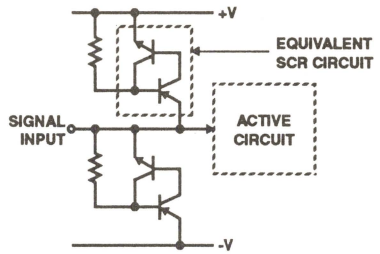


FIGURE 4. PROTECTION CELLS OF THE SP720 SCR ARRAY

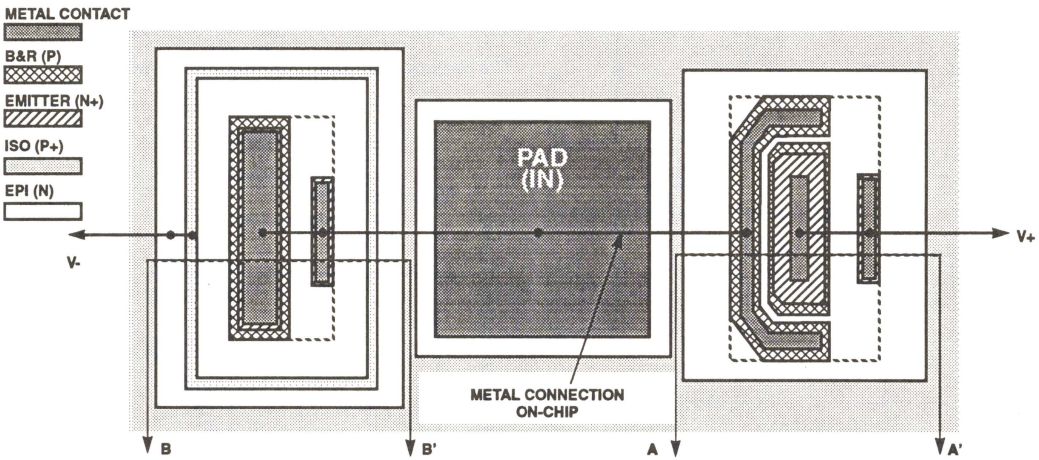


FIGURE 5A. HIGH AND LOW CELL PAIR LAYOUT; SHOWN WITHOUT PROTECT, METAL AND FIELD OXIDE LEVELS (NOT TO SCALE)

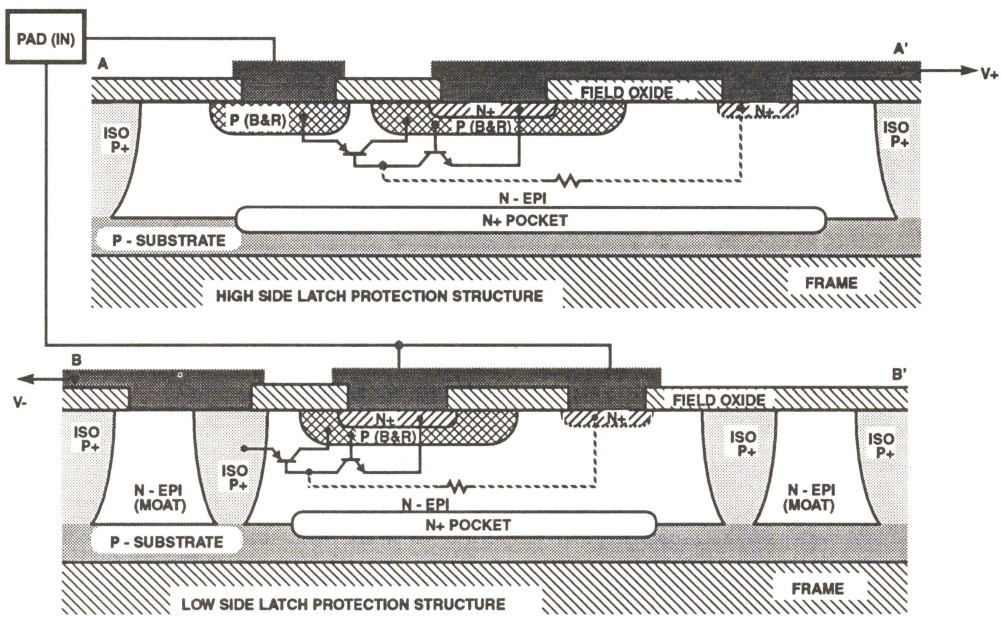


FIGURE 5B. PROFILES OF THE HIGH AND LOW SIDE SP720 SCR PROTECTION PAIR (NOT TO SCALE)

forward voltage drop). Similarly, each negative switching pair is referenced to the V- terminal minus one V_{BE}.

The internal protection cells of the SP720 are directly connect to the on-chip power supply line (+V) and the negative supply line (-V), which are substantial in surface metal content to provide low dropping resistance for the high peak currents encountered. Since both positive or negative transients can be expected, the SCR switches direct the positive voltage energy to V+ and the negative voltage sourced energy to V- (substrate) potential to provide fast turn-ON with low ON resistance to protect the active circuit.

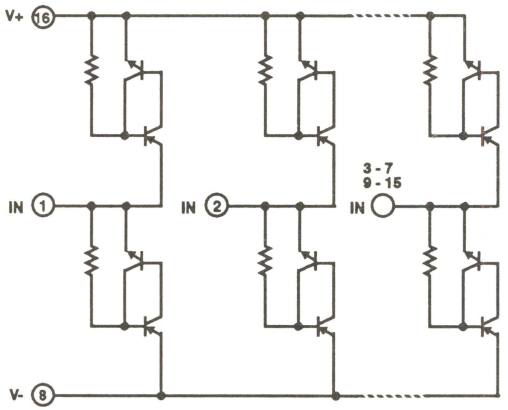


FIGURE 6. EQUIVALENT CIRCUIT DIAGRAM OF THE SP720

The V+ and V- supply lines of the SP720 are not required to be the same as those of the circuit to be protected. However, over-voltage protection is referenced to the V+ and V- supply voltages for all of the signal input terminals, IN1-IN7 and IN9-IN15. The V+ and V- supply voltages to the SP720 may be changed to suite the needs of the circuit under protection. The range of voltage may be power supply levels ranging from 4.5V up to the 35V maximum rating of the SP720. Lower levels of voltage are possible but with some degradation of the switching speed which is nominally 6ns. Also, the input capacitance which is nominally 3pF can be expected to increase. There is no significant quiescent current in the SP720 other than reverse diode junction current which nominally less than 50nA over the rated -40°C to +105°C operating temperature. At room temperatures, this may be as low as a few nanoamperes. Because of the low dissipation of the SP720, the chip temperature can be expected to be close to the environment of the physical location where it is applied to use.

Protection Levels of the SP720

For a given level of voltage or power, there is a defined degree of protection compatible to that need. For the SP720, the protection circuits are designed to clamp over-voltage within a range of peak current that will substantially improve the survival input expectancy of average monolithic silicon circuits used for small signal and digital processing applications. Within itself, the SP720 should be expected to survival peak current and voltage surges within the maximum ratings defined in the data sheet. For voltage, the static DC and short duration transient capability is essentially the same. The process capability is typically better than 45 volts, allowing maximum continuous DC supply ratings to be conservatively rated at 35 volts. The current capability of any one SCR section is rated at 2A peak but is duration limited by the transient heating effect on the chip. As shown in Figure 7, the resistance of the SCR, when it is latched, is approximately 0.96Ω and the SCR latch threshold has 1.08V of offset. For EOS, the peak dissipation can be calculated as follows:

For: 2A Peak Current, R_D = 1500Ω,

Then: $V_{IN(PK)}$ = 1.08V (Offset) + (0.96Ω x 2A) = 3V

The peak dissipation is P_D = 3V x 2A = 6 Watts

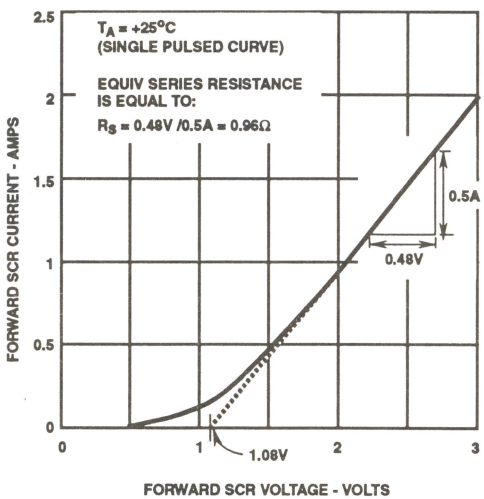


FIGURE 7. SCR FORWARD CURRENT vs VOLTAGE CHARACTERISTICS

While 2A through 1500 ohms is 3000V, which is not an exceptionally high ESD level of voltage, it does represent the EOS capability, provided the time duration for the 6 Watts of dissipation is limited to a few milliseconds. The dissipation of the 16 pin DIP and 16 pin SOIC packages are typically less than 1 Watt for steady state conditions. The thermal capacity of the chip will allow discharge levels several times higher than this because ESD normally has a much shorter duration. The actual results for ESD tests on the SP720 as an isolated device are as follows:

1. Human Body Model using a modified version of the Mil-Std-883, Method 3015.7; with V+ and V- grounded and ESD discharge applied to each individual IN pin - Passed all test levels from ±9KV to ±16KV (1KV steps).
2. Human Body Model using the Mil-Std-883, Method 3015.7 (with V- only grounded) and ESD discharge applied to each individual IN pin - Passed all test levels to ±6KV, failed ±7KV (1KV steps).

3. Machine Model using EIAJ IC121 (R_D = 0Ω); discharge applied to IN pins with all others grounded - Passed all test levels to ±1KV, failed ±1.2KV; (200V steps).

4. While there are many potential uses for the SP720, the circuit of Figure 8 shows a normal configuration for protecting input lines to a sensitive digital IC. Each line is connected to an IN- Input of the SP720 in a shunt connection. As a test model a 2μ digital ASIC CMOS IC was used to evaluate the ESD level of capability provided by the SP720. Without external protection, the ESD level of capability of the CMOS process was typically no better than ±2.5KV. When the SP720 was applied to use as shown in Figure 8, the ESD resistance to damage was better than ±10.2KV. (Higher levels were not evaluated at the time due to high voltage limitations.)

It should be noted that the Mil-Std-883, Method 3015.7 test allows for one pin as a reference when testing. While this cannot be disputed as handling limitation, it is not a test for all aspects of applied use. To properly apply the SP720 to use in the application specifically requires that the V- pin be connected to a negative supply or ground and the V+ pin be connected to a positive supply. The SP720 was designed to be used with the supply terminals bias and, as such, has better than ±16KV of ESD capability. For this reason, the modified test method as described, with the V+ pin connected via a ground return, is correct when the circuit is assembled for use.

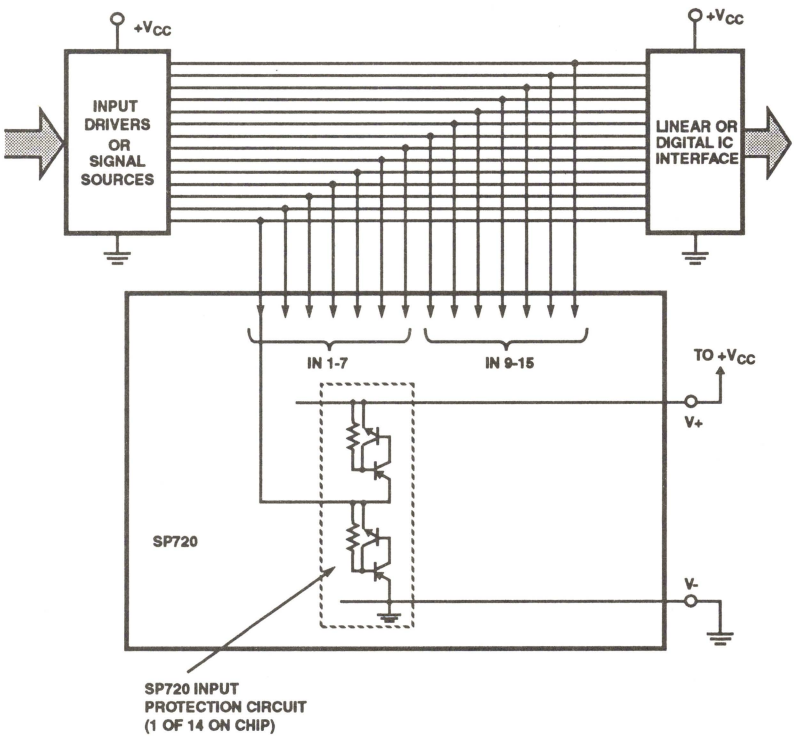


FIGURE 8. PRACTICAL APPLICATION AND TEST EVALUATION CIRCUIT

SP720 CMOS Protection Model

Where the need to provide ESD protection for CMOS circuits is the primary interest for the application of the SP720, interface characteristics of the device to be protected may lead to some specific problems. Application related issues and precautions are discussed here to assist the circuit designer in achieving maximum success in EOS/ESD protection.

CMOS Input Protection

CMOS logic has limited on-chip protection and may contain circuit elements that add difficulty to the task of providing external protection. Consider the case where the input structure of a CMOS device has on-chip protection but only to the extent that it will withstand Human Body Model minimum requirement for ESD when tested under the Mil-Std-883, Method 3015.7. This is normally ±2KV where the charged capacitor is 100pF and the series resistor to the device under test is 1500Ω. The circuit of Figure 9 shows the typical network for an HC logic circuit where the input polysilicon resistor, R_P is typically 120Ω.

When there is a surge or ESD voltage applied to the input structure, the diodes shunt current to V_{CC} or GND to protect the logic circuits on the chip. The on-chip series resistors limit peak currents. If there is a positive transient voltage, $V_{CS}(t)$, applied to the input of the CMOS device, the diode, D_1 will conduct when the forward voltage threshold exceeds the power supply voltage, V_{CC} plus the forward diode voltage drop of D_1, V_{FWD1}. As the voltage at the input is further increased, the CMOS current, I_{CS} is shunted through R_P and D_1 to V_{CC} such that the transient input voltage is

(1) $V_{CS}(t) = I_{CS}(t) \cdot R_P + V_{FWD1} + V_{CC}$ [for Pos. $V_{CS}(t)$]

or

(1a) $I_{CS}(t) = [V_{CS}(t) - (V_{FWD1} + V_{CC})]/R_P$

Similarly, when there is a negative transient, current initially conducts at the negative threshold of diode D_2, V_{FWD2} to shunt negative current at the input, i.e.

(2) $V_{CS}(t) = I_{CS}(t) \cdot R_P + V_{FWD2}$ [for Neg. $V_{CS}(t)$]

or

(2a) $I_{CS}(t) = [V_{CS}(t) - V_{FWD2}]/R_P$

While the circuit of Figure 9 is specifically that of the HC logic family (one cell of the Hex Inverter, 74HCU04), many CMOS devices have a similar or an equivalent internal protection circuit. When compared to the SCR structure of the SP720, the on-chip diodes of the protection network in Figure 9 have lower conduction thresholds.

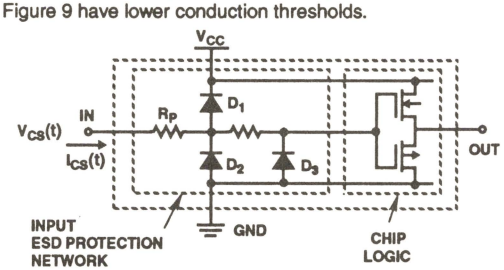


FIGURE 9. TYPICAL CMOS IC INPUT PROTECTION CIRCUIT

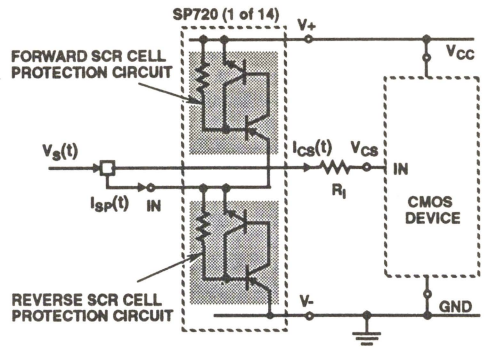


FIGURE 10. SP720 SCR INTERFACE TO A CMOS INPUT WITH R_I ADDED TO ILLUSTRATE MORE EFFECTIVE ESD PROTECTION FOR CMOS DEVICES

SP720 to CMOS Interface

Figure 10 shows the SCR cell structures of one protection pair in the SP720. In this example, the V+ of the SP720 is connected to the V_{CC} logic supply and the V- is connected to logic GND. The IN terminal of the SP720 is connected to the CMOS logic device input through a resistor R_I. When a negative transient voltage is applied to the input circuit of Figure 10, the Reverse SCR Protection Circuit turns on when voltage reaches the forward threshold of the PNP device and current conducts through the SCR resistor to forward bias the PNP transistor. The PNP device then supplies base current to forward bias and turn on the NPN device. Together, the PNP and NPN transistors form an SCR which is latched on to shunt transient current from IN to V-. The Forward SCR Protection Circuit has the same sequence for turn on when a positive transient voltage is applied to the input and conducts to shunt transient current from IN to V+ (V_{CC}).

The Voltage-Current characteristic of the SCR is similar to a diode at low currents but changes to low saturated on resistance at high currents. As shown in the SP720 data sheet, the forward SCR (latched on) voltage is ~1V at 60mA which is ~0.2V higher than a typically junction diode. The fully saturated turn on approaches 0.5A at 1.5V. When the SCR is paralleled with the a CMOS device input having an on-chip protection circuit equivalent to Figure 9, some of the current necessary to latch the SCR is shunted into the CMOS input. For some devices this may be sufficient for an ESD discharge to damage the CMOS input structure before the SP720 is latched on.

The trade-off for achieving a safe level of ESD protection is switching speed. The most effective method is the addition of the series resistor, R_I as shown in Figure 10. The series input resistor, as shown, is a practical method to limit current into the CMOS chip during the latch turn on of the SP720 SCR network. The value of R_I is dependent on the safe level of current that would be allowed to flow into the CMOS input and the loss of switching speed that can be tolerated. The level of transient current, I_{CS} that is shunted into the CMOS device is determined by the series resistor, R_I and the volt-

age developed across the CMOS protection devices, R_P and D_1 or D_2, plus some contribution from the path of diode, D_3 for negative transients.

As shown in Figure 11, the voltage across the SP720 SCR element is determined by its turn on threshold, V_{TH} and the saturated resistance, R_S when latched. The empirically derived equation for the voltage drop across the SP720 voltage is

(3) $V_{SP}(t) = I_{SP}(t) \cdot R_S + V_{TH}$

or

(3a) $I_{SP}(t) = [V_{SP}(t) - V_{TH}]/(R_S)$

where $V_{TH} \sim \pm 1.1V$ and $R_S \sim 1\Omega$.

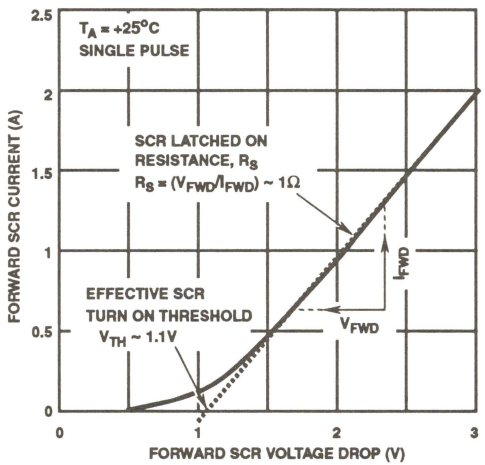


FIGURE 11. FORWARD TURN ON CHARACTERISTIC OF AN SP720 SCR CELL

where current conduction in the SP720 may be positive or negative, depending on the polarity of the transient. For the circuit of Figure 10, $V_S(t)$ is also the input voltage to the resistor, R_I in series to the input of the CMOS device. When latched on, the impedance of the SP720 is much less than the input impedance of either R_I or the CMOS input protection circuit. Therefore, the CMOS loop current can be determined by the voltage, $V_S(t)$ and the known conditions from equation (3).

For a **negative** transient input to the CMOS HCU04, the loop equation is

(4) $V_S(t) = I_{CS}(t) \cdot (R_I + R_P) + V_{FWD2}$

or

(4a) $I_{CS}(t) = [V_S(t) - V_{FWD2}]/(R_I + R_P)$

An equation solution for an input transient may be more directly solved by empirical methods because of the non-linear characteristics. Given a transient voltage, $V_S(t)$ at the input, a value for R_I can be determined for a safe level of peak current into a CMOS device. The input Voltage-Current characteristic of CMOS device should be known. As a first order approximation, the CMOS V-I curve tracer input characteristics of the 74HCU04 are shown in Figure 12. As indicated in Figure 12, the voltage drop across R_P and R_I in series ($R_P \sim 120\Omega$) will be significantly larger than the delta changes in the forward voltage drop of the D_1 or D_2 diodes over a wide range of current. As such, we can effectively assume $V_{FWD} \sim 0.75V$ for moderate levels of current.

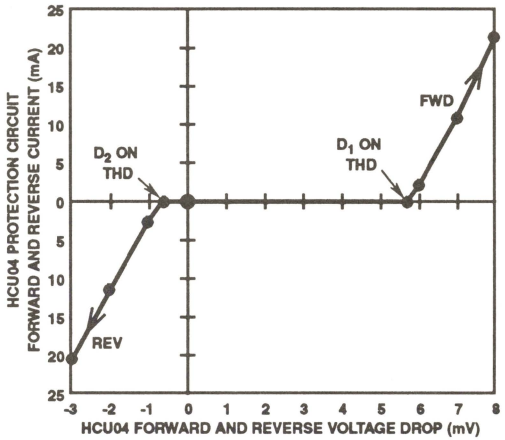


FIGURE 12. FORWARD AND REVERSE PROTECTION CIRCUIT INPUT VOLTAGE-CURRENT CHARACTERISTIC OF THE HCU04 SHOWN FOR V_{CC} = 5V, (I.e. D_1 THD ~ 5V + 0.7V)

Example Transient Solution

Based on the circuit of Figure 10, negative and positive ESD discharge circuit models of the SP720 and HCU04 are shown in Figure 13A and 13B. The negative ESD voltage is taken as the worse case condition because a positive ESD voltage will discharge to the V_{CC} power supply and the positive offset voltage will reduce the forward current. Using the negative model, a peak current value for I_{SP} can be determined by the transient conditions of the applied voltage, $V_S(t)$ at the input.

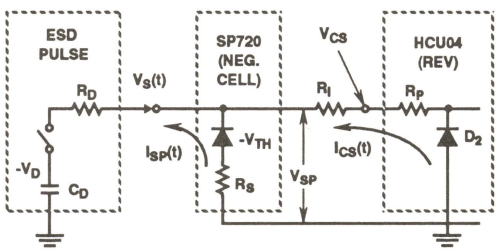


FIGURE 13A. NEGATIVE ESD DISCHARGE MODEL

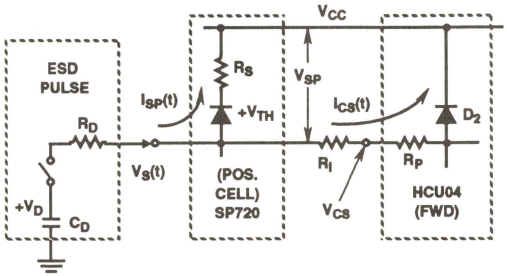


FIGURE 13B. POSITIVE ESD DISCHARGE MODEL

Given Mil-Std ESD HBM test conditions (C_D = 100pF and R_D = 1500Ω), equation (3) with the resistors R_D and R_S in series, we can calculate the peak current for a specified voltage, V_D on the capacitor, C_D.

(5) $$I_{SP}(t) = [V_D(t) - V_{TH}]/(R_D + R_S) \sim V_D(t)/R_D$$

Here, V_D replaces V_S as the driving voltage; and assumes that (1) R_S is much less than R_D; (2) R_S is much less than (R_I+R_P); and (3) V_{TH} is much less than V_D. This may or may not be the general case but is true for the values indicated here. As such,

$$[I_{SP}]_{t=0} \sim V_D/1500.$$

Given an ESD discharge of -15KV, neglecting inductive effects and distributed capacitance, the peak current at time t = 0 will be ~10A. And, with the SP720 latched on as shown in Equation (3), the 10A peak current will result in an ESD pulse at the input of the SP720 of ~11V. For the HCU04 to withstand this surge of voltage, it is required that the dropping resistor, R_I attenuate the peak voltage, V_{CS} at the HCU04 input to within acceptable ratings.

The negative reverse current path is through R_I, R_P and D_2; where R_P and D_2 are part of the HCU04. For a negative ESD discharge voltage, V_D from capacitor C_D, the equation for the peak voltage, V_{CS} at the input to the HCU04 is derived as follows:

Substituting Equation (5) into Equation (3), we have

(6) $$V_S \sim (V_D/R_D)\bullet R_S - 1.1$$

and from equation (2) and (4a), a general solution for the V_{CS} voltage is

(7) $$V_{CS} = [(V_S - V_{FWD2})/(R_I + R_P)]\bullet R_P + V_{FWD2}$$

For a simpler approach, one can work backwards to arrive at the correct solution. The reverse CMOS voltage vs current curve of Figure 11 indicates that a peak voltage, V_{CS} of -3V will produce a negative current of approximately -20mA which is the rated absolute maximum limit. For a -15KV ESD discharge and from Equation (6), the peak voltage, V_S is

$$V_S = (V_D/R_D)\bullet R_S - 1.1 = (-15/1500) - 1.1 = -11.1V$$

The peak current, I_{CS} from equation (4a) is

$$I_{CS} = [(V_S - V_{FWD2})/(R_I + R_P)]$$
$$= [(-11.1 - (-0.7))]/(R_I + 120\Omega)$$

Given the I_{CS} current of -20mA and solving for R_I,

$$R_I = 397.5\Omega$$

The same result can be derived from equation (7) but is more susceptible to rounding errors and the assumed voltage drop of V_{FWD2} due to the (V_{CS} - V_{FWD2}) difference that appears in the equation.

The approximation solution given here is based on a ±20mA current rating for the HCU04 device; although, input voltage ratings are exceeded at this level of current. As such, the solution is intended to apply only to short duration pulse conditions similar to the Mil-Std-883, Method 3015.7 specifications for ESD discharge conditions. For long periods of sustained dissipation, the SP720 is limited by the rated capability of its package.

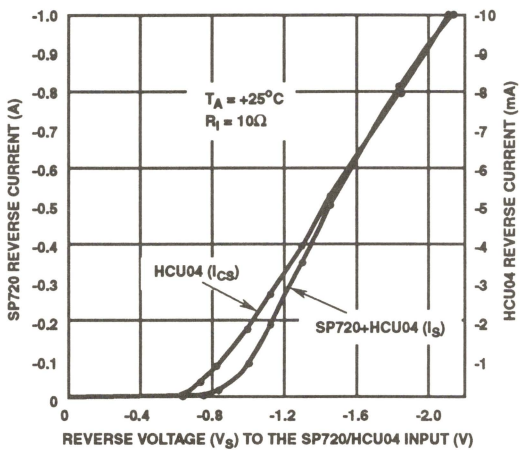


FIGURE 14. MEASURED REVERSE CURRENT vs VOLTAGE CHARACTERISTIC OF THE SP720/HCU04 FOR THE FIGURE 10 CIRCUIT PROTECTION MODE

Figure 14 shows the distribution of currents for the circuit of Figure 10 given a specific value of R_I. Curves are shown for both I_S (HCU04 + SP720) and I_{SP} (SP720) versus a negative input voltage, V_S. The resistor, R_I value of 10Ω is used here primarily to sense the current flow into the HCU04. (This data was taken with the unused inputs to the HCU04 connected to ground and the unused inputs to the SP720 biased to V_{CC}/2 on a resistive divider.) The Figure 14 curves verify the model condition of Figure 13A with the exception that resistive heating at higher currents increases the resistance in the latched on SCR. This curve explains the ESD protection of the Harris High Speed Logic "HC" family and, in particular, demonstrates the value of the R_P internal resistor as protection for the HCU04 gate input. Added series resistance external to a signal input is always recommended for maximum ESD protection.

Range of Capability

While the SP720 has substantially greater ESD self protection capability than small signal or logics circuits such as the HCU04, it should be understood that it is not intended for

interface protection beyond the limits implied in the data sheet or the application note. The Mil-Std-883, Method 3015.7 condition noted here defines a human body model of 100pF and 1500Ω where the capacitor is charged to a specified level and discharged through the series resistor into the circuit being tested. The capability of the SP720 under this condition has been noted as ±15KV. And, for a machine model where no resistance is specified, a 200pF capacitor is discharged into the input under test. For the machine model the level of capability is ±1KV; again demonstrating that the series resistor used in the test or as part of the application circuit has pronounced effect for improving the level of ESD protection.

While a series resistor at the input to a signal device can greatly extend the level of ESD protection, a circuit application, for speed or other restrictions, may not be tolerant to added series resistance. However, even a few ohms of resistance can substantially improve ESD protection levels. Where an ESD sensitive signal device to be protected has no internal input series resistance and interfaces to a potentially damaging environment, added resistance between the SP720 and the device is essential for added ESD protection. Circuits often contain substrate or pocket diodes at the input to GND or V_{CC}. and will shunt very high peak currents during an ESD discharge. For example, if the HCU04 of Figure 14 is replaced with device having a protection diode to ground and no series resistor, the anticipated increase in input current is 10 times.

Shunt capacitance is sometimes added to a signal input for added ESD protection but, for practical values of capacitance, is much less effective in suppressing transients. For most applications, added series resistance can substantially improve ESD transient protection with less signal degradation.

A further concern for devices to be protected is forward or reverse conduction thresholds within the power supply range (not uncommon in analog circuits). Depending on the cost considerations, the power supply V+ and V- levels for the SP720 could be adjusted to match specific requirements. This may not be practical unless the levels are also common to an existing power supply. The solution of this problem goes beyond added series resistance for improved protection. Each case must be treated with respect to the precise V-I input characteristics of the device to be protected.

Interface and Power Supply Switching

Where separate system components with different power supplies are used for the source signal output and the receiving signal input, additional interface protection circuitry maybe needed. The SP720 would normally have the same power supply levels as the receiving (input) device it is intended to protect. When the SP720 with its receiving interface circuit is powered off, a remote source signal may be activated from a separate supply (i.e., remote bus connected systems). The user should be aware that the SP720 remains active when powered down and may conduct current from the IN input to the V+ (or V-) supply.

Within its own structure, **any** IN input of the SP720 will forward conduct to V+ when the input voltage increases to a level greater than a V_{BE} threshold above the V+ supply. Similarly, the SP720 will reverse conduct to V- when the input voltage decreases to a level less than a V_{BE} threshold below the V- supply. Either condition will exist as the V+ or V- level changes and will continue to exist as the V+ collapses to ground (or V-) when the SP720 supply is switched off. If a transient or power surge is provided from the source input to the IN terminal of the SP720, after the V+ has been switched off, forward current will be conducted to the V+/V_{CC} power supply line. Without a power supply to clamp or limit the rising voltage, a power surge on the input line may damage other signal devices common to the V_{CC} power supply. Bypassing the V_{CC} line may not be adequate to protect for large energy surges. The best choice for protection against this type of damage is to add a zener diode clamp to the V_{CC} line. The zener voltage level should be greater than V_{CC} but within the absolute maximum ratings of all devices powered from the V_{CC} supply line.

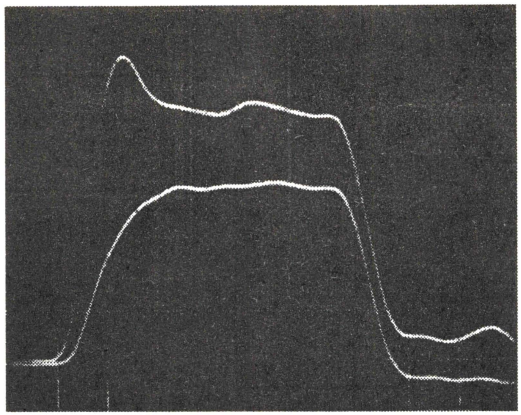
Power Supply Off Protection, Rise/Fall Speed

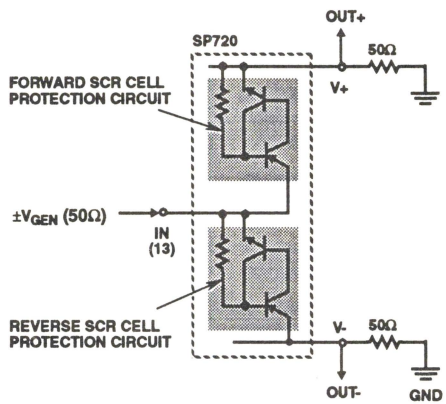
To illustrate the active switching of the SP720 and the speed of the SCR for both turn on and turn off, oscilloscope traces were taken for the circuit conditions of Figure 15. A pulse input signal is applied with **NO** supply voltage applied to the SP720. Figure 15 shows the positive and negative pulse conditions to V+ and V- respectively. The trace scales for Figure 15 are 10ns/division horizontal and 1V/division vertical. Input and output pulses are shown on each trace with the smaller pulse being the output. The smaller output trace is due to an offset resulting from the voltage dropped across the SCR in forward conduction. The OUT+ and OUT- pulses quickly respond to the rising edge of the input pulse, following within ~2ns delay from the start of the IN pulse and tracking the input signal. The output falls with approximately the same delay.

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POSITIVE/FORWARD CONDUCTION
HIGH SPEED ON/OFF PULSE (OUT+)





NEGATIVE/REVERSE CONDUCTION
HIGH SPEED ON/OFF PULSE (OUT-)

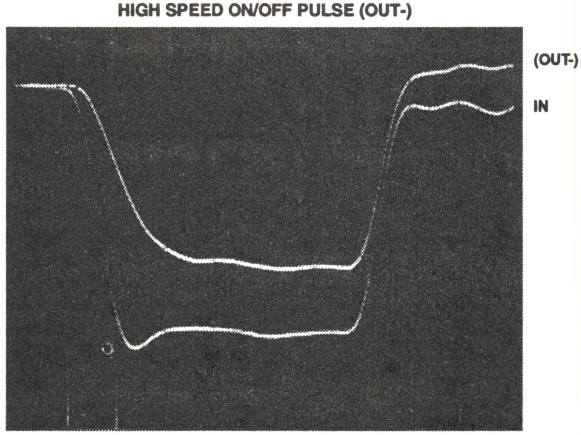


FIGURE 15. SP720 CIRCUIT WITH NO POWER SUPPLY INPUT PULSE TEST WITH 50Ω, (0V TO ±5V) INPUT. THE TRACE SCALES FOR OUT+ AND OUT- ARE 1V/DIV VERTICAL AND 10ns/DIV HORIZONTAL

APPNOTE

No. AN9323.1 April 1994

HIP5061 HIGH EFFICIENCY, HIGH PERFORMANCE, HIGH POWER CONVERTER

Authors: Charles Hawkes, Tom Jochum and Hal Wittlinger

Introduction

As the complexity of sophisticated, modern day equipment grows, the need for high efficiency, high performance and high power converters continues to expand. Demand for smaller, lighter, more efficient supplies for this equipment is addressed by the HIP5061. The HIP5061 contains a 60V, 5A (7A minimum at <30% duty cycle, 5A at DC) DMOS power transistor with an $r_{DS(ON)}$ of approximately 0.18Ω. This low $r_{DS(ON)}$ of the switching device permits high rms currents without excessive device dissipation. The IC is housed in a 7 lead, TO220 style package. By including a DMOS power transistor with its associated driver and the current-mode PWM control circuitry within a single package, simplification and improved performance of many power supply systems can be achieved. This note explains the operation and proper application of the HIP5061 so that this high performance device can be utilized. A 50W, 28V boost converter will be presented to demonstrate a typical application of the IC. Supplies using an external high voltage, power MOSFET transistor in a cascode configuration with the internal DMOS transistor can have higher power outputs, many in excess of 200W.

Operation in a Typical Application Circuit

Figure 1 shows a Simplified Block Diagram of the HIP5061 in a typical Boost converter. A resistor connected from the V_{IN} supply to the V_{DD} terminal of the IC powers the internal 14V shunt regulator. The Gate Driver supply is decoupled from the main supply by a small external resistor connected between V_{DD} and the V_G terminal. A bypass capacitor is connected between the V_{DD} terminal and ground to reduce coupling between analog and digital circuitry. A Schottky diode insures efficient energy transfer from the DMOS drain circuit inductor to the load. To set the output voltage, two resistors are used to scale the output supply voltage down to the 5.1V internal reference.

The heart of the IC is the high current DMOS power transistor with its associated gate driver and high-speed peak current control loop. A portion of the converter's DC output is applied to a transconductance error amplifier that compares the fed back signal with the internal 5.1V reference. The output of this amplifier is brought out at the V_C terminal to provide for soft start and frequency

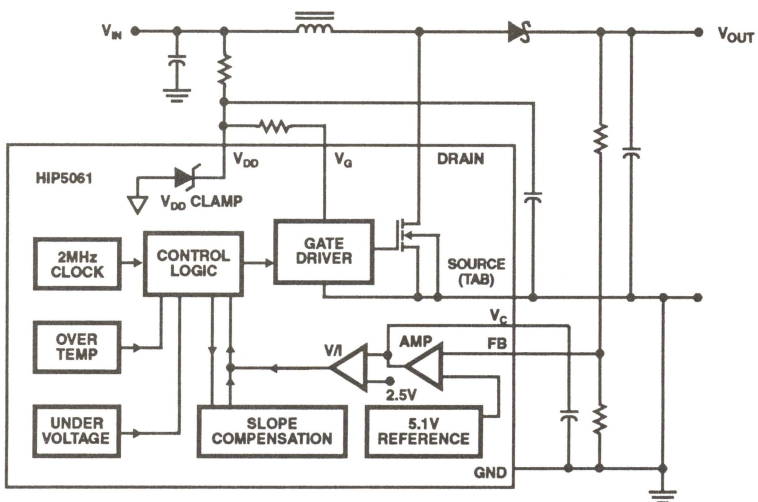


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF THE HIP5061 IN A TYPICAL "BOOST" CONFIGURATION

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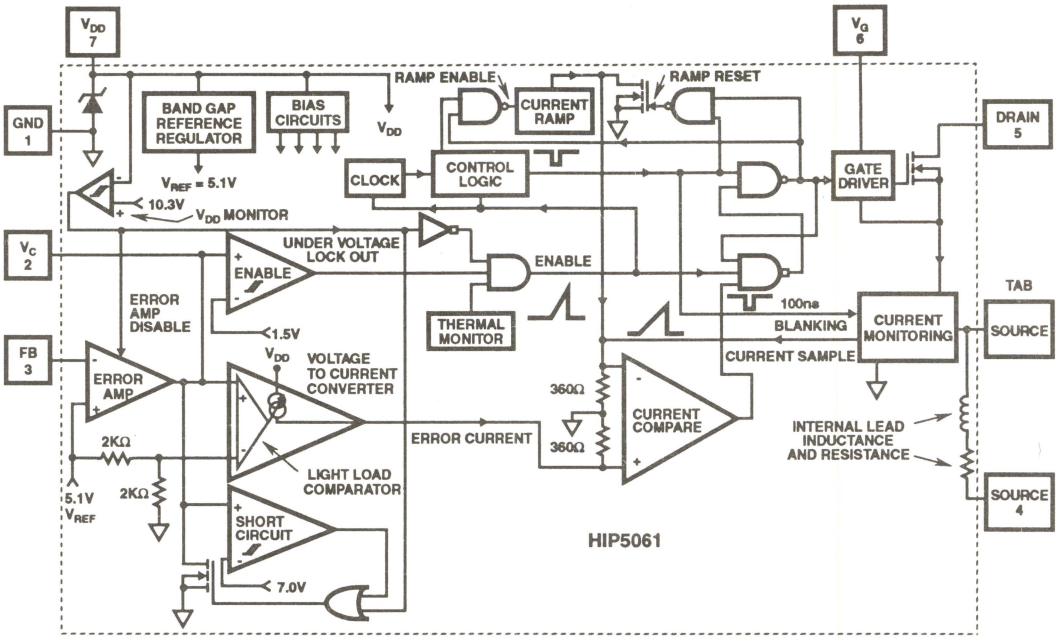


FIGURE 2. FUNCIONAL BLOCK DIAGRAM OF THE HIP5061

compensation of the control loop. This same signal is also applied internally to program the peak DMOS transistor drain current. To assure precise current control, the response time of this peak current control loop is less than 50ns.

A 2MHz internal clock provides all the timing signals for the converter operating at 250kHz. A slope compensation circuit is also incorporated within the converter IC to eliminate sub-harmonic oscillation that occurs in continuous-current mode converters operating with duty cycles greater than 50%.

HIP5061 Description of Operation

Figure 2 shows a more detailed Functional Block Diagram of the HIP5061. An internal 14V shunt regulator in conjunction with an external series resistor provides internal operating voltage to the IC in applications where no 12V auxiliary supply is available. Note that in applications where the input voltage at V_{DD} is 12V, ±10%, the regulator is not used. This regulator is shown as a zener diode on the diagrams of Figure 1 and Figure 2.

The 2MHz clock is processed in the Control Logic block to provide various timing signals. A cycle of operation begins when a 100ns pulse (which occurs at a 4µs interval) triggers the latch that initiates the DMOS transistor on-time. This pulse also provides a blanking interval in the Current Monitoring block to eliminate false turn-offs caused by high transient pulse currents that occur during turn-on. The output of the Current Ramp block is summed with the sensed DMOS transistor current (to provide slope compensation) before being compared with the Error Current signal. The current ramp, -0.45A/µs, is inhibited for the first 1.5µs (37.5%) of the duty cycle by the Ramp Enable signal, since ramp is not needed for slope compensation during this interval. Inhibiting of the compensating ramp has the effect of reducing the peak short-circuit current.

The output of the power supply is divided down and monitored at the FB terminal. A transconductance error amplifier compares the dc level of the fed back voltage with an internal bandgap reference, while providing voltage loop compensation by means of external resistors and capacitors. The Error Amplifier output (the error voltage) is then converted into a current (the Error Current) that is used to program the required peak DMOS transistor current that produces the desired output voltage. When the sum of the sensed DMOS transistor current and the compensating Current Ramp exceed the Error Current signal, the latch is reset and the DMOS transistor is turned off. Current comparison around this loop takes place in less than 50ns, allowing for excellent 250kHz converter operation. The latch can also be reset by an under-voltage (V_{DD} < 10.3V typical), over-temperature (T_J > +125°C typical) or a shutdown signal externally applied at the V_C terminal, see Figure 5.

Note that if the error voltage (at the V_C pin) is less that 2.55V, then the output of the Voltage-to-Current Converter will be held at zero. This condition will produce the minimum possible pulse width, typically 150ns (100ns blanking pulse plus 50ns delay). Error voltages lower than this 2.55V level will not produce shorter pulse widths. Under very light loads (when V_C goes below 1.5V), the Enable Comparator will temporarily hold-off the PWM latch (and the DMOS transistor) until the V_C voltage rises above 1.5V. This low V_C inhibit circuit results in a burst-mode of operation that maintains regulation under light or no loads.

During an over-current condition, the output of the Error Amplifier will attempt to exceed the 7.0V threshold. At this point, the Short-Circuit Comparator will pull down on this signal and induce a low-level oscillation about the threshold, serving to clamp the peak error voltage. This clamping action, in turn, will limit the peak current in the DMOS transistor, reducing the duty ratio of the switch as the demand for current continues to increase. This action, in conjunction with the Thermal Monitor, serves to protect the IC from over-current (short-circuit) conditions.

Using the Transconductance Error Amplifier

A transconductance amplifier with a typical g_m of 30mS is used as the input gain stage where the power supply output voltage is compared with the internally generated 5.1V reference voltage. A PNP transistor input structure allows this amplifier to accommodate large negative going transient voltages without causing amplifier phase reversal, often associated with PNP input structures. Negative transients up to 5V applied to the input through at least 5.1K will not result in phase reversal. The amplifier output stage has the customary drain to drain output to help improve the output impedance, ideally infinity. The amplifier gain is typically 50dB and is not significantly altered when operating into the stages that follow within the IC. To minimize the output stage idling current, while providing high peak currents to insure rapid response to load and input transients, a class B type of output stage was used in the amplifier. Placing a 100k resistor from the amplifier output terminal, V_C, to ground will bias the output stage to an active state and still minimize power consumption. In all cases, the resistor shunting the transconductance amplifier output must be greater than 10kΩ to insure that the output will rise sufficiently high to obtain the maximum DMOS transistor drain current.

Start-Up Sequence

Upon initial power up of the HIP5061 in a typical application circuit, the voltage at V_C will be zero, and the DMOS transistor will be off. When the voltage at V_{DD} rises above the 10.3V typical threshold, the error amplifier output is enabled and the V_C voltage begins to rise in response to the low voltage at the FB terminal. When the V_C voltage rises above 1.5V the DMOS transistor begins to switch at the minimum duty cycle, and when it rises above 2.55V the duty cycle begins to increase. The V_C voltage (and peak DMOS transistor current) will then continue to rise until the voltage loop gains control and establishes regulation. Note that the rate of rise in the V_C voltage can be controlled by an external soft start circuit (See **Soft Start Implementation**).

If the V_C voltage is unrestricted in its rate of rise, then it will typically rise quickly to its maximum (peak current) value, causing the DMOS transistor to turn-on and stay on until it reaches the peak current value. At this point, the DMOS transistor begins switching, and the V_C voltage (and peak DMOS transistor current) will drop down to the level commanded by the voltage loop.

Using the Shunt Regulator

The internal 14V shunt regulator in conjunction with an external series resistor allows the IC to operate from quite high input voltages, limited only by power dissipation in the external resistor. When only higher voltages are available, a bootstrap or other 12V auxiliary supply can be used to eliminate this dissipation. The series resistor should be chosen to be as large as possible to reduce power dissipation at high line, while ensuring adequate V_{DD} voltage at low line. The maximum value for this resistor, R, is given by:

$$R_{MAX}(\Omega) = \frac{V_{I,MIN} - 10.5}{0.033}$$

Where V_I is the input voltage to the power supply. The value chosen for this resistor must also result in a current, I, into the V_{DD} clamp that is less than 105mA when the input voltage is at its maximum:

$$I_{MAX}(A) = \frac{(V_{I,MAX} - 13.3)}{R_{MAX}}$$

Inductor Selection

The selection of the energy storage inductor(s) L_{STOR} for a DC to DC converter has tremendous influence on the behavior of the converter. It is particularly important in light of the high level of integration (and necessarily few degrees of freedom) achieved in the HIP5061. There are several factors influencing the selection of this inductor. First, the inductance of L_{STOR} will determine the basic mode of operation for the converter: continuous or discontinuous current. In order to maximize the output power for the given maximum controllable DMOS transistor current, a converter may be designed to operate in continuous current mode (CCM). However, this tends to require a larger inductor, and for many converter topologies results in a feedback loop that is difficult to stabilize. For these and other reasons, the inductor L_{STOR} may be chosen so as to operate the converter in discontinuous current mode (DCM). The relative merits of CCM and DCM operation for various topologies and the corresponding selection of L_{STOR} is well documented and will not be covered here.

A second factor influencing the selection of L_{STOR} is the stability requirement for current-mode control. This constraint is only applicable for converters operating in CCM, since open-loop instabilities of this type are not observed in converters operating in DCM. For marginal stability, the compensating ramp (internal to the HIP5061) must have a slope that is greater than one-half the difference between the inductor current's down slope and up slope. (To ensure stability for duty ratios D > 0.8, the slope of the compensating ramp should be equal to the inductor current downslope.) A generally accepted goal is to set the slope of the compensating ramp to be at least one-half of the inductor current down slope. Since there is no external control over the internal compensating ramp, one must be sure that the inductor is large enough so that the down slope of the inductor current is not too large. Table 1 summarizes this requirement for minimum inductance for several common topologies.

TABLE 1. MINIMUM INDUCTANCE FOR STABLE CCM OPERATION ABOVE 50% DUTY CYCLE

CONVERTER TYPE	MINIMUM INDUCTANCE
Boost	$L > \frac{V_O + V_D - V_{I,MIN}}{2M_{R,MIN}}$
SEPIC[1]	$\frac{L_1 L_2}{L_1 + L_2} > \frac{V_O + V_D}{2M_{R,MIN}}$
Cuk[1]	$\frac{L_1 L_2}{L_1 + L_2} > \frac{V_O - V_D}{2M_{R,MIN}}$
Flyback	$L_P > \left(\frac{N_P}{N_S}\right)\frac{(V_O + V_D)}{2M_{R,MIN}}$
Forward	$L > \left(\frac{N_S}{N_P}\right)\frac{(V_O + V_D)}{2M_{R,MIN}}$

[1] Assumes that L1 and L2 are both in CCM.

NOTE:

L = Inductance in Henrys, V_O = Output Voltage,
V_D = Diode Voltage Drop, V_I = Input Voltage,
$M_{R,MIN} = (\Delta I/\Delta t)_{MIN} = 0.45A/\mu s$
L_1 = Drain Inductor, L_2 = Secondary Inductor,
N_P = Primary Turns, N_S = Secondary Turns

A third constraint on the size of the inductor is one that is common among current-mode controlled PWM converters, and applies to both DCM and CCM operation. The stable generation of the desired DMOS transistor pulse width depends on the accurate comparison of the error signal and the peak L_{STOR} (DMOS) transistor drain current. Thus, as the peak L_{STOR} ripple current becomes smaller, immunity from noise on the error signal is eventually reduced until the pulse width can no longer be adequately controlled. For the HIP5061, the inductor current ripple must be at least 200mA peak to peak to ensure proper control of the DMOS transistor current. This effectively establishes a maximum value for the inductor L_{STOR}, so as to maintain at least 200mA of ripple. Note that under extremely light or no load conditions, all converters will eventually operate in DCM, and the 200mA requirement will eventually be violated. Under these conditions, the HIP5061 will continue to regulate, although the switching of the DMOS transistor will be in a burst-mode, controlled by the Light Load Comparator. (See Figure 2.)

DMOS Transistor Turn-Off Snubber

In order to reduce dissipation in the DMOS transistor due to turn-off losses, the turn-off time has been minimized. However, the rapid reduction of current that occurs in the drain of the DMOS transistor can result in large transient voltages being induced across any parasitic inductance in the drain path. For this reason, it is important that such parasitic inductance be reduced by good, high frequency layout practices. Nevertheless, there are many instances (e.g., transformer isolated topologies) in which voltages in excess of 60V may be developed at the DMOS transistor drain. In some cases, a simple R-C snubber may be added to reduce the overshoot of the drain voltage to a safe level.

It is also possible that the large amount of ringing that can occur at the DMOS transistor drain at turn-off will induce noise in the IC. This noise may result in false triggering of the PWM latch, particularly at high peak DMOS transistor drain currents. Noise related instability can also be eliminated by the addition of a snubber, which will rapidly damp out such turn-off ringing. Good layout practices will reduce the need for such protective measures, and ensure that the DMOS transistor is not overstressed.

Under-Voltage Lockout

The V_{DD} input voltage is monitored by a comparator that holds off the DMOS transistor gate drive signal when the V_{DD} voltage is less that about 10.3V. The typical 0.5V hysteresis of this comparator is intended to reduce oscillation when the voltage at V_{DD} is in the vicinity of 10V. Note, however, that when an external series resistor is used to feed the shunt regulator, the voltage drop across this resistor (which sharply decreases when the IC shuts down), effectively reduces the hysteresis. To reduce the tendency for oscillation in the vicinity of the 10V threshold, the impedance of the source that feeds the DC to DC converter input should be minimized. The addition of a capacitor (1µF - 47µF) at the V_{DD} terminal can also help to provide smooth turn-on or turn-off of the converter if the input supply rises or falls gradually through the V_{DD} Comparator threshold.

Peak Controllable DMOS Transistor Current

Figure 3 shows the guaranteed minimum, peak controllable DMOS transistor current versus duty cycle. This peak current value is established by the current limit circuitry, which effectively clamps the voltage at V_C (the error voltage) to perform current limiting. Since the sensed DMOS transistor current is summed with a compensating current ramp that begins its rise 1.5µs after the initiation of a cycle, current limiting will *begin* to occur at a peak DMOS transistor current that varies with the operating duty cycle. The highest current limit threshold occurs for D < 0.375, where no ramp is added to the sensed DMOS transistor current. At higher operating duty ratios, the onset of current limit will occur at increasingly lower currents, due to the effect of adding the compensating ramp to the sensed current. Note that this curve represents guaranteed minimum values. The guaranteed maximum values are considerably higher, although they are still limited to levels that protect the IC.

When the DMOS transistor first turns ON there may be substantial current spikes exceeding the normal maximum peak current established by the current control stages within the IC. To prevent these spurious spikes from conveying erroneous information to the Current Comparator, a 100ns

blanking signal is applied to the current monitoring circuitry. Thus, there is no peak current protection during the first 6% of the duty cycle (see Figure 3).

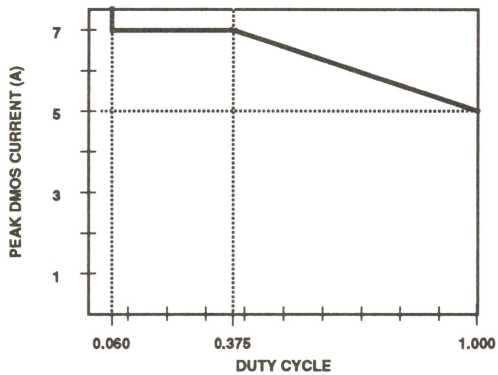


FIGURE 3. PEAK DMOS TRANSISTOR DRAIN CURRENT vs DUTY CYCLE

DMOS Transistor Turn-On Noise

Although the large DMOS transistor turn-on current spikes are "blanked over" by the control circuit, it is important to minimize these current spikes, since they often result in voltage spikes considerably below the device substrate that can activate parasitic devices within the IC. Such activation of parasitic devices will often result in improper operation of the IC. An external terminal labeled V_G brings out the power supply to the gate drive circuitry. This allows for the control of the peak current delivered to the gate of the DMOS transistor, which in turn establishes the turn-on speed. The V_G pin may be externally bypassed for the fastest possible turn-on, or series resistance may be added with no bypassing capacitor to slow down the turn-on of the DMOS transistor. Depending upon the actual layout of the supply, it is generally recommended that a series resistor be added (10Ω - 150Ω) so that the DMOS transistor turn-on speed is reduced. By properly adjusting the turn-on speed, undershoot can be avoided while turn-on switching losses are kept to a minimum.

Soft Start Implementation

It is often desirable to allow the regulator to start up slowly, Figure 4 shows one means of implementing this action. The normally high output current from the HIP5061 transconductance amplifier (when V_{FB} = 0 and V_{REF} = 5.1V) is directed to an external capacitor through a diode. This slows down the rate of rise of the voltage at the V_C terminal. After the regulator starts, the external capacitor is charged to V_{DD} and is effectively removed from the frequency compensation network by a reverse biased diode. To ensure rapid recycling of the capacitor voltage with removal of power, a diode is placed across the 100kΩ resistor.

The DC to DC converter may be shut down by returning the V_C output terminal to ground. A sinking current greater than 4mA will insure that this output is pulled to ground. It must be remembered that once switching operation ceases, the drain of the DMOS transistor is open. When the supply is in the Boost configuration, the output voltage is not zero but the input voltage minus diode and inductor voltage drops. If the SEPIC topology is used, this is not the case. Shutting down the regulator via the V_C terminal will cut off the output. Figure 5 shows two methods of shutting down the IC. In each case the current sinking circuit must be able to sink at least 4mA, the maximum current from the HIP5061 V_C terminal.

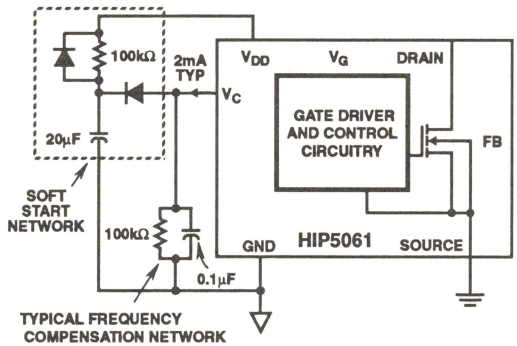
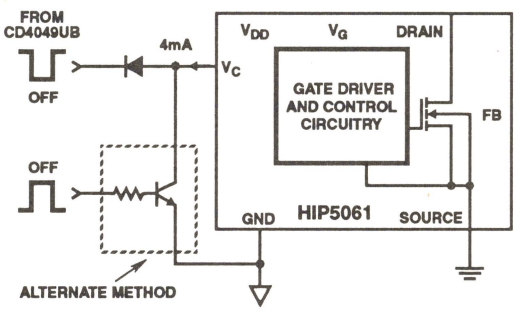


FIGURE 4. SOFT START CIRCUIT FOR THE HIP5061



NOTE: Frequency Compensation Network Not Shown

FIGURE 5. TWO METHODS OF SHUTTING DOWN THE HIP5061

Mounting, Layout and Component Selection

The TO220 package with its gullwing leads was designed to be surface mounted. To aid in the external reduction of lead length and hence inductance and resistance, the IC leads were staggered. To keep the inductance and resistance of the critical drain terminal as low as possible, it is suggested that the PC trace to the DMOS transistor drain terminal be made as wide as possible. The adjacent source terminal is not recommended to be used and therefore allows the metal to the drain terminal to be widened beyond the normal widths for these terminals. Figure 6 illustrates these points.

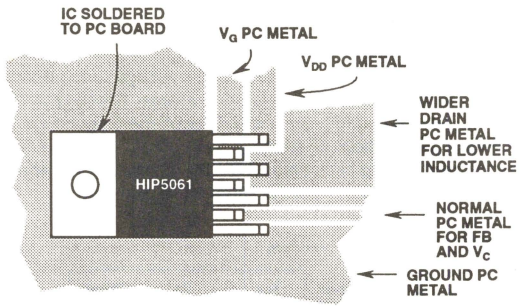


FIGURE 6. SHOWING WIDER PC BOARD METAL FOR CRITICAL LEADS

One of the most important aspects to the proper application of this device is high frequency bypassing. In a Boost converter, for example, there should be a low-inductance interconnect from the DMOS transistor drain, through the output diode and capacitors, and returning to the TAB (source) of the HIP5061. Inductance in this line results in large transient voltages on the DMOS transistor drain terminal which can result in voltages above the maximum DMOS transistor drain voltage rating.

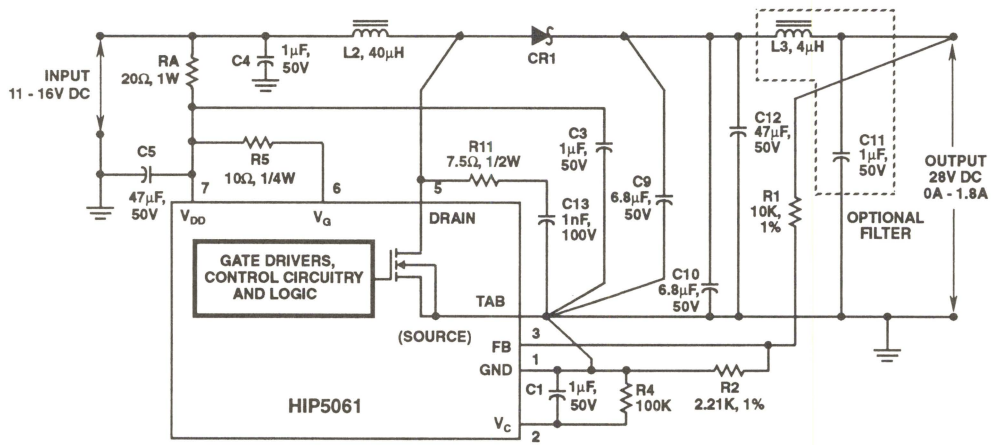
All the capacitors shown with values of 1µF or less are of the multilayer ceramic type with the X7R dielectric material. This material has a fairly flat voltage and temperature coefficient that assures that the capacitance remains comparatively constant at extreme operating temperatures and voltages. The multilayer construction allows for comparatively large values with good volumetric efficiency and low inductance. Capacitors around the power input and output circuits should be returned to the device TAB via a low inductance ground plane. This TAB is internally connected to the DMOS transistor source. The schematic diagram of Figure 7 was drawn with the diagonal leads to show the critical paths for the various high frequency elements. These short interconnects assure the lowest inductance around the output power circuit.

Design of a 28V, 1.8A Boost Converter

Figure 7 shows the schematic diagram and a parts list of a 50W supply designed with the HIP5061. Table 2 tabulates the performance of the power supply.

TABLE 2. TYPICAL LABORATORY PERFORMANCE OF 50W, 28V/1.8A REGULATOR

Input Voltage	11V to 16V
Line Regulation	12mV/V
Output Voltage	28.0V
Load Regulation	64mV/A
Output Ripple, FL (20MHz BW)	600mV P-P
Output Ripple, after Filter, FL (20MHz BW)	80mV P-P
Efficiency: VI = 11V, IL = 0.18A	90%
VI = 11V, IL = 1.8A	89%
VI = 16V, IL = 0.18A	73%
VI = 16V, IL = 1.8A	93%



PARTS LIST

RA	20Ω, 1W, Wirebound - Dale RWR81S20R0FR or Equivalent
R1	10K, 1%
R2	2.2K, 1%
R4	100K, 1/4W
R5	10Ω, 1/4W
R11	7.5Ω, 1/2W, Carbon - Allen Bradley EB75G5
C1, C3, C4 and C11	1µF, 50V, Ceramic - Murata Erie RPE113X7R105050V
C5 and C12	47µF, 50V, Alum - United Chemicon 515D476M050
C9 and C10	6.8µF, 50V, Ceramin - Mallory M60u6r8M50
C13	1nF, 100V, Ceramin - Kemet C322C102K1G5CA
CR1	Schottky Diode - Motorola MBRD360
L2	40µH at 5A, Pulse Engineering PE - 53571
L3	4µH at 5.5A, Pulse Engineering PE - 53570

FIGURE 7. HIP5061 50W, 28V BOOST REGULATOR SCHEMATIC AND PARTS LIST

Inductor Selection

In order to maximize the output power for the given maximum controllable DMOS transistor current, this converter has been designed to operate in continuous current mode (CCM). In this mode, the inductor value will generally be large, resulting in a lower inductor ripple current and a lower peak DMOS current. To ensure that the converter operates in CCM over the usable range of input voltage and output current, the value of L2 must be greater than the "critical inductance," given by:

$$L_{CRIT} = \frac{V_O V_{I,MAX}^2 (V_O + V_D - V_{I,MAX}) T_S}{2P_{O,MIN}(V_O + V_D)^2}$$

$$= \frac{(28)(16)^2(28+0.5-16)4\times10^{-6}}{2(5.6)(28+0.5)^2}$$

$$= 39\mu H$$

where $P_{O,MIN}$ has been arbitrarily chosen as 5.6W, corresponding to an output current of 0.2A, and V_D is the forward voltage of CR1. Thus, for L2 > 39µH, the converter will be in CCM for VI = 11V to 16V and IL = 0.2A to 1.8A.

A second factor influencing the selection of L2 is the stability requirement for current-mode control. Using the above equation for L_{MIN} for the Boost converter:

$$L > \frac{V_O + V_D - V_{I,MIN}}{2 \times M_{RAMP,MIN}} = \frac{28+0.5-11}{2\times(0.45\times10^6 A/s)} = 19\mu H$$

Thus, L2 must be at least 19µH to ensure good stability of the current loop, and a choice of L2 = 40µH satisfies this requirement, while maintaining CCM operation over a wide load range.

The chosen core material for L2 is Kool Mu ferrous alloy powder from Magnetics, Inc. This material was chosen because of its relatively low cost, while its losses due to AC flux are five to ten times less than conventional powdered iron.

Loop Compensation

The control to output transfer function for this current-mode boost converter has the following characteristics over the specified load and line conditions:

D.C. Gain: 20dB - 40dB
Pole at 88Hz - 880 Hz
LHP Zero at 1MHz
RHP Zero at 11.0kHz - 110kHz
Double Pole at 80kHz (from filter)

To stabilize the voltage loop, it is necessary to establish the unity gain crossover frequency well below the RHP zero, since this zero introduces positive gain and negative phase. A crossover of 4kHz is fairly conservative, and is achieved by adding a 1µF capacitor at the Vc pin, which provides near infinite DC gain, and about -5dB of gain at 4kHz. This results in a phase margin of about 15° at full load. Note that R4 is required for proper operation of the transconductance amplifier, since it is providing bias current for the output stage as discussed under **Using the Transconductance Error Amplifier** section.

Output Filter Design

Inductor L3 was chosen with C11 to provide at least 15db of ripple attenuation at the switching frequency. The corner frequency (80kHz) of this filter is well above the crossover frequency of the voltage loop (4kHz), and has no effect on stability. This secondary LC filter was used to reduce output ripple instead of a lower-cost, high-value, low ESR aluminum electrolytic capacitor. This filter demonstrates the reduction in volume possible at this switching frequency. A lower cost solution could achieve the same output ripple by replacing C9,10,12 and L3 with one or two large capacitors (e.g., 390µF, 50V, type 673D from United Chemicon). This change would also greatly improve load transient response, provided that the loop compensation is appropriately adjusted. Note that in the circuit of Figure 7, capacitor C12 does not significantly affect output ripple, but is necessary to absorb the energy stored in L2 during severe load transients. In the event of a step change in load from 1.8A to 0A, C12 will limit the output voltage overshoot to about 10V and protect the drain of the DMOS transistor from overvoltage breakdown.

Input and V_{DD} Filters

Since the boost converter is current fed, input filtering is easily achieved by the addition of a small capacitor, C4. This capacitor provides nearly 40db of ripple current attenuation for the input, reducing the AC ripple current flowing into the converter to less than 200mA.

R5 and C3 have been chosen to provide good filtering of high frequency pulse currents. R5 provides isolation between the analog V_{DD} pin and the high pulse current V_G pin, and also provides a means to control the turn-on speed of the DMOS transistor by limiting the peak current available to the internal gate drive circuitry. Thus the output transition time may be increased to prevent drain voltage undershoot. Undershoot may result in activation of device parasitics and improper circuit operation. For the two-layer board used for this design, C3 could be reduced to 0.22µF without affecting circuit operation. C5 was added to provide low-frequency filtering at the V_{DD} pin. This reduces the tendency of the circuit to oscillate off and on when the voltage at the V_{DD} pin in the vicinity of the under voltage lockout threshold, typically 10V, and the output power is high (30W - 50W).

Shunt Regulator Resistor

Resistor RA has been chosen to be as large as possible to reduce power dissipation at high line, while ensuring adequate V_{DD} voltage at low line. Note that the guaranteed range of input voltage for proper operation of this circuit is 11.2V to 15.3V DC, based upon data sheet limits. However, the circuit was found to perform well at room temperature for VI = 10.7 to 17VDC. The maximum value for RA is

$$R_{MAX} = \frac{V_{I,MIN} - 10.5}{0.033} = 21\Omega$$

RA has been chosen as 20Ω, which results in a current into

the V_{DD} clamp that is less than 105mA when the input voltage is at its maximum:

$$I_{MAX} = \frac{(V_{I,MAX} - 13.3)}{20.0} = 100mA < 105mA$$

Snubber Network

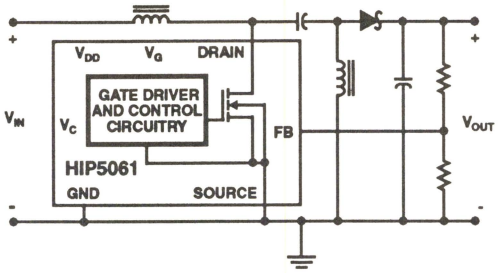
A snubber network has been added to reduce the ringing at the drain due to parasitic layout inductances. In particular, under severe load transient conditions, this snubber is necessary to protect the drain from voltage breakdown. A second benefit of reducing the noise and ringing at the drain is that it reduces the tendency of the HIP5061 to exhibit noise-related instabilities at high peak DMOS transistor currents (4A - 6A). A value of 1000pF was chosen for C13, since this is adequate to dampen the ringing associated with the 200pF drain capacitance of the DMOS transistor. R11 was chosen as 7.5Ω to provide the best possible dampening given the parasitic inductances that exist in the layout. Note that this snubber may not be necessary if the layout of the circuit were improved, or if the application did not push the envelope of DMOS transistor current.

Other Power Supply Topologies

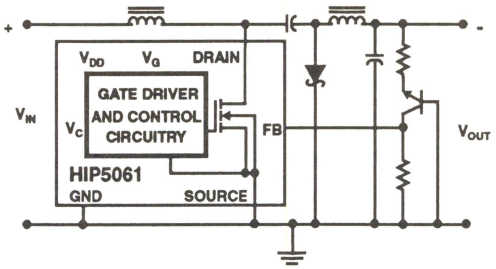
Figure 8 shows three other topologies besides the Boost that may be implemented with the grounded source DMOS power transistor used in the HIP5061. Other, more complex power supply topologies such as the Quadratic are also possible to implement with the HIP5061. One noteworthy feature of the Quadratic topology as shown in Figure 8 is the wide input to output voltage transfer ratio possible with reasonable duty cycles. This permits easier control at the extremes of the transfer ratio. Compensating the control loop can pose challenges because of the wider changes in the transfer ratio and hence loop gain.

The SEPIC topology[11,13] does not have quite as wide input-output voltage range with reasonably controlled duty cycles as the Quadratic converter mentioned above, but it does allow both voltage increase and decrease with the same circuit. This is particularly advantageous when a power supply is being used in the stabilizing mode and isolation is not required. For example, in an application where a regulated 24V output is required and the input voltage varies ±20% from a nominal 24V. The SEPIC supply can provide both the Boost and Buck functions.

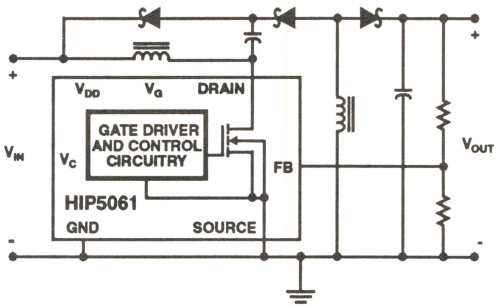
Another outstanding advantage of the SEPIC topology is its fault isolation of the input and output voltage. All energy is transferred via the coupling capacitor. Moreover if the clock stops, voltage transfer stops. If the switching transistor shorts there is no output. The Buck circuit will apply full input voltage to the load with a shorted transistor. This is the reason that the SEPIC topology is referred to as the fail-safe Buck.



SEPIC (FAIL-SAFE BUCK) CONVERTER



CUK CONVERTER



QUADRATIC CONVERTER

FIGURE 8. THREE OTHER TOPOLOGIES

It should be noted that when the Cuk topology is implemented, a transistor current source is used to convert the negative output voltage of the Cuk converter to a current that is level shifted to the FB terminal on the HIP5061.

Two other useful topologies that may be used are the Forward and the Flyback as shown in Figure 9 and Figure 10. As shown, they may either be operated as an isolated or non-isolated converter.

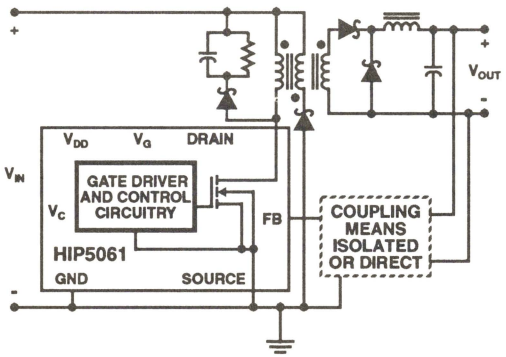


FIGURE 9. FORWARD CONVERTER

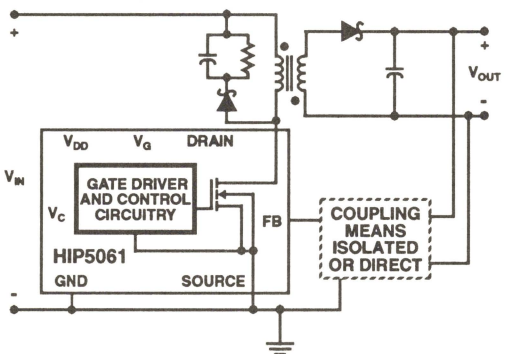


FIGURE 10. FLYBACK CONVERTER

Both the SEPIC and the Boost topologies may be operated at high voltages with the addition of a high voltage cascode transistor. Figure 11 shows the Cascode SEPIC converter that is essentially limited by the selection of the external power transistor. The burden of voltage, and power is placed upon the external transistor. The HIP5061 still performs the drain current sampling and the control function is the same as the non cascode configuration.

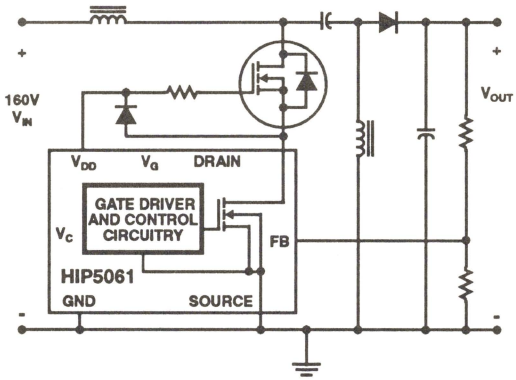


FIGURE 11. OFF LINE CASCODE SEPIC

Figure 12 shows the voltage transfer as a function of duty cycle for the power supply topologies discussed.

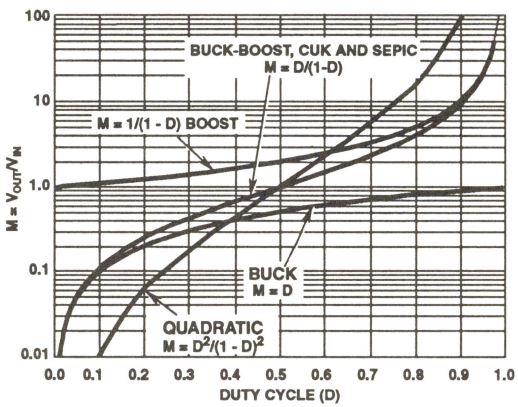


FIGURE 12. VOLTAGE TRANSFER AS A FUNCTION OF DUTY CYCLE FOR VARIOUS TOPOLOGIES

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No. AN9324.1 April 1994

HIP4080, 80V HIGH FREQUENCY H-BRIDGE DRIVER

Author: George E. Danz

Introduction

The HIP4080 is a member of the HIP408X family of High Frequency H-Bridge Driver ICs. A simplified application diagram is shown in Figure 1. The HIP4080 H-Bridge driver IC provides the ability to operate from 8VDC to 80VDC busses for driving N-Channel MOSFET H-Bridges, The HIP4080 packaged in either 20 lead DIP or 20 lead SOIC, provides peak gate current drive of 2.5A.

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper MOSFETs of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to maintain bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin "float" with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals to 95VDC.

The HIP4080 can drive lamp loads for automotive and industrial applications as shown in Figure 2. When inductive loads are switched, flyback diodes must be placed around the loads to protect the MOSFET switches.

The HIP408X family of devices is fabricated using a proprietary Harris IC process which allows this family to switch at frequencies of over 500kHz. Therefore the HIP408X family is ideal for use in voice coil motor, class-D audio amplifier, DC-DC converters and high performance AC, DC and step-motor control applications.

Many applications utilize the full bridge topology. These are voice coil motor drives, stepper and DC brush motors, audio amplifiers and even power supply inverters used in uninterruptable power supplies, just to name a few. Of the above, voice coil motor drives and audio amplifiers can take advantage of the built-in comparator available in the HIP4080. Using the output of the comparator to add some positive feedback, a hysteresis control, so popular with voice coil motor drivers, can be implemented as shown in Figure 3. In the figure, R3 is fed back from the comparator output, OUT, to the positive input of the comparator, IN+. Capacitor, C1, integrates in a direction to satisfy the reference current signal at IN. The IN- input of the comparator sums this current reference with a signal proportional to load current through resistor, R4, which comes from a differential amplifier, A1. A bias voltage of 6V (represents half of the bias voltage and the maximum rail to rail voltage of the comparator and amplifier, A1) biases the comparator's IN+ terminal through R2 and the amplifier, A1's, positive summing junction.

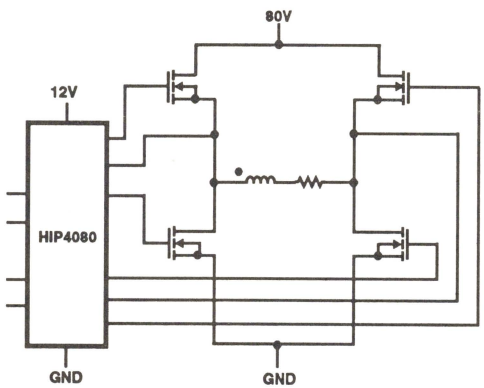


FIGURE 1. HIP4080 SIMPLIFIED APPLICATION DIAGRAM

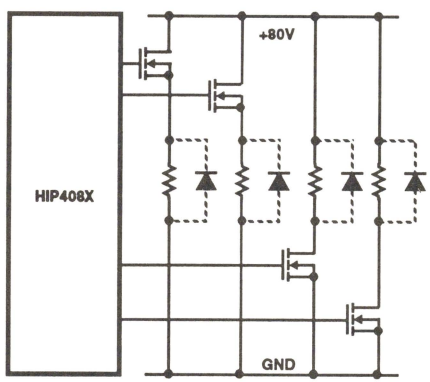


FIGURE 2. HIP4080 AS LAMP SWITCH DRIVER, DUAL HIGH/LOW SWITCHES FOR AUTOMOTIVE AND INDUSTRIAL CONTROLS

When no current is flowing in either direction in the load, the output of A1 is exactly 6V. The reference input, IN, would also have to be 6V to request zero current from the bridge. The bridge would still switch in this case, because of the positive feedback connection of the HIP4080 internal comparator. The frequency of oscillation of the output will be a function of the amount of dc hysteresis gain, R3/R1 and the

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size of capacitor, C1. As the capacitor, C1, is made larger, the steady-state frequency of the bridge will become smaller. It is beyond the scope of this application note to provide a full analysis. A valuable characteristic of hysteresis control is that as the error becomes smaller (i.e. the reference and feedback signals match) the frequency increases. Usually this occurs when the load current is small or at a minimum. When the error signal is large, the frequency becomes very small, perhaps even dc. One advantage of this is that when currents are largest, switching losses are a minimum, and when switching losses are largest, the dc current component is small.

To provide accurate dead-time control for the twin purposes of shoot-through avoidance and duty-cycle maximization, two resistors tied to pins HDEL and LDEL provide precise delay matching of upper and lower propagation delays, which are typically only 55ns. The HIP408X family of H-Bridge drivers have enough voltage margin to be applied to all SELV (UL classification for operation at ≤ 42.0V) applications and most Automotive applications where "load dump" capability over 65V is required. This capability makes the HIP408X family a more cost-effective solution for driving N-channel power MOSFETs than either discrete solutions or other solutions relying on transformer or opto-coupling gate-drive techniques as shown in Figure 1.

The HIP4080 differs from the HIP4081 regarding the function of pins 2, 5, 6 and 7 of the IC and the truth table which governs the switching function of the two ICs. In the HIP4080, pins 2, 5, 6 and 7 are labeled HEN, OUT, IN+ and IN-, respectively. In the HIP4081, pins 2, 5, 6 and 7 are labeled BHI (B-side high input), BLI (B-side low input), ALI (A-side low input) and AHI (A-side high input), respectively. The HIP4081's inputs individually control each of the four power MOSFETs, or in pairs (excepting the shoot-through case). The HIP4080 provides an internal comparator and a "HEN...high enable" pin. The comparator can be used to provide a PWM logic signal to switch the appropriate MOSFETs within the H-bridge, and can facilitate "Hysteresis" control to be illustrated later. The HEN pin enables (when HEN is high) or disables (when HEN is low) the upper MOSFETs. With HEN held low, it is possible to switch only the lower H-bridge MOSFETs. The HEN input can also be PWM-switched with the IN+ and IN- inputs used only for direction control, thereby minimizing switching losses.

Description of the HIP4080

The block diagram of the HIP4080 relating to driving the A-side of the H-Bridge is shown in Figure 4. The blocks associated with each side of the H-Bridge are identical, so the B-side is not shown for simplicity.

The two bias voltage terminals on the HIP408X H-Bridge Drivers, V_{CC} and V_{DD} should be tied together. They were separated within the HIP408X IC to avoid possible ground loops internal to the IC. Tieing them together and providing a decoupling capacitor from the common tie-point to V_{SS} greatly improves noise immunity.

Input Logic

The HIP4080 accepts inputs which control the output state of the power MOSFET H-bridge and provides a comparator output pin, OUT, which can provide compensation or hysteresis.

The DIS, "Disable," pin disables gate drive to all H-bridge MOSFETs regardless of the command states of the input pins, IN+, IN– and HEN. The HEN, "High Enable," pin enables and disables gate drive to the two high side MOSFETs. A high level on the HEN pin "enables" high side gate drive as further determined by the states of the IN+ and IN– comparator input pins, since the IN+ and IN– pins control which diagonal pair of MOSFETs are gated. Upper drive can be "modulated" through use of the HEN pin while drive to diagonally opposing lower MOSFETs is continuous. To simultaneously modulate both upper and lower drivers, HEN is continuously held high while modulating the IN+ and IN– pins.

Modulating only the upper switches can nearly halve the switching losses in both the driver IC and in the lower MOSFETs. The power dissipation saved at high switching frequencies can be significant. Table 1 summarizes the input control logic.

TABLE 1. INPUT LOGIC TRUTH TABLE

IN+ > IN-	DIS	HEN	ALO	AHO	BLO	BHO
X	1	X	0	0	0	0
1	0	1	0	1	1	0
0	0	1	1	0	0	1
1	0	0	0	0	1	0
0	0	0	1	0	0	0

X = DON'T CARE 1 = HIGH/ON 0 = LOW/OFF

The input sensitivity of the DIS and HEN input pins are best described as "enhanced TTL" levels. Inputs which fall below 1.0V or above 2.5V are recognized, respectively, as low level or high level inputs. The IN+ and IN- comparator inputs have a common mode input voltage range of 1.0V to V_{DD} -1.5V, whereas the offset voltage is less than 5mV. For more information on the comparator specifications, see Harris Data Sheet HIP4080, File Number 3178.

Propagation Delay Control

Propagation delay control is a major feature of the HIP4080. Two identical sub-circuits within the IC delay the commutation of the power MOSFET gate turn-on signals for both sides of the H-bridge. The gate turn-off signals are not delayed. Propagation delays related to the level-translation function (see section on Level-Translation) cause both upper on/off propagation delays to be longer than the lower on/off propagation delays. Four delay sub-circuits are needed to fully balance the H-bridge delays, two for upper delay control and two for lower delay control.

Users can tailor the low side to high side commutation delay times by placing a resistor from the HDEL pin to the V_{SS} pin. Similarly, a resistor connected from LDEL to V_{SS} controls the high side to low side commutation delay times of the lower power switches. The HDEL resistor controls both upper commutation delays and the LDEL resistor controls the lower commutation delays. Each of the resistors sets a current

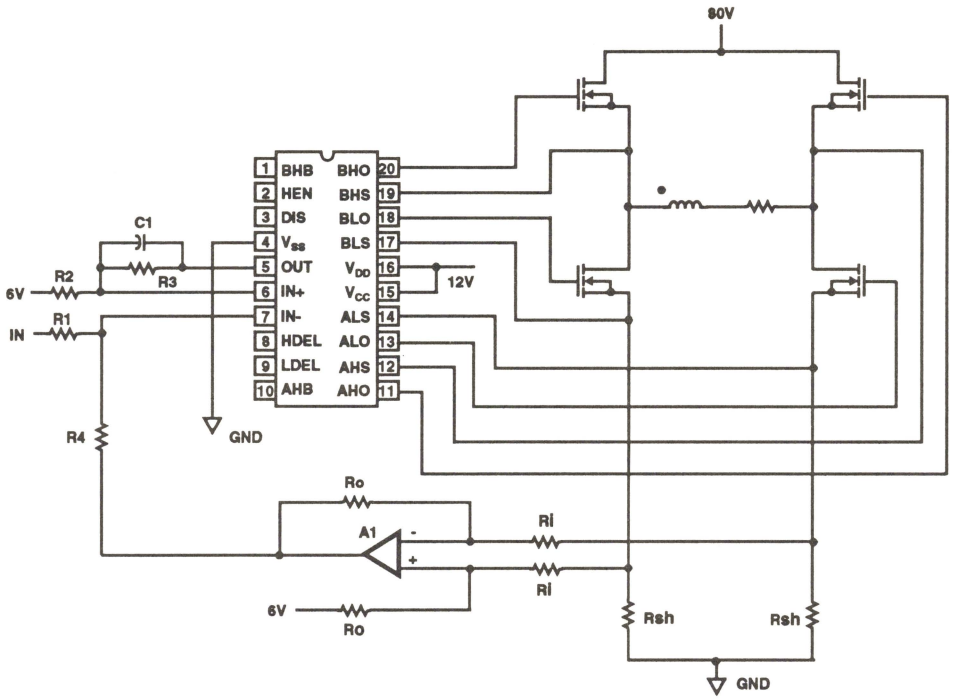


FIGURE 3. HYSTERESIS MODE SWITCHING

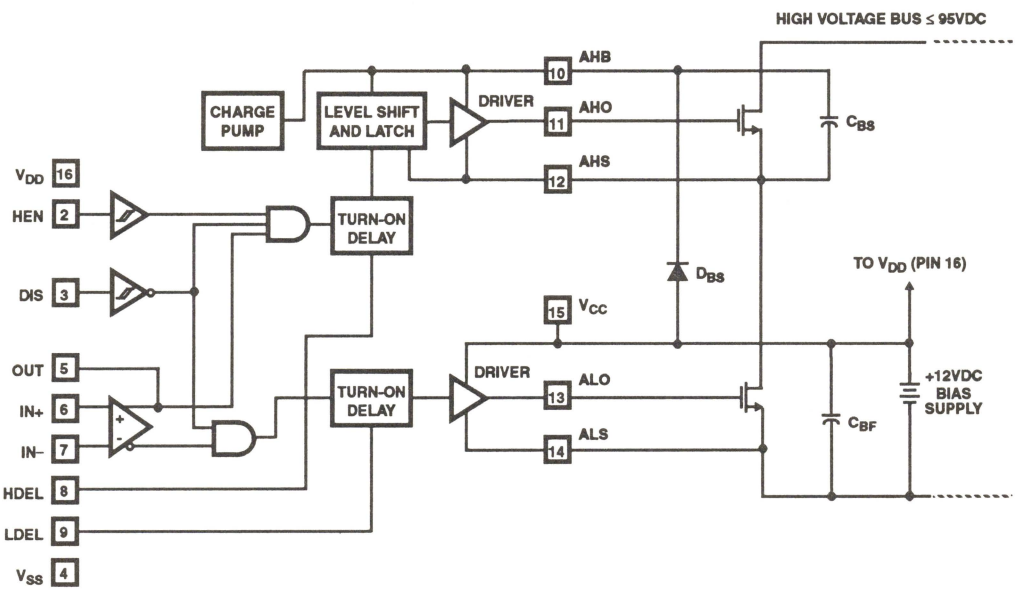


FIGURE 4. HIP4080 BLOCK DIAGRAM (A SIDE ONLY)

which is inversely proportional to the created delay. The delay is added to the falling edge of the "off" pulse associated with the MOSFET which is being commutated off. When the delay is complete, the "on" pulse is initiated. This has the effect of "delaying" the commanded on pulse by the amount set by the delay, thereby creating dead-time.

Proper choice of resistor values connected from HDEL and LDEL to V_{SS} provides a means for matching the commutation dead times whether commutating high to low or low to high. Values for the resistors ranging from 10kΩ to 200kΩ are recommended. Figure 5 shows the delays obtainable as a function of the resistor values used.

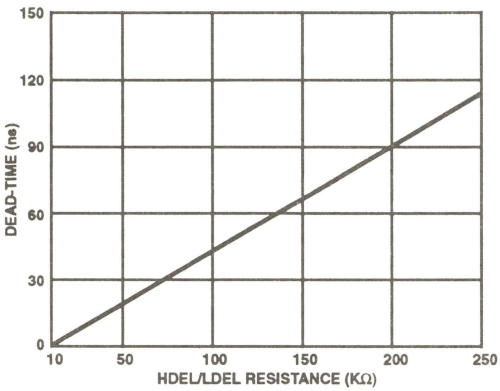


FIGURE 5. MINIMUM DEAD-TIME vs DEL RESISTANCE

Level-Translation

The lower power MOSFET gate drive signals from the propagation delay and control circuits go to amplification circuits which are described in more detail under the section "Driver Circuits". The upper power MOSFET gate drive signals are directed first to the Level-Translation circuits before going to the upper power MOSFET "Driver Circuits".

The Level-Translation circuit communicate "on" and "off" pulses from the Propagation Delay sub-circuit to the upper logic and gate drive sub-circuits which "float" at the potential of the upper power MOSFET source connections. This voltage can be as much as 85V when the bias supply voltage is only 10V (the sum of the bias supply voltage and bus voltages must not exceed 95VDC).

In order to minimize power dissipation in the level-shifter circuit, it is important to minimize the width of the pulses translated because the power dissipation is proportional to the product of switching frequency and pulse energy in joules. The pulse energy in turn is equal to the product of the bus voltage magnitude, translation pulse current and translation pulse duration. To provide a reliable, noise free pulse requires a nominal current pulse magnitude of approximately 3mA. The translated pulses are then "latched" to maintain the "on" or "off" state until another level-translation pulse comes along to set the latch to the opposite state. Very reliable operation can be obtained with pulse widths of approximately 80ns. At a switching frequency of even 1.0MHz, with an 80VDC bus potential, the power developed by the level-translation circuit will be less than 0.08W.

Charge Pump Circuits

There are two charge pump circuits in the HIP4080, one for each of the two upper logic and driver circuits. Each charge pump uses a switched capacitor doubler to provide about 30μA to 50μA of gate load current. The sourcing current charging capability drops off as the floating supply voltage increases. Eventually the gate voltage approaches the level set by an internal zener clamp, which prevents the voltage from exceeding about 15V, the safe gate voltage rating of most commonly available MOSFETs.

Driver Circuits

Each of the four output drivers are comprised of bipolar high speed NPN transistors for both sourcing and sinking gate charge to and from the MOSFET switches. In addition, the sink driver incorporates a parallel-connected n-channel MOSFET to enable the gate of the power switch gate-source voltage to be brought completely to 0V.

The propagation delays through the gate driver sub-circuits while driving 500pF loads is typically less than 10ns. Nevertheless, the gate driver design nearly eliminates all gate driver shoot-through which significantly reduces IC power dissipation.

Application Considerations

To successfully apply the HIP4080 the designer should address the following concerns:

- General Bias Supply Design Issues
- Upper Bias Supply Circuit Design
- Bootstrap Bias Supply Circuit Design

General Bias Supply Design Issues

The bias supply design is simple. The designer must first establish the desired gate voltage for turning on the power switches. For most power MOSFETs, increasing the gate-source voltage beyond 10V yields little reduction in switch drain-source voltage drop.

Overcharging the power switch's gate-source capacitance also delays turn-off, increases MOSFET switching losses and increases the energy to be switched by the gate driver of the HIP4080, which increases the dissipation within the HIP4080. Overcharging the MOSFET gate-source capacitance also can lead to "shoot-through" where both upper and lower MOSFETs in a single bridge leg find themselves on simultaneously, thereby shorting out the high voltage DC bus supply. Values close to 12V are optimum for supplying V_{DD} and V_{CC}, although the HIP4080 will operate up to 15V.

Lower Bias Supply Design

Since most applications use identical MOSFETs for both upper and lower power switches, the bias supply requirements with respect to driving the MOSFET gates will also be identical. If switching frequencies for driving upper and lower MOSFETs differ, two sets of calculations must be done; one for the upper switches and one for the lower switches. The bias current budget for upper and lower switches will be the sum of each calculation.

Always keep in mind that the lower bias supply must supply current to the upper gate drive and logic circuits as well as the lower gate drive circuits and logic circuits. This is due to the fact that the low side bias supplies (V_{CC}/V_{DD}) charge the bootstrap capacitors and the charge pumps, which maintain voltage across the upper power switch's gate-source terminals.

Good layout practice and capacitor bypassing technique avoids transient voltage dips of the bias power supply to the HIP4080. Always place a low ESR (equivalent series resistance) ceramic capacitor adjacent to the IC, connected between the bias terminals V_{CC} and V_{DD} and the common terminal, V_{SS} of the IC. A value in the range of 0.22µF and 0.5µF is usually sufficient.

Minimize the effects of Miller feedback by keeping the source and gate return leads from the MOSFETs to the HIP4080 short. This also reduces ringing, by minimizing the length and the inductance of these connections. Another way to minimize inductance in the gate charge/discharge path, in addition to minimizing path length, is to run the outbound gate lead directly "over" the source return lead. Sometimes the source return leads can be made into a small "ground plane" on the back side of the PC board making it possible to run the outbound gate lead "on top" of the board. This minimizes the "enclosed area" of the loop, thus minimizing inductance in this loop. It also adds some capacitance between gate and source which shunts out some of the Miller feedback effect.

Upper Bias Supply Circuit Design

Before discussing bootstrap circuit design in detail, it is worth mentioning that it is possible to operate the HIP4080 without a bootstrap circuit altogether. Even the bootstrap capacitor, which functions to supply a reservoir of charge for rapidly turning on the MOSFETs, is optional in some cases. In situations where very slow turn-on of the MOSFETs is tolerable, one may consider omitting some or all bootstrap components. Applications such as driving relays or lamp loads, where the MOSFETs are switched infrequently and switching losses are low, may provide opportunities for omitting the boot strap operation. Generally, loads with a lot of resistance and inductance are candidates.

Operating the HIP4080 without a bootstrap diode and/or capacitor will severely slow gate turn-on. Without a bootstrap capacitor, gate current only comes from the internal charge pump. The peak charge pump current is only about 30µA to 50µA. The gate voltage waveform, when operating without a bootstrap capacitor, will appear similar to the dotted line shown in Figure 6.

If a bootstrap capacitor value approximately equal to the equivalent MOSFET gate capacitance is used, the upper bias supply (labeled "bootstrap voltage" in Figure 6) will drop approximately in half when the gate is turned on. The larger the bootstrap capacitance used, the smaller is the instantaneous drop in bootstrap supply voltage when an upper MOSFET is turned on.

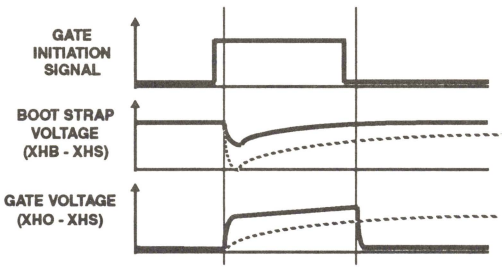


FIGURE 6.

Although not recommended, one may employ a bootstrap capacitor without a bootstrap diode. In this case the charge pump is used to charge up a capacitor whose value should be much larger than the equivalent gate-source capacitance of the driven MOSFET. A value of bootstrap capacitance about 10 times greater than the equivalent MOSFET gate-source capacitance is usually sufficient. Provided that sufficient time elapses before turning on the MOSFET again, the bootstrap capacitor will have a chance to recharge to the voltage value that the bootstrap capacitor had prior to turning on the MOSFET. Assuming 2Ω of series resistance is in the bootstrap change path, an output frequency of up to $\frac{1}{5 \times 2\Omega \times C_{BS}}$ should allow sufficient refresh time.

A bootstrap capacitor 10 times larger than the equivalent gate-source capacitance of the driven MOSFET prevents the drop in bootstrap supply voltage from exceeding 10% of the bias supply voltage during turn-on of the MOSFET. When operating without the bootstrap diode the time required to replenish the charge on the bootstrap capacitor will be the same time as it would take to charge up the equivalent gate capacitance from 0V. This is because the charge lost on the bootstrap capacitor is exactly equal to the charge transferred to the gate capacitance during turn-on. Note that the very first time that the bootstrap capacitor is charged up, it takes much longer to do so, since the capacitor must be charged from 0V. With a bootstrap diode, the initial charging of the bootstrap supply is almost instantaneous, since the charge required comes from the low-side bias supply. Therefore, before any upper MOSFETs can initially be gated, time must be allowed for the upper bootstrap supply to reach full voltage. Without a bootstrap diode, this initial "charge" time can be excessive.

If the switching cycle is assumed to begin when an upper MOSFET is gated on, then the bootstrap capacitor will undergo a charge withdrawal when the source driver connects it to the equivalent gate-source capacitance of the MOSFET. After this initial "dump" of charge, the quiescent

current drain experienced by the bootstrap supply is infinitesimal. In fact, the quiescent supply current is more than offset by the charge pump current.

The charge pump continuously supplies current to the bootstrap supply and eventually would charge the bootstrap capacitor and the MOSFET gate capacitance back to its initial value prior to the beginning of the switching cycle. The problem is that "eventually" may not be fast enough when the switching frequency is greater than a few hundred Hz.

Bootstrap Bias Supply Circuit Design

For high frequency applications all bootstrap components, both diodes and capacitors, are required. Therefore, one must be familiar with bootstrap capacitor sizing and proper choice of bootstrap diode.

Just after the switch cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is the lowest that it will ever be during the switch cycle. The charge lost on the bootstrap capacitor will be very nearly equal to the charge transferred to the equivalent gate-source capacitance of the MOSFET as shown in Equation 1.

$$Q_G = (V_{BS1} - V_{BS2}) \times C_{BS} \quad \text{(EQ.1)}$$

where:

V_{BS1} = Bootstrap voltage immediately before turn-on

V_{BS2} = Bootstrap voltage immediately after turn-on

C_{BS} = Bootstrap Capacitance

Q_G = Gate charge transferred during turn-on

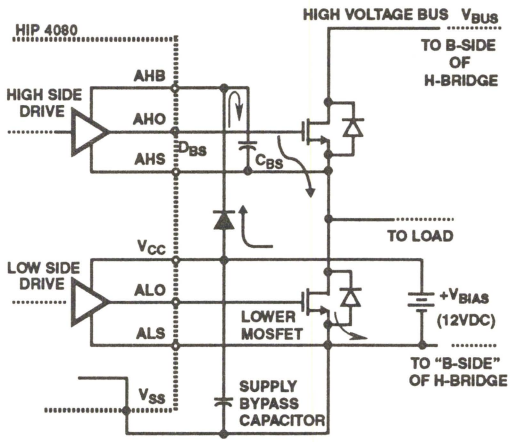
Were it not for the internal charge pump, the voltage on the bootstrap capacitor and the gate capacitor (because an upper MOSFET is now turned on) would eventually drain down to zero due to bootstrap diode leakage current and the very small supply current associated with the level-shifters and upper gate driver sub-circuits.

In PWM switch-mode, the switching frequency is equal to the reciprocal of the period between successive turn-on (or turn-off) pulses. Between any two turn-on gate pulses exists one turn-off pulse. Each time a turn-off pulse is issued to an upper MOSFET, the bootstrap capacitor of that MOSFET begins its "refresh" cycle. A refresh cycle ends when the upper MOSFET is turned on again, which varies depending on the PWM frequency and duty cycle. As the duty cycle approaches 100%, the available "off-time", t_{OFF} approaches zero. Equation 2 shows the relationship between t_{OFF}, f_{PWM} and the duty cycle.

$$t_{OFF} = (1 - DC)/f_{PWM} \quad \text{(EQ.2)}$$

As soon as the upper MOSFET is turned off, the voltage on the phase terminal (the source terminal of the upper MOSFET) begins its descent toward the negative rail of the high voltage bus. When the phase terminal voltage becomes less than the V_{CC} voltage, refreshing (charging) of the bootstrap capacitor begins. As long as the phase voltage is below V_{CC} refreshing continues until the bootstrap and V_{CC} voltages are equal.

The off-time of the upper MOSFET is dependent on the gate control input signals, but it can never be shorter than the dead-time delay setting, which is set by the resistors connecting HDEL and LDEL to V_{SS}. If the bootstrap capacitor is not fully charged by the time the upper MOSFET turns on again, incomplete refreshing occurs. The designer must insure that the dead-time setting be consistent with the size of the bootstrap capacitor in order to guarantee complete refreshing. Figure 7 illustrates the circuit path for refreshing the bootstrap capacitor.



NOTE: Only "A-side" of H-bridge Is Shown for Simplicity. Arrows Show Bootstrap Charging Path.

FIGURE 7. BOOTSTRAP CAPACITOR CHARGING PATH

The bootstrap charging and discharging paths should be kept short, minimizing the inductance of these loops as mentioned in the section, "Lower Bias Supply Design".

Bootstrap Circuit Design - An Example

Equation 1 describes the relationship between the gate charge transferred to the MOSFET upon turn-on, the size of the bootstrap capacitor and the change in voltage across the bootstrap capacitor which occurs as a result of turn-on charge transfer.

The effects of reverse leakage current associated with the bootstrap diode and the bias current associated with the upper gate drive circuits also affect bootstrap capacitor sizing. At the instant that the upper MOSFET turns on and its source voltage begins to rapidly rise, the bootstrap diode becomes rapidly reverse biased resulting in a reverse recovery charge which further depletes the charge on the bootstrap capacitor. To completely model the total charge transferred during turn-on of the upper MOSFETs, these effects must be accounted for, as shown in Equation 3.

$$C_{BS} = \frac{Q_G + Q_{RR} + \frac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \quad \text{(EQ.3)}$$

where:

I_{DR} = Bootstrap diode reverse leakage current

I_{QBS} = Upper supply quiescent current

Q_{RR} = Bootstrap diode reverse recovered charge

Q_G = Turn-on gate charge transferred

f_{PWM} = PWM operating frequency

V_{BS1} = Bootstrap capacitor voltage just after refresh

V_{BS2} = Bootstrap capacitor voltage just after upper turn on

C_{BS} = Bootstrap capacitance

From a practical standpoint, the bootstrap diode reverse leakage and the upper supply quiescent current are negligible, particularly since the HIP4080's internal charge pump continuously sources a minimum of about 30µA. This current more than offsets the leakage and supply current components, which are fixed and not a function of the switching frequency. The higher the switching frequency, the lower is the charge effect contributed by these components and their effect on bootstrap capacitor sizing is negligible, as shown in Equation 3. Supply current due to the bootstrap diode recovery charge component increases with switching frequency and generally is not negligible. Hence the need to use a fast recovery diode. Diode recovery charge information can usually be found in most vendor data sheets.

For example, if we choose a Harris IRF520R power MOSFET, the data book states a gate charge, Qg, of 12nC typical and 18nC maximum, both at V_{DS} = 12V. Using the maximum value of 18nC the maximum charge we should have to transfer will be less than 18nC.

Suppose a General Instrument UF4002, 100V, fast recovery, 1A, miniature plastic rectifier is used. The data sheet gives a reverse recovery time of 25ns. Since the recovery current waveform is approximately triangular, the recovery charge can be approximated by taking the product of half the peak reverse current magnitude (1A peak) and the recovery time duration (25ns). In this case the recovery charge should be 12.5nC.

Since the internal charge pump offsets any possible diode leakage and upper drive circuit bias currents, these sources of discharge current for the bootstrap capacitor will be ignored. The bootstrap capacitance required for the example above can be calculated as shown in Equation 4, using Equation 2.

$$C_{BS} = \frac{18nC + 12.5nC}{12.0 - 11.0} \quad \text{(EQ. 4)}$$

Therefore a bootstrap capacitance of 0.033µF will result in less than a 1.0V droop in the voltage across the bootstrap capacitor during the turn-on period of either of the upper MOSFETs. If typical values of gate charge and bootstrap diode recovered charge are used rather than the maximum value, the voltage droop on the bootstrap supply will be only about 0.5V

Power Dissipation and Thermal Design

One way to model the power dissipated in the HIP4080 is by lumping the losses into static losses and dynamic (switching) losses. The static losses are due to bias current losses for the upper and lower sections of the IC and include the sum of the I_{CC} and I_{DD} currents when the IC is not switching. The quiescent current is approximately 9mA. Therefore with a 12V bias supply, the static power dissipation in the IC is slightly over 100mW.

The dynamic losses associated with switching the power MOSFETs are much more significant and can be divided into the following categories:

- Low Voltage Gate Drive (charge transfer)
- High Voltage Level-shifter (V-I) losses
- High Voltage Level-shifter (charge transfer)

In practice, the high voltage level-shifter and charge transfer losses are small compared to the gate drive charge transfer losses.

The more significant low voltage gate drive charge transfer losses are caused by the movement of charge in and out of the equivalent gate-source capacitor of each of the 4 MOSFETs comprising the H-bridge. The loss is a function of PWM (switching) frequency, the applied bias voltage, the equivalent gate-source capacitance and a minute amount of CMOS gate charge internal to the HIP4080. The low voltage charge transfer losses are given by Equation 5.

$$P_{SWLO} = f_{PWM} \times (Q_G + Q_{IC}) \times V_{BIAS} \quad \text{(EQ. 5)}$$

The high voltage level-shifter power dissipation is much more difficult to evaluate, although the equation which defines it is simple as shown in Equation 6. The difficulty arises from the fact that the level-shift current pulses, I_{ON} and I_{OFF}, are not perfectly in phase with the voltage at the upper MOSFET source terminals, V_{SHIFT} due to propagation delays within the IC. These time-dependent source voltages (or "phase" voltages) are further dependent on the gate capacitance of the driven MOSFETs and the type of load (resistive, capacitive or inductive) which determines how rapidly the MOSFETs turn on. For example, the level-shifter I_{ON} and I_{OFF} pulses may come and go and be latched by the upper logic circuits before the phase voltage even moves. As a result, little level-shift power dissipation may result from the i_{ON} pulse, whereas the I_{OFF} pulse may have a significant power dissipation associated with it, since the phase voltage generally remains high throughout the duration of the i_{OFF} pulse.

$$P_{SHIFT} = \frac{I}{T}\int_0^T (I_{ON}(t) + I_{OFF}(t)) \times V_{SHIFT}(t) \times dt \quad \text{(EQ. 6)}$$

Lastly, there is power dissipated within the IC due to charge transfer in and out of the capacitance between the upper driver circuits and V_{SS}. Since it is a charge transfer phenomena, it closely resembles the form of Equation 5, except that the capacitance is much smaller than the equivalent gate-source capacitances associated with power MOSFETs. On the other hand, the voltages associated with the level-shifting function are much higher than the voltage changes experienced at the gate of the MOSFETs. The relationship is shown in Equation 7.

$$P_{TUB} = C_{TUB} \times V_{SHIFT}^2 \times f_{PWM} \quad \text{(EQ. 7)}$$

The power associated with each of the two high voltage tubs in the HIP4080 derived from Equation 7 is quite small, due to the extremely small capacitance associated with these tubs. A "tub" is the isolation area which surrounds and isolates the high side circuits from the ground referenced circuits of the IC. The important point for users is that the power dissipated is linearly related to switching frequency and the square of the applied bus voltage.

The tub capacitance in Equation 7 varies with applied voltage, V_{SHIFT}, making its solution difficult, and the phase shift of the I_{ON} and I_{OFF} pulses with respect to the phase voltage, V_{SHIFT}, in Equation 6 are difficult to measure. Even the Q_{IC} in Equation 5 is not easy to measure. Hence the use of Equation 5 through Equation 7 to calculate total power dissipation is at best difficult. The equations do, however, allow users to understand the significance that MOSFET choice, switching frequency and bus voltage play in determining power dissipation. This knowledge can lead to corrective action when power dissipation becomes excessive.

Fortunately, there is an easy method which can be used to **measure** the components of power dissipation rather than **calculating** them, except for the tiny "tub capacitance" component.

Power Dissipation, the Easy Way

The average power dissipation associated with the IC and the gate of the connected MOSFETs can easily be measured using a signal generator, an averaging milliameter and a voltmeter.

Low Voltage Power Dissipation

Two sets of measurements are required. The first set uses the circuit of Figure 8 and evaluates all of the low voltage power dissipation components. These components include the MOSFET gate charge and internal CMOS charge transfer losses shown in Equation 5 as well as the quiescent bias current losses associated with the IC. The losses are calculated very simply by calculating the product of the bias voltage and current measurements as performed using the circuit shown in Figure 8. For measurement purposes, the phase terminals (AHS and BHS) for both A and B phases are both tied to the chip common, V_{SS} terminal, along with the lower source terminals, ALS and BLS. Capacitors equal to the equivalent gate-source capacitance of the MOSFETs are connected from each gate terminal to V_{SS}. The value of the capacitance chosen comes from the MOSFET manufacturers data sheet. Notice that the MOSFET data sheet usually gives the value in units of charge (usually nanocoulombs) for different drain-source voltages. Choose the drain-source voltage closest to the particular dc bus voltage of interest.

Simply substituting the actual MOSFETs for the capacitors, C_L, doesn't yield the correct average current because the Miller capacitance will not be accounted for. This is because the drains don't switch using the test circuit shown in Figure 8. Also the gate capacitance of the devices you are using may not represent the maximum values which only the data sheet will provide.

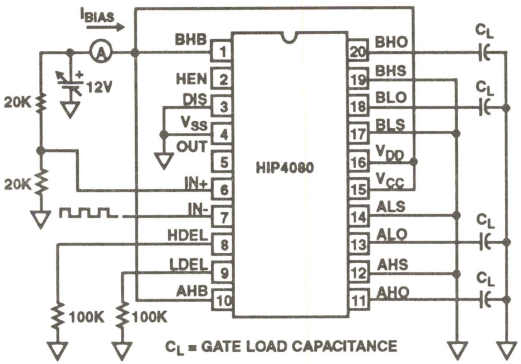


FIGURE 8. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

The low voltage charge transfer switching currents are shown in Figure 9. Figure 9 does not include the quiescent bias current component, which is the bias current which flows in the IC when switching is disabled. The quiescent bias current component is approximately 10mA. Therefore the quiescent power loss at 12V would be 120mW. Note that the bias current at a given switching frequency grows almost proportionally to the load capacitance, and the current is directly proportional to switching frequency, as previously suggested by Equation 5.

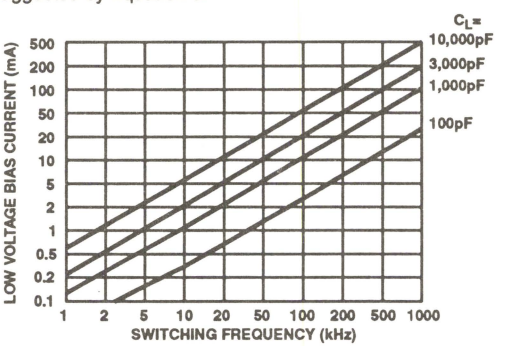


FIGURE 9. LOW VOLTAGE BIAS CURRENT vs FREQUENCY AND LOAD CAPACITANCE

High Voltage Power Dissipation

The high voltage power dissipation component is largely comprised of the high voltage level-shifter component as described by Equation 6. All of the difficulties associated with the time variance of the I_{ON} and I_{OFF} pulses and the level shift voltage, V_{SHIFT}, under the integrand in Equation 6 are avoided. For completeness, the total loss must include a small leakage current component, although the latter is usually smaller compared to the level-shifter component. The high voltage power loss calculation is the product of the high voltage bus voltage level, V_{BUS}, and the average high voltage bus current, I_{BUS}, as measured by the circuit shown in Figure 10. Averaging meters should be used to make the measurements.

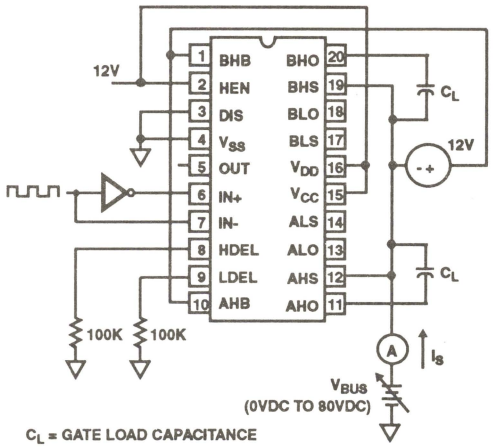


FIGURE 10. HIGH VOLTAGE LEVEL-SHIFT CURRENT TEST CIRCUIT

Figure 11 shows that the high voltage level-shift current varies directly with switching frequency. This result should not be surprising, since Equation 6 can be re-arranged to show the current as a function of frequency, which is the reciprocal of the switching period, 1/T. The test circuit of Figure 10 measures quiescent leakage current as well as the switching component. Notice that the current increases somewhat with applied bus voltage. This is due to the finite output resistance of the level-shift transistors in the IC.

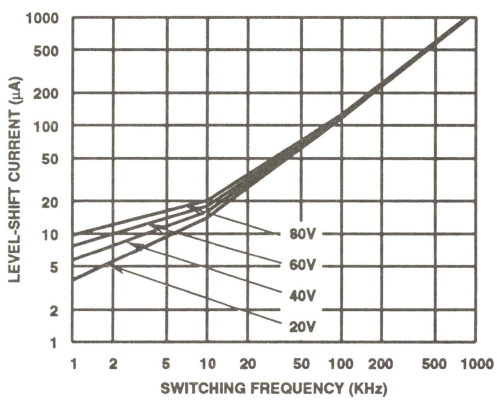


FIGURE 11. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

Layout Issues

In fast switching, high frequency systems, poor layout can result in problems. It is crucial to consider PCB layout. The HIP4080 pinout configuration encourages tight layout by placing the gate drive output terminals strategically along the right side of the chip (pin 1 is in the upper left-hand corner). This provides for short gate and source return leads connecting the IC with the power MOSFETs.

Minimize the series inductance in the gate drive loop by running the lead going out to the gate of the MOSFETs from the IC over the top of the return lead from the MOSFET sources back to the IC by using a double-sided PCB if possible. The PC board separates the traces and provides a small amount of capacitance as well as reducing the loop inductance by reducing the encircled area of the gate drive loop. The benefit is that the gate drive currents and voltages are much less prone to ringing which can similarly modulate the drain current of the MOSFET. The following table summarizes some of the layout problems which can occur and the corrective action to take.

Layout Problems and Effects

The Bootstrap circuit path should also be short to minimize series inductance that may cause the voltage on the bootstrap capacitor to ring, slowing down refresh or causing an overvoltage on the bootstrap bias supply.

A compact power circuit layout (short circuit path between upper/lower power switches) minimizes ringing on the phase lead(s) keeping BHS and AHS voltages from ringing excessively below the V_{SS} terminal which can cause excessive charge extraction from the substrate and possible malfunction of the IC.

Excessive gate lead lengths can cause gate voltage ringing and subsequent modulation of the drain current, thereby amplifying the Miller Effect.

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance may cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on the bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead(s) causing BHS and AHS to ring excessively below the V_{SS} terminal causing excessive charge extraction from the substrate and possible malfunction of the IC.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing the miller effect when an opposing switch is being rapidly turned on.

Quick Help Table

The quick help table has been included to help locate solutions to problems you may have in applying the HIP4080.

PROBLEM	EFFECT
Low chip bias voltages (V_{CC} and V_{DD})	May cause power MOSFETs to exhibit excessive R_{DSON}, possibly overheating them. below about 6V, the IC may not function properly.
High chip bias voltages (V_{CC} and V_{DD})	At V_{DD} voltages above about 12V, The charge pump limiter will begin to operate, in turn drawing heavier V_{DD} current. above 16V, Breakdown may occur.
Bootstrap capacitor(s) too small	May cause insufficient or soft charge delivery to MOSFETs at turn-on causing MOSFET overheating. Charge pump will pump charge, but possibly not quickly enough to avoid excessive switching losses.
Bootstrap capacitor(s) too large	Dead time may need to be increased in order to allow sufficient bootstrap refresh time. The alternative is to decrease bootstrap capacitance.
R_{GATE} too small	Smaller values of R_{GATE} reduces turn-on/off times and may cause excessive emi problems. Incorporating a series gate resistor with an anti-parallel diode can solve EMI problem and add to the dead time, reducing shoot-through tendency.
R_{GATE} too large	Increases switching losses and MOSFET heating. If anti-parallel diode mentioned above is in backwards, turn-off time is increased, but turn-on time is not, possibly causing a shoot-through fault.
Dead time too small	Reduces "refresh" time as well as dead time, with increased shoot-through tendency. Try increasing HDEL and LDEL resistors (don't exceed 1mΩ.)
HIP4080 IC gets too hot	Reduce bus voltage, switching frequency, choose a MOSFET with lower gate capacitance or reduce bias voltage (if it is not below 10V to 12V). Shed some of the low voltage gate switching losses in the HIP4080 by placing a small amount of series resistance in the leads going to the MOSFET gates, thereby transferring some of the IC losses to the resistors.
Lower MOSFETs turn on, but upper MOSFETs don't	Check that the HEN terminal is not tied low inadvertently.

Application Demonstration PC Board

Harris has developed a demonstration PC board to allow fast prototyping of numerous types of applications. The board was also tailored to be used to aid in characterizing the HIP4080 and HIP4081 devices under actual operating conditions.

Figure 12 and Figure 13 show the schematic and the silkscreen indicating component placement, respectively, for the HIP4080/1 demo board. Note that the board can be used to evaluate either the HIP4080 or the HIP4081, simply by changing a few jumpers.

The PC board incorporates a CD4069UB to "buffer" inputs to the HIP4080 on input terminals IN1 and IN2. Normally the polarities of IN1 and IN2 should be opposite in polarity to obtain proper H-Bridge operation. If all 4 MOSFETs are to be PWM-ed, then JMPR3 should be removed (or opened). Also the OUT terminal of the IC should not be driven, so insure JMPR1 is open. Specific recommendations for working with the HIP4081 will be discussed in the corresponding section of the application note for the HIP4081. JMPR5 should always be removed in order to implement the power up reset circuit described in data sheet HIP4080, File Number 3178. Resistors R27 and R28 as well as capacitor, C7 are not required.

Consistent with good design practice, the +12V bias supply is bypassed by capacitors C6 and C5 (at the IC terminals directly). Capacitor C6 is a 4.7µF tantalum, designed to bypass the whole PCB, whereas C5 is a 0.22µF, designed to bypass the HIP4080. The bootstrap capacitors, C3 and C4, and the high voltage bus bypass capacitors are 0.1µF, 100V ceramic. Ceramic is used here because of the low inductance required of these capacitors in the application. The bootstrap diodes are 1A, fast recovery (t_{RR} = 200ns), 100V, to minimize the charge loss from the bootstrap capacitors when the diodes become reverse-biased.

The MOSFETs supplied with the demo board is a Harris IRF520, 100V, 9A device. Since it has a gate charge of approximately 12nC, 10Ω gate resistors, R21 through R24, have been employed to deliberately slow down turn-on and turn-off of these switches. Finally, R33 and R34 provide adjustment of the dead-time. These are 500kΩ normally set for 100kΩ, which will result in a dead-time of approximately 50ns. Resistors, R30 and R31 are shunt resistors (0.1Ω, 2W, 2%, wirewound) used to provide a current-limiting signal, if desired. These may be replaced with wire jumpers if not required.

Finally, space has been provided for filter reactors, L1 and L2, and filter capacitors, C1 and C2, to provide filtering of PWM switching components from appearing at output terminals AO and BO. To facilitate placement of user-defined ICs, such as op-amps, comparators, etc., space for 3 fourteen pin standard width ICs has been reserved at the far left side of the demo board. The output terminations of the 3 optional locations are wired to holes which can be used to mount application-specific components, easing the process for building up working amplifiers for motor controls and audio amplifiers.

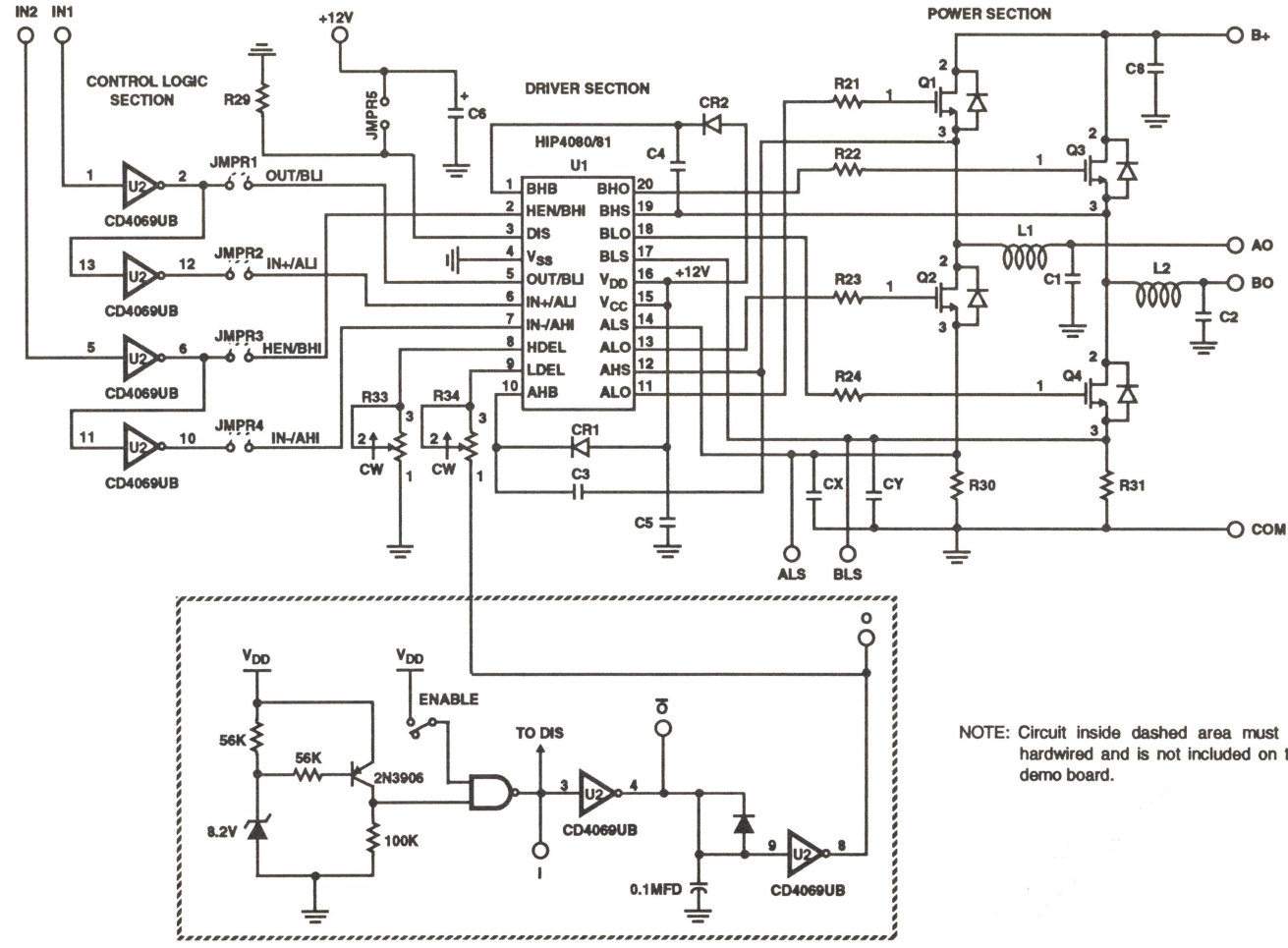


FIGURE 12. HIP4080 EVALUATION PC BOARD SCHEMATIC

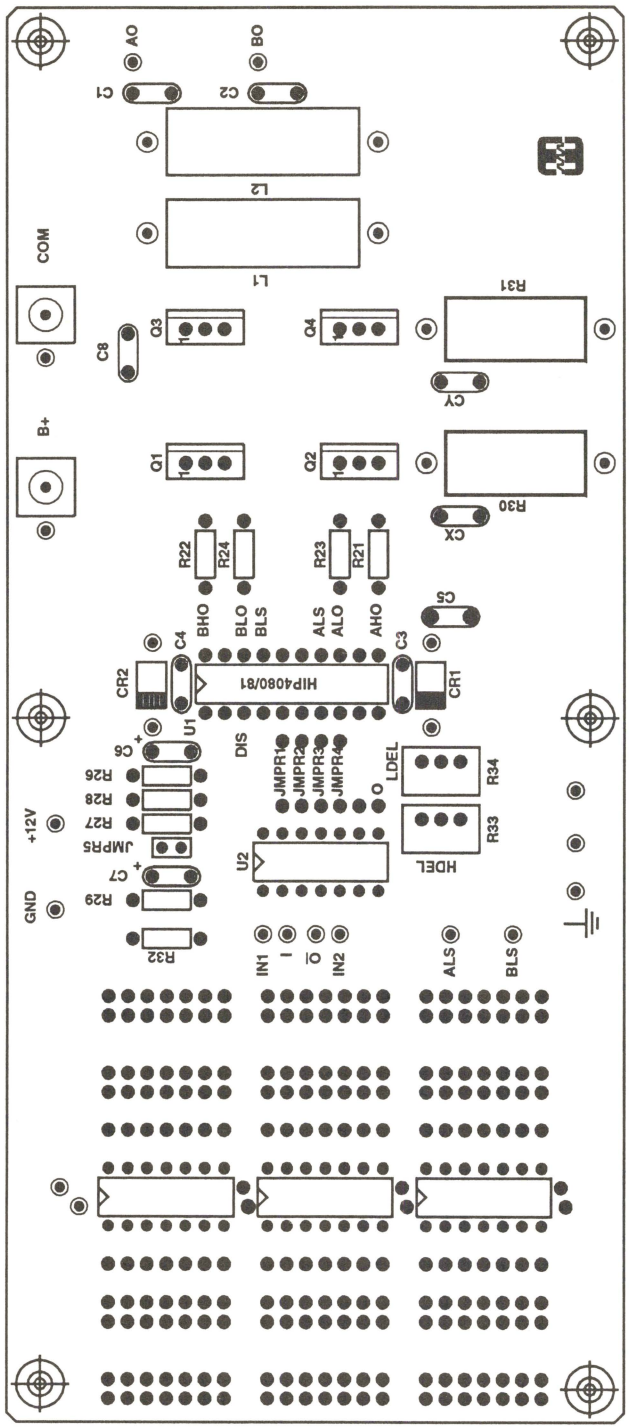


FIGURE 13. EVALUATION BOARD SILKSCREEN

Harris Semiconductor

APPNOTE

No. AN9325 April 1994

Harris Intelligent Power

HIP4081, 80V HIGH FREQUENCY H-BRIDGE DRIVER

Author: George E. Danz

Introduction

The HIP4081 is a member of the HIP408X family of High Frequency H-Bridge Driver ICs. A simplified block diagram of the HIP4081 application is shown in Figure 1. The HIP408X family of H-Bridge driver ICs provide the ability to operate from 8VDC to 80VDC busses for driving N-channel MOSFET H-Bridges, operating in class-D switch-mode. The HIP408X family, packaged in both 20 pin DIP and 20 pin SOIC DIPs, provide peak gate current drive of 2.5A.

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper halves of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to "maintain" bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin "float" along with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals to 95VDC.

The HIP4081 can drive lamp loads for automotive and industrial applications as shown in Figure 2. When inductive loads are switched, flyback diodes must be placed around the loads to protect the MOSFET switches.

Many applications utilize the full bridge topology. These are voice coil motor drives, stepper and DC brush motors, audio amplifiers and even power supply inverters used in uninterruptable power supplies, just to name a few. The HIP408X family of devices is fabricated using a proprietary Harris IC process which allows this family to switch at frequencies up to 1MHz. Therefore the HIP408X family is ideal for use in all kinds of class-D high frequency converter applications.

Two resistors tied to pins HDEL and LDEL can provide precise delay matching of upper and lower propagation delays, which are typically only 55ns. The result is accurate deadtime control for avoiding shoot-through and for maximizing the duty-cycle. The HIP4081 H-Bridge driver has enough voltage margin to meet all SELV (UL classification for operation at ≤ 42.0V) applications and most Automotive applications where "load dump" capability over 65V is required. The HIP408X family is a cost-effective solution for driving N-channel power MOSFETs, replacing discrete solutions or other solutions relying on transformer- or opto-coupling gate-drive techniques, as shown in Figure 1.

The biggest difference between the HIP4080 and the HIP4081 is that the HIP4081 allows separate and individual control of the 4 MOSFET gates, whereas the HIP4080 does not. Also the HIP4081 does not include an internal comparator which can create a PWM signal directly within the HIP4080.

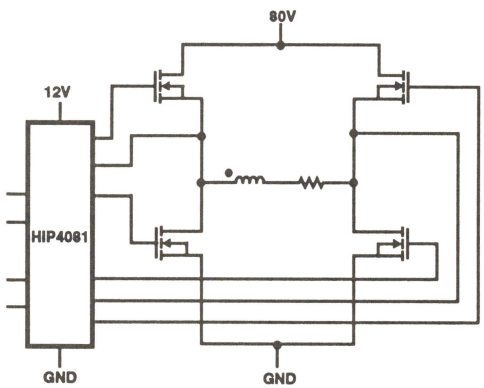


FIGURE 1. HIP4081 SIMPLIFIED APPLICATION DIAGRAM

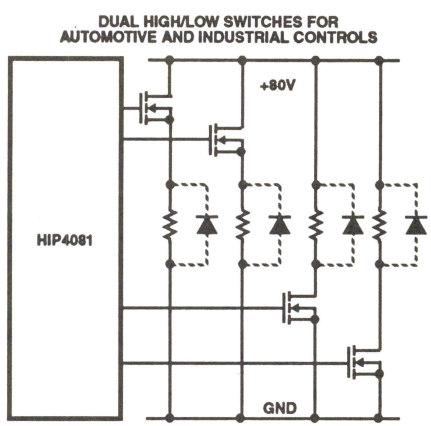


FIGURE 2. HIP4081 AS LAMP SWITCH DRIVER

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Description of the HIP4081

The block diagram of the HIP4081 relating to driving the A-side of the H-Bridge is shown in Figure 3. The blocks associated with each half of the H-Bridge are identical, so the B-side is not shown for simplicity.

The V_{CC} and V_{DD} terminals on the HIP4081 should be tied together. They were separated within the HIP4081 IC to avoid possible ground loops internal to the IC. Tieing them together and providing a decoupling capacitor from the common tie-point to V_{SS} greatly improves noise immunity.

Input Logic

The HIP4081 has 4 inputs, ALI, BLI, AHI and BHI, which control the gate outputs of the H-bridge. In addition, the DIS, "Disable," pin disables gate drive to all H-bridge MOSFETs regardless of the command states of the input pins above. The HIP4081 has pullups on the high input terminals, AHI and BHI, so that the bridge can be totally controlled using only the lower input control pins, ALI and BLI, which can greatly simplifiy the external control circuitry needed to control the HIP4081. As Table 1 suggests, the lower inputs ALI and BLI dominate the upper inputs. That is, when one of the lower nputs is high, it doesn't matter what the level of the upper input is, because the lower will turn on and the upper will remain off.

TABLE 1. INPUT LOGIC TRUTH TABLE

ALI, BLI	AHI, BHI	DIS	ALO, BLO	AHO, BHO
X	X	1	0	0
1	X	0	1	0
0	1	0	0	1
0	0	0	0	0

X = DON'T CARE 1 = HIGH/ON 0 = LOW/OFF

The input sensitivity of the DIS input pin is best described as "enhanced TTL" levels. Inputs which fall below 1.0V or rise above 2.5V are recognized, respectively, as low level or high level inputs.

Propagation Delay Control

Propagation delay control is a major feature of the HIP4081. Two identical sub-circuits within the IC delay the commutation of the power MOSFET gate turn-on signals for both A and B sides of the H-bridge. The gate turn-off signals are not delayed. Propagation delays related to the level-translation function (see section on Level-Translation) cause both upper on/off propagation delays to naturally be longer than the lower on/off propagation delays. Four delay trim sub-circuits are incorporated to better match the H-bridge delays, two for upper delay control and two for lower gate control.

Users can tailor the low side to high side commutation delay times by placing a resistor from the HDEL pin to the V_{SS} pin. Similarly, a resistor connected from LDEL to V_{SS} controls the high side to low side commutation delay times of the lower power switches. The HDEL resistor controls both upper commutation delays and the LDEL resistor controls the lower commutation delays. Each of the resistors sets a current which is inversely proportional to the created delay. The delay is added to the falling edge of the "off" pulse associated with the MOSFET which is being commutated off. When the delay is complete, the "on" pulse is initiated. This has the effect of "delaying" the commanded on pulse by the amount set by the delay, thereby creating dead-time.

Proper choice of resistor values connected from HDEL and LDEL to V_{SS} provides a means for matching the commutation dead times whether commutating high to low or low to high. Values for the resistors ranging from 10kΩ to 200kΩ are recommended. Figure 4 shows the delays obtainable as a function of the resistor values used.

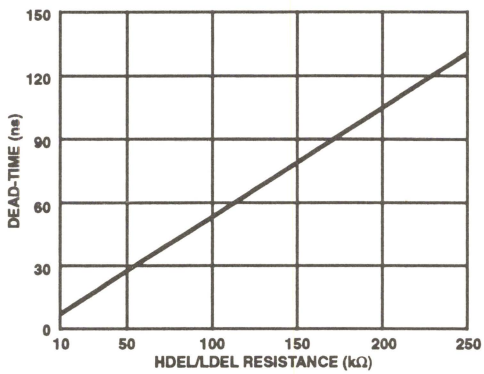


FIGURE 4. MINIMUM DEAD-TIME vs DEL RESISTANCE

Level-Translation

The lower power MOSFET gate drive signals from the propagation delay and control circuits go to amplification circuits which are described in more detail under the section "Driver Circuits". The upper power MOSFET gate drive signals are directed first to the Level-Translation circuits before going to the upper power MOSFET "Driver Circuits".

The Level-Translation circuit communicate "on" and "off" pulses from the Propagation Delay sub-circuit to the upper logic and gate drive sub-circuits which "float" at the potential of the upper power MOSFET source connections. This voltage can be as much as 85V when the bias supply voltage is only 10V (the sum of the bias supply voltage and bus voltages must not exceed 95VDC).

In order to minimize power dissipation in the level-shifter circuit, it is important to minimize the width of the pulses translated because the power dissipation is proportional to the product of switching frequency and pulse energy in joules. The pulse energy in turn is equal to the product of the bus voltage magnitude, translation pulse current and translation pulse duration. To provide a reliable, noise free pulse requires a nominal current pulse magnitude of approximately 3mA. The translated pulses are then "latched" to maintain the "on" or "off" state until another level-translation pulse

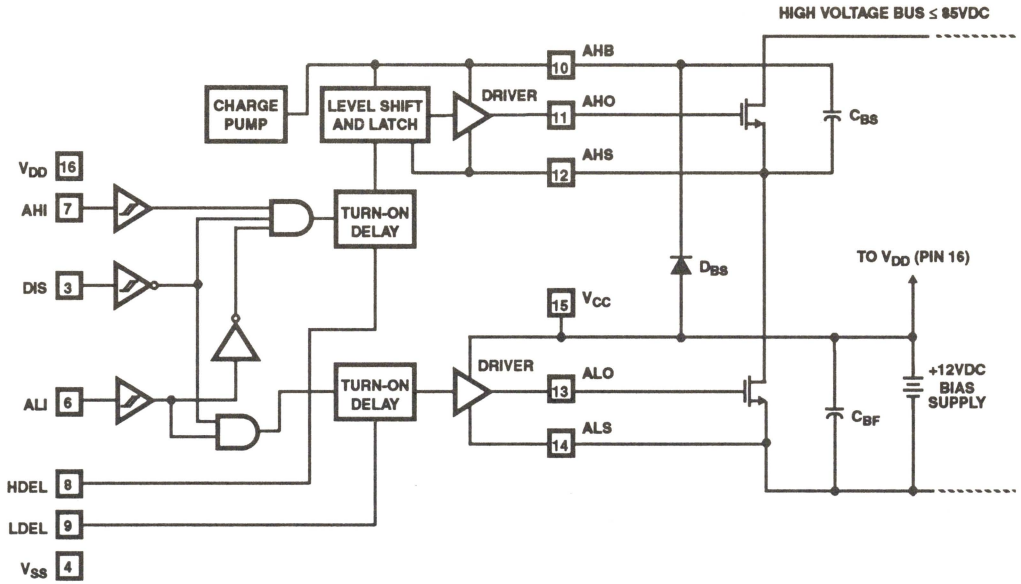


FIGURE 3. HIP4081 FUNCTIONAL BLOCK DIAGRAM

comes along to set the latch to the opposite state. Very reliable operation can be obtained with pulse widths of approximately 80ns. At a switching frequency of even 1.0MHz, with an 80VDC bus potential, the power developed by the level-translation circuit will be less than 0.08W.

Charge Pump Circuits

There are two charge pump circuits in the HIP4081, one for each of the two upper logic and driver circuits. Each charge pump uses a switched capacitor doubler to provide about 30µA to 50µA of gate load current. The sourcing current charging capability drops off as the floating supply voltage increases. Eventually the gate voltage approaches the level set by an internal zener clamp, which prevents the voltage from exceeding about 15V, the safe gate voltage rating of most commonly available MOSFETs.

Driver Circuits

Each of the four output drivers are comprised of bipolar high speed NPN transistors for both sourcing and sinking gate charge to and from the MOSFET switches. In addition, the sink driver incorporates a parallel-connected n-channel MOSFET to enable the gate of the power switch gate-source voltage to be brought completely to 0V.

The propagation delays through the gate driver sub-circuits while driving 500pF loads is typically less than 10ns. Nevertheless, the gate driver design nearly eliminates all gate driver shoot-through which significantly reduces IC power dissipation.

Application Considerations

To successfully apply the HIP4081 the designer should address the following concerns:

- General Bias Supply Design Issues
- Upper Bias Supply Circuit Design
- Bootstrap Bias Supply Circuit Design

General Bias Supply Design Issues

The bias supply design is simple. The designer must first establish the desired gate voltage for turning on the power switches. For most power MOSFETs, increasing the gate-source voltage beyond 10V yields little reduction in switch drain-source voltage drop.

Overcharging the power switch's gate-source capacitance also delays turn-off, increases MOSFET switching losses and increases the power dissipation of the HIP4081. Overcharging the MOSFET gate-source capacitance also can lead to "shoot-through" (both upper and lower MOSFETs in a single bridge leg find themselves conducting simultaneously), thereby shorting out the high voltage DC. Bias supply voltages from 12V to 150V are optimum for V_{DD} and V_{CC}.

Lower Bias Supply Design

Since most applications use identical MOSFETs for both upper and lower power switches, the bias supply requirements with respect to driving the MOSFET gates will also be identical. In case switching frequencies for driving upper and

lower MOSFETs differ, two sets of calculations must be done; one for the upper switches and one for the lower switches. The bias current budget for upper and lower switches will be the sum of each calculation. Keep in mind that the lower bias supply must also supply current to the upper gate drive and logic circuits. because the low side bias supplies (V_{CC}/V_{DD}) charge the bootstrap capacitors and the charge pumps.

Capacitor bypassing of V_{CC} and V_{DD} avoids transient voltage dips of the bias power supply to the HIP4081. Always place a low ESR (equivalent series resistance) ceramic capacitor adjacent to the IC, connected between the bias terminals V_{CC} and V_{DD} and the common terminal, V_{SS} of the IC. A value in the range of 0.22µF and 0.5µF is usually sufficient.

Minimize the effects of Miller feedback by keeping the source and gate return leads from the MOSFETs to the HIP4081 short. This also reduces ringing, by minimizing the inductance of these connections. Another way to minimize inductance in the gate charge/discharge path, in addition to minimizing path length, is to run the outbound gate lead directly "over" the source return lead. Sometimes the source return leads can form a small "ground plane" on the back side of the PC board making it possible to run the outbound gate lead "topside" on the pc board over this ground plane. This minimizes the "enclosed area" of the loop, thus minimizing inductance in this loop. It also adds some capacitance between gate and source which reduces the Miller feedback effect.

Upper Bias Supply Circuit Design

Before discussing bootstrap circuit design in detail, it is worth mentioning that it is possible to operate the HIP4081 without a bootstrap circuit altogether. Even the bootstrap capacitor, which functions to supply a reservoir of charge for rapidly turning on the MOSFETs is optional in some cases. In situations where very slow turn-on of the MOSFETs is tolerable, one may consider omitting some or all bootstrap components. Applications such as driving relays or lamp loads, where the MOSFETs are switched infrequently and switching losses are low, may provide opportunities for boot strapless operation. Generally, loads with lots of resistance and inductance are possible candidates.

Operating the HIP4081 without a bootstrap diode and/or capacitor will severely slow gate turn-on. Without a bootstrap capacitor, gate current only comes from the internal charge pump. The peak charge pump current is only about 30µA to 50µA. The gate voltage waveform, when operating without a bootstrap capacitor, will appear similar to the dotted line shown in Figure 6.

If a bootstrap capacitor value approximately equal to the equivalent MOSFET gate capacitance is used, the upper bias supply (labeled "bootstrap voltage" in Figure 5) will drop approximately in half when the gate is turned on. The larger the bootstrap capacitance used, the smaller is the instantaneous drop in bootstrap supply voltage when an upper MOSFET is turned on.

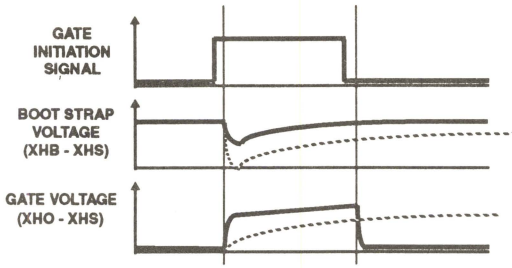


FIGURE 5.

Although not recommended, one may employ a bootstrap capacitor without a bootstrap diode. In this case the charge pump is used to charge up a capacitor whose value should be much larger than the equivalent gate-source capacitance of the driven MOSFET. A value of bootstrap capacitance about 10 times greater than the equivalent MOSFET gate-source capacitance is usually sufficient. Provided that sufficient time elapses before turning on the MOSFET again, the bootstrap capacitor will have a chance to recharge to the voltage value that the bootstrap capacitor had prior to turning on the MOSFET. Assuming 2Ω of series resistance is in the bootstrap change path, an output frequency of up to $\frac{1}{5 \times 2\Omega \times C_{BS}}$ should allow sufficient refresh time.

A bootstrap capacitor 10 times larger than the equivalent gate-source capacitance of the driven MOSFET prevents the drop in bootstrap supply voltage from exceeding 10% of the bias supply voltage during turn-on of the MOSFET. When operating without the bootstrap diode the time required to replenish the charge on the bootstrap capacitor will be the same time as it would take to charge up the equivalent gate capacitance from 0V. This is because the charge lost on the bootstrap capacitor is exactly equal to the charge transferred to the gate capacitance during turn-on. Note that the very first time that the bootstrap capacitor is charged up, it takes much longer to do so, since the capacitor must be charged from 0V. With a bootstrap diode, the initial charging of the bootstrap supply is almost instantaneous, since the charge required comes from the low-side bias supply. Therefore, before any upper MOSFETs can initially be gated, time must be allowed for the upper bootstrap supply to reach full voltage. Without a bootstrap diode, this initial "charge" time can be excessive.

If the switching cycle is assumed to begin when an upper MOSFET is gated on, then the bootstrap capacitor will undergo a charge withdrawal when the source driver connects it to the equivalent gate-source capacitance of the MOSFET. After this initial "dump" of charge, the quiescent current drain experienced by the bootstrap supply is infinitesimal. In fact, the quiescent supply current is more than offset by the charge pump current.

The charge pump continuously supplies current to the bootstrap supply and eventually would charge the bootstrap capacitor and the MOSFET gate capacitance back to its initial value prior to the beginning of the switching cycle. The problem is that "eventually" may not be fast enough when the switching frequency is greater than a few hundred Hz.

Bootstrap Bias Supply Circuit Design

For high frequency applications all bootstrap components, both diodes and capacitors, are required. Therefore, one must be familiar with bootstrap capacitor sizing and proper choice of bootstrap diode.

Just after the switch cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is the lowest that it will ever be during the switch cycle. The charge lost on the bootstrap capacitor will be very nearly equal to the charge transferred to the equivalent gate-source capacitance of the MOSFET as shown in Equation 1.

$$Q_G = (V_{BS1} - V_{BS2}) \times C_{BS} \quad \text{(EQ.1)}$$

where:

V_{BS1} = Bootstrap capacitor voltage just after refresh

V_{BS2} = Bootstrap voltage immediately after upper turn-on

C_{BS} = Bootstrap Capacitance

Q_G = Gate charge transferred during turn-on

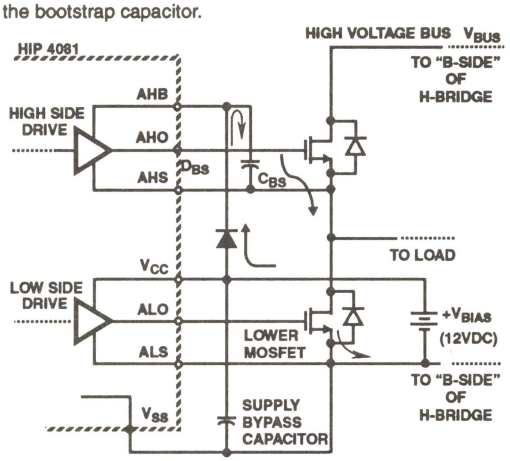
Were it not for the internal charge pump, the voltage on the bootstrap capacitor and the gate capacitor (because an upper MOSFET is now turned on) would eventually drain down to zero due to bootstrap diode leakage current and the very small supply current associated with the level-shifters and upper gate driver sub-circuits.

In PWM switch-mode, the switching frequency is equal to the reciprocal of the period between successive turn-on (or turn-off) pulses. Between any two turn-on gate pulses exists one turn-off pulse. Each time a turn-off pulse is issued to an upper MOSFET, the bootstrap capacitor of that MOSFET begins its "refresh" cycle. A refresh cycle ends when the upper MOSFET is turned on again, which varies depending on the PWM frequency and duty cycle. As the duty cycle approaches 100%, the available "off-time", t_{OFF} approaches zero. Equation 2 shows the relationship between t_{OFF}, f_{PWM} and the duty cycle.

$$t_{OFF} = (1 - DC)/f_{PWM} \quad \text{(EQ.2)}$$

As soon as the upper MOSFET is turned off, the voltage on the phase terminal (the source terminal of the upper MOSFET) begins its descent toward the negative rail of the high voltage bus. When the phase terminal voltage becomes less than the V_{CC} voltage, refreshing (charging) of the bootstrap capacitor begins. As long as the phase voltage is below V_{CC} refreshing continues until the bootstrap and V_{CC} voltages are equal.

The off-time of the upper MOSFET is dependent on the gate control input signals, but it can never be shorter than the dead-time delay setting, which is set by the resistors connecting HDEL and LDEL to V_{SS}. If the bootstrap capacitor is not fully charged by the time the upper MOSFET turns on again, incomplete refreshing occurs. The designer must insure that the dead-time setting be consistent with the size of the bootstrap capacitor in order to guarantee complete refreshing. Figure 6 illustrates the circuit path for refreshing the bootstrap capacitor.



NOTE: Only "A-side" of H-bridge Is Shown for Simplicity. Arrows Show Bootstrap Charging Path.

FIGURE 6. BOOTSTRAP CAPACITOR CHARGING PATH

The bootstrap charging and discharging paths should be kept short, minimizing the inductance of these loops as mentioned in the section, "Lower Bias Supply Design".

Bootstrap Circuit Design - An Example

Equation 1 describes the relationship between the gate charge transferred to the MOSFET upon turn-on, the size of the bootstrap capacitor and the change in voltage across the bootstrap capacitor which occurs as a result of turn-on charge transfer.

The effects of reverse leakage current associated with the bootstrap diode and the bias current associated with the upper gate drive circuits also affect bootstrap capacitor sizing. At the instant that the upper MOSFET turns on and its source voltage begins to rapidly rise, the bootstrap diode becomes rapidly reverse biased resulting in a reverse recovery charge which further depletes the charge on the bootstrap capacitor. To completely model the total charge transferred during turn-on of the upper MOSFETs, these effects must be accounted for, as shown in Equation 3.

$$C_{BS} = \frac{Q_G + Q_{RR} + \frac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \quad \text{(EQ.3)}$$

where:

I_{DR} = Bootstrap diode reverse leakage current

I_{QBS} = Upper supply quiescent current

Q_{RR} = Bootstrap diode reverse recovered charge

Q_G = Turn-on gate charge transferred

f_{PWM} = PWM operating frequency

V_{BS1} = Bootstrap capacitor voltage just after refresh

V_{BS2} = Bootstrap capacitor voltage just after upper turn on

C_{BS} = Bootstrap capacitance

From a practical standpoint, the bootstrap diode reverse leakage and the upper supply quiescent current are negligible, particularly since the HIP4081's internal charge pump continuously sources a minimum of about 30µA. This current more than offsets the leakage and supply current components, which are fixed and not a function of the switching frequency. The higher the switching frequency, the lower is the charge effect contributed by these components and their effect on bootstrap capacitor sizing is negligible, as shown in Equation 3. Supply current due to the bootstrap diode recovery charge component increases with switching frequency and generally is not negligible. Hence the need to use a fast recovery diode. Diode recovery charge information can usually be found in most vendor data sheets.

For example, if we choose a Harris IRF520R power MOSFET, the data book states a gate charge, Q_G, of 12nC typical and 18nC maximum, both at V_{DS} = 12V. Using the maximum value of 18nC the maximum charge we should have to transfer will be less than 18nC.

Suppose a General Instrument UF4002, 100V, fast recovery, 1A, miniature plastic rectifier is used. The data sheet gives a reverse recovery time of 25ns. Since the recovery current waveform is approximately triangular, the recovery charge can be approximated by taking the product of half the peak reverse current magnitude (1A peak) and the recovery time duration (25ns). In this case the recovery charge should be 12.5nC.

Since the internal charge pump offsets any possible diode leakage and upper drive circuit bias currents, these sources of discharge current for the bootstrap capacitor will be ignored. The bootstrap capacitance required for the example above can be calculated as shown in Equation 4, using Equation 2.

$$C_{BS} = \frac{18nC + 12.5nC}{12.0 - 11.0} \quad \text{(EQ. 4)}$$

Therefore a bootstrap capacitance of 0.033µF will result in less than a 1.0V droop in the voltage across the bootstrap capacitor during the turn-on period of either of the upper MOSFETs. If typical values of gate charge and bootstrap diode recovered charge are used rather than the maximum value, the voltage droop on the bootstrap supply will be only about 0.5V

Power Dissipation and Thermal Design

One way to model the power dissipated in the HIP4081 is by lumping the losses into static losses and dynamic (switching) losses. The static losses are due to bias current losses for the upper and lower sections of the IC and include the sum of the I_{CC} and I_{DD} currents when the IC is not switching. The quiescent current is approximately 9mA. Therefore with a 12V bias supply, the static power dissipation in the IC is slightly over 100mW.

The dynamic losses associated with switching the power MOSFETs are much more significant and can be divided into the following categories:

- Low Voltage Gate Drive (charge transfer)
- High Voltage Level-shifter (V-I) Losses
- High Voltage Level-shifter (charge transfer)

In practice, the high voltage level-shifter and charge transfer losses are small compared to the gate drive charge transfer losses.

The more significant low voltage gate drive charge transfer losses are caused by the movement of charge in and out of the equivalent gate-source capacitor of each of the 4 MOSFETs comprising the H-bridge. The loss is a function of PWM (switching) frequency, the applied bias voltage, the equivalent gate-source capacitance and a minute amount of CMOS gate charge internal to the HIP4081. The low voltage charge transfer losses are given by Equation 5.

$$P_{SWLO} = f_{PWM} \times (Q_G + Q_{IC}) \times V_{BIAS} \quad \text{(EQ. 5)}$$

The high voltage level-shifter power dissipation is much more difficult to evaluate, although the equation which defines it is simple as shown in Equation 6. The difficulty arises from the fact that the level-shift current pulses, I_{ON} and I_{OFF}, are not perfectly in phase with the voltage at the upper MOSFET source terminals, V_{SHIFT} due to propagation delays within the IC. These time-dependent source voltages (or "phase" voltages) are further dependent on the gate capacitance of the driven MOSFETs and the type of load (resistive, capacitive or inductive) which determines how rapidly the MOSFETs turn on. For example, the level-shifter I_{ON} and I_{OFF} pulses may come and go and be latched by the upper logic circuits before the phase voltage even moves. As a result, little level-shift power dissipation may result from the i_{ON} pulse, whereas the I_{OFF} pulse may have a significant power dissipation associated with it, since the phase voltage generally remains high throughout the duration of the i_{OFF} pulse.

(EQ. 6)

$$P_{SHIFT} = \frac{1}{T}\int_0^T (I_{ON}(t) + I_{OFF}(t)) \times V_{SHIFT}(t) \times dt$$

Lastly, there is power dissipated within the IC due to charge transfer in and out of the capacitance between the upper driver circuits and V_{SS}. Since it is a charge transfer phenomena, it closely resembles the form of Equation 5, except that the capacitance is much smaller than the equivalent gate-source capacitances associated with power MOSFETs. On the other hand, the voltages associated with the level-shifting function are much higher than the voltage changes experienced at the gate of the MOSFETs. The relationship is shown in Equation 7.

$$P_{TUB} = C_{TUB} \times V_{SHIFT}^2 \times f_{PWM} \quad \text{(EQ. 7)}$$

The power associated with each of the two high voltage tubs in the HIP4081 derived from Equation 7 is quite small, due to the extremely small capacitance associated with these tubs. A "tub" is the isolation area which surrounds and isolates the

high side circuits from the ground referenced circuits of the IC. The important point for users is that the power dissipated is linearly related to switching frequency and the square of the applied bus voltage.

The tub capacitance in Equation 7 varies with applied voltage, V_{SHIFT}, making its solution difficult, and the phase shift of the I_{ON} and I_{OFF} pulses with respect to the phase voltage, V_{SHIFT}, in Equation 6 are difficult to measure. Even the Q_{IC} in Equation 5 is not easy to measure. Hence the use of Equation 5 through Equation 7 to calculate total power dissipation is at best difficult. The equations do, however, allow users to understand the significance that MOSFET choice, switching frequency and bus voltage play in determining power dissipation. This knowledge can lead to corrective action when power dissipation becomes excessive.

Fortunately, there is an easy method which can be used to measure the components of power dissipation rather than calculating them, except for the tiny "tub capacitance" component.

Power Dissipation, the Easy Way

The average power dissipation associated with the IC and the gate of the connected MOSFETs can easily be measured using a signal generator, an averaging milliameter and a voltmeter.

Low Voltage Power Dissipation

Two sets of measurements are required. The first set uses the circuit of Figure 7 and evaluates all of the low voltage power dissipation components. These components include the MOSFET gate charge and internal CMOS charge transfer losses shown in Equation 5 as well as the quiescent bias current losses associated with the IC. The losses are calculated very simply by calculating the product of the bias voltage and current measurements as performed using the circuit shown in Figure 8. For measurement purposes, the phase terminals (AHS and BHS) for both A and B phases are both tied to the chip common, V_{SS} terminal, along with the lower source terminals, ALS and BLS. Capacitors equal to the equivalent gate-source capacitance of the MOSFETs are connected from each gate terminal to V_{SS}. The value of the capacitance chosen comes from the MOSFET manufacturers data sheet. Notice that the MOSFET data sheet usually gives the value in units of charge (usually nanocoulombs) for different drain-source voltages. Choose the drain-source voltage closest to the particular DC bus voltage of interest.

Simply substituting the actual MOSFETs for the capacitors, C_L, doesn't yield the correct average current because the Miller capacitance will not be accounted for. This is because the drains don't switch using the test circuit shown in Figure 7. Also the gate capacitance of the devices you are using may not represent the maximum values which only the data sheet will provide.

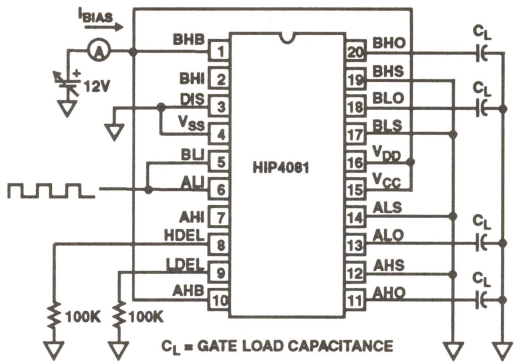


FIGURE 7. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

The low voltage charge transfer switching currents are shown in Figure 8. Figure 8 does not include the quiescent bias current component, which is the bias current which flows in the IC when switching is disabled. The quiescent bias current component is approximately 10mA. Therefore the quiescent power loss at 12V would be 120mW. Note that the bias current at a given switching frequency grows almost proportionally to the load capacitance, and the current is directly proportional to switching frequency, as previously suggested by Equation 5.

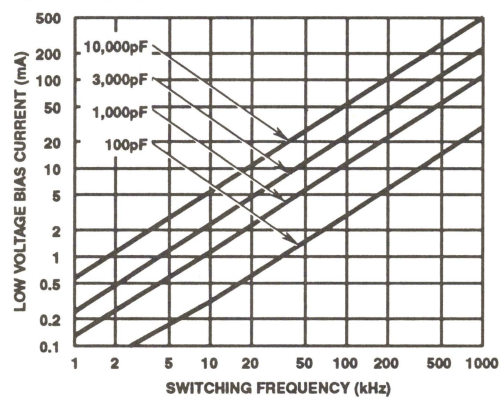


FIGURE 8. LOW VOLTAGE BIAS CURRENT I_{DD} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

High Voltage Power Dissipation

The high voltage power dissipation component is largely comprised of the high voltage level-shifter component as described by Equation 6. All of the difficulties associated with the time variance of the I_{ON} and I_{OFF} pulses and the level shift voltage, V_{SHIFT}, under the integrand in Equation 6 are avoided. For completeness, the total loss must include a small leakage current component, although the latter is usually smaller compared to the level-shifter component. The

high voltage power loss calculation is the product of the high voltage bus voltage level, V_{BUS}, and the average high voltage bus current, I_{BUS}, as measured by the circuit shown in Figure 9. Averaging meters should be used to make the measurements.

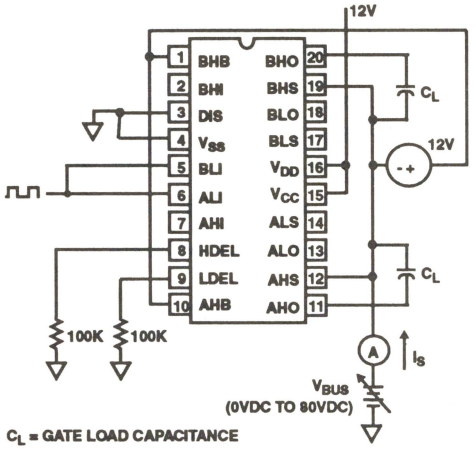


FIGURE 9. HIGH VOLTAGE LEVEL-SHIFT CURRENT TEST CIRCUIT

Figure 10 shows that the high voltage level-shift current varies directly with switching frequency. This result should not be surprising, since Equation 6 can be re-arranged to show the current as a function of frequency, which is the reciprocal of the switching period, 1/T. Notice that the current increases somewhat with applied bus voltage. This is due to the finite output resistance of the level-shift transistors in the IC.

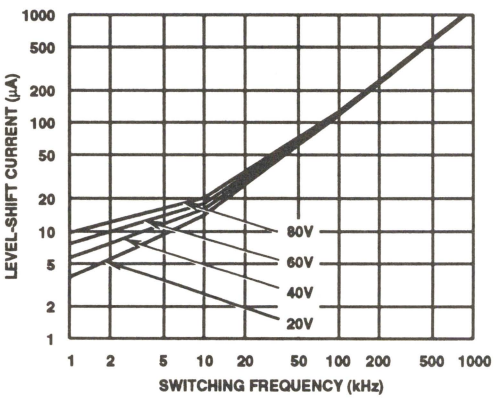


FIGURE 10. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

Layout Problems and Effects

In fast switching, high frequency systems, proper PC board layout is crucial. to consider PCB layout. The HIP4081 pinout configuration encourages tight layout by placing the gate drive output terminals strategically along the right side of the chip (pin 1 is in the upper left-hand corner). This provides for short gate and source return leads connecting the IC with the power MOSFETs.

Always minimize the series inductance in the gate drive loop by running the gate leads to the MOSFETs over the top of the source return leads of the MOSFETs. A double-sided PCB makes this easy. The PC board separates the traces and provides a small amount of capacitance as well as reducing the loop inductance by reducing the encircled area of the gate drive loop. The result is reduced ringing which can similarly reduce drain current modulate in the MOSFET. The table below summarizes some layout problems which can occur and the corrective action to take.

The Bootstrap circuit path should also be kept short. This minimizes series inductance that may cause the voltage on the boot-strap capacitor to ring, slowing down refresh or causing an overvoltage on the bootstrap bias supply.

A compact power circuit layout (short circuit path between upper/lower power switches) minimizes ringing on the phase lead(s) keeping BHS and AHS voltages from ringing excessively below the V_{SS} terminal which can cause excessive charge extraction from the substrate and possible malfunction of the IC.

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance may cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on the bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead(s) causing BHS and AHS to ring excessively below the V_{SS} terminal causing excessive charge extraction from the substrate and possible malfunction of the IC.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing the miller effect when an opposing switch is being rapidly turned on.

Quick Help Table

The quick help table has been included to help locate solutions to problems you may have in applying the HIP4081.

PROBLEM	EFFECT
Low chip bias voltages (V_{CC} and V_{DD})	May cause power MOSFETs to exhibit excessive R_{DSON}, possibly overheating them. Below 6V, the IC will not function properly.
High chip bias voltages (V_{CC} and V_{DD})	At V_{DD} voltages above about 12V. The charge pump limiter will begin to operate, in turn drawing heavier V_{DD} current. Above 16V, breakdown may occur.
Bootstrap capacitor(s) too small	May cause insufficient or soft charge delivery to MOSFETs at turn-on causing MOSFET overheating. Charge pump will pump charge, but possibly not quickly enough to avoid excessive switching losses.
Bootstrap capacitor(s) too large	Dead time may need to be increased in order to allow sufficient bootstrap refresh time. The alternative is to decrease bootstrap capacitance.
R_{GATE} too small	Smaller values of R_{GATE} reduces turn-on/off times and may cause excessive emi problems. Incorporating a series gate resistor with an anti-parallel diode can solve EMI problem and add to the dead time, reducing shoot-through tendency.
R_{GATE} too large	Increases switching losses and MOSFET heating. If anti-parallel diode mentioned above is in backwards, turn-off time is increased, but turn-on time is not, possibly causing a shoot-through fault.
Dead time too small	Reduces "refresh" time as well as dead time, with increased shoot-through tendency. Try increasing HDEL and LDEL resistors (don't exceed 1mΩ).
HIP4081 IC gets too hot	Reduce bus voltage, switching frequency, choose a MOSFET with lower gate capacitance or reduce bias voltage (if it is not below 6V to 12V). Shed some of the low voltage gate switching losses in the HIP4081 by placing a small amount of series resistance in the leads going to the MOSFET gates, thereby transferring some of the IC losses to the resistors.
Lower MOSFETs turn on, but upper MOSFETs don't	Check that the HEN terminal is not tied low inadvertently.

Application Demonstration PC Board

Harris has developed a demonstration PC board to allow fast prototyping of numerous types of applications. The board was also tailored to be used to aid in characterizing the HIP4081device under actual operating conditions.

Figure 11 and Figure 12 show the schematic and the silkscreen indicating component placement, respectively, for the HIP4080/81 demo board. Note that the board can be used to evaluate either the HIP4080 or the HIP4081, simply by changing a few jumpers. Refer to the appropriate application note for instructions on jumber placement.

The PC board incorporates a CD4069UB to "buffer" inputs to the HIP4081. JMPR5, resistors R27 and R28, and capacitor C7 must be removed in order to implement the power up reset circuit described in this application note and in the HIP4081 data sheet, File Number 3556.

Consistent with good design practice, the +12V bias supply is bypassed by capacitors C6 and C5 (at the IC terminals directly). Capacitor C6 is a 4.7µF tantalum, designed to bypass the whole PCB, whereas C5 is a 0.22µF, designed to bypass the HIP4081. The bootstrap capacitors, C3 and C4, and the high voltage bus bypass capacitors are 0.1µF, 100V ceramic. Ceramic is used here because of the low inductance required of these capacitors in the application. The bootstrap diodes are 1A, fast recovery (t_{RR} = 200ns), 100V, to minimize the charge loss from the bootstrap capacitors when the diodes become reverse-biased.

The MOSFETs supplied with the demo board is a Harris IRF520, 100V, 9A device. Since it has a gate charge of approximately 12nC, 10Ω gate resistors, R21 through R24, have been employed to deliberately slow down turn-on and turn-off of these switches. Finally, R33 and R34 provide adjustment of the dead-time. These are 500kΩ normally set for 100kΩ, which will result in a dead-time of approximately 50ns. Resistors, R30 and R31 are shunt resistors (0.1Ω, 2W, 2%, wirewound) used to provide a current-limiting signal, if desired. These may be replaced with wire jumpers if not required.

Finally, space has been provided for filter reactors, L1 and L2, and filter capacitors, C1 and C2, to provide filtering of PWM switching components from appearing at output terminals AO and BO. To facilitate placement of user-defined ICs, such as op-amps, comparators, etc., space for 3 fourteen pin standard width ICs has been reserved at the far left side of the demo board. The output terminations of the 3 optional locations are wired to holes which can be used to mount application-specific components, easing the process for building up working amplifiers for motor controls and audio amplifiers.

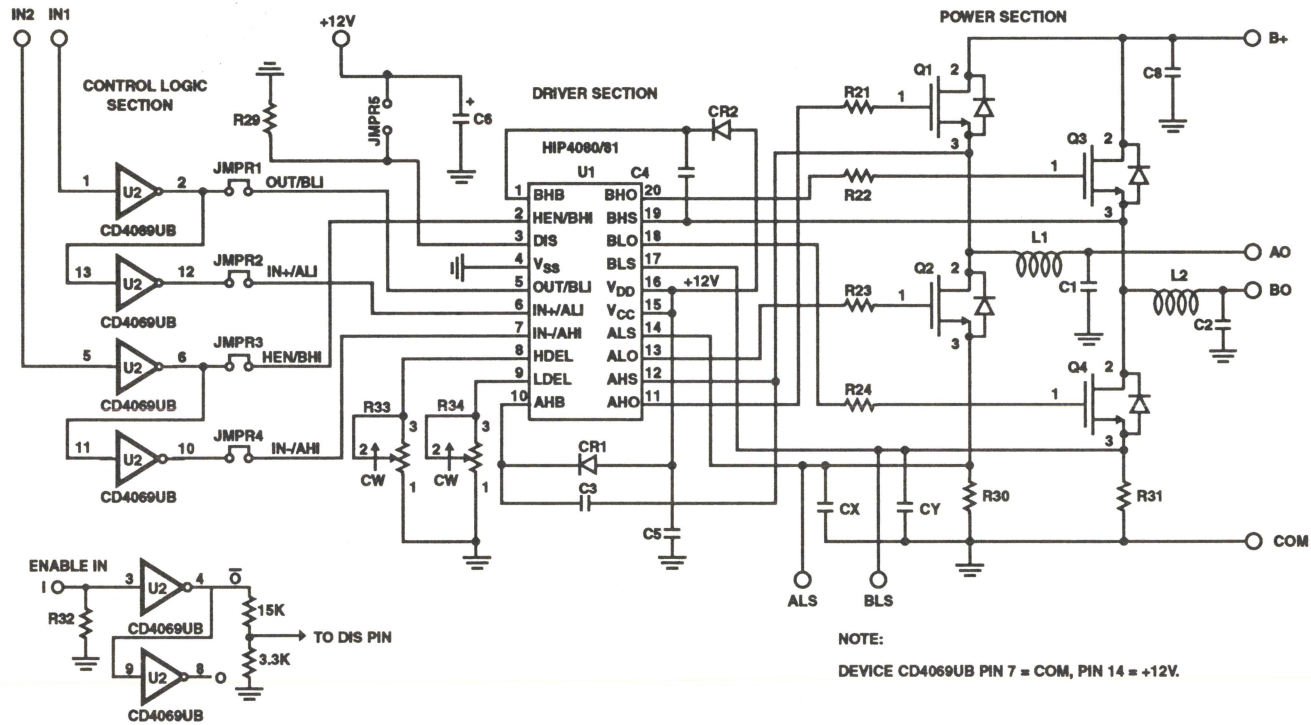


FIGURE 12. HIP4081 EVALUATION PC BOARD SCHEMATIC

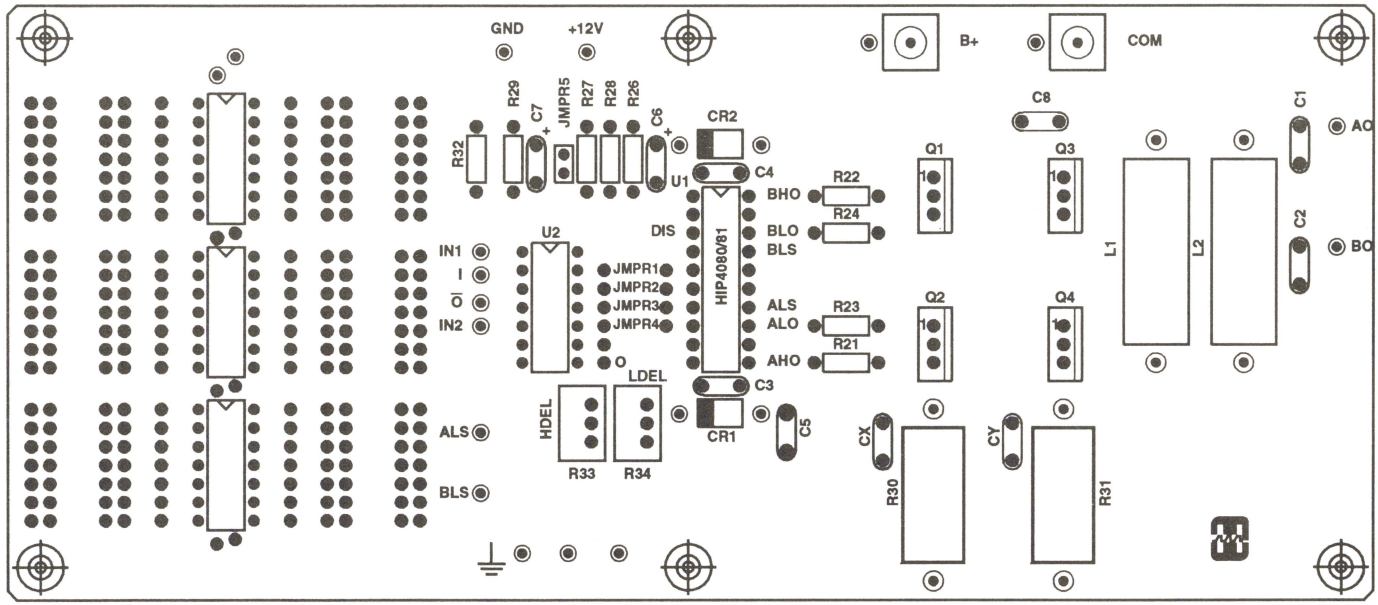


FIGURE 13. EVALUATION BOARD SILKSCREEN

Harris Semiconductor

APPNOTE

No. AN9404 April 1994

Harris Intelligent Power

HIP4080A, 80V HIGH FREQUENCY H-BRIDGE DRIVER

Author: George E. Danz

Introduction

The HIP4080A is a member of the HIP408X family of High Frequency H-Bridge Driver ICs. A simplified application diagram of the HIP4080A IC is shown in Figure 1. The HIP408X family of H-Bridge driver ICs provide the ability to operate from 10VDC to 80VDC busses for driving H-Bridges, operating in class-D switch-mode, whose switch elements are comprised of power N-channel MOSFETs. The HIP408X family, packaged in both 20 pin DIP and 20 pin SOIC DIPs, provide peak gate current drive of 2.5A. The HIP4080A includes undervoltage protection, which sends a continuous gate turn-off pulse to all gate outputs when the V_{DD} voltage falls below a nominal 8.25 volts. The startup sequence of the HIP4080A is initiated when the V_{DD} voltage returns above a nominal 8.75 volts. Of course, the DIS pin must be in the low state for the IC to be enabled. The startup sequence turns on both low side outputs, ALO and BLO, so that the bootstrap capacitors for both sides of the H-bridge can be fully charged. During this time the AHO and BHO gate outputs are held low continuously to insure that no shoot-through can occur during the nominal 400ns boot-strap refresh period. At the end of the boot strap refresh period the outputs respond normally to the state of the input control signals.

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper halves of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to "maintain" bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin "float" along with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals to 95VDC.

The HIP4080A can drive lamp loads for automotive and industrial applications as shown in Figure 2. When inductive loads are switched, flyback diodes must be placed around the loads to protect the MOSFET switches.

Many applications utilize the full bridge topology. These are voice coil motor drives, stepper and DC brush motors, audio amplifiers and even power supply inverters used in uninterruptable power supplies, just to name a few. Of the above, voice coil motor drives and audio amplifiers can take advantage of the built-in comparator available in the HIP4080A. Using the output of the comparator to add some positive feedback, a hysteresis control, so popular with voice coil motor drivers, can be implemented as shown in Figure 3. In the figure, R3 is fed back from the comparator output, OUT, to the positive input of the comparator, IN+. Capacitor, C1, integrates in a direction to satisfy the reference current signal at IN. The IN- input of the comparator sums this current reference with a signal proportional to load current through resistor, R4, which comes from a differential amplifier, A1. A bias voltage of 6V (represents half of the bias voltage and the maximum rail to rail voltage of the comparator and amplifier, A1) biases the comparator's IN+ terminal through R2 and the amplifier, A1's, positive summing junction.

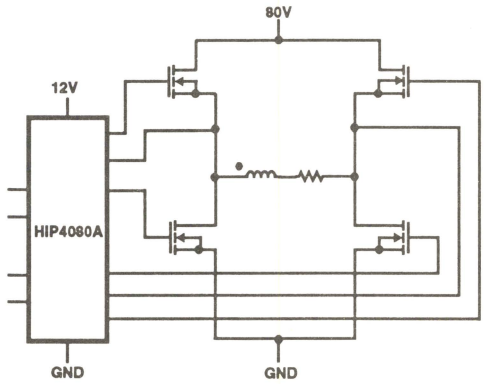


FIGURE 1. HIP4080A SIMPLIFIED APPLICATION DIAGRAM

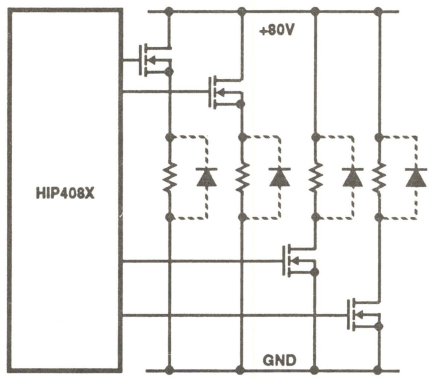


FIGURE 2. HIP4080A AS LAMP SWITCH DRIVER, DUAL HIGH/ LOW SWITCHES FOR AUTOMOTIVE AND INDUS-

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When no current is flowing in either direction in the load, the output of A1 is exactly 6V. The reference input, IN, would also have to be 6V to request zero current from the bridge.

The bridge would still switch in this case, because of the positive feedback connection of the HIP4080A internal comparator. The frequency of oscillation of the output will be a function of the amount of dc hysteresis gain, R3/R1 and the size of capacitor, C1. As the capacitor, C1, is made larger, the steady-state frequency of the bridge will become smaller. It is beyond the scope of this application note to provide a full analysis. A valuable characteristic of hysteresis control is that as the error becomes smaller (i.e. the reference and feedback signals match) the frequency increases. Usually this occurs when the load current is small or at a minimum. When the error signal is large, the frequency becomes very small, perhaps even dc. One advantage of this is that when currents are largest, switching losses are a minimum, and when switching losses are largest, the dc current component is small.

The HIP408X family of devices is fabricated using a proprietary Harris IC process which allows this family to switch at frequencies of over 500kHz. Therefore the HIP408X family is ideal for use in Voice coil motor, class-D audio amplifier, DC-DC converters and high performance AC, DC and step-motor control applications.

To provide accurate dead-time control for the twin purposes of shoot-through avoidance and duty-cycle maximization, two resistors tied to pins HDEL and LDEL provide precise delay matching of upper and lower propagation delays, which are typically only 55ns. The HIP408X family of H-bridge drivers has enough voltage margin to be applied to all SELV (UL classification for operation at ≤ 42.0V) applications and most Automotive applications where "load dump" capability over 65V is required. This capability makes the HIP408X family a more cost-effective solution for driving N-channel power MOSFETs than either discrete solutions or other solutions relying on transformer- or opto-coupling gate-drive techniques as shown in Figure 1.

The HIP4080A differs from the HIP4081A regarding the function of pins 2, 5, 6 and 7 of the IC and the truth table which governs the switching function of the two ICs. In the HIP4080A, pins 2, 5, 6 and 7 are labeled HEN, OUT, IN+ and IN-, respectively. In the HIP4081A, pins 2, 5, 6 and 7 are labeled BHI (B-side high input), BLI (B-side low input), ALI (A-side low input) and AHI (A-side high input), respectively. The HIP4081A's inputs individually control each of the four power MOSFETs, or in pairs (excepting the shoot-through case). The HIP4080A provides an internal comparator and a "high enable...HEN" pin. The comparator can be used to provide a PWM logic signal to switch the appropriate MOSFETs within the H-bridge, and can facilitate "Hysteresis" control to be illustrated later. The HEN pin enables (when HEN is high) or disables (when HEN is low) the A-side and B-side upper MOSFETs. With HEN held low, it is possible to switch only the lower H-bridge MOSFETs. When HEN is high both upper and lower MOSFETs of the H-bridge are switched. The HEN input can also be PWM-switched with the IN+ and IN- inputs used only for direction control, thereby minimizing switching losses.

Description of the HIP4080A

The block diagram of the HIP4080A relating to driving the A-side of the H-Bridge is shown in Figure 4. The blocks associated with each side of the H-Bridge are identical, so the B-side is not shown for simplicity.

The two bias voltage terminals, V_{CC} and V_{DD}, on the HIP4080A should be tied together. They were separated within the HIP4080A to avoid possible ground loops internal to the IC. Tieing them together and providing a decoupling capacitor from the common tie-point to V_{SS} greatly improves noise immunity.

Input Logic

The HIP4080A accepts inputs which control the output state of the power MOSFET H-bridge and provides a comparator output pin, OUT, which can provide compensation or hysteresis.

The DIS, "Disable," pin disables gate drive to all H-bridge MOSFETs regardless of the command states of the input pins, IN+, IN- and HEN. The state of the bias voltage, V_{DD}, also can disable all gate drive as discussed in the introduction. The HEN, "High Enable," pin enables and disables gate drive to the two high side MOSFETs. A high level on the HEN pin "enables" high side gate drive as further determined by the states of the IN+ and IN- comparator input pins, since the IN+ and IN- pins control which diagonal pair of MOSFETs are gated. Upper drive can be "modulated" through use of the HEN pin while drive to diagonally opposing lower MOSFETs is continuous. To simultaneously modulate both upper and lower drivers, HEN is continuously held high while modulating the IN+ and IN- pins.

Modulating only the upper switches can nearly halve the switching losses in both the driver IC and in the lower MOSFETs. The power dissipation saved at high switching frequencies can be significant. Table 1 summarizes the input control logic.

The input sensitivity of the DIS and HEN input pins are best described as "enhanced TTL" levels. Inputs which fall below 1.0V or above 2.5V are recognized, respectively, as low level or high level inputs. The IN+ and IN- comparator inputs have a common mode input voltage range of 1.0V to V_{DD} -1.5V, whereas the offset voltage is less than 5mV. For more information on the comparator specifications, see Harris Data Sheet HIP4080A, File Number 3658.

TABLE 1. INPUT LOGIC TRUTH TABLE

IN+ > IN-	U/V	DIS	HEN	ALO	AHO	BLO	BHO
X	X	1	X	0	0	0	0
X	1	X	X	0	0	0	0
1	0	0	1	0	1	1	0
0	0	0	1	1	0	0	1
1	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0

X = DON'T CARE 1 = HIGH/ON 0 = LOW/OFF

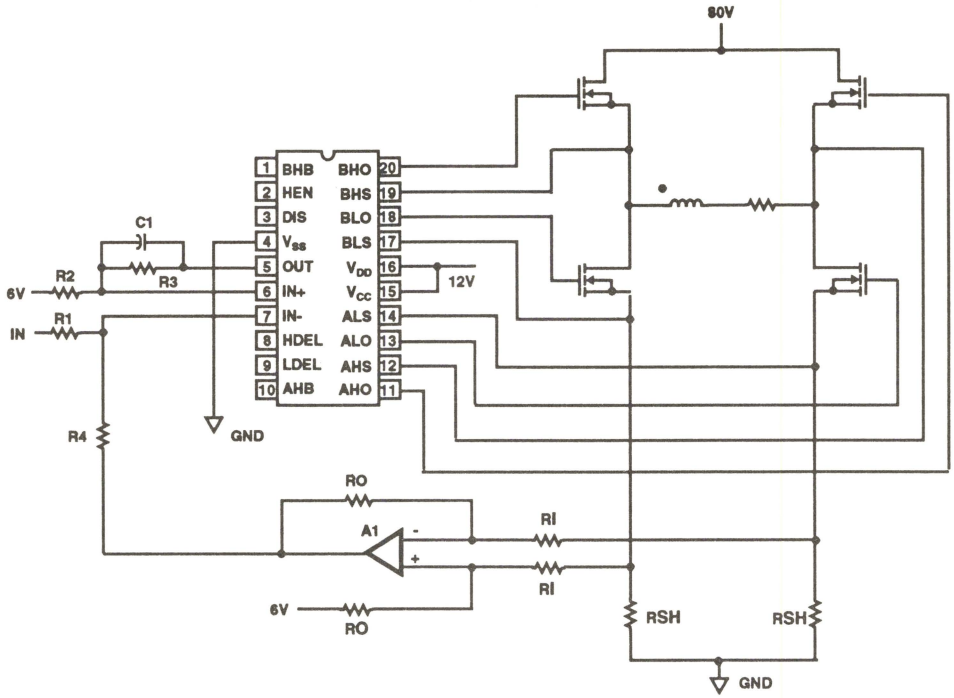


FIGURE 3. HYSTERESIS MODE SWITCHING

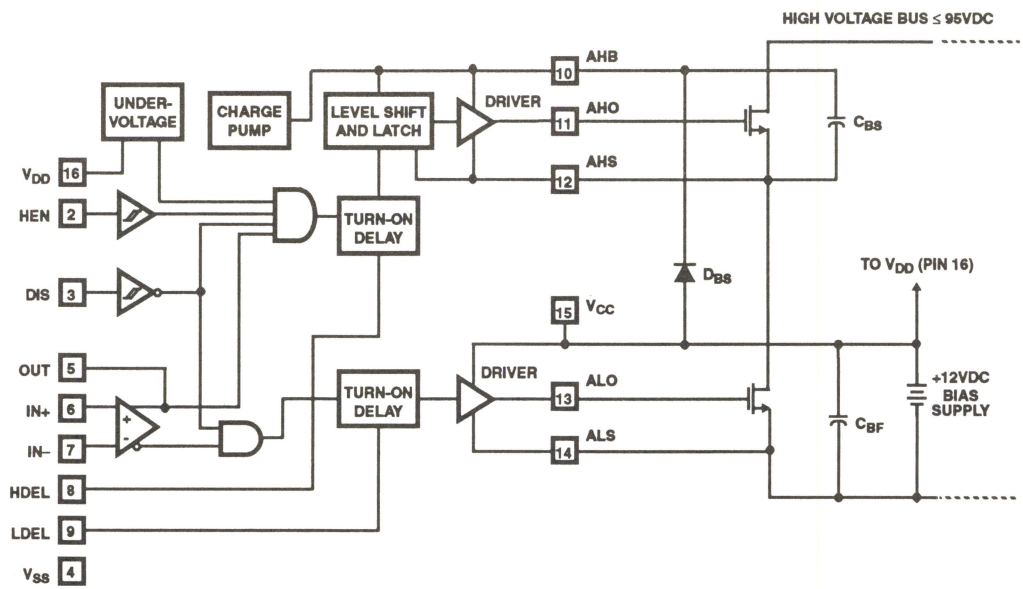


FIGURE 4. HIP4080A BLOCK DIAGRAM

Propagation Delay Control

Propagation delay control is a major feature of the HIP4080A. Two identical sub-circuits within the IC delay the commutation of the power MOSFET gate turn-on signals for both A and B sides of the H-bridge. The gate turn-off signals are not delayed. Propagation delays related to the level-translation function (see section on Level-Translation) cause both upper on/off propagation delays to be longer than the lower on/off propagation delays. Four delay sub-circuits are needed to fully balance the H-bridge delays, two for upper delay control and two for lower gate control.

Users can tailor the low side to high side commutation delay times by placing a resistor from the HDEL pin to the V_{SS} pin. Similarly, a resistor connected from LDEL to V_{SS} controls the high side to low side commutation delay times of the lower power switches. The HDEL resistor controls both upper commutation delays and the LDEL resistor controls the lower commutation delays. Each of the resistors sets a current which is inversely proportional to the created delay. The delay is added to the falling edge of the "off" pulse associated with the MOSFET which is being commutated off. When the delay is complete, the "on" pulse is initiated. This has the effect of "delaying" the commanded on pulse by the amount set by the delay, thereby creating dead-time.

Proper choice of resistor values connected from HDEL and LDEL to V_{SS} provides a means for matching the commutation dead times whether commutating high to low or low to high. Values for the resistors ranging from 10kΩ to 200kΩ are recommended. Figure 5 shows the delays obtainable as a function of the resistor values used.

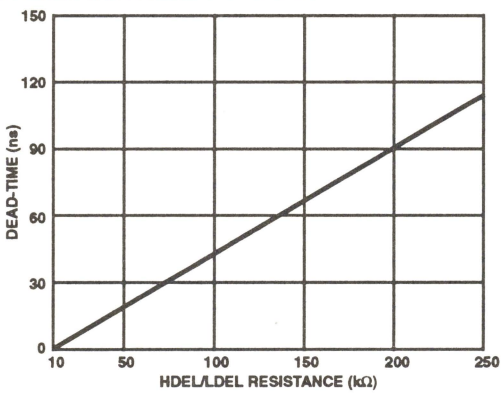


FIGURE 5. MINIMUM DEAD-TIME vs DEL RESISTANCE

Level-Translation

The lower power MOSFET gate drive signals from the propagation delay and control circuits go to amplification circuits which are described in more detail under the section "Driver Circuits". The upper power MOSFET gate drive signals are directed first to the Level-Translation circuits before going to the upper power MOSFET "Driver Circuits".

The Level-Translation circuit communicate "on" and "off" pulses from the Propagation Delay sub-circuit to the upper logic and gate drive sub-circuits which "float" at the potential of the upper power MOSFET source connections. This voltage can be as much as 85V when the bias supply voltage is only 10V (the sum of the bias supply voltage and bus voltages must not exceed 95VDC).

In order to minimize power dissipation in the level-shifter circuit, it is important to minimize the width of the pulses translated because the power dissipation is proportional to the product of switching frequency and pulse energy in joules. The pulse energy in turn is equal to the product of the bus voltage magnitude, translation pulse current and translation pulse duration. To provide a reliable, noise free pulse requires a nominal current pulse magnitude of approximately 3mA. The translated pulses are then "latched" to maintain the "on" or "off" state until another level-translation pulse comes along to set the latch to the opposite state. Very reliable operation can be obtained with pulse widths of approximately 80ns. At a switching frequency of even 1.0MHz, with an 80VDC bus potential, the power developed by the level-translation circuit will be less than 0.08W.

Charge Pump Circuits

There are two charge pump circuits in the HIP4080A, one for each of the two upper logic and driver circuits. Each charge pump uses a switched capacitor doubler to provide about 30µA to 50µA of gate load current. The sourcing current charging capability drops off as the floating supply voltage increases. Eventually the gate voltage approaches the level set by an internal zener clamp, which prevents the voltage from exceeding about 15V, the safe gate voltage rating of most commonly available MOSFETs.

Driver Circuits

Each of the four output drivers are comprised of bipolar high speed NPN transistors for both sourcing and sinking gate charge to and from the MOSFET switches. In addition, the sink driver incorporates a parallel-connected n-channel MOSFET to enable the gate of the power switch gate-source voltage to be brought completely to 0V.

The propagation delays through the gate driver sub-circuits while driving 500pF loads is typically less than 10ns. Nevertheless, the gate driver design nearly eliminates all gate driver shoot-through which significantly reduces IC power dissipation.

Application Considerations

To successfully apply the HIP4080A the designer should address the following concerns:

- General Bias Supply Design Issues
- Upper Bias Supply Circuit Design
- Bootstrap Bias Supply Circuit Design

General Bias Supply Design Issues

The bias supply design is simple. The designer must first establish the desired gate voltage for turning on the power switches. For most power MOSFETs, increasing the gate-source voltage beyond 10V yields little reduction in switch drain-source voltage drop.

Overcharging the power switch's gate-source capacitance also delays turn-off, increases MOSFET switching losses and increases the energy to be switched by the gate driver of the HIP4080A, which increases the dissipation within the HIP4080A. Overcharging the MOSFET gate-source capacitance also can lead to "shoot-through" where both upper and lower MOSFETs in a single bridge leg find themselves on simultaneously, thereby shorting out the high voltage DC bus supply. Values close to 12V are optimum for supplying V_{DD} and V_{CC}, although the HIP4080A will operate up to 15V.

Lower Bias Supply Design

Since most applications use identical MOSFETs for both upper and lower power switches, the bias supply requirements with respect to driving the MOSFET gates will also be identical. In case switching frequencies for driving upper and lower MOSFETs differ, two sets of calculations must be done; one for the upper switches and one for the lower switches. The bias current budget for upper and lower switches will be the sum of each calculation.

Always keep in mind that the lower bias supply must supply current to the upper gate drive and logic circuits as well as the lower gate drive circuits and logic circuits. This is due to the fact that the low side bias supplies (V_{CC}/V_{DD}) charge the bootstrap capacitors and the charge pumps, which maintain voltage across the upper power switch's gate-source terminals.

Good layout practice and capacitor bypassing technique avoids transient voltage dips of the bias power supply to the HIP4080A. Always place a low ESR (equivalent series resistance) ceramic capacitor adjacent to the IC, connected between the bias terminals V_{CC} and V_{DD} and the common terminal, V_{SS} of the IC. A value in the range of 0.22µF and 0.5µF is usually sufficient.

Minimize the effects of Miller feedback by keeping the source and gate return leads from the MOSFETs to the HIP4080A short. This also reduces ringing, by minimizing the length and the inductance of these connections. Another way to minimize inductance in the gate charge/discharge path, in addition to minimizing path length, is to run the outbound gate lead directly "over" the source return lead. Sometimes the source return leads can be made into a small "ground plane" on the back side of the PC board making it possible to run the outbound gate lead "on top" of the board. This minimizes the "enclosed area" of the loop, thus minimizing inductance in this loop. It also adds some capacitance between gate and source which shunts out some of the Miller feedback effect.

Upper Bias Supply Circuit Design

Before discussing bootstrap circuit design in detail, it is worth mentioning that it is possible to operate the HIP4080A without a bootstrap circuit altogether. Even the bootstrap capacitor, which functions to supply a reservoir of charge for rapidly turning on the MOSFETs is optional in some cases. In situations where very slow turn-on of the MOSFETs is tolerable, one may consider omitting some or all bootstrap components. Applications such as driving relays or lamp loads, where the MOSFETs are switched infrequently and switching losses are low, may provide opportunities for boot strapless operation. Generally, loads with a lot of resistance and inductance are possible candidates.

Operating the HIP4080A without a bootstrap diode and/or capacitor will severely slow gate turn-on. Without a bootstrap capacitor, gate current only comes from the internal charge pump. The peak charge pump current is only about 30µA to 50µA. The gate voltage waveform, when operating without a bootstrap capacitor, will appear similar to the dotted line shown in Figure 6.

If a bootstrap capacitor value approximately equal to the equivalent MOSFET gate capacitance is used, the upper bias supply (labeled "bootstrap voltage" in Figure 6) will drop approximately in half when the gate is turned on. The larger the bootstrap capacitance used, the smaller is the instantaneous drop in bootstrap supply voltage when an upper MOSFET is turned on.

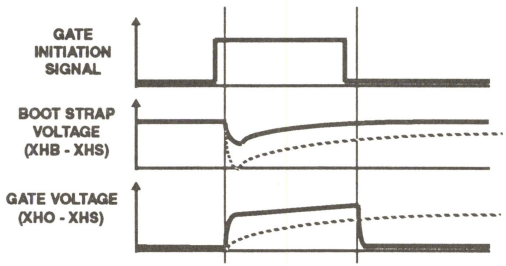


FIGURE 6.

Although not recommended, one may employ a bootstrap capacitor without a bootstrap diode. In this case the charge pump is used to charge up a capacitor whose value should be much larger than the equivalent gate-source capacitance of the driven MOSFET. A value of bootstrap capacitance about 10 times greater than the equivalent MOSFET gate-source capacitance is usually sufficient. Provided that sufficient time elapses before turning on the MOSFET again, the bootstrap capacitor will have a chance to recharge to the voltage value that the bootstrap capacitor had prior to turning on the MOSFET. Assuming 2Ω of series resistance is in the bootstrap change path, an output frequency of up to $\frac{1}{5 \times 2\Omega \times C_{BS}}$ should allow sufficient refresh time.

A bootstrap capacitor 10 times larger than the equivalent gate-source capacitance of the driven MOSFET prevents the drop in bootstrap supply voltage from exceeding 10% of the bias supply voltage during turn-on of the MOSFET. When operating without the bootstrap diode the time required to replenish the charge on the bootstrap capacitor will be the same time as it would take to charge up the equivalent gate capacitance from 0V. This is because the charge lost on the bootstrap capacitor is exactly equal to the charge transferred to the gate capacitance during turn-on. Note that the very first time that the bootstrap capacitor is charged up, it takes

much longer to do so, since the capacitor must be charged from 0V. With a bootstrap diode, the initial charging of the bootstrap supply is almost instantaneous, since the charge required comes from the low-side bias supply. Therefore, before any upper MOSFETs can initially be gated, time must be allowed for the upper bootstrap supply to reach full voltage. Without a bootstrap diode, this initial "charge" time can be excessive.

If the switching cycle is assumed to begin when an upper MOSFET is gated on, then the bootstrap capacitor will undergo a charge withdrawal when the source driver connects it to the equivalent gate-source capacitance of the MOSFET. After this initial "dump" of charge, the quiescent current drain experienced by the bootstrap supply is infinitesimal. In fact, the quiescent supply current is more than offset by the charge pump current.

The charge pump continuously supplies current to the bootstrap supply and eventually would charge the bootstrap capacitor and the MOSFET gate capacitance back to its initial value prior to the beginning of the switching cycle. The problem is that "eventually" may not be fast enough when the switching frequency is greater than a few hundred Hz.

Bootstrap Bias Supply Circuit Design

For high frequency applications all bootstrap components, both diodes and capacitors, are required. Therefore, one must be familiar with bootstrap capacitor sizing and proper choice of bootstrap diode.

Just after the switch cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is the lowest that it will ever be during the switch cycle. The charge lost on the bootstrap capacitor will be very nearly equal to the charge transferred to the equivalent gate-source capacitance of the MOSFET as shown in Equation 1.

$$Q_G = (V_{BS1} - V_{BS2}) \times C_{BS} \qquad \text{(EQ.1)}$$

where:

V_{BS1} = Bootstrap voltage immediately before turn-on
V_{BS2} = Bootstrap voltage immediately after turn-on
C_{BS} = Bootstrap Capacitance
Q_G = Gate charge transferred during turn-on

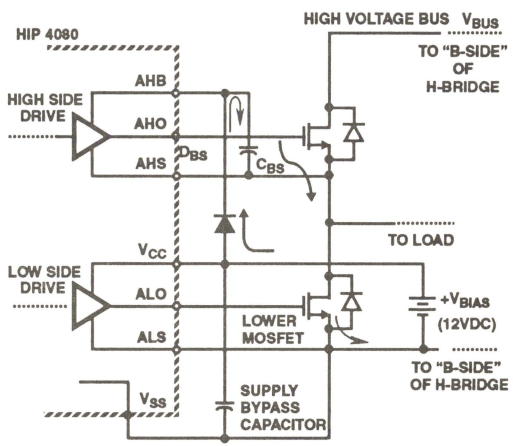
Were it not for the internal charge pump, the voltage on the bootstrap capacitor and the gate capacitor (because an upper MOSFET is now turned on) would eventually drain down to zero due to bootstrap diode leakage current and the very small supply current associated with the level-shifters and upper gate driver sub-circuits.

In PWM switch-mode, the switching frequency is equal to the reciprocal of the period between successive turn-on (or turn-off) pulses. Between any two turn-on gate pulses exists one turn-off pulse. Each time a turn-off pulse is issued to an upper MOSFET, the bootstrap capacitor of that MOSFET begins its "refresh" cycle. A refresh cycle ends when the upper MOSFET is turned on again, which varies depending on the PWM frequency and duty cycle. As the duty cycle approaches 100%, the available "off-time", t_{OFF} approaches zero. Equation 2 shows the relationship between t_{OFF}, f_{PWM} and the duty cycle.

$$t_{OFF} = (1 - DC)/f_{PWM} \qquad \text{(EQ.2)}$$

As soon as the upper MOSFET is turned off, the voltage on the phase terminal (the source terminal of the upper MOSFET) begins its descent toward the negative rail of the high voltage bus. When the phase terminal voltage becomes less than the V_{CC} voltage, refreshing (charging) of the bootstrap capacitor begins. As long as the phase voltage is below V_{CC} refreshing continues until the bootstrap and V_{CC} voltages are equal.

The off-time of the upper MOSFET is dependent on the gate control input signals, but it can never be shorter than the dead-time delay setting, which is set by the resistors connecting HDEL and LDEL to V_{SS}. If the bootstrap capacitor is not fully charged by the time the upper MOSFET turns on again, incomplete refreshing occurs. The designer must insure that the dead-time setting be consistent with the size of the bootstrap capacitor in order to guarantee complete refreshing. Figure 7 illustrates the circuit path for refreshing the bootstrap capacitor.



NOTE: Only "A-side" of H-bridge Is Shown for Simplicity. Arrows Show Bootstrap Charging Path.

FIGURE 7. BOOTSTRAP CAPACITOR CHARGING PATH

The bootstrap charging and discharging paths should be kept short, minimizing the inductance of these loops as mentioned in the section, "Lower Bias Supply Design".

Bootstrap Circuit Design - An Example

Equation 1 describes the relationship between the gate charge transferred to the MOSFET upon turn-on, the size of the bootstrap capacitor and the change in voltage across the bootstrap capacitor which occurs as a result of turn-on charge transfer.

The effects of reverse leakage current associated with the bootstrap diode and the bias current associated with the upper gate drive circuits also affect bootstrap capacitor sizing. At the instant that the upper MOSFET turns on and its source voltage begins to rapidly rise, the bootstrap diode becomes rapidly reverse biased resulting in a reverse recov-

ery charge which further depletes the charge on the bootstrap capacitor. To completely model the total charge transferred during turn-on of the upper MOSFETs, these effects must be accounted for, as shown in Equation 3.

$$C_{BS} = \frac{Q_G + Q_{RR} + \frac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \quad \text{(EQ.3)}$$

where:

I_{DR} = Bootstrap diode reverse leakage current

I_{QBS} = Upper supply quiescent current

Q_{RR} = Bootstrap diode reverse recovered charge

Q_G = Turn-on gate charge transferred

f_{PWM} = PWM operating frequency

V_{BS1} = Bootstrap capacitor voltage just after refresh

V_{BS2} = Bootstrap capacitor voltage just after upper turn on

C_{BS} = Bootstrap capacitance

From a practical standpoint, the bootstrap diode reverse leakage and the upper supply quiescent current are negligible, particularly since the HIP4080A's internal charge pump continuously sources a minimum of about 30µA. This current more than offsets the leakage and supply current components, which are fixed and not a function of the switching frequency. The higher the switching frequency, the lower is the charge effect contributed by these components and their effect on bootstrap capacitor sizing is negligible, as shown in Equation 3. Supply current due to the bootstrap diode recovery charge component increases with switching frequency and generally is not negligible. Hence the need to use a fast recovery diode. Diode recovery charge information can usually be found in most vendor data sheets.

For example, if we choose a Harris IRF520R power MOSFET, the data book states a gate charge, Q_G, of 12nC typical and 18nC maximum, both at V_{DS} = 12V. Using the maximum value of 18nC the maximum charge we should have to transfer will be less than 18nC.

Suppose a General Instrument UF4002, 100V, fast recovery, 1A, miniature plastic rectifier is used. The data sheet gives a reverse recovery time of 25ns. Since the recovery current waveform is approximately triangular, the recovery charge can be approximated by taking the product of half the peak reverse current magnitude (1A peak) and the recovery time duration (25ns). In this case the recovery charge should be 12.5nC.

Since the internal charge pump offsets any possible diode leakage and upper drive circuit bias currents, these sources of discharge current for the bootstrap capacitor will be ignored. The bootstrap capacitance required for the example above can be calculated as shown in Equation 4, using Equation 2.

$$C_{BS} = \frac{18nC + 12.5nC}{12.0 - 11.0} \quad \text{(EQ. 4)}$$

Therefore a bootstrap capacitance of 0.033µF will result in less than a 1.0V droop in the voltage across the bootstrap capacitor during the turn-on period of either of the upper MOSFETs. If typical values of gate charge and bootstrap diode recovered charge are used rather than the maximum value, the voltage droop on the bootstrap supply will be only about 0.5V

Power Dissipation and Thermal Design

One way to model the power dissipated in the HIP4080A is by lumping the losses into static losses and dynamic (switching) losses. The static losses are due to bias current losses for the upper and lower sections of the IC and include the sum of the I_{CC} and I_{DD} currents when the IC is not switching. The quiescent current is approximately 9mA. Therefore with a 12V bias supply, the static power dissipation in the IC is slightly over 100mW.

The dynamic losses associated with switching the power MOSFETs are much more significant and can be divided into the following categories:

- Low Voltage Gate Drive (charge transfer)
- High Voltage Level-shifter (V-I) Losses
- High Voltage Level-shifter (charge transfer)

In practice, the high voltage level-shifter and charge transfer losses are small compared to the gate drive charge transfer losses.

The more significant low voltage gate drive charge transfer losses are caused by the movement of charge in and out of the equivalent gate-source capacitor of each of the 4 MOSFETs comprising the H-bridge. The loss is a function of PWM (switching) frequency, the applied bias voltage, the equivalent gate-source capacitance and a minute amount of CMOS gate charge internal to the HIP4080A. The low voltage charge transfer losses are given by Equation 5.

$$P_{SWLO} = f_{PWM} \times (Q_G + Q_{IC}) \times V_{BIAS} \quad \text{(EQ. 5)}$$

The high voltage level-shifter power dissipation is much more difficult to evaluate, although the equation which defines it is simple as shown in Equation 6. The difficulty arises from the fact that the level-shift current pulses, I_{ON} and I_{OFF}, are not perfectly in phase with the voltage at the upper MOSFET source terminals, V_{SHIFT} due to propagation delays within the IC. These time-dependent source voltages (or "phase" voltages) are further dependent on the gate capacitance of the driven MOSFETs and the type of load (resistive, capacitive or inductive) which determines how rapidly the MOSFETs turn on. For example, the level-shifter I_{ON} and I_{OFF} pulses may come and go and be latched by the upper logic circuits before the phase voltage even moves. As a result, little level-shift power dissipation may result from the I_{ON} pulse, whereas the I_{OFF} pulse may have a significant power dissipation associated with it, since the phase voltage generally remains high throughout the duration of the I_{OFF} pulse.

$$P_{SHIFT} = \frac{1}{T}\int_0^T (I_{ON}(t) + I_{OFF}(t)) \times V_{SHIFT}(t) \times dt \quad \text{(EQ. 6)}$$

Lastly, there is power dissipated within the IC due to charge transfer in and out of the capacitance between the upper driver circuits and V_{SS}. Since it is a charge transfer phenomena, it closely resembles the form of Equation 5, except that the capacitance is much smaller than the equivalent gate-source capacitances associated with power MOSFETs. On the other hand, the voltages associated with the level-shifting function are much higher than the voltage changes experienced at the gate of the MOSFETs. The relationship is shown in Equation 7.

$$P_{TUB} = C_{TUB} \times V_{SHIFT}^2 \times f_{PWM} \quad \text{(EQ. 7)}$$

The power associated with each of the two high voltage tubs in the HIP4080A derived from Equation 7 is quite small, due to the extremely small capacitance associated with these tubs. A "tub" is the isolation area which surrounds and isolates the high side circuits from the ground referenced circuits of the IC. The important point for users is that the power dissipated is linearly related to switching frequency and the square of the applied bus voltage.

The tub capacitance in Equation 7 varies with applied voltage, V_{SHIFT}, making its solution difficult, and the phase shift of the I_{ON} and I_{OFF} pulses with respect to the phase voltage, V_{SHIFT}, in Equation 6 are difficult to measure. Even the Q_{IC} in Equation 5 is not easy to measure. Hence the use of Equation 5 through Equation 7 to calculate total power dissipation is at best difficult. The equations do, however, allow users to understand the significance that MOSFET choice, switching frequency and bus voltage play in determining power dissipation. This knowledge can lead to corrective action when power dissipation becomes excessive.

Fortunately, there is an easy method which can be used to **measure** the components of power dissipation rather than **calculating** them, except for the tiny "tub capacitance" component.

Power Dissipation, the Easy Way

The average power dissipation associated with the IC and the gate of the connected MOSFETs can easily be measured using a signal generator, an averaging millimeter and a voltmeter.

Low Voltage Power Dissipation

Two sets of measurements are required. The first set uses the circuit of Figure 8 and evaluates all of the low voltage power dissipation components. These components include the MOSFET gate charge and internal CMOS charge transfer losses shown in Equation 5 as well as the quiescent bias current losses associated with the IC. The losses are calculated very simply by calculating the product of the bias voltage and current measurements as performed using the circuit shown in Figure 8. For measurement purposes, the phase terminals (AHS and BHS) for both A and B phases are both tied to the chip common, V_{SS} terminal, along with the lower source terminals, ALS and BLS. Capacitors equal to the equivalent gate-source capacitance of the MOSFETs are connected from each gate terminal to V_{SS}. The value of the capacitance chosen comes from the MOSFET manufacturers data sheet. Notice that the MOSFET data sheet usually gives the value in units of charge (usually nanocoulombs) for different drain-source voltages. Choose the drain-source voltage closest to the particular DC bus voltage of interest.

Simply substituting the actual MOSFETs for the capacitors, C_L, doesn't yield the correct average current because the Miller capacitance will not be accounted for. This is because the drains don't switch using the test circuit shown in Figure 8. Also the gate capacitance of the devices you are using may not represent the maximum values which only the data sheet will provide.

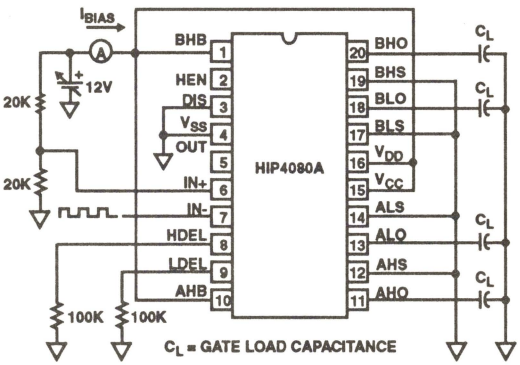


FIGURE 8. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

The low voltage charge transfer switching currents are shown in Figure 9. Figure 9 does not include the quiescent bias current component, which is the bias current which flows in the IC when switching is disabled. The quiescent bias current component is approximately 10mA. Therefore the quiescent power loss at 12V would be 120mW. Note that the bias current at a given switching frequency grows almost proportionally to the load capacitance, and the current is directly proportional to switching frequency, as previously suggested by Equation 5.

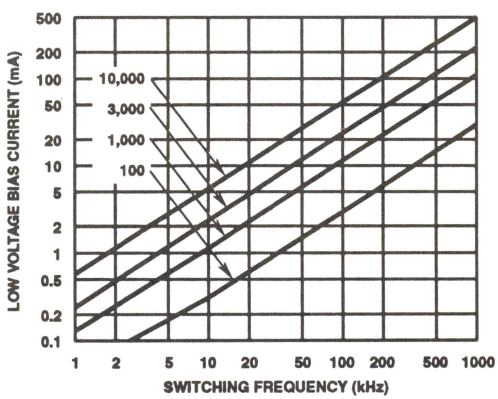


FIGURE 9. LOW VOLTAGE BIAS CURRENT I_{DD} AND I_{CC} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

High Voltage Power Dissipation

The high voltage power dissipation component is largely comprised of the high voltage level-shifter component as described by Equation 6. All of the difficulties associated with the time variance of the I_{ON} and I_{OFF} pulses and the level shift voltage, V_{SHIFT}, under the integrand in Equation 6 are avoided. For completeness, the total loss must include a small leakage current component, although the latter is usually smaller compared to the level-shifter component. The high voltage power loss calculation is the product of the high voltage bus voltage level, V_{BUS}, and the average high voltage bus current, I_{BUS}, as measured by the circuit shown in Figure 10. Averaging meters should be used to make the measurements.

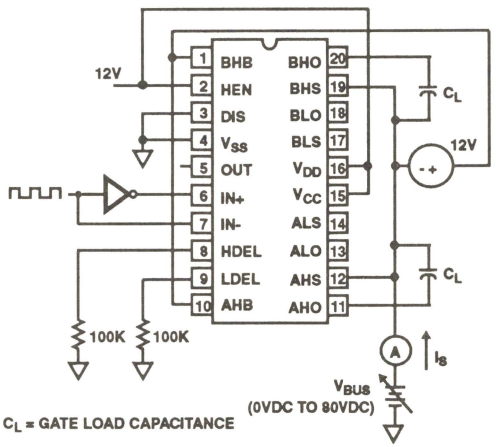


FIGURE 10. HIGH VOLTAGE LEVEL-SHIFT CURRENT TEST CIRCUIT

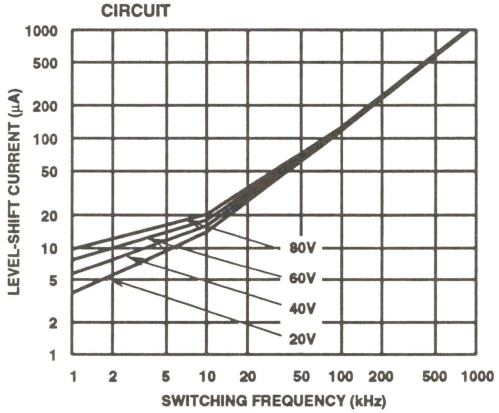


FIGURE 11. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

Figure 11 shows that the high voltage level-shift current varies directly with switching frequency. This result should not be surprising, since Equation 6 can be rearranged to show the current as a function of frequency, which is the reciprocal of the switching period, 1/T. The test circuit of Figure 10 measures quiescent leakage current as well as the switching component. Notice that the current increases somewhat with applied bus voltage. This is due to the finite output resistance of the level-shift transistors in the IC.

Layout Issues

In fast switching, high frequency systems, poor layout can result in problems. It is crucial to consider PCB layout. The HIP4080A pinout configuration encourages tight layout by placing the gate drive output terminals strategically along the right side of the chip (pin 1 is in the upper left-hand corner). This provides for short gate and source return leads connecting the IC with the power MOSFETs.

Minimize the series inductance in the gate drive loop by running the lead going out to the gate of the MOSFETs from the IC over the top of the return lead from the MOSFET sources back to the IC by using a double-sided PCB if possible. The PC board separates the traces and provides a small amount of capacitance as well as reducing the loop inductance by reducing the encircled area of the gate drive loop. The benefit is that the gate drive currents and voltages are much less prone to ringing which can similarly modulate the drain current of the MOSFET. The following table summarizes some of the layout problems which can occur and the corrective action to take.

Layout Problems and Effects

The Bootstrap circuit path should also be short to minimize series inductance that may cause the voltage on the bootstrap capacitor to ring, slowing down refresh or causing an overvoltage on the bootstrap bias supply.

A compact power circuit layout (short circuit path between upper/lower power switches) minimizes ringing on the phase lead(s) keeping BHS and AHS voltages from ringing excessively below the V_{SS} terminal which can cause excessive charge extraction from the substrate and possible malfunction of the IC.

Excessive gate lead lengths can cause gate voltage ringing and subsequent modulation of the drain current, thereby amplifying the Miller Effect.

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance may cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on the bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead(s) causing BHS and AHS to ring excessively below the V_{SS} terminal causing excessive charge extraction from the substrate and possible malfunction of the IC.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing the miller effect when an opposing switch is being rapidly turned on.

Quick Help Table

The quick help table has been included to help locate solutions to problems you may have in applying the HIP4080A.

PROBLEM	EFFECT
Low chip bias voltages (V_{CC} and V_{DD})	May cause power MOSFETs to exhibit excessive R_{DSON}, possibly overheating them. Below about 6V, the IC may not function properly.
High chip bias voltages (V_{CC} and V_{DD})	At V_{DD} voltages above about 12V. The charge pump limiter will begin to operate, in turn drawing heavier V_{DD} current. Above 16V, breakdown may occur.
Bootstrap capacitor(s) too small	May cause insufficient or soft charge delivery to MOSFETs at turn-on causing MOSFET overheating. Charge pump will pump charge, but possibly not quickly enough to avoid excessive switching losses.
Bootstrap capacitor(s) too large	Dead time may need to be increased in order to allow sufficient bootstrap refresh time. The alternative is to decrease bootstrap capacitance.
R_{GATE} too small	Smaller values of R_{GATE} reduces turn-on/off times and may cause excessive emi problems. Incorporating a series gate resistor with an anti-parallel diode can solve EMI problem and add to the dead time, reducing shoot-through tendency.
R_{GATE} too large	Increases switching losses and MOSFET heating. If anti-parallel diode mentioned above is in backwards, turn-off time is increased, but turn-on time is not, possibly causing a shoot-through fault.
Dead time too small	Reduces "refresh" time as well as dead time, with increased shoot-through tendency. Try increasing HDEL and LDEL resistors (don't exceed 250kΩ).
HIP4080A IC gets too hot	Reduce bus voltage, switching frequency, choose a MOSFET with lower gate capacitance or reduce bias voltage (if it is not below 10V to 12V). Shed some of the low voltage gate switching losses in the HIP4080A by placing a small amount of series resistance in the leads going to the MOSFET gates, thereby transferring some of the IC losses to the resistors.
Lower MOSFETs turn on, but upper MOSFETs don't	Check that the HEN terminal is not tied low inadvertently.

Application Demonstration PC Board

Harris has developed a demonstration PC board to allow fast prototyping of numerous types of applications. The board was also tailored to be used to aid in characterizing the HIP4080A and HIP4081A devices under actual operating conditions.

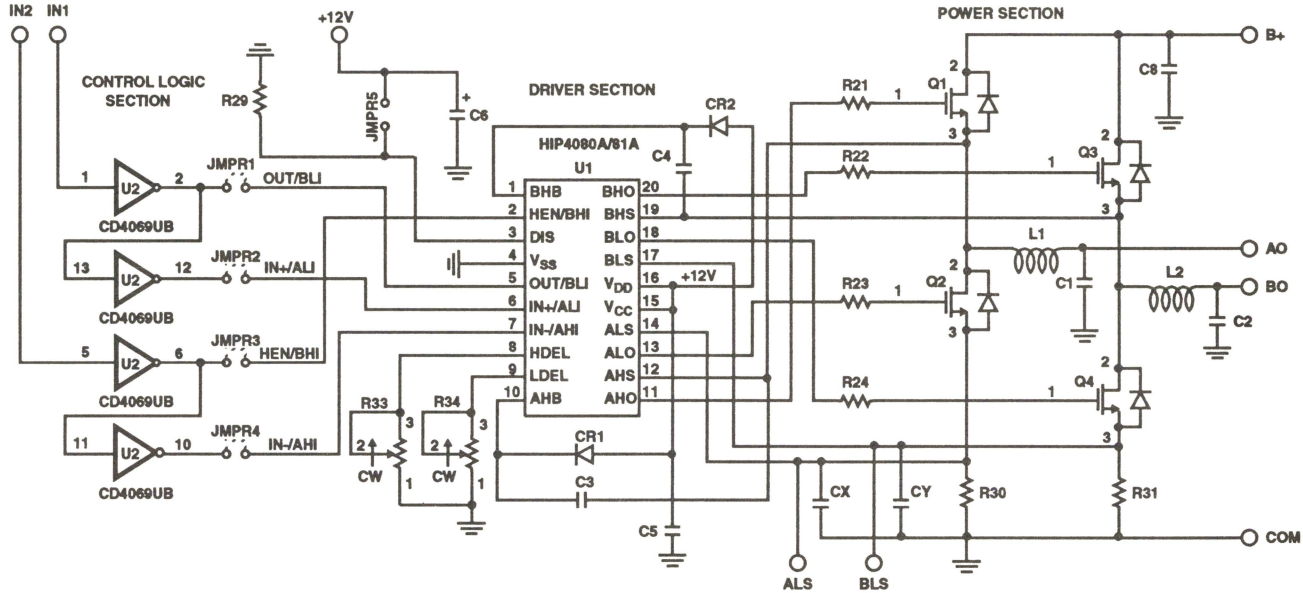
Figure 12 and Figure 13 show the schematic and the silkscreen indicating component placement, respectively, for the HIP408X demo board. Note that the board can be used to evaluate either the HIP4080A or the HIP4081A, simply by changing a few jumpers.

The PC board incorporates a CD4069UB to "buffer" inputs to the HIP4080A on input terminals IN1 and IN2. Normally the polarities of IN1 and IN2 should be opposite in polarity to obtain proper H-Bridge operation. If all 4 MOSFETs are to be PWM-ed, then JMPR3 should be removed (or opened). Also the OUT terminal of the IC should not be driven, so insure JMPR1 is open. Specific recommendations for working with the HIP4081A will be discussed in the corresponding section of the application note for the HIP4081A. JMPR5 should always be removed in order to implement the power up reset circuit described in data sheet HIP4080A, File Number 3178. Resistors R27 and R28 as well as capacitor, C7 are not required.

Consistent with good design practice, the +12V bias supply is bypassed by capacitors C6 and C5 (at the IC terminals directly). Capacitor C6 is a 4.7µF tantalum, designed to bypass the whole PCB, whereas C5 is a 0.22µF, designed to bypass the HIP4080A. The bootstrap capacitors, C3 and C4, and the high voltage bus bypass capacitors are 0.1µF, 100V ceramic. Ceramic is used here because of the low inductance required of these capacitors in the application. The bootstrap diodes are 1A, fast recovery (t_{RR} = 200ns), 100V, to minimize the charge loss from the bootstrap capacitors when the diodes become reverse-biased.

The MOSFETs supplied with the demo board is a Harris IRF520, 100V, 9A device. Since it has a gate charge of approximately 12nC, 10Ω gate resistors, R21 through R24, have been employed to deliberately slow down turn-on and turn-off of these switches. Finally, R33 and R34 provide adjustment of the dead-time. These are 500kΩ normally set for 100kΩ, which will result in a dead-time of approximately 50ns. Resistors, R30 and R31 are shunt resistors (0.1Ω, 2W, 2%, wirewound) used to provide a current-limiting signal, if desired. These may be replaced with wire jumpers if not required.

Finally, space has been provided for filter reactors, L1 and L2, and filter capacitors, C1 and C2, to provide filtering of PWM switching components from appearing at output terminals AO and BO. To facilitate placement of user-defined ICs, such as op-amps, comparators, etc., space for 3 fourteen pin standard width ICs has been reserved at the far left side of the demo board. The output terminations of the 3 optional locations are wired to holes which can be used to mount application-specific components, easing the process for building up working amplifiers for motor controls and audio amplifiers.



NOTE:

DEVICE CD4069UB PIN 7 = COM, PIN 14 = +12V.

FIGURE 12. HIP4080A EVALUATION PC BOARD SCHEMATIC

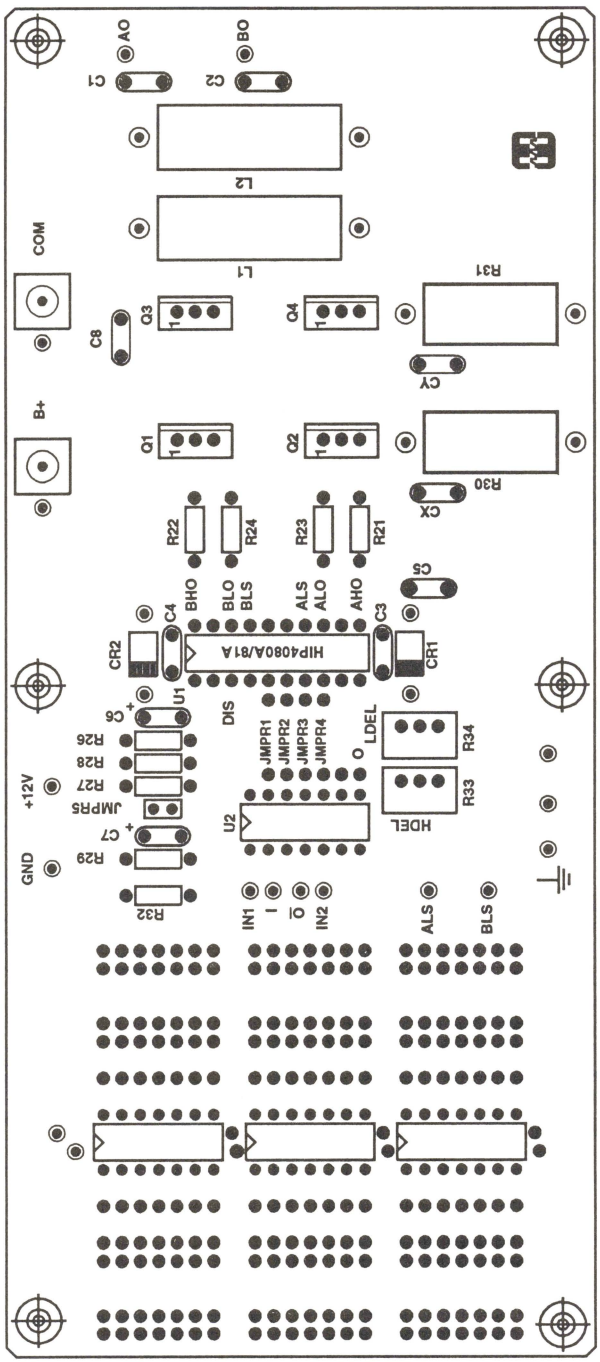


FIGURE 13. HIP4080A EVALUATION BOARD SILKSCREEN

Harris Semiconductor

APPNOTE

No. AN9405 April 1994

Harris Intelligent Power

HIP4081A, 80V HIGH FREQUENCY H-BRIDGE DRIVER

Author: George E. Danz

Introduction

The HIP4081A is a member of the HIP408X family of High Frequency H-Bridge Driver ICs. A simplified application diagram of the HIP4081A IC is shown in Figure 1. The HIP408X family of H-Bridge driver ICs provide the ability to operate from 10VDC to 80VDC busses for driving H-Bridges, operating in class-D switch-mode, whose switch elements are comprised of power N-channel MOSFETs. The HIP408X family, packaged in both 20 pin DIP and 20 pin SOIC DIPs, provide peak gate current drive of 2.5A. The HIP4081A includes undervoltage protection, which sends a continuous gate turn-off pulse to all gate outputs when the V_{DD} voltage falls below a nominal 8.25 volts. The startup sequence of the HIP4081A is initiated when the V_{DD} voltage returns above a nominal 8.75 volts. Of course, the DIS pin must be in the low state for the IC to be enabled. The startup sequence turns on both low side outputs, ALO and BLO, so that the bootstrap capacitors for both sides of the H-bridge can be fully charged. During this time the AHO and BHO gate outputs are held low continuously to insure that no shoot-through can occur during the nominal 400ns boot-strap refresh period. At the end of the boot strap refresh period the outputs respond normally to the state of the input control signals.

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper halves of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to "maintain" bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin "float" along with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals to 95VDC.

The HIP4081A can drive lamp loads for automotive and industrial applications as shown in Figure 2. When inductive loads are switched, flyback diodes must be placed around the loads to protect the MOSFET switches.

Many applications utilize the full bridge topology. These are voice coil motor drives, stepper and DC brush motors, audio amplifiers and even power supply inverters used in uninterruptable power supplies, just to name a few. The HIP408X family of devices is fabricated using a proprietary Harris IC process which allows this family to switch at frequencies over 250kHz. Therefore the HIP408X family is ideal for use in various high frequency converter applications, such as motor drives, class-D audio amplifiers, and high-performance DC-DC converters. A typical application is shown in Figure 5.

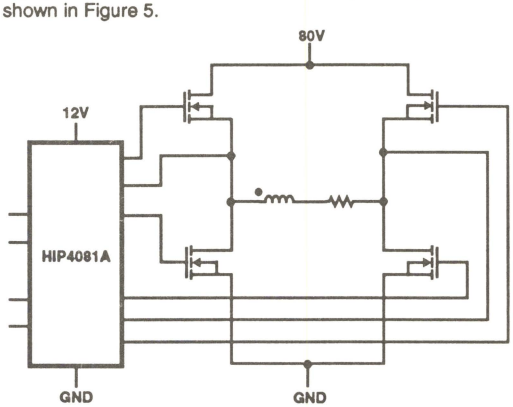


FIGURE 1. HIP4081A SIMPLIFIED APPLICATION DIAGRAM

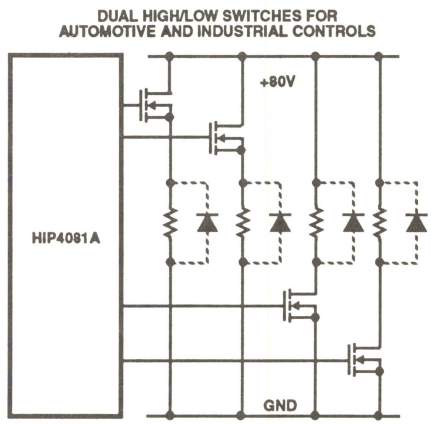


FIGURE 2. HIP4081A AS LAMP SWITCH DRIVER

To provide accurate dead-time control for shoot-through avoidance and duty-cycle maximization, two resistors tied to

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upper and lower propagation delays, which are typically only 55ns. The HIP4081A H-Bridge driver has enough voltage margin to meet all SELV (UL classification for operation at ≤ 42.0V) applications and most Automotive applications where "load dump" capability over 65V is required. This capability makes the HIP408X family a more cost-effective solution for driving N-channel power MOSFETs than either discrete solutions or other solutions relying on transformer- or opto-coupling gate-drive techniques.

The biggest difference between the HIP4080A and the HIP4081A is that the HIP4081A allows separate and individual control of the 4 MOSFET gates, whereas the HIP4080A does not. Also the HIP4081A does not include an internal comparator which can create a PWM signal directly within the HIP4080A.

Description of the HIP4081A

The block diagram of the HIP4081A relating to driving the A-side of the H-Bridge is shown in Figure 4. The blocks associated with each half of the H-Bridge are identical, so the B-side is not shown for simplicity.

The V_{CC} and V_{DD} terminals on the HIP4081A should be tied together. They were separated within the HIP4081A IC to avoid possible ground loops internal to the IC. Tieing them together and providing a decoupling capacitor from the common tie-point to V_{SS} greatly improves noise immunity.

Input Logic

The HIP4081A has 4 inputs, ALI, BLI, AHI and BHI, which control the gate outputs of the H-bridge. The DIS, "Disable," pin disables gate drive to all H-bridge MOSFETs regardless of the command states of the input pins above. The state of the bias voltage, V_{DD}, also can disable all gate drive as discussed in the introduction. The HIP4081A has pullups on the high input terminals, AHI and BHI, so that the bridge can be totally controlled using only the lower input control pins, ALI and BLI, which can greatly simplify the external control circuitry needed to control the HIP4081A. As Table 1 suggests, the lower inputs ALI and BLI dominate the upper inputs. That is, when one of the lower inputs is high, it doesn't matter what the level of the upper input is, because the lower will turn on and the upper will remain off.

TABLE 1. INPUT LOGIC TRUTH TABLE

INPUT				OUTPUT	
ALI, BLI	AHI, BHI	U/V	DIS	ALO, BLO	AHO, BHO
X	X	X	1	0	0
1	X	0	0	1	0
0	1	0	0	0	1
0	0	0	0	0	0
X	X	1	X	0	0

NOTE: X signifies that input can be either a "1" or "0".

The input sensitivity of the DIS input pin is best described as "enhanced TTL" levels. Inputs which fall below 1.0V or rise above 2.5V are recognized, respectively, as low level or high level inputs.

Propagation Delay Control

Propagation delay control is a major feature of the HIP4081A. Two identical sub-circuits within the IC delay the commutation of the power MOSFET gate turn-on signals for both A and B sides of the H-bridge. The gate turn-off signals are not delayed. Propagation delays related to the level-translation function (see section on Level-Translation) cause both upper on/off propagation delays to naturally be longer than the lower on/off propagation delays. Four delay trim sub-circuits are incorporated to better match the H-bridge delays, two for upper delay control and two for lower gate control.

Users can tailor the low side to high side commutation delay times by placing a resistor from the HDEL pin to the V_{SS} pin. Similarly, a resistor connected from LDEL to V_{SS} controls the high side to low side commutation delay times of the lower power switches. The HDEL resistor controls both upper commutation delays and the LDEL resistor controls the lower commutation delays. Each of the resistors sets a current which is inversely proportional to the created delay. The delay is added to the falling edge of the "off" pulse associated with the MOSFET which is being commutated off. When the delay is complete, the "on" pulse is initiated. This has the effect of "delaying" the commanded on pulse by the amount set by the delay, thereby creating dead-time.

Proper choice of resistor values connected from HDEL and LDEL to V_{SS} provides a means for matching the commutation dead times whether commutating high to low or low to high. Values for the resistors ranging from 10kΩ to 200kΩ are recommended. Figure 3 shows the dead-time delays obtainable as a function of the resistor values used.

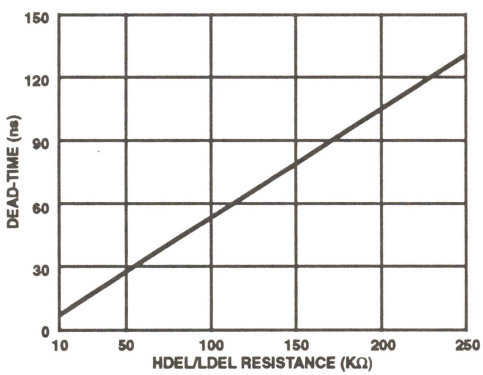


FIGURE 3. MINIMUM DEAD-TIME vs DEL RESISTANCE

Level-Translation

The lower power MOSFET gate drive signals from the propagation delay and control circuits go to amplification circuits which are described in more detail under the section "Driver Circuits". The upper power MOSFET gate drive signals are directed first to the Level-Translation circuits before going to the upper power MOSFET "Driver Circuits".

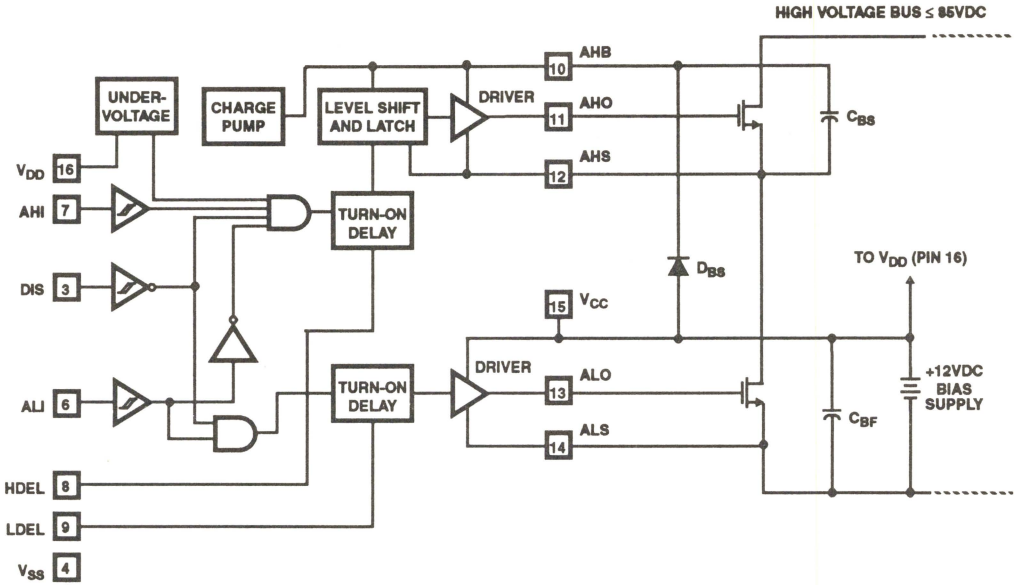


FIGURE 4. HIP4081A BLOCK DIAGRAM

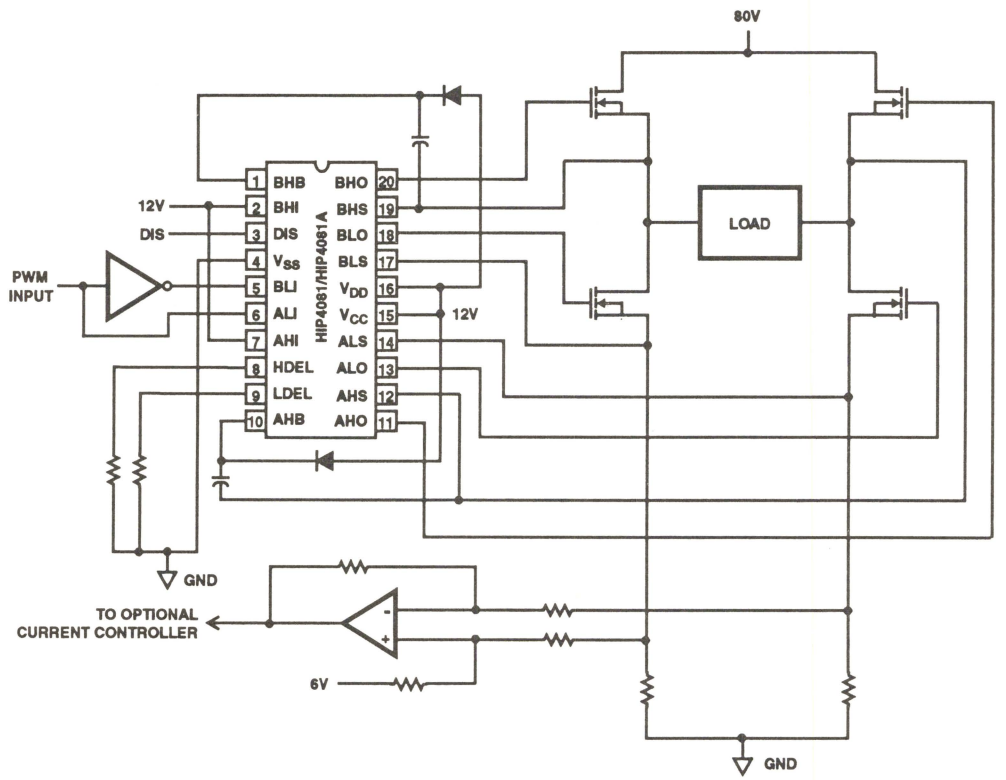


FIGURE 5. TYPICAL APPLICATION (PWM MODE SWITCHING)

The Level-Translation circuit communicate "on" and "off" pulses from the Propagation Delay sub-circuit to the upper logic and gate drive sub-circuits which "float" at the potential of the upper power MOSFET source connections. This voltage can be as much as 85V when the bias supply voltage is only 10V (the sum of the bias supply voltage and bus voltages must not exceed 95VDC).

In order to minimize power dissipation in the level-shifter circuit, it is important to minimize the width of the pulses translated because the power dissipation is proportional to the product of switching frequency and pulse energy in joules. The pulse energy in turn is equal to the product of the bus voltage magnitude, translation pulse current and translation pulse duration. To provide a reliable, noise free pulse requires a nominal current pulse magnitude of approximately 3mA. The translated pulses are then "latched" to maintain the "on" or "off" state until another level-translation pulse comes along to set the latch to the opposite state. Very reliable operation can be obtained with pulse widths of approximately 80ns. At a switching frequency of even 1.0MHz, with an 80VDC bus potential, the power developed by the level-translation circuit will be less than 0.08W.

Charge Pump Circuits

There are two charge pump circuits in the HIP4081A, one for each of the two upper logic and driver circuits. Each charge pump uses a switched capacitor doubler to provide about 30μA to 50μA of gate load current. The sourcing current charging capability drops off as the floating supply voltage increases. Eventually the gate voltage approaches the level set by an internal zener clamp, which prevents the voltage from exceeding about 15V, the safe gate voltage rating of most commonly available MOSFETs.

Driver Circuits

Each of the four output drivers are comprised of bipolar high speed NPN transistors for both sourcing and sinking gate charge to and from the MOSFET switches. In addition, the sink driver incorporates a parallel-connected n-channel MOSFET to enable the gate of the power switch gate-source voltage to be brought completely to 0V.

The propagation delays through the gate driver sub-circuits while driving 500pF loads is typically less than 10ns. Nevertheless, the gate driver design nearly eliminates all gate driver shoot-through which significantly reduces IC power dissipation.

Application Considerations

To successfully apply the HIP4081A the designer should address the following concerns:

- General Bias Supply Design Issues
- Upper Bias Supply Circuit Design
- Bootstrap Bias Supply Circuit Design

General Bias Supply Design Issues

The bias supply design is simple. The designer must first establish the desired gate voltage for turning on the power switches. For most power MOSFETs, increasing the gate-source voltage beyond 10V yields little reduction in switch drain-source voltage drop.

Overcharging the power switch's gate-source capacitance also delays turn-off, increases MOSFET gate switching losses and increases the power dissipation of the HIP4081A. Overcharging the MOSFET gate-source capacitance also can lead to "shoot-through" (both upper and lower MOSFETs in a single bridge leg find themselves conducting simultaneously), thereby shorting out the high voltage DC. Bias supply voltages close to 12V are optimum for V_{DD} and V_{CC}, although the HIP4081A will operate up to 15V.

Lower Bias Supply Design

Since most applications use identical MOSFETs for both upper and lower power switches, the bias supply requirements with respect to driving the MOSFET gates will also be identical. In case switching frequencies for driving upper and lower MOSFETs differ, two sets of calculations must be done; one for the upper switches and one for the lower switches. The bias current budget for upper and lower switches will be the sum of each calculation.

Always keep in mind that the lower bias supply must supply current to the upper gate drive and logic circuits as well as the lower gate drive circuits and logic circuits. This is due to the fact that the low side bias supplies (V_{CC}/V_{DD}) charge the bootstrap capacitors and the charge pumps, which maintain voltage across the upper power switch's gate-source terminals.

Good layout practice and capacitor bypassing technique avoids transient voltage dips of the bias power supply to the HIP4081A. Always place a low ESR (equivalent series resistance) ceramic capacitor adjacent to the IC, connected between the bias terminals V_{CC} and V_{DD} and the common terminal, V_{SS} of the IC. A value in the range of 0.22μF and 0.5μF is usually sufficient.

Minimize the effects of Miller feedback by keeping the source and gate return leads from the MOSFETs to the HIP4081A short. This also reduces ringing, by minimizing the length and the inductance of these connections. Another way to minimize inductance in the gate charge/discharge path, in addition to minimizing path length, is to run the outbound gate lead directly "over" the source return lead. Sometimes the source return leads can be made into a small "ground plane" on the back side of the PC board making it possible to run the outbound gate lead "on top" of the board. This minimizes the "enclosed area" of the loop, thus minimizing inductance in this loop. It also adds some capacitance between gate and source which shunts out some of the Miller feedback effect.

Upper Bias Supply Circuit Design

Before discussing bootstrap circuit design in detail, it is worth mentioning that it is possible to operate the HIP4081A without a bootstrap circuit altogether. Even the bootstrap

capacitor, which functions to supply a reservoir of charge for rapidly turning on the MOSFETs is optional in some cases. In situations where very slow turn-on of the MOSFETs is tolerable, one may consider omitting some or all bootstrap components. Applications such as driving relays or lamp loads, where the MOSFETs are switched infrequently and switching losses are low, may provide opportunities for boot strapless operation. Generally, loads with lots of resistance and inductance are possible candidates.

Operating the HIP4081A without a bootstrap diode and/or capacitor will severely slow gate turn-on. Without a bootstrap capacitor, gate current only comes from the internal charge pump. The peak charge pump current is only about 30µA to 50µA. The gate voltage waveform, when operating without a bootstrap capacitor, will appear similar to the dotted line shown in Figure6.

If a bootstrap capacitor value approximately equal to the equivalent MOSFET gate capacitance is used, the upper bias supply (labeled "bootstrap voltage" in Figure 6) will drop approximately in half when the gate is turned on. The larger the bootstrap capacitance used, the smaller is the instantaneous drop in bootstrap supply voltage when an upper MOSFET is turned on.

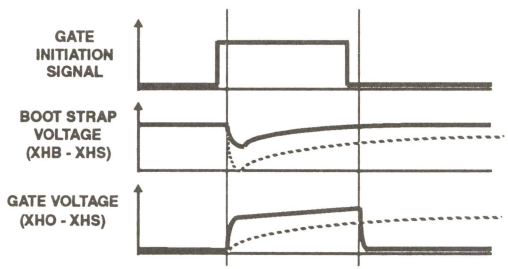


FIGURE 6.

Although not recommended, one may employ a bootstrap capacitor without a bootstrap diode. In this case the charge pump is used to charge up a capacitor whose value should be much larger than the equivalent gate-source capacitance of the driven MOSFET. A value of bootstrap capacitance about 10 times greater than the equivalent MOSFET gate-source capacitance is usually sufficient. Provided that sufficient time elapses before turning on the MOSFET again, the bootstrap capacitor will have a chance to recharge to the voltage value that the bootstrap capacitor had prior to turning on the MOSFET. Assuming 2Ω of series resistance is in the bootstrap change path, an output frequency of up to $\frac{1}{5 \times 2\Omega \times C_{BS}}$ should allow sufficient refresh time.

A bootstrap capacitor 10 times larger than the equivalent gate-source capacitance of the driven MOSFET prevents the drop in bootstrap supply voltage from exceeding 10% of the bias supply voltage during turn-on of the MOSFET. When operating without the bootstrap diode the time required to replenish the charge on the bootstrap capacitor will be the same time as it would take to charge up the equivalent gate capacitance from 0V. This is because the charge lost on the bootstrap capacitor is exactly equal to the charge transferred to the gate capacitance during turn-on. Note that the very first time that the bootstrap capacitor is charged up, it takes much longer to do so, since the capacitor must be charged from 0V. With a bootstrap diode, the initial charging of the bootstrap supply is almost instantaneous, since the charge required comes from the low-side bias supply. Therefore, before any upper MOSFETs can initially be gated, time must be allowed for the upper bootstrap supply to reach full voltage. Without a bootstrap diode, this initial "charge" time can be excessive.

If the switching cycle is assumed to begin when an upper MOSFET is gated on, then the bootstrap capacitor will undergo a charge withdrawal when the source driver connects it to the equivalent gate-source capacitance of the MOSFET. After this initial "dump" of charge, the quiescent current drain experienced by the bootstrap supply is infinitesimal. In fact, the quiescent supply current is more than offset by the charge pump current.

The charge pump continuously supplies current to the bootstrap supply and eventually would charge the bootstrap capacitor and the MOSFET gate capacitance back to its initial value prior to the beginning of the switching cycle. The problem is that "eventually" may not be fast enough when the switching frequency is greater than a few hundred Hz.

Bootstrap Bias Supply Circuit Design

For high frequency applications all bootstrap components, both diodes and capacitors, are required. Therefore, one must be familiar with bootstrap capacitor sizing and proper choice of bootstrap diode.

Just after the switch cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is the lowest that it will ever be during the switch cycle. The charge lost on the bootstrap capacitor will be very nearly equal to the charge transferred to the equivalent gate-source capacitance of the MOSFET as shown in Equation 1.

$$Q_G = (V_{BS1} - V_{BS2}) \times C_{BS} \qquad \text{(EQ.1)}$$

where:

V_{BS1} = Bootstrap capacitor voltage just after refresh
V_{BS2} = Bootstrap voltage immediately after upper turn-on
C_{BS} = Bootstrap Capacitance
Q_G = Gate charge transferred during turn-on

Were it not for the internal charge pump, the voltage on the bootstrap capacitor and the gate capacitor (because an upper MOSFET is now turned on) would eventually drain down to zero due to bootstrap diode leakage current and the very small supply current associated with the level-shifters and upper gate driver sub-circuits.

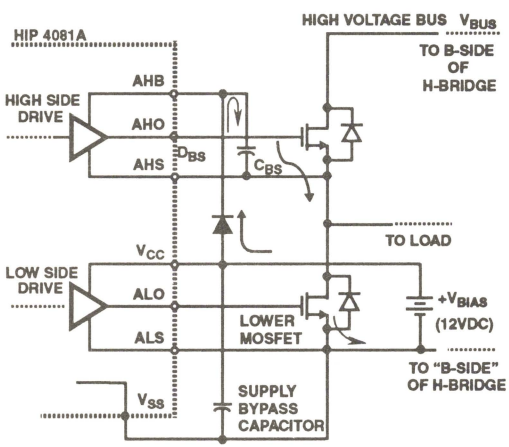
In PWM switch-mode, the switching frequency is equal to the reciprocal of the period between successive turn-on (or turn-off) pulses. Between any two turn-on gate pulses exists one turn-off pulse. Each time a turn-off pulse is issued to an upper MOSFET, the bootstrap capacitor of that MOSFET begins its "refresh" cycle. A refresh cycle ends when the

upper MOSFET is turned on again, which varies depending on the PWM frequency and duty cycle. As the duty cycle approaches 100%, the available "off-time", t_{OFF} approaches zero. Equation 2 shows the relationship between t_{OFF}, f_{PWM} and the duty cycle.

$$t_{OFF} = (1 - DC)/f_{PWM} \quad \text{(EQ.2)}$$

As soon as the upper MOSFET is turned off, the voltage on the phase terminal (the source terminal of the upper MOSFET) begins its descent toward the negative rail of the high voltage bus. When the phase terminal voltage becomes less than the V_{CC} voltage, refreshing (charging) of the bootstrap capacitor begins. As long as the phase voltage is below V_{CC} refreshing continues until the bootstrap and V_{CC} voltages are equal.

The off-time of the upper MOSFET is dependent on the gate control input signals, but it can never be shorter than the dead-time delay setting, which is set by the resistors connecting HDEL and LDEL to V_{SS}. If the bootstrap capacitor is not fully charged by the time the upper MOSFET turns on again, incomplete refreshing occurs. The designer must insure that the dead-time setting be consistent with the size of the bootstrap capacitor in order to guarantee complete refreshing. Figure 7 illustrates the circuit path for refreshing the bootstrap capacitor.



NOTE: Only "A-side" of H-bridge Is Shown for Simplicity. Arrows Show Bootstrap Charging Path.

FIGURE 7. BOOTSTRAP CAPACITOR CHARGING PATH

The bootstrap charging and discharging paths should be kept short, minimizing the inductance of these loops as mentioned in the section, "Lower Bias Supply Design".

Bootstrap Circuit Design - An Example

Equation 1 describes the relationship between the gate charge transferred to the MOSFET upon turn-on, the size of the bootstrap capacitor and the change in voltage across the bootstrap capacitor which occurs as a result of turn-on charge transfer.

The effects of reverse leakage current associated with the bootstrap diode and the bias current associated with the upper gate drive circuits also affect bootstrap capacitor sizing. At the instant that the upper MOSFET turns on and its source voltage begins to rapidly rise, the bootstrap diode becomes rapidly reverse biased resulting in a reverse recovery charge which further depletes the charge on the bootstrap capacitor. To completely model the total charge transferred during turn-on of the upper MOSFETs, these effects must be accounted for, as shown in Equation 3.

$$C_{BS} = \frac{Q_G + Q_{RR} + \frac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \quad \text{(EQ.3)}$$

where:

I_{DR} = Bootstrap diode reverse leakage current
I_{QBS} = Upper supply quiescent current
Q_{RR} = Bootstrap diode reverse recovered charge
Q_G = Turn-on gate charge transferred
f_{PWM} = PWM operating frequency
V_{BS1} = Bootstrap capacitor voltage just after refresh
V_{BS2} = Bootstrap capacitor voltage just after upper turn on
C_{BS} = Bootstrap capacitance

From a practical standpoint, the bootstrap diode reverse leakage and the upper supply quiescent current are negligible, particularly since the HIP4081A's internal charge pump continuously sources a minimum of about 30µA. This current more than offsets the leakage and supply current components, which are fixed and not a function of the switching frequency. The higher the switching frequency, the lower is the charge effect contributed by these components and their effect on bootstrap capacitor sizing is negligible, as shown in Equation 3. Supply current due to the bootstrap diode recovery charge component increases with switching frequency and generally is not negligible. Hence the need to use a fast recovery diode. Diode recovery charge information can usually be found in most vendor data sheets.

For example, if we choose a Harris IRF520R power MOSFET, the data book states a gate charge, Qg, of 12nC typical and 18nC maximum, both at V_{DS} = 12V. Using the maximum value of 18nC the maximum charge we should have to transfer will be less than 18nC.

Suppose a General Instrument UF4002, 100V, fast recovery, 1A, miniature plastic rectifier is used. The data sheet gives a reverse recovery time of 25ns. Since the recovery current waveform is approximately triangular, the recovery charge can be approximated by taking the product of half the peak reverse current magnitude (1A peak) and the recovery time duration (25ns). In this case the recovery charge should be 12.5nC.

Since the internal charge pump offsets any possible diode leakage and upper drive circuit bias currents, these sources of discharge current for the bootstrap capacitor will be ignored. The bootstrap capacitance required for the example above can be calculated as shown in Equation 4, using Equation 2.

$$C_{BS} = \frac{18nC + 12.5nC}{12.0 - 11.0} \quad \text{(EQ. 4)}$$

Therefore a bootstrap capacitance of 0.033µF will result in less than a 1.0V droop in the voltage across the bootstrap capacitor during the turn-on period of either of the upper MOSFETs. If typical values of gate charge and bootstrap diode recovered charge are used rather than the maximum value, the voltage droop on the bootstrap supply will be only about 0.5V

Power Dissipation and Thermal Design

One way to model the power dissipated in the HIP4081A is by lumping the losses into static losses and dynamic (switching) losses. The static losses are due to bias current losses for the upper and lower sections of the IC and include the sum of the I_{CC} and I_{DD} currents when the IC is not switching. The quiescent current is approximately 9mA. Therefore with a 12V bias supply, the static power dissipation in the IC is slightly over 100mW.

The dynamic losses associated with switching the power MOSFETs are much more significant and can be divided into the following categories:

- Low Voltage Gate Drive (charge transfer)
- High Voltage Level-shifter (V-I) losses
- High Voltage Level-shifter (charge transfer)

In practice, the high voltage level-shifter and charge transfer losses are small compared to the gate drive charge transfer losses.

The more significant low voltage gate drive charge transfer losses are caused by the movement of charge in and out of the equivalent gate-source capacitor of each of the 4 MOSFETs comprising the H-bridge. The loss is a function of PWM (switching) frequency, the applied bias voltage, the equivalent gate-source capacitance and a minute amount of CMOS gate charge internal to the HIP4081A. The low voltage charge transfer losses are given by Equation 5.

$$P_{SWLO} = f_{PWM} \times (Q_G + Q_{IC}) \times V_{BIAS} \quad \text{(EQ. 5)}$$

The high voltage level-shifter power dissipation is much more difficult to evaluate, although the equation which defines it is simple as shown in Equation 6. The difficulty arises from the fact that the level-shift current pulses, I_{ON} and I_{OFF}, are not perfectly in phase with the voltage at the upper MOSFET source terminals, V_{SHIFT} due to propagation delays within the IC. These time-dependent source voltages (or "phase" voltages) are further dependent on the gate capacitance of the driven MOSFETs and the type of load (resistive, capacitive or inductive) which determines how rapidly the MOSFETs turn on. For example, the level-shifter I_{ON} and I_{OFF} pulses may come and go and be latched by the upper logic circuits before the phase voltage even moves. As a result, little level-shift power dissipation may result from the i_{ON} pulse, whereas the I_{OFF} pulse may have a significant power dissipation associated with it, since the phase voltage generally remains high throughout the duration of the i_{OFF} pulse.

(EQ. 6)

$$P_{SHIFT} = \frac{1}{T}\int_0^T (I_{ON}(t) + I_{OFF}(t)) \times V_{SHIFT}(t) \times dt$$

Lastly, there is power dissipated within the IC due to charge transfer in and out of the capacitance between the upper driver circuits and V_{SS}. Since it is a charge transfer phenomena, it closely resembles the form of Equation 5, except that the capacitance is much smaller than the equivalent gate-source capacitances associated with power MOSFETs. On the other hand, the voltages associated with the level-shifting function are much higher than the voltage changes experienced at the gate of the MOSFETs. The relationship is shown in Equation 7.

$$P_{TUB} = C_{TUB} \times V_{SHIFT}^2 \times f_{PWM} \quad \text{(EQ. 7)}$$

The power associated with each of the two high voltage tubs in the HIP4081A derived from Equation 7 is quite small, due to the extremely small capacitance associated with these tubs. A "tub" is the isolation area which surrounds and isolates the high side circuits from the ground referenced circuits of the IC. The important point for users is that the power dissipated is linearly related to switching frequency and the square of the applied bus voltage.

The tub capacitance in Equation 7 varies with applied voltage, V_{SHIFT}, making its solution difficult, and the phase shift of the I_{ON} and I_{OFF} pulses with respect to the phase voltage, V_{SHIFT}, in Equation 6 are difficult to measure. Even the Q_{IC} in Equation 5 is not easy to measure. Hence the use of Equation 5 through Equation 7 to calculate total power dissipation is at best difficult. The equations do, however, allow users to understand the significance that MOSFET choice, switching frequency and bus voltage play in determining power dissipation. This knowledge can lead to corrective action when power dissipation becomes excessive.

Fortunately, there is an easy method which can be used to measure the components of power dissipation rather than calculating them, except for the tiny "tub capacitance" component.

Power Dissipation, the Easy Way

The average power dissipation associated with the IC and the gate of the connected MOSFETs can easily be measured using a signal generator, an averaging milliameter and a voltmeter.

Low Voltage Power Dissipation

Two sets of measurements are required. The first set uses the circuit of Figure 8 and evaluates all of the low voltage power dissipation components. These components include the MOSFET gate charge and internal CMOS charge transfer losses shown in Equation 5 as well as the quiescent bias current losses associated with the IC. The losses are calculated very simply by calculating the product of the bias voltage and current measurements as performed using the circuit shown in Figure 9. For measurement purposes, the phase terminals (AHS and BHS) for both A and B phases are both tied to the chip common, V_{SS} terminal, along with the lower source terminals, ALS and BLS. Capacitors equal to the equivalent gate-source capacitance of the MOSFETs

are connected from each gate terminal to V_{SS}. The value of the capacitance chosen comes from the MOSFET manufacturers data sheet. Notice that the MOSFET data sheet usually gives the value in units of charge (usually nanocoulombs) for different drain-source voltages. Choose the drain-source voltage closest to the particular dc bus voltage of interest.

Simply substituting the actual MOSFETs for the capacitors, C_L, doesn't yield the correct average current because the Miller capacitance will not be accounted for. This is because the drains don't switch using the test circuit shown in Figure 8. Also the gate capacitance of the devices you are using may not represent the maximum values which only the data sheet will provide.

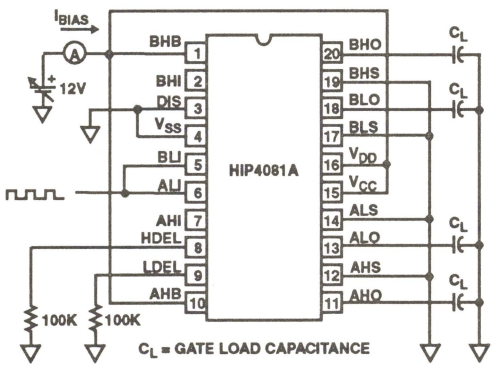


FIGURE 8. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

The low voltage charge transfer switching currents are shown in Figure 9. Figure 9 does not include the quiescent bias current component, which is the bias current which flows in the IC when switching is disabled. The quiescent bias current component is approximately 10mA. Therefore the quiescent power loss at 12V would be 120mW. Note that the bias current at a given switching frequency grows almost proportionally to the load capacitance, and the current is directly proportional to switching frequency, as previously suggested by Equation 5.

High Voltage Power Dissipation

The high voltage power dissipation component is largely comprised of the high voltage level-shifter component as described by Equation 6. All of the difficulties associated with the time variance of the I_{ON} and I_{OFF} pulses and the level shift voltage, V_{SHIFT}, under the integrand in Equation 6 are avoided. For completeness, the total loss must include a small leakage current component, although the latter is usually smaller compared to the level-shifter component. The high voltage power loss calculation is the product of the high voltage bus voltage level, V_{BUS}, and the average high voltage bus current, I_{BUS}, as measured by the circuit shown in Figure 10. Averaging meters should be used to make the measurements.

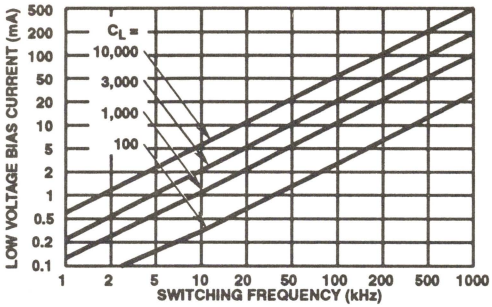


FIGURE 9. LOW VOLTAGE BIAS CURRENT vs FREQUENCY AND LOAD CAPACITANCE

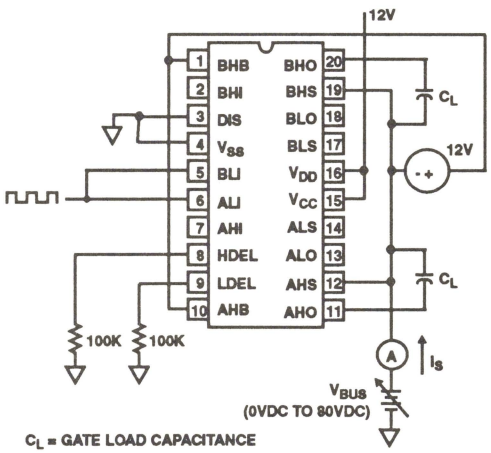


FIGURE 10. HIGH VOLTAGE LEVEL-SHIFT CURRENT TEST CIRCUIT

Figure 11 shows that the high voltage level-shift current varies directly with switching frequency. This result should not be surprising, since Equation 6 can be re-arranged to show the current as a function of frequency, which is the reciprocal of the switching period, 1/T. Notice that the current increases somewhat with applied bus voltage. This is due to the finite output resistance of the level-shift transistors in the IC.

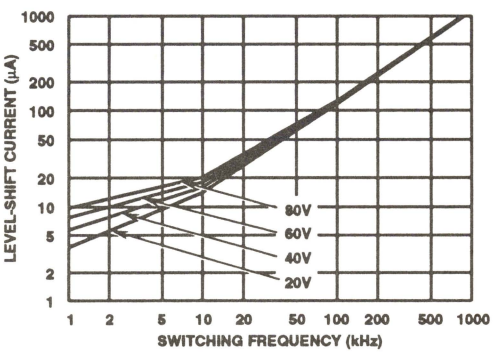


FIGURE 11. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

Layout Problems and Effects

In fast switching, high frequency systems, proper PC board layout is crucial. to consider PCB layout. The HIP4081A pinout configuration encourages tight layout by placing the gate drive output terminals strategically along the right side of the chip (pin 1 is in the upper left-hand corner). This provides for short gate and source return leads connecting the IC with the power MOSFETs.

Always minimize the series inductance in the gate drive loop by running the gate leads to the MOSFETs over the top of the source return leads of the MOSFETs. A double-sided PCB makes this easy. The PC board separates the traces and provides a small amount of capacitance as well as reducing the loop inductance by reducing the encircled area of the gate drive loop. The result is reduced ringing which can similarly reduce drain current modulate in the MOSFET. The table below summarizes some layout problems which can occur and the corrective action to take.

The Bootstrap circuit path should also be kept short. This minimizes series inductance that may cause the voltage on the boot-strap capacitor to ring, slowing down refresh or causing an overvoltage on the bootstrap bias supply.

A compact power circuit layout (short circuit path between upper/lower power switches) minimizes ringing on the phase lead(s) keeping BHS and AHS voltages from ringing excessively below the V_{SS} terminal which can cause excessive charge extraction from the substrate and possible malfunction of the IC.

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance may cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on the bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead(s) causing BHS and AHS to ring excessively below the V_{SS} terminal causing excessive charge extraction from the substrate and possible malfunction of the IC.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing the miller effect when an opposing switch is being rapidly turned on.

Quick Help Table

The quick help table has been included to help locate solutions to problems you may have in applying the HIP4081A.

PROBLEM	EFFECT
Low chip bias voltages (V_{CC} and V_{DD})	May cause power MOSFETs to exhibit excessive R_{DSON}, possibly overheating them. Below 6 V, the IC will not function properly.
High chip bias voltages (V_{CC} and V_{DD})	At V_{DD} voltages above about 12V, The charge pump limiter will begin to operate, in turn drawing heavier V_{DD} current. above 16V, Breakdown may occur.
Bootstrap capacitor(s) too small	May cause insufficient or soft charge delivery to MOSFETs at turn-on causing MOSFET overheating. Charge pump will pump charge, but possibly not quickly enough to avoid excessive switching losses.
Bootstrap capacitor(s) too large	Dead time may need to be increased in order to allow sufficient bootstrap refresh time. The alternative is to decrease bootstrap capacitance.
R_{GATE} too small	Smaller values of R_{GATE} reduces turn-on/off times and may cause excessive emi problems. Incorporating a series gate resistor with an anti-parallel diode can solve EMI problem and add to the dead time, reducing shoot-through tendency.
R_{GATE} too large	Increases switching losses and MOSFET heating. If anti-parallel diode mentioned above is in backwards, turn-off time is increased, but turn-on time is not, possibly causing a shoot-through fault.
Dead time too small	Reduces "refresh" time as well as dead time, with increased shoot-through tendency. Try increasing HDEL and LDEL resistors (don't exceed 250KΩ.)
HIP4081A IC gets too hot	Reduce bus voltage, switching frequency, choose a MOSFET with lower gate capacitance or reduce bias voltage (if it is not below 6 V to 12V). Shed some of the low voltage gate switching losses in the HIP4081A by placing a small amount of series resistance in the leads going to the MOSFET gates, thereby transferring some of the IC losses to the resistors.
Lower MOSFETs turn on, but upper MOSFETs don't	Check that the HEN terminal is not tied low inadvertently.

Application Demonstration PC Board

Harris has developed a demonstration PC board to allow fast prototyping of numerous types of applications. The board can be used to aid in characterizing the HIP4081A device under actual operating conditions.

Figure 12 and Figure 13 show the silkscreen and the schematic indicating component placement, respectively, for the HIP4080A/1A demo board. Note that the board can be used to evaluate either the HIP4080A or the HIP4081A, simply by changing a few jumpers. Refer to the appropriate application note for instructions on jumper placement.

The PC board incorporates a CD4069UB to "buffer" inputs to the HIP4081A. JMPR5, resistors R27 and R28, and capacitor, C7 must be removed in order to implement the power up reset circuit described in this application note and in the HIP4081A data sheet, File Number 3659. Depending on the positions of JMPR1-4, one can operate the driver as two separate half-bridges or an H-bridge.

Consistent with good design practice, the +12V bias supply is bypassed by capacitors C6 and C5 (at the IC terminals directly). Capacitor C6 is a 4.7µF tantalum, designed to bypass the whole PCB, whereas C5 is a 0.22µF, designed to bypass the HIP4081A. The bootstrap capacitors, C3 and C4, and the high voltage bus bypass capacitors are 0.1µF, 100V ceramic. Ceramic is used here because of the low inductance required of these capacitors in the application. The bootstrap diodes are 1A, fast recovery (t_{RR} = 200ns), 100V, to minimize the charge loss from the bootstrap capacitors when the diodes become reverse-biased.

The MOSFETs supplied with the demo board is a Harris IRF520, 100V, 9A device. Since it has a gate charge of approximately 12nC, 10Ω gate resistors, R21 through R24, have been employed to deliberately slow down turn-on and turn-off of these switches. Finally, R33 and R34 provide adjustment of the dead-time. These are 500kΩ normally set for 100kΩ, which will result in a dead-time of approximately 50ns. R30 and R31 provide space for optional shunt resistors (0.1Ω, 2W, 2%, wirewound) which can be used to provide a current-limiting signal, if desired. R30 and R31 should be replaced with wire jumpers if resistors are not used.

Finally, space has been provided for filter reactors, L1 and L2, and filter capacitors, C1 and C2, to provide filtering of PWM switching components from appearing at output terminals AO and BO. To facilitate placement of user-defined ICs, such as op-amps, comparators, etc., space for 3 fourteen pin standard width ICs has been reserved at the far left side of the demo board. The output terminations of the 3 optional locations are wired to holes which can be used to mount application-specific components, easing the process for building up working amplifiers for motor controls and audio amplifiers.

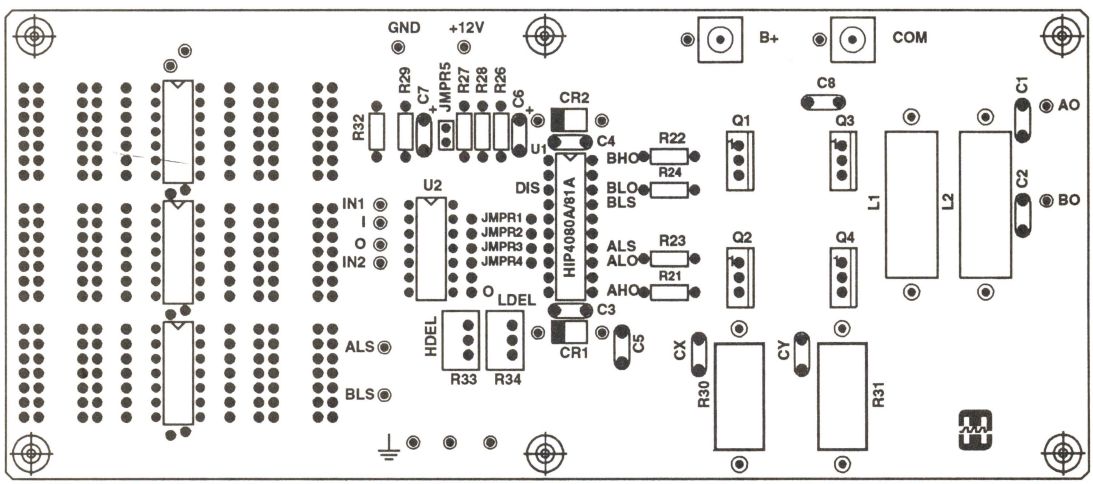


FIGURE 12. EVALUATION BOARD SILKSCREEN

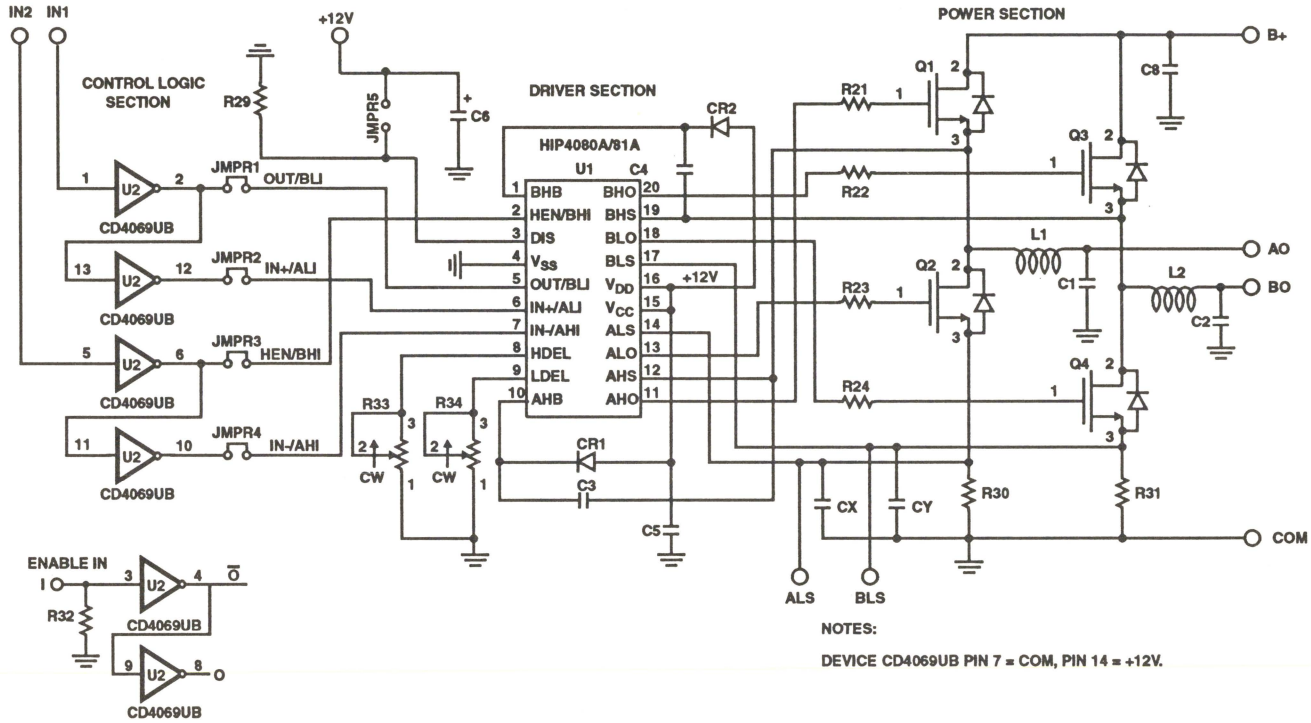


FIGURE 13. HIP4081A EVALUATION PC BOARD SCHEMATIC

INTELLIGENT POWER ICs 12

HARRIS QUALITY AND RELIABILITY

		PAGE
HARRIS QUALITY		12-2
Introduction		12-2
The Role of The Quality Organization		12-2
The Improvement Process		12-2
Designing for Manufacturability		12-2
Special Testing		12-4
Harris Semiconductor Standard Processing Flows		12-5
Controlling and Improving the Manufacturing Process - SPC/DOX		12-7
Average Outgoing Quality (AOQ)		12-8
Training		12-8
Incoming Materials		12-8
Calibration Laboratory		12-10
Manufacturing Science - CAM, JIT, TPM		12-10
HARRIS RELIABILITY		12-11
Introduction		12-11
Reliability Engineering		12-11
Design for Reliability (Wear-Out Characterization)		12-12
Process/Product/Package Qualifications		12-12
Product/Package Reliability Monitors		12-12
Customer Return Services		12-14
Product Analysis Lab		12-18
Analytical Services Laboratory		12-19
Reliability Fundamentals and Calculation of Failure Rate		12-20
ESD Protection and Prevention Measures		12-22
Do's and Don'ts for Integrated Circuit Handling		12-22
TECH BRIEF 52	Electrostatic Discharge Control a Guide to Handling Integrated Circuits	12-22
RELIABILITY REPORT 001	High Voltage Integrated Circuit (HVIC) Reliability Qualification	12-24
RELIABILITY REPORT 002	Concurrent Design, Test and Reliability Engineering of Power ASICs	12-28

Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

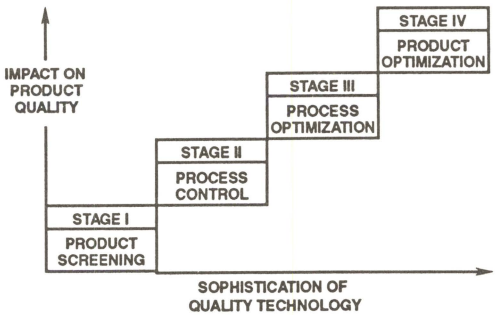


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance	X	
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Ball Bond Shear/Controls		X
	- Die Shear Controls		X
	- Post-Bond/Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	
	- Lead Finish Visuals, Thickness	X	X
	- Solderability		X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	X
	- Mold Parameters	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

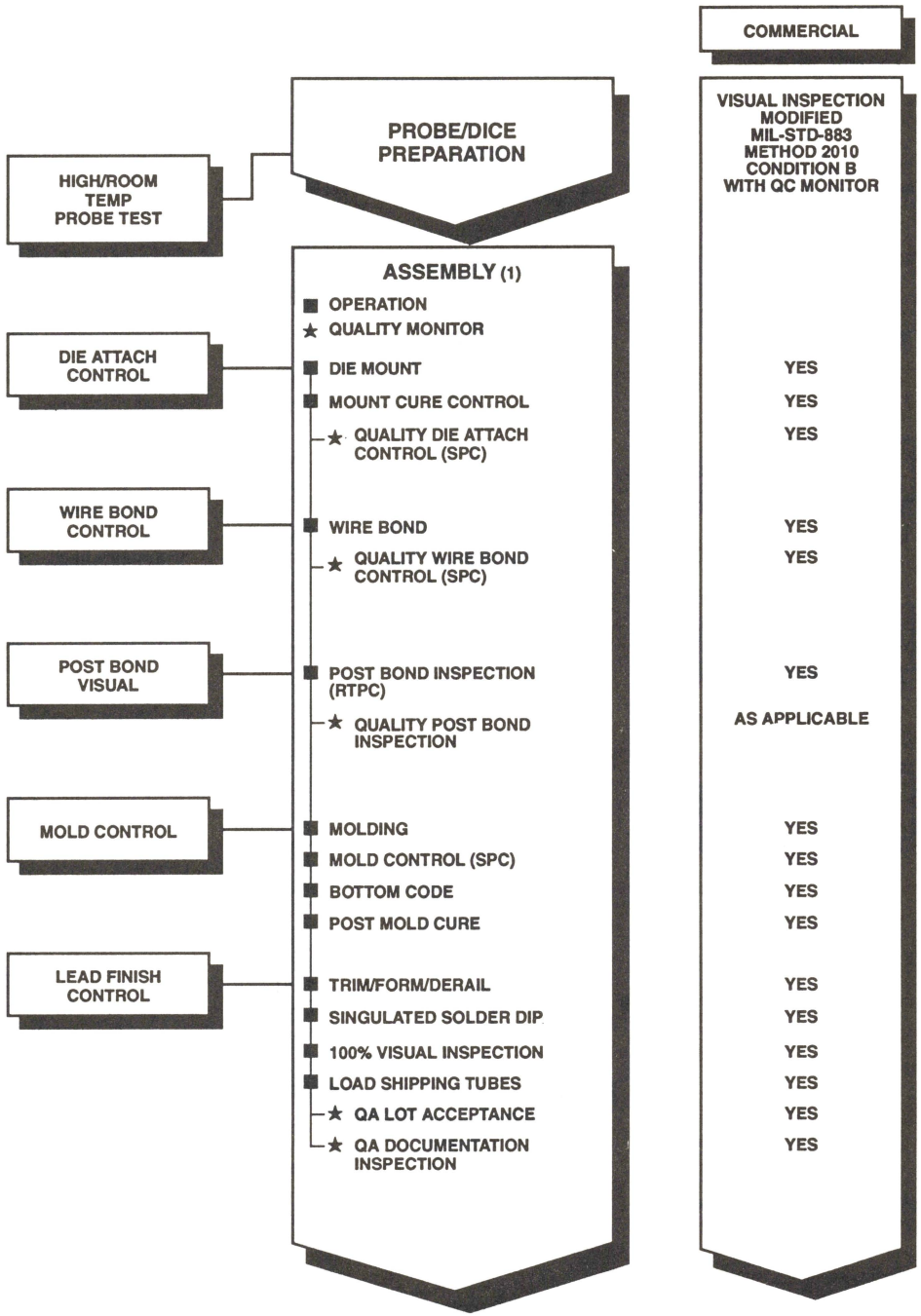
TABLE 2. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Special Testing

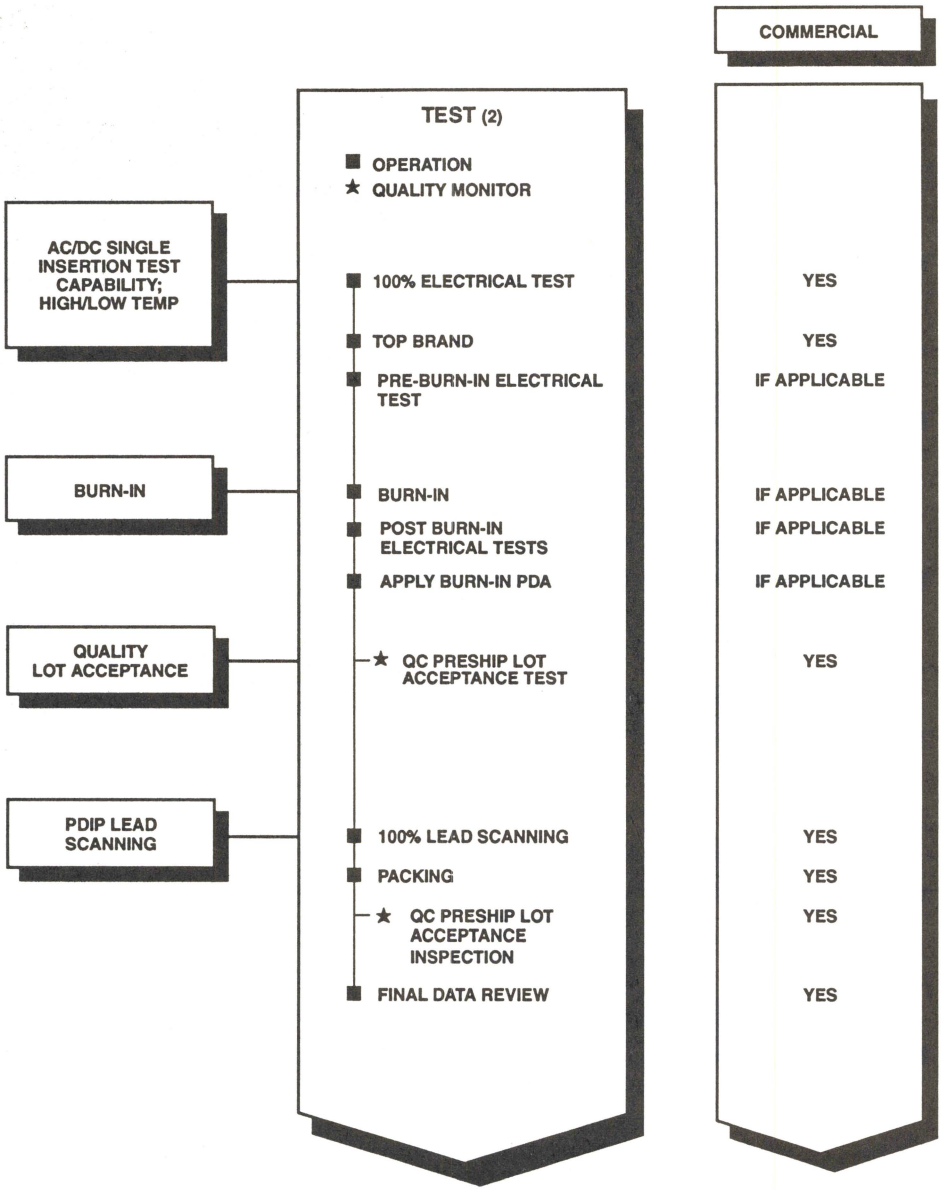
Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown in Figures 1 and 2 indicate the Harris standard processing flows for a Commercial Linear part in PDIP Package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

Harris Semiconductor Standard Processing Flows



(1) Example for a PDIP Package Part

FIGURE 2.



(2) Example for a Linear Part in PDIP Package

FIGURE 3.

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates	• Measurement Equipment - Critical Dimension - Film Thickness - 4 Point Probe - Ellipsometer
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost. (See Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M-38510 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, supervisors, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris's manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials.

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs

Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificated of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

Introduction

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing processes. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life.

Reliability Engineering

The Reliability Engineering department is responsible for all aspects of reliability assurance at Harris Semiconductor:

- Charter
  - To ensure that Harris is recognized by our customers and competitors as a company that consistently delivers products with high reliability.

- Mission
  - To develop systems for assessing, enhancing, and assuring that quality and reliability are integrated into all aspects of our business.

- Vision
  - To establish excellence and integrity through all design and manufacturing processes as it relates to quality and reliability.

Values:

- To be considered responsive and service oriented by our customers.
- To be acknowledged by Harris as a highly qualified resource for reliability assurance, product analysis, and electronic materials characterization.
- To successfully utilize the organization's talents through trained, empowered employees/employee team participation.
- To maintain an attitude of integrity, dignity and respect for all.

Strategy:

- To provide quantitative assessments of product reliability focusing on the identification and timely elimination of design and processing deficiencies that degrade product performance and operating life expectancy.
- To provide systems for continuous improvement of reliability and quality through the assessment of existing processes, products, and packages.
- To perform product analysis as a means of problem solving and feedback to our customers, both internal and external.
- To exercise full authority over the internal qualifications of new products, processes, and packages.

The reliability organization is comprised of a team that possesses a broad cross section of expertise in these areas:

- Custom Military (Radiation Hardened)
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities
- Failure Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics, and service systems. These major systems are summarized below:

- A process and product development system known as ACT PTM (Applying Concurrent Teams to Product-To-Market) has been established. The ACT PTM philosophy is one of new product development through a team that pursues customer involvement. The team has the authority, responsibility, and training necessary to successfully bring the product to market. This not only includes product definition and design, but also all manufacturing capabilities as well.
- Standard test vehicles (over 100) have been developed for process characterization of wear-out failure mechanisms. These vehicles are used for conventional stresses (for modeling failure rates) and for wafer level reliability characterization during development.
- Common qualification standards have been established for all sites.
- A reliability monitoring system (also known as the Matrix monitoring system) is utilized for products in production to ensure ongoing reliability and verification of continuous improvement.
- The field return system is designed to handle a variety of customer issues in a timely manner. Product issues are often handled by routing the product into the PFAST (Product Failure Analysis Solution Team) system. Return authorizations (RAs) are issued where an entire lot of product needs to be returned to Harris. The Customer Return Services (CRS) group is responsible for the administration of this system (see Customer Return Services.)
- The PFAST system has been established to expedite failure analysis, failure root cause determination, and corrective actions for field returns. PFAST is a team effort involving many functional areas at all Harris sites. The purpose of this system is to enable Harris's Field Sales and Quality operations to properly route, track, and respond to our customer's needs as they relate to product analysis.

Design for Reliability (Wear-Out Characterization)

The concept of "Design for Reliability" focuses on moving reliability assessment away from tests on sample product to a point much earlier in the design cycle. Effort is directed at building in and verifying the reliability of a new process well before manufacture of the first shippable product that uses that technology. This gives these first new products a higher probability of success and achieves reduced product-to-market cycle times.

In practice, a set of standardized test vehicles containing special test structures are transferred to the new process using the layout ground rules specified for that process. Each test structure is designed for a specific wear-out failure mechanism. Highly accelerated stress tests are performed on these structures and the results can be extrapolated to customer use conditions. Generally, log-normal statistics are used to define wear-out distributions for the life prediction models. The results are used to establish reliability design ground rules and critical node lists for each process. These ground rules and critical nodes ensure that wear-out failures do not occur during the customer's projected use of the product.

Process/Product/Package Qualifications

Once the new process has successfully completed wear-out characterization, the final qualification consists of more conventional testing (e.g. biased life, storage life, temp cycle etc.). These tests are performed on the first new product designs (sampled across multiple wafer production lots). Successful completion of the final qualification tests concurrently qualifies the new process and the new products that were used in the qualification. Subsequent products designed within the now-established ground rules are qualified individually prior to introduction. New package configurations are also qualified individually prior to being available for use with new products.

Harris's qualification procedures are specified via controlled documentation and the same standard is used at Harris's sites worldwide. Figure 4 gives more information on the new process/product development and life cycle.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard product. Harris's continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. Table 7 outlines the Matrix tests used to monitor plastic packaged ICs in Harris's off-shore assembly plants, where each wafer fab technology is sampled. Matrix I consists of highly accelerated, short duration (typically 48 hours) tests, sampled biweekly, which provide real-time feedback on product reliability. Matrix II consists of the more conventional, longer term stress-tests, sampled monthly, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with containment and corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, to ensure that failure rates are continuously being reduced over time.

Reliability data, including the Matrix Monitor results, can be obtained by contacting your local Harris sales office.

TABLE 7. PLASTIC PACKAGED IC MONITORING TESTS

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	96 Hours	45/5
Biased Life	+175°C	48 Hours	45/5
Biased Life	+125°C	48 Hours	45/5
HAST	+135°C, 85% RH	48 Hours	45/5
Thermal Shock	-65°C to +150°C	200 Cycles	45/5

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	192 Hours	45/5
Biased Humidity	+85°C, 85% RH	1000 Hours	45/5
Biased Life	+125°C	1000 Hours	45/5
Dynamic Life	+125°C	1000 Hours	45/5
Storage Life	+150°C	1000 Hours	45/5
Temp. Cycle	-65°C to +150°C	1000 Cycles	45/5

MATRIX III

TEST	CONDITIONS	SAMPLE/LTPD
Brand Adhesion	Mil-Std 883/2015	15/15
Flammability	(UL-94 Vertical Burn)	11/20
Lead Fatigue	Mil-Std 883/2004	15/15
Physical Dimensions	Mil-Std 883/2016	11/20
Solderability	Mil-Std 883/2003	45/15

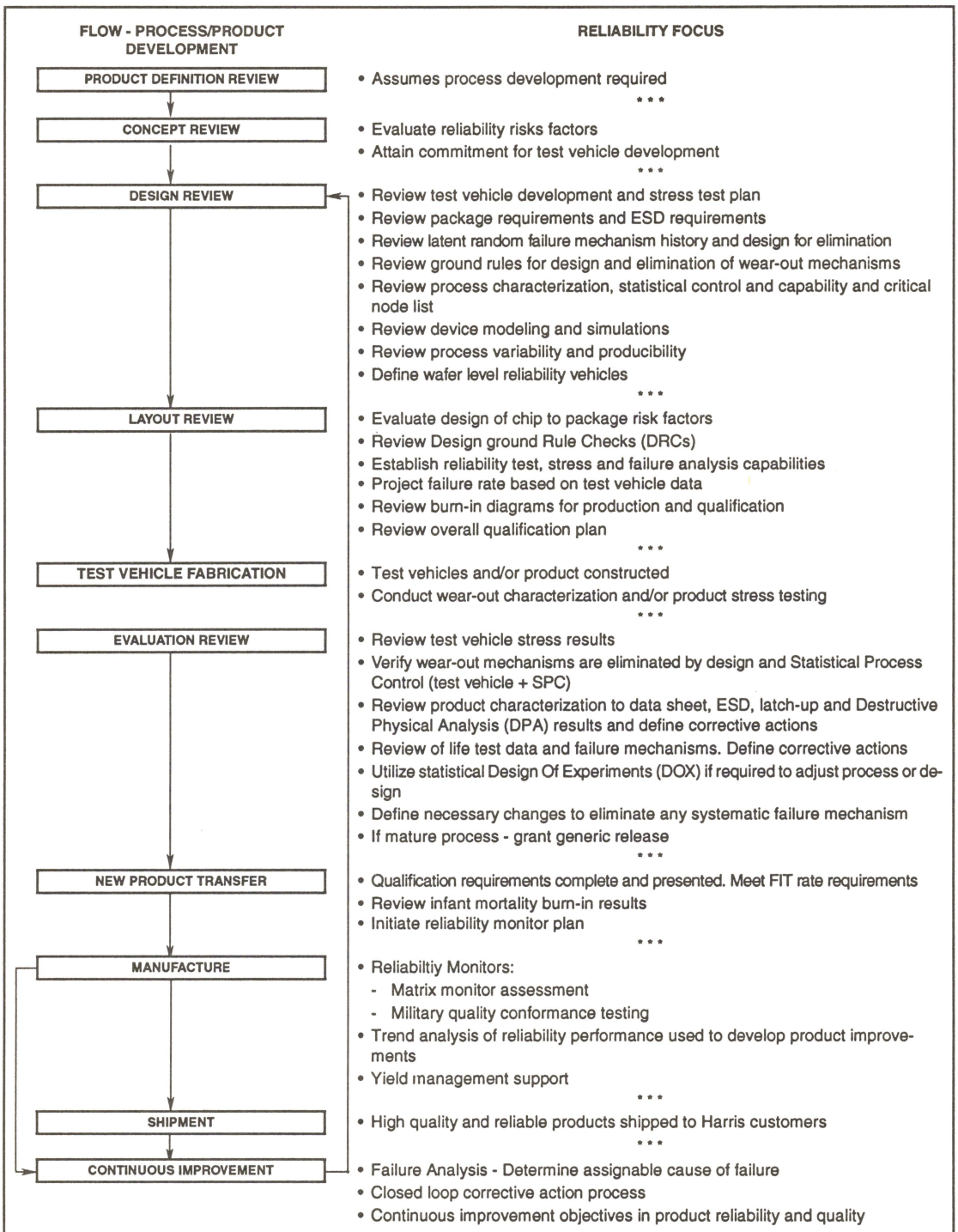


FIGURE 4. NEW PROCESS/PRODUCT DEVELOPMENT AND LIFE CYCLE

Customer Return Services

Harris places a high priority on resolving customer return issues. The Customer Return Services (CRS) department is responsible for determining the best manner to handle a return issue as illustrated in Figure 5.

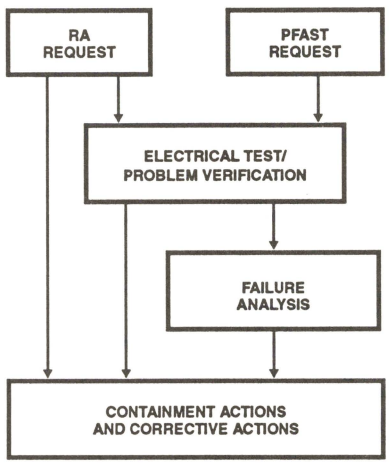


FIGURE 5. GENERAL RETURN FLOW

The diversity of return reasons requires that many different organizations be involved to test, analyze, and correct field return issues. The CRS group coordinates the responses from the supporting organizations to drive closure of issues within the customer response time requirements, see Table 8. The results from the work performed on customer returns are used to initiate corrective actions and continuous improvements within the factories. When the work on a return is completed, the customer is contacted to be certain all issues have been satisfactorily resolved.

The two methods used to return devices are by a RA (Return Authorization) request or by a PFAST (Product Failure Analysis Solution Team) request. The main difference between RA and PFAST is that the PFAST requests often require extensive analysis and a more formal response to the customer. All returns follow the same general procedure from the customer's perspective as seen in steps one to five of the customer return procedure.

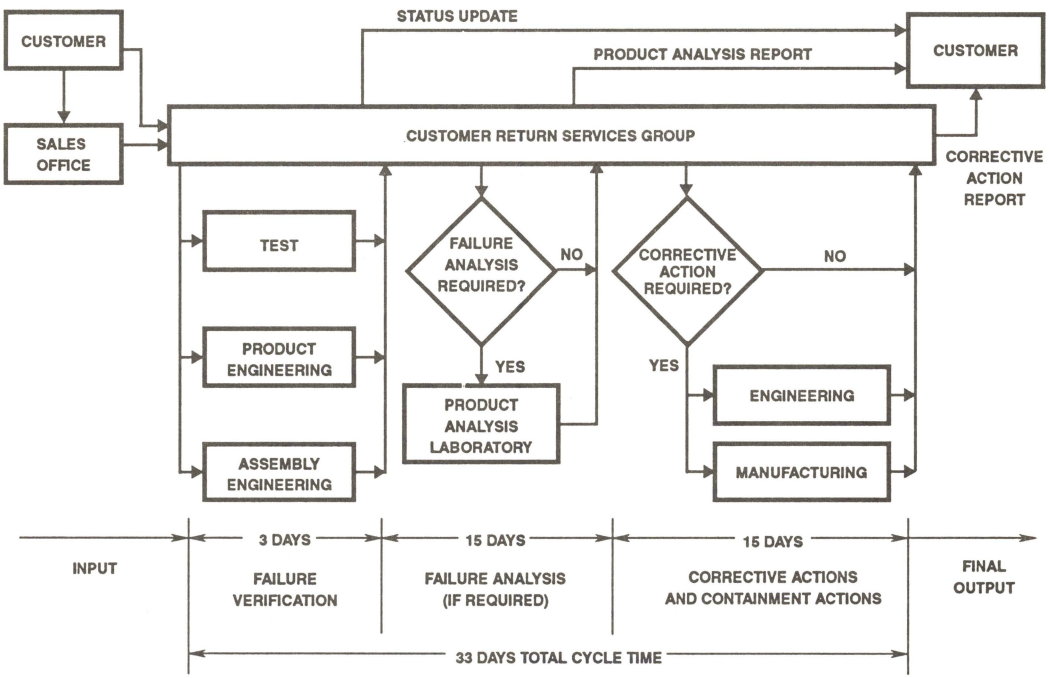
- **Step 1** - Customer or Sales office contacts the Customer Return Services department. If a return is to be routed into the PFAST system, then a PFAST Action Request (see the PFAST form in this section) needs to completed to understand the customer's issue and direct the analysis efforts.
  - **Phone Number: (407)-724-7400**
  - **FAX Number: (407)-724-7658**
  - **Internet: creturn@huey.mls.semi.harris.com**
  - **PROFS: CRETURN**
- **Step 2** - The Customer Return Services department notifies all affected sales, factory, and engineering organizations of the issue.
- **Step 3** - When product is received, the issue is verified and any required analysis is performed. Where applicable, a preliminary analysis report is sent to the customer.
- **Step 4** - A determination of the root cause of failure initiates the corrective actions to address the source of the problem. A final corrective action report is sent to the customer if requested.
- **Step 5** - The Customer Return Services department contacts the customer to confirm that all issues have been handled properly and the customer is satisfied that the return is completed.

The RA request is used to return and replace an entire lot of product. The lot is returned to Harris for replacement or credit. Once the product is received various tests and evaluations will be performed to determine the appropriate actions that should be taken to resolve any problems or issues.

A PFAST request is used to return a small sample for analysis of a problem. The ultimate outcome of both types of requests is to determine corrective actions that would preclude the same problem occurring in the future. Where appropriate, a containment plan is also implemented to prevent a re-occurrence of the problem in the field. The customer return flow diagram (Figure 6) provides the typical activities and cycle times for processing a PFAST request.

TABLE 8. CUSTOMER RETURN SERVICES

CHARTER	MISSION	RESPONSIBILITIES
To resolve product quality issues while providing feedback to both external and internal customers to facilitate corrective actions and continuous improvement of the product.	To provide a single point interface between the customer and the factory for resolving technical problems, issues, and field returns.	1. Maintain customer return history. 2. Track returns through the factory. 3. Establish a history library of problems and corrective actions. 4. Ensure closure with customers.



NOTE: The days indicated are the typical number of 'working days' not calendar days. analysis difficulty and the nature of the corrective actions may either improve or degrade the total cycle time.

FIGURE 6. CUSTOMER RETURN FLOW DIAGRAM

HARRIS SEMICONDUCTOR

PFAST ACTION REQUEST

(Product Failure Analysis Solution Team)

Request # _____

Date: _____

Originator _____
Company/Phone No. _____
Device Type/Part No. _____
No. Samples Returned _____

Customer _____
Location _____
Customer's Reference No. _____
Quantity Received _____

Instructions and requirements are on the back of this form.

Has Field Applications been contacted for assistance? ☐ No ☐ Yes - Who was contacted _____

SOURCE OF PROBLEM

(Enter the sequence of events in the boxes provided)

1. Visual/Mechanical
   ☐ Describe _____
2. Incoming Test ☐ Not Performed
   ☐ 100% Tested ☐ Sample Tested
   No. Tested _____ No. of Rejects _____
   Are results representative of previous lots?
   ☐ YES ☐ NO
3. In Process/Manufacturing Failure
   ☐ Board Test ☐ System Test
   How many units failed? _____
   Failed after _____hours of testing
   Was unit retested at incoming inspection?
   ☐ YES ☐ NO
   Are results representative of previous lots?
   ☐ YES ☐ NO
4. Field Failure
   Failed after _____hours operation
   Estimated failure rate_____ % per _____
   End User_____ Location _____
   Min. _____°C Ave. _____°C Max. _____°C
5. Other _____

ACTION REQUESTED BY CUSTOMER

Specific Action Requested (Contact PFAST Coordinator for other options)

- ☐ Test Sample for Correlation Only
- ☐ Test Sample for Product Return >$5k
- ☐ Failure Analysis
- ☐ Other

Impact of Failed Units on Customer's Situation: _____

Customer Contact with Specific Knowledge of Rejects
Name _____
Position _____ Phone_____

REASON FOR ELECTRICAL REJECT

(Where appropriate serialize units and specify for each)

Test Conditions Relating to Failure
Tester Used (Mfgr/Model) _____
Test Temperature _____
Test Time ☐ Continuous (T = _____sec)
☐ One Shot (T = _____sec)
Describe any observed condition to which failure appears sensitive _____

1. ☐ DC Failure
   ☐ Open ☐ Short ☐ Leakage
   ☐ Power Drain ☐ Input Level ☐ Output Level
   Pin Number_____
2. ☐ AC Failure
   Power Supply Voltages = _____V
   Input Voltages V_{IH} = _____V V_{IL} = _____V
   Pin Number_____
   Failing characteristics _____
3. ☐ RAM and ROM Failures (ROM failures must be returned with a good master unit if failure analysis is requested).
   Address of Failing Location _____
   Describe Pattern Used (If not standard patterns, give very complete description including address sequence). _____
   Include timing diagrams and circuit schematic if available.
   ROM Programmer Used (If purchased unprogrammed) _____

Conformal Coating (Mfgr/Model) _____

Additional Comments:

FIGURE 7. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:

This section requests the product flow leading to the failure. Mark an 'X' in the appropriate boxes up to and including the step which detected the failure. Also mark an 'X' in the appropriate box under "ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?" to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed; the units were installed onto boards; the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to the Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☒ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED _____ NO. OF REJECTS _____
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☒ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ☒ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☒ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____°C AVE. _____°C MAX._____°C
5. OTHER _____

Action Requested by Customer:

This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:

This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical and hermeticity testing.

1. Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.
2. Units must be intact (lid not removed and at least part of each package lead present). This is a requirement since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause of failure and lead to an incorrect conclusion.
3. Programmable parts (ROMs, PROMs, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 7. PFAST ACTION REQUEST (Continued)

Product Analysis Lab

The Product Analysis Laboratory capabilities and charter encompass the isolation and identification of failure modes and mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. The primary activities of the Product Analysis Lab are electrical verification/characterization of the failure, package inspection/analysis, die inspection/analysis, and circuit isolation/probing. A variety of tools and techniques have been developed to ensure the accuracy and integrity of the product analysis. This section lists some of the tools and techniques that are employed during a typical analysis.

The electrical verification/characterization of devices failing electrical parameters is essential prior to performing an analysis. The information obtained from the electrical verification provides a direction for the analysis efforts. The following electrical verification/characterization equipment may be used to obtain electrical data on a device:

- LV500 ASIC verification system
- LTS2020 Analog tester
- Curve Tracer
- Parametric Analyzer

Prior to die level analysis, package inspection and analysis are performed. These steps are performed routinely since valuable data may not be obtainable once the package is opened. The package inspection and analysis may require the use of some of the following lab equipment:

- X-ray
- C-mode Scanning Acoustic Microscope (C-SAM)
- Optical inspection microscopes
- Package opening tools and techniques

Once the device has been opened, die inspection and analysis can be performed. Depending on the type of failure, several tools and techniques may be used to identify the failure mechanism. Usually the faster and easier to use operations are performed first in an attempt to expedite the analysis. The list of equipment and techniques for performing die inspection and analysis is as follows:

- Optical microscopes
- Liquid crystal
- Emission microscope
- Scanning electron microscopes - SEM

The final step of circuit isolation is ready to be performed when an area of the circuit has been identified as the source of the problem through one of the previous analysis efforts. Circuit analysis is performed using the following probing and isolation tools:

- Mechanical probing
- Laser cutter and isolation
- E-beam probing
- Cross sectioning and chemical deprocessing

A typical analysis flow is shown in the Figure 8 below. The exact analysis steps and sequence are determined as the situation dictates. For the analysis to be conclusive, it is essential that the failure mechanism correlates to the initial product failure conditions. Some failure mechanisms require elemental and chemical analysis to identify the root cause within the manufacturing process. Elemental and chemical analysis tasks are sent to the Analytical Services Lab for further evaluation.

The results of each analysis are entered into a computer data base. This data base is used to search for specific types of problems, to identify trends, and to verify that the corrective actions were effective.

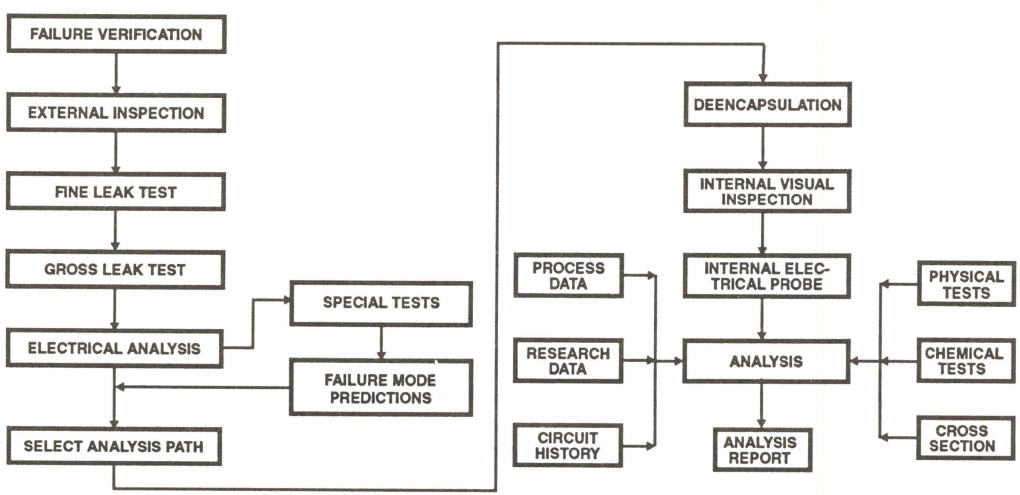


FIGURE 8. ANALYSIS SEQUENCE

Analytical Services Laboratory

Chemical and physical analysis of materials and processes is an integral part of Harris's Total Quality/Continuous Improvement efforts to build reliability into processes and products. Manufacturing operations are supported with real-time analyses to help maintain robust processes. Analyses are run in cooperation with raw material suppliers to help them provide controlled materials in dock-to-stock procurement programs.

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies.

The department also maintains ongoing working arrangements with commercial laboratories, universities, and equipment manufacturers to obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

Figure 9 and Figure 10 show the capabilities of each area.

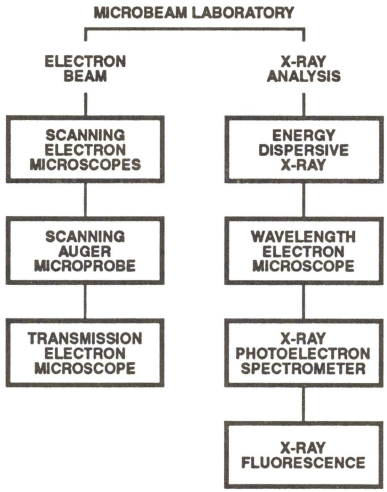


FIGURE 9. MICROBEAM LABORATORY

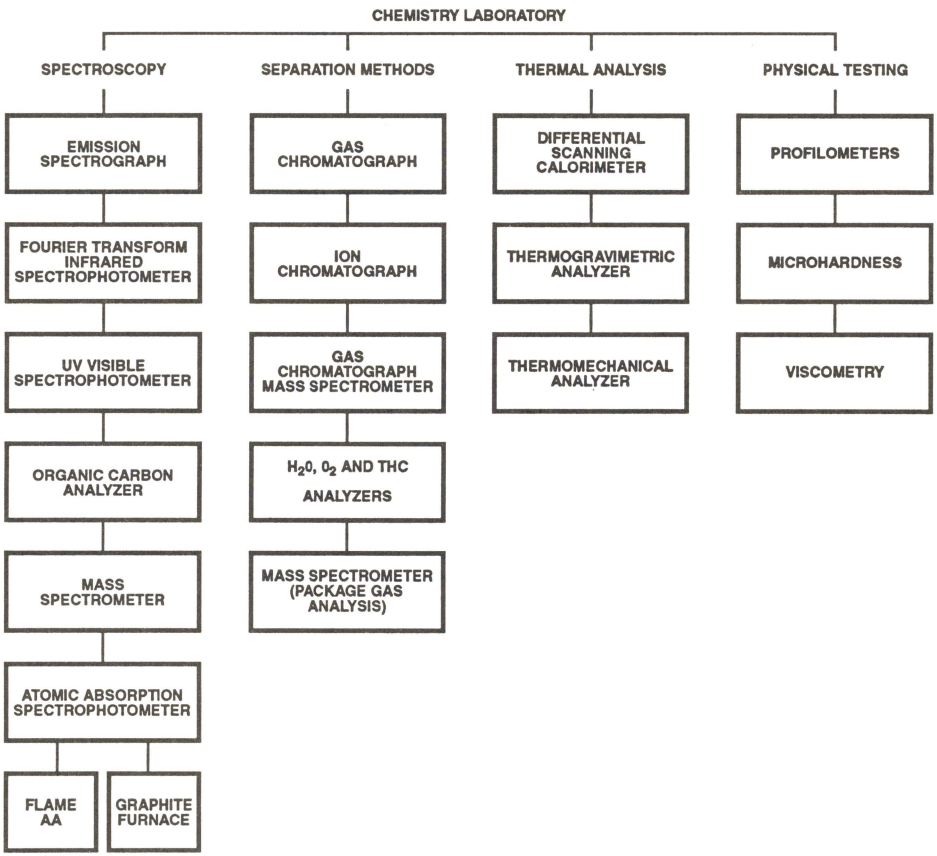


FIGURE 10. CHEMISTRY LABORATORY

Reliability Fundamentals and Calculation of Failure Rate

Table 9 defines some of the more important terminology used in describing the lifetime of integrated circuits. Of prime importance is the concept of "failure rate" and its calculation.

Failure Rate Calculations

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanism in a life test, since the failure mechanisms are thermally activated at different rates The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = number of distinct possible failure mechanisms

k = number of life tests being combined

x_i = number of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test $j, j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$M = X^2_{(\alpha, 2r+2)}/2$
where,
X^2 = chi square factor for $2r + 2$ degrees of freedom
r = total number of failures (Σx_i)
α = risk associated with UCL;
i.e. $\alpha = (100\text{-UCL}(\%))/100$

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 9. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The early life failure rate is typically higher, decreases slightly, and then becomes relatively constant over time. The onset of wear-out will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution.
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln(t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln(t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 10. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3eV - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3eV - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5eV - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

Harris Semiconductor

TechBrief

No. TB52 January 1994

Harris Digital

ELECTROSTATIC DISCHARGE CONTROL A GUIDE TO HANDLING INTEGRATED CIRCUITS

This paper discusses methods and materials recommended for protection of ICs against ESD damage or degradation during manufacturing operations vulnerable to ESD exposure. Areas of concern include dice prep and handling, dice and package inspection, packing, shipping, receiving, testing, assembly and all operations wurhere ICs are involved.

All integrated circuits are sensitive to electrostatic discharge (ESD) to some degree. Since the introduction of integrated circuits with MOS structures and high quality junctions, safe and effective means of handling these devices have been of primary importance.

If static discharge occurs at a sufficient magnitude, 2kV or greater, some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. Avoiding any damage or degradation by ESD when handling devices during the manufacturing flow is therefore essential.

ESD Protection and Prevention Measures

One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry.

In areas where ICs are being handled, certain equipment should be utilized to reduce the damaging effects of ESD. Typically, equipment such as grounded work stations, conductive wrist straps, conductive floor mats, ionized air blowers and conductive packaging materials are included in the IC handling environment. Any time an individual intends to handle an IC, in any way, they must insure they have been grounded to eliminate circuit damage.

Grounding personnel can, practically, be performed by two methods. First, grounded wrist straps which are usually made of a conductive material, such as Velostat or metal. A resistor value of 1 megohm (1/2 watt) in series with the strap to ground completes a discharge path for ESD when the operator wears the strap in contact with the skin. Another method is to insure direct physical contact with a grounded, conductive work surface.

This consists of a conductive surface like Velostat, covering the work area. The surface is connected to a 1 megohm (1/2 watt) resistor in series with ground.

In addition to personnel grounding, areas where work is being performed with ICs, should be equipped with an ionized air blower. Ionized air blowers force positive and negative ions simultaneously over the work area so that any nonconductors that are near the work surface would have their static charge neutralized before it would cause device damage or degradation.

Relative humidity in the work area should be maintained as high as practical. When the work environment is less than 40% RH, a static build-up condition can exist on nonconductors allowing stored charges to remain near the ICs causing possible static electricity discharge to ICs.

Integrated circuits that are being shipped or transported require special handling and packaging materials to eliminate ESD damage. Dice or packaged devices should be in conductive carriers during all phases of transport and handling. Leads of packaged devices can be shorted by tubular metallic carriers, conductive foam or foil.

Do's and Don'ts for Integrated Circuit Handling

Do's

Do keep paper, nonconductive plastic, plastic foams and films or cardboard off the static controlled conductive bench top. Placing devices, loaded sticks or loaded burn-in boards on top of any of these materials effectively insulates them from ground and defeats the purpose of the static controlled conductive surface.

Do keep hand creams and food away from static controlled conductive work surfaces. If spilled on the bench top, these materials will contaminate and increase the resistivity of the work area.

Do be especially careful when using soldering guns around conductive work surfaces. Solder spills and heat from the gun may melt and damage the conductive mat.

Do check the grounded wrist strap connections daily. Make certain they are snugly fitted before starting work with the product.

Do put on grounded wrist strap before touching any devices. This drains off any static build-up from the operator.

Do know the ESD caution symbols.

Do remove devices or loaded sticks from shielding bags only when grounded via wrist strap at grounded work station. This also applies when loading or removing devices from the antistatic sticks or the loading on or removing from the burn-in boards.

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Do wear grounded wrist straps in direct contact with the bare skin never over clothing.

Do use the same ESD control with empty burn-in boards as with loaded boards if boards contain permanently mounted ICs as part of driver circuits.

Do insure electrical test equipment and solder irons at an ESD control station are grounded and only uninsulated metal hand tools be used. Ordinary plastic solder suckers and other plastic assembly aids shall not be used.

Do use ionizing air blowers in static controlled areas when the use of plastic (nonconductive) materials cannot be avoided.

Don'ts

Don't allow anyone not grounded to touch devices, loaded sticks or loaded burn-in boards. To be grounded they must be standing on a conductive floor mat with conductive heel straps attached to footwear or must wear a grounded wrist strap.

Don't touch the devices by the pins or leads unless grounded since most ESD damage is done at these points.

Don't handle devices or loaded sticks during transport from work station to work station unless protected by shielding bags. These items must never be directly handled by anyone not grounded.

Don't use freon or chlorinated cleaners at a grounded work area.

Don't wax grounded static controlled conductive floor and bench top mats. This would allow build-up of an insulating layer and thus defeating the purpose of a conductive work surface.

Don't touch devices or loaded sticks or loaded burn-in boards with clothing or textiles even though grounded wrist strap is worn. This does not apply if conductive coats are worn.

Don't allow personnel to be attached to hard ground. There must always be 1 megohm series resistance (1/2 watt between the person and the ground).

Don't touch edge connectors of loaded burn-in boards or empty burn-in boards containing permanently mounted driver circuits when not grounded. This also applies to burn-in programming cards containing ICs.

Don't unload stick on a metal bench top allowing rapid discharge of charged devices.

Don't touch leads. Handle devices by their package even though grounded.

Don't allow plastic "snow or peanut" polystyrene foam or other high dielectric materials to come in contact with devices or loaded sticks or loaded burn-in boards.

Don't allow rubber/plastic floor mats in front of static controlled work benches.

Don't solvent-clean devices when loaded in antistatic sticks since this will remove antistatic inner coating from sticks.

Don't use antistatic sticks for more than one throughput process. Used sticks should not be reused unless recoated.

Recommended Maintenance Procedures

Daily

Perform visual inspection of ground wires and terminals on floor mats, bench tops, and grounding receptacles to ensure that proper electrical connections via 1 megohm resistor (1/2 watt) exist.

Clean bench top mats with a soft cloth or paper towel dampened with a mild solution of detergent and water.

Weekly

Damp mop conductive floor mats to remove any accumulated dirt layer which causes high resistivity.

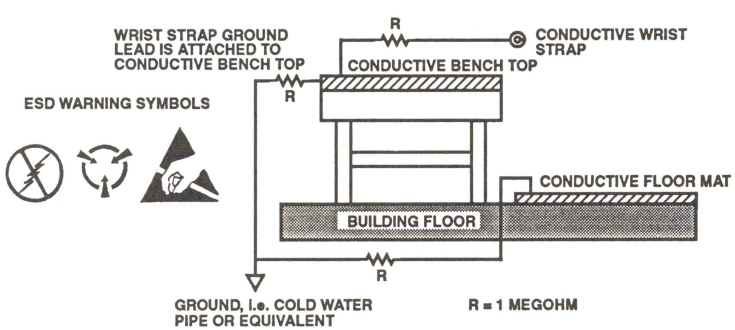
Annually

Replace nuclear elements for ionized air blowers.

Review ESD protection procedures and equipment for updating and adequacy.

Static Controlled Work Station

The figure below shows an example of a work bench properly equipped to control electro-static discharge. Note that the wrist strap is connected to a 1 megohm resistor. This resistor can be omitted in the setup if the wrist strap has a 1 megohm assembled on the cable attached.



RR001.1 April 1992

Reliability Report

HIGH VOLTAGE INTEGRATED CIRCUIT (HVIC) RELIABILITY QUALIFICATION

By Erwin A. Herr

Strategy

The application requirements of the SP600 and the SP601 HVIC in a general industrial environment were reviewed and the desired properties of the HVIC to meet these requirements were identified. These properties were grouped into four main categories:

1. Semiconductor die bulk and surface stability,
2. Sealed junction integrity,
3. Thermal, mechanical and environmental stability,
4. Long term reliability.

It was desirable to demonstrate these properties of the HVIC with several key accelerated tests on a timely basis.Therefore, an analysis was made of several accelerated stresses that would assure the properties. Based on this analysis and previous experience the stresses chosen included: High Temperature Bias (HTB), High Temperature Storage, Damp Heat Bias, Temperature Cycling and Vibration Fatigue. The device properties and the accelerated stresses to assure them are shown in Figure 1. The objectives of each of the accelerated tests are shown in Figure 2. Also this analysis was used to design the Qualification Plan. A description of the accelerated tests used in this plan and the results of the tests are shown in Figure 3.

DEVICE PROPERTIES	HIGH TEMP BIAS	HIGH TEMP STORAGE	DAMP HEAT BIAS	TEMP CYCLE	VIBRATION FATIGUE
Die Bulk and Surface Stability	X	X	X		
Sealed Junction Integrity	X		X	X	
Thermal, Mechanical Environmental Stability	X	X	X	X	X
Long Term Reliability	X	X	X	X	X

FIGURE 1. TESTS REQUIRED TO ASSURE DEVICE PROPERTIES

Production of the HVIC's was initiated as a result of passing these qualifications. A Quarterly Product Monitor Plan was implemented to measure and control the reliability of the product during production. The tests in this plan are illustrated in Figure 4.

Technical Approach Taken to Determine the Expected Annual Field Failure Rate

There was also a need to determine the expected reliability in field applications based on these accelerated test results. An estimate of the expected annual field failure rate at application conditions was calculated for the first year. This was based on the favorable results of the accelerated qualification tests and the expected results from the quarterly monitor tests. The acceleration multipliers between the HTB stress levels and the application stress levels were determined by multi-level testing. This is an example of how these accelerated results can be used to predict the product reliability under application conditions.

In order to calculate the expected annual reliability or field failure rate the following information is needed:

1. Application stress conditions,
2. Reliability model to be used,
3. The acceleration multipliers between the test and the application conditions.

ACCELERATED STRESSES	STRESS OBJECTIVES
High Temperature Bias (HTB)	Die bulk and surface stability under electrical bias and elevated temperature conditions.
High Temperature Storage	Device physical and chemical stability under accelerated high temperature.
Damp Heat Bias (DHB)	Device physical and surface stability and package material compatibility under accelerated electrical bias, temperature and humidity.
Temperature Cycling	Device mechanical strength and durability under accelerated conditions of thermal expansion and contraction.
Vibration Fatigue	Ability of the mechanical parts of the device to withstand accelerated forces and low frequency vibration.

FIGURE 2. OBJECTIVES OF THE ACCELERATED STRESSES

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STRESS HIGH TEMPERATURE BIAS V = 400V, 15V. T_J = +125°C	SAMPLES FROM PRODUCTION LOTS	CUMULATIVE FAILURES/SAMPLE SIZE HOURS UNDER STRESS			
		168	500	1000	2000
(1991)	120	0/120	0/120	0/120	–
	400	1/400 (Note 3) –	2/400 (Note 3) –	2/400 (Note 3) 1/400 (Note 4)	–
	240	0/240	1/240 (Note 4)	1/240 (Note 4)	1/240 (Note 4)
SUB TOTAL	760 (Note 1)	–	–	–	–
V = 450V,15V. T_J = +125°C (1990)	90 (Note 2)	0/90	0/90	0/90	0/90
HIGH TEMPERATURE STORAGE T_A = +150°C	100 (Note 2)	0/100	0/100	0/100	–
DAMP HEAT BIAS(DHB) V = 300V,15V. +85°C, 81% RH	100 (Note 2)	1/100 (Note 5)	1/100 (Note 5)	1/100 (Note 5)	–
TEMPERATURE CYCLING -40°C/+25°C/+150°C 27/3/27 minutes		CYCLES OF STRESS			
		100	500		
	100 (Note 2)	0/100	0/100		
VIBRATION FATIGUE X1,Y1,Z1 planes 10 g's, 32 hours per plane		PLANES OF STRESS			
		X_1	Y_1	Z_1	
	10 (Note 2)	0/10	0/10	0/10	

NOTES:

1. Random samples from eight production lots.
2. Random samples from three production lots except for Vibration Fatigue which had samples from one lot.
3. High voltage leakage failure: corrective action is defined and implemented.
4. Failed on test: corrective action is defined and implemented.
5. Parametric failure.

FIGURE 3. QUALIFICATION TEST RESULTS

STRESS CONDITIONS	SAMPLES FROM 3 RANDOM PRODUCTION LOTS	HOURS/ CYCLES UNDER STRESS	NO. OF FAILURES ALLOWED PER LOT
HIGH TEMPERATURE BIAS (HTB)			
V = 400V, 15V T_j = +125°C	50/Lot Total 150	1000	0
HIGH TEMPERATURE STORAGE			
T_A = +150°C	20/Lot Total 60	1000	0
DAMP HEAT BIAS (DHB)			
V = 300V, 15V: +85°C 81%RH	20/Lot Total 60	1000	1
TEMPERATURE CYCLE			
-40°C/+25°C/ +150°C 27/3/27 Minutes	20/Lot Total 60	500	0

FIGURE 4. QUARTERLY PRODUCT MONITORING TESTS

The application conditions are: V = 350V, 15V. T_J = 100°C Operating time is 8760 hours per year.

The model used for predicting the product reliability is based on a negative exponential failure distribution with a constant failure rate. This can be expressed with the following equation:

P_S = exp [-t / MTBF] (1)

where: P_S is the reliability or probability of survival.

t is the operating time in hours.

MTBF is the Mean Time Between Failure in hours.

The Probability of Failure (P_F) is: $P_F = 1 - P_S$ (2)

Extensive reliability studies and accelerated tests have been conducted on discrete semiconductors and integrated circuits for a number of years.[1] Based on this experience it was decided to use the High Temperature Bias test as the primary accelerating stress for predicting the reliability of the HVIC under application conditions. It was found that matrix testing of devices under several levels of high temperature reverse bias led to the development of an accelerated reverse voltage model and an accelerated temperature model i.e. the Arrhenius model.[2] This information enables a quantitative extrapolation of the results from high level accelerated tests to the expected results at the lower stress levels found in applications.

Voltage Multiplier:

The reverse voltage model of response is shown on page 211 of the second reference.[2] This was used to determine the Voltage Multiplier (M_V) for derating from high to low voltage stress levels. This relationship is shown in the following equation:

$M_V =$ $[V1/V2]^{1.6534}$ (3)

where V1 and V2 are given in volts

Temperature Multiplier:

The predominant failure mechanisms found in semiconductors during operation are related to temperature and often fit the Arrhenius Model of response. This model can be expressed by the equation:

$\lambda =$ $\exp [A + B/T]$ (4)

$\lambda =$ $A' \exp [-E/(kT)]$

λ failure rate

T absolute temperature (°Kelvin)

A, B empirically derived constants from life test data.

A′ exp (A)

k Boltsman's constant, 8.62×10^{-5}eV/K

E activation energy, empirically derived from: E = -kB. The slope B is negative.

The temperature acceleration multiplier (M_T) between a high temperature test and a lower temperature test can be obtained from the ratio of the failure rates at the two temperatures. This results in:

$M_T =$ $\exp [B/T_2] / \exp [B/T_1]$ (5)

where: T_1 is the low temperature in °K.

T_2 is the high temperature in °K.

Total Multiplier:

The total multiplier (M) is equal to the product of M_V and M_T:

$M =$ $M_V M_T$ (6)

A test was performed to determine the capability of the HVIC over a temperature range of +21.7°C to +150°C. The high voltage leakage current (I_{LKG}) vs temperature was measured on a sample of HVIC'S. The average value at each temperature was plotted on an Arrhenius graph resulting in a reasonable fit to the model. A computer program was used to transform the data and plot the natural Log I_{LKG} vs 1000/T_{ABS} and this is shown in Figure 5. A linear regression analysis of the data gave this general equation:

$y =$ $22.81178 - 6.900413z$ (7)

This has a correlation coefficient of 0.998 which is very good. From this data "E" was calculated to be 0.595eV. This was used to determine the temperature multiplier (M_T) of the HVIC.

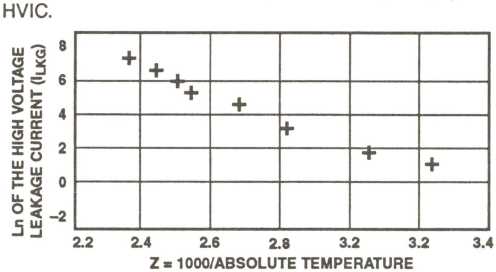


FIGURE 5. PLOT OF Ln OF LEAKAGE CURRENT (I_{LKG}) vs 1000/T_{ABS}

Estimated Annual Field Failure Rate

The calculation of the expected annual field failure rate at application conditions is outlined below. This is based on the results of the HTB tests included in the qualification tests performed in 1990 and in 1991 as well as the favorable results expected on the quarterly monitor tests. A calculation of the acceleration multipliers is shown below:

Voltage Multiplier:

The voltage multipliers between the two HTB test voltages and the application voltage, from equation (3), are:

$M_{V1} =$ $[400/350]^{1.6534}$ $= 1.2471$

$M_{V2} =$ $[450/350]^{1.6534}$ $= 1.5152$

Temperature Multiplier:

From the Arrhenius equation (4) the activation energy E = -kB. Also from the test on high voltage leakage current vs temperature it was found that E was 0.595eV. Solving the above equation, E = -kB, for B results in:

$B =$ -6902.55.

The temperature multiplier between the HTB test at +125°C and the application condition of +100°C, from (5), is:

$M_T =$ $\exp [-6902.55/398] / \exp [-6902.55/373]$

$M_T =$ 3.198

Total Multiplier:

The total multipliers between the two HTB test conditions and the application conditions, from (6), are:

M1 = [1.247] [3.198] = 3.98791

M2 = [1.515] [3.198] = 4.8450

Unit Test Hours

TESTS	HTB UNIT HOURS 400V, +1 25°C	M	APPLICATION UNIT HOURS 350V, +100°C
Qualification (1991)	1006760	3.98791	4014868.3
Quarterly Monitor	600000	3.98791	2392746.0
Qualification (1990)	HTB 450V, +125°C 180000	4.8450	872100.0
	TOTAL		7279714.3

Failure Calculation:

For zero failures and at a 50% confidence level the expected average failure rate would be:

$\lambda =$ $0.7[10^5]$ / Unit Hours

$\lambda =$ $0.7[10^5] / 7279714.3$ $= 0.009616\%/1000$ hours

MTBF = $1[10^5] / 0.009616$ $= 10,399,591.9$ hours

The probability of failure in the first year from equation (2) would be:

$P_F =$ $1 - \exp - [8760/10,399,591.9]$

$P_F =$ 0.00084 or 0.084% per year

The improvement in the HVIC reliability when the operating chip temperature is lowered in the application is shown in Figure 6. For example, this shows that the annual reliability is improved about 4 to 1 when the operating chip (die) temperature is lowered to +75°C instead of +100°C. Similarly there is an improvement of over 12 to 1 when the operating chip temperature is lowered to +55°C.

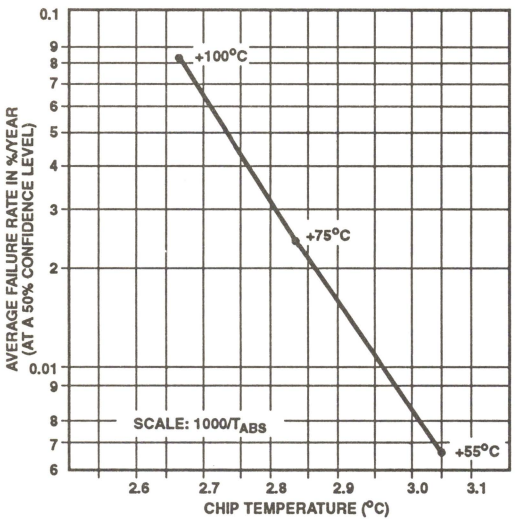


FIGURE 6. RELIABILITY IMPROVEMENT WITH A DECREASE IN OPERATING CHIP TEMPERATURE

Conclusions

1. The average failure rate during the first year is expected to be 0.00962%/1000 hours or 96.2 FITs when the application operating chip temperature is at +100°C and 25.4 FITs at +75°C and 7.6 FITs at +55°C. Note: 1 FIT = 1 Failure/10^9 hours.
2. Similarly, with continued favorable quarterly monitoring test results, the expected average failure rate would decrease from 96.2 to 72.4 FITs after the second year and to 58 FITs after the third year at a chip temperature of +100°C.
3. There is a good chance that the reliability could be better than the predictions since short term evaluation tests showed that samples of HVIC's are capable of withstanding leakage current measurements at V = 500V and +150°C. This is 150 volts and +50°C above the application operating conditions of 350V and +100°C.

Acknowledgment

The author wishes to acknowledge the analytical contributions and encouragement for this report from Pete Shafer, Ray Dyer, and Jack Essom.

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RR002 April 1992

Reliability Report

CONCURRENT DESIGN, TEST AND RELIABILITY ENGINEERING OF POWER ASICs

By Erwin A. Herr

Introduction

A program was initiated in July 1987 to develop a new Intelligent Power ASIC chip technology using state-of-the-art type components and processing. This process utilized mixed signal technology that was optimized for motor/ motion control, power supply and interface applications. The first application chosen was a DC/DC converter chip which was mounted in a module with an output of 5 VDC and a current of 10 amperes continuous and 20 amperes peak. The environment for this application was to be in office equipment, for commercial and industrial usage.

The reliability objective of this product was very aggressive in terms of both operating conditions and failure rate. Accelerated testing techniques were used to demonstrate that the failure rate objective was achieved.

Technical Strategy for Design, Test and Reliability Engineering

The Intelligent Power ASIC technology had to produce chips which could be designed and developed in a minimum of time, be cost effective, easily manufactured as well as being very reliable. Normally this would be accomplished with mature designs and products that had been manufactured over a period of time with known capabilities and established reliability. However, since this was to be a state-of-the-art technology a new approach had to be taken in order to meet the required time table. These requirements led to the concept of concurrent product, test and reliability development.

An overview of the major activities of this program is illustrated in Figure 1. It is to be noted that this starts with product concept phase and sequences through a number of the major steps up to the production phase. It can also be seen that there were early and concurrent activities in Design, Test and Reliability Engineering. This required the ultimate in communication, cooperation, team work and leadership in many technical areas. This resulted in parallel actions in several areas which traditionally were performed in series. The concurrent action approach not only saved time and cost but it inspired commitment for success from the contributors.

PRODUCT CONCEPT AND APPLICATIONS

PRODUCT FUNCTIONAL SPECIFICATIONS

PROGRAM PLAN AND DEVELOPMENT SCHEDULE

TEST DEVELOPMENT ENGINEERING	ADVANCED DESIGN AND DEVELOPMENT ENGINEERING	ADVANCED RELIABILITY ENGINEERING
• Test methods & software design	• Product and process development plan	• Accelerated reliability program plan
• Test hardware design	• Mask design of WATs, TEGs and Macros	• Design and construct reliability test equipment
• Characterization of WATs, TEGs & Macros	• Process samples of TEGs and Macros	• Accelerated reliability testing of TEGs and Macros
• Analysis of results - Corrective actions	• Analysis of results - Design out defects if design related - Process improvements where applicable	• Analysis of results - Failure Analysis - Recommend corrective action
• Characterization & evaluation	• Process samples of TEGs, Macros and prototype ASICs with applicable improvements	• Accelerated reliability testing and evaluation of improved TEGs, Macros and prototype ASICs
• Characterization & evaluation	• Design of Relmon and production ASICs	• Accelerated reliability testing and evaluation
• Characterization for production	• Technical Review and approval production	• Accelerated testing of Relmon and production ASICs

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DEVICE PROPERTIES	HIGH TEMPERATURE BIAS	OPERATING LIFE AND POWER CYCLING	DAMP HEAT BIAS	TEMPERATURE CYCLE	ELECTRO-MIGRATION
Die Bulk and Surface Stability	X	X	X		
Sealed Junction Integrity	X	X	X	X	
Thermal, Mechanical Environmental Stability	X	X	X	X	X
Long Term Reliability	X	X	X	X	X

FIGURE 2. TESTS REQUIRED TO ASSURE DEVICE PROPERTIES

This concept of Concurrent Engineering meant that, as the building blocks of the Power ASIC technology were being developed, they were independently characterized and assessed for reliability under accelerated test conditions. These building blocks included new component structures as well as new Macro circuits for the primary functions of the chip. In order to evaluate these building blocks under accelerated test conditions an analysis was made of the desired properties and the accelerated stresses that would assure them. The test matrix in Figure 2 shows the stresses chosen on this program. The objectives of each of the accelerated stresses are shown in Figure 3. Based on this analysis and previous experience the stresses chosen included High Temperature Bias (HTB), Operating Life, Power Cycling, Damp Heat Bias (DHB), Temperature Cycling and Electromigration testing. The overall objective of this early testing was to provide rapid reliability information feed- back to the designers so that they could select the most reliable structures for the new Macro designs.

The approach taken was to use Test Element Groups (TEGs)[1], that were packaged in a manner similar to that which was planned to be used in production. These TEGs included structures of elements such as NPN & PNP bipolar transistors, NMOS and PMOS transistors, LDMOS power FET, zener diodes and electromigration test sites.

As the program progressed these elements were fabricated on the same semiconductor wafers as the Macro and the ASIC circuits. After packaging, the TEG devices were subjected to the same type of stresses that they would normally see in the ASIC circuit. However, the stress levels were usually higher in order to obtain accelerated test results. For example, samples of the components were subjected to multi-level accelerated stresses of high temperature bias for 1000 to 2000 hours. High Humidity Bias or Damp Heat Bias stresses for 1000 to 2000 hours were also used. Temperature cycling was performed to 3000 cycles. Measurements were made of the critical characteristics of the isolated structures initially and at several times after hours of stress. Analyses were made of the distribution of the characteristics and the changes in critical characteristics with stress. The objective was to stress the TEGs to destruction so as to have sufficient failures for failure analysis. This allowed isolation and identification of the failure modes and mechanisms which suggested corrective actions. These led to improvements in design and processing.

The Macros were similarly packaged as the TEGs and submitted to accelerated high temperature bias at +125°C and +150°C for 1000 to 2000 hours. Analysis of the failures from these tests brought out any failure mechanisms that could occur between the combination of structures in the functional circuit. This allowed an in-depth evaluation of the building block circuits for the final ASIC chip.

The production Intelligent Power ASIC chip was constructed from the building block Macros and power switching functions. Samples of this type of chip were mounted in several types of packages to evaluate the capability of the chip to withstand electrical, temperature and environmental stresses. One group of Power ASIC samples was subjected to accelerated conditions of a dynamic operating life of Vin = 20VDC, Vout = 5V at 10 amperes DC. The junction temperature at the chip was +125°C and the duration of the test was 2000 hours. Another group was subjected to a power cycling test for 2000 hours at maximum operating life conditions with a 10 minute "on" and a 10 minute "off" cycle. In a third group the chip was similarly packaged and these devices were subjected to 1000 to 2000 hours of Damp Heat Bias at

ACCELERATED STRESSES	STRESS OBJECTIVES
High Temperature Bias (HTB)	Die bulk and surface stability under electrical bias and elevated temperature conditions
Operating life and Power cycling	Die bulk and surface stability under electrical operation and elevated temperature conditions
Damp Heat Bias (DHB)	Device physical and surface stability and package material compatibility under accelerated electrical bias, temperature and humidity.
Temperature Cycling	Device mechanical strength and durability under accelerated conditions of thermal expansion and contraction.
Electromigration	Capability of metallization runs to withstand current in power integrated circuits

FIGURE 3. OBJECTIVES OF THE ACCELERATED STRESSES

+85°C 81% RH and 45 volts. A fourth group was subjected to a temperature cycle test of 3000 cycles. In a fifth case samples were subjected to a high temperature bias test of 60 volts on the power section and 42 volts on the control section at a junction temperature of +150°C for 500 hours duration. This series of multi-level stresses was used to evaluate the combined functions of the Macros and the power switching sections of the final Power ASIC. Reliability predictions are made based on the HTB, operating life, power cycling and DHB test results.

The process technologies used on this program included low and high speed bipolar and complementary MOS signal processing designs as well as combinations of bipolar and MOS power structures. The semiconductor chips were processed with a two level metallization system that is compatible with plastic packaging.

Accelerated Test Results on Components, Macros and Power ASICs

Accelerated testing was used on this Concurrent Engineering Program in order to obtain an early reliability evaluation of the building blocks to be used to construct the Power ASIC chip. It was imperative to obtain this information in a minimum time in order to have an efficient design cycle. Care was taken to choose stress levels that would accelerate the changes in characteristics caused by failure mechanisms that exist at lower stress levels. Analysis was made of the initial distribution of critical characteristics as well as changes in the distribution with time under stress. Comparisons were made of the accelerated test results of the components and Macros to gain the maximum information. This helped identify the failure mechanisms for a thorough analysis of any failures obtained. It also allowed the selection and use of semiconductor structures and processes in the final ASIC design that were free from these sensitive mechanisms. This enabled the accelerated reliability information and corrective actions to be in phase with the normal test characterization of the building blocks which resulted in an optimized design and process development cycle.

A general summary of the accelerated constant stress-in-time program conducted during the concurrent product, process and reliability development cycle is given in Figure 4. This includes the number of units tested, the unit hours of stress and the number of failures obtained each year for the components, Macros and ASICs. The constant stress-in-time tests included high temperature bias, operating life, power cycling and a damp heat bias test. Some interesting observations and conclusions can be drawn from this information. It points out the inherent advantages of this Concurrent Engineering Program in the development of a state-of-the-art Power ASIC semiconductor chip.

- About 24% of all the test vehicles were stressed during 1988. In the traditional serial development cycle only minimal reliability tests would occur in the first year. This saved at least a year of program time.
- Forty three percent of all the vehicles tested were the less complex structures; namely, TEGs or Macros. This allowed a more thorough and effective analysis of failures which made it easier to isolate failure mechanisms and implement corrective actions.
- Corrective actions were implemented in the first year when the cost of making design changes and process improvements was at a minimum.
- Test systems for the measurement of device parameters and accelerated stress equipment were developed and procured early in the cycle.
- The general testing trend showed that the majority of the Components and Macros were tested during the first year. Long term accelerated testing (2000 hours) of the Power ASIC™ chips was completed during the second year.
- A total of 11385 vehicles were tested under acclerated conditions during the program. A distribution of the vehicles showed that there were 25% components, 18% Macros and 57% Power ASICs.
- The trend in failure occurrence was highest in the early years of development, but decreased dramatically in subsequent years. This gave a favorable reliability growth pattern.
- This accelerated program enabled production ASICs to be shipped during the second year.

The accelerated tests used to evaluate components or TEGs included high temperature bias at +125°C and +150°C, damp heat bias and temperature cycling. The duration of the high temperature and damp heat bias tests was 1000 to 2000 hours. The general plan for the evaluation of the semiconductor structures used was to stress the structures in the components at the highest bias level (20V), in the Macros at an intermediate level (16V) and in the ASIC circuits at the use level (12.5V).

As previously mentioned the extensive unit hours of testing during the initial evaluation phase are summarized in Figure 4. During the latter part of this evaluation qualification tests were run. The criteria for qualification of components was to pass the appropriate bias tests at the accelerated temperature of +125°C for at least 1000 hours with zero failures out of a sample of twenty. The results of these tests on bipolar transistors, MOS transistors, the LDMOS power FET as well as the zener diodes are summarized in Figure 5. Bias tests at +150°C were also performed to assess the temperature margin for reliability on these components.

Component sample groups of transistors, zeners and the power FETs were subjected to the accelerated test of Damp Heat Bias at +85°C, 81% RH and the appropriate bias for 1000 to 2000 hours. Samples of these devices were also subjected to temperature cycling for 1000 cycles at -40°C to +150°C. Other general evaluation tests were conducted on special structures to measure their capability to withstand electromigration, ESD and latch up stresses.

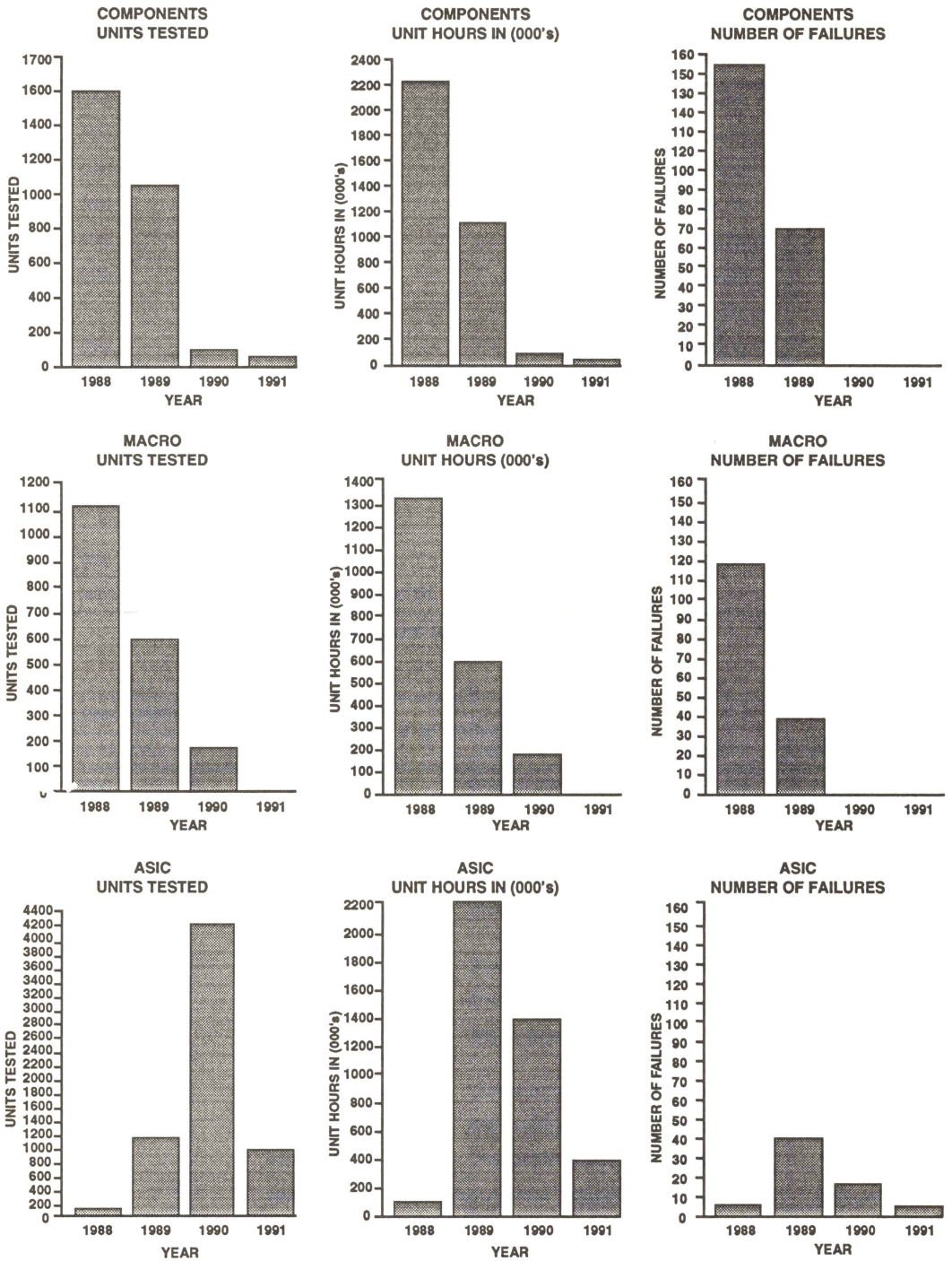


FIGURE 4. CONCURRENT PRODUCT, PROCESS AND RELIABILITY DEVELOPMENT

TEGs	PACKAGE	HIGH TEMPERATURE BIAS (HTB)	1000 HOURS FAILURES/SAMPLE	
			HTB AT +125°C	HTB AT +150°C
NPN	16 Lead DIP	HTB, 20V	0/39	0/20
PNP	16 Lead DIP	HTB, 20V	0/20	0/20
PMOS	16 Lead DIP	HTB, 20V	0/20	0/20
	16 Lead DIP	HTGB, 25V	0/20	0/20
NMOS	16 Lead DIP	HTB, 20V	0/40	3/20
	16 Lead DIP	HTGB, 20V	-	0/20
	16 Lead DIP	HTGB, 25V	0/20	-
Zener-A	16 Lead DIP	0.5mA	-	0/20
Zener-B	16 Lead DIP	1.0V	-	0/20
Zener-C	16 Lead DIP	HTB, 100mA	0/20	0/20
Zener-D	16 Lead DIP	HTB, 6.5V	0/20	0/20
	16 Lead DIP	HTB, 100mA	0/20	1/20
5A LDMOS	TO 218	HTB, 60V	0/20	1/20
	TO 218	HTGB, 20V	0/20	0/20
		TOTAL	0/259	5/260

FIGURE 5. COMPONENT TEG QUALIFICATION

MACRO TYPES	PACKAGE	HIGH TEMPERATURE BIAS (HTB)	1000 HOURS FAILURES/SAMPLE	
			HTB AT +125°C	HTB AT +150°C
Bandgap Voltage Reference	16 Lead DIP	16V, +125°C/+150°C	0/60	0/60
MOS OPAMP A	16 Lead DIP	16V, +125°C/+150°C	0/20	0/20
MOS OPAMP B	16 Lead DIP	16V, +125°C/+150°C	0/20	0/20
Reference Current Generator	16 Lead DIP	16V, +125°C/+150°C	0/20	0/20
Comparator A	16 Lead DIP	16V, +125°C/+150°C	0/20	0/20
Comparator B	16 Lead DIP	16V, +125°C/+150°C	0/20	1/20
Transconductance Amplifier	16 Lead DIP	16V, +125°C/+150°C	0/20	0/20
Comparator C	16 Lead DIP	16V, +125°C/+150°C	0/20	0/8
Gate Driver	16 Lead DIP	16V, +125°C/+150°C	0/20	0/20
Oscillator	16 Lead DIP	16V, +125°C/+150°C	0/20	0/20
Voltage Regulator	16 Lead DIP	45V/5/V, +125°C/+150°C	0/20	0/20
		TOTAL	0/260	1/248

FIGURE 6. MACRO QUALIFICATION

The eleven Macro types listed in Figure 6 were also subjected to the same type of general bias tests at elevated temperature and damp heat that were used on the components. These are summarized in Figure 4. They were also subjected to temperature cycling for 1000 cycles at -40°C to +150°C. Again the criteria for qualification was to pass the appropriate bias tests at the accelerated temperature of +125°C for at least 1000 hours with zero failures out of a sample of twenty. The elevated temperature margin for reliability was assessed at +150°C. The results of these tests are summarized in Figure 6.

The failures generated during the early phase of the accelerated tests on components and Macros were particularly important for identifying failure mechanisms for product design and process improvements. The corrective actions included improvements in design resulting from the selection of the most reliable structures based on test results. This timely information was used to establish practical and robust design rules. These rules, based on early component results, were used to design the Macros. Progressively the design rules were further improved from the results of accelerated testing of the Macros. These improvements were implemented into the final ASIC design.

If the failure analysis indicated that the failure mechanisms were process related then process improvements were implemented. These were monitored by testing the Wafer Acceptance Test (WAT) structures on subsequent wafers to demonstrate the improvement. From this information control limits were established on key parameters to maintain statistical process control.

YEAR	STRESS	SAMPLES	HOURS OF STRESS	FAILURES
1989	HTOP & HTB at +125°C, Power cycling up to +125°C	732	2000	1 (100 Hrs)
	Damp Heat Bias +85°C, 81% RH	231	2000	1 (24 Hrs)
	TOTAL	963		3
1990	HTB at +125°C	400	1020	1 (484 Hrs)
	HTB at +125°C	1450	143	0
	HTB at +150°C	217	190	1 (170 Hrs)
	HTB at +150°C	494	505	1 (118 Hrs)
	HTB at +150°C	965	122	0
	TOTAL	3526		3
1991	HTB at +125°C	443	126	0
	HTB at +125°C	179	1010	1 (112 Hrs)
	HTB at +150°C	100	500	1 (182 Hrs)
	HTB at +150°C	248	126	0
	TOTAL	970		2
	Grand Total	5459		8

FIGURE 7. POWER ASIC™ QUALIFICATION

The evaluation of the Power ASIC chips included tests on high temperature bias and operating life at a chip temperature of +125°C, damp heat bias at +85°C, 81% RH and temperature cycling of 3000 cycles to the package limits of -5°C to +105°C. The results from high temperature bias, high temperature operating life (HTOP), power cycling and damp heat bias were considered the primary stresses the chip would have to endure in the application. This testing is illustrated in Figure 7. Failure analysis was used to confirm any failures that occurred. Corrective actions were determined, implemented and demonstrated for most of the failures. The remaining failures, for which corrective action had not been determined, were used in the failure rate calculation. This information, as shown in Figure 7, was used to assess the reliability of the Power ASIC under the application conditions.

Power ASIC Reliability Assurance

A reliability database ages very rapidly unless it is kept current. Even if no known changes are made, the database needs a continuous flow of current data. To meet this need, a device called the Relmon (Reliability monitor) was designed. This device is a functional part number which is made part of every mask set. The Relmon is used to periodically sample the process and thus update the database with data resulting from improvements such as design rules for more efficient layout, circuit design innovations, and process modifications. The library based Power ASIC design approach enables these types of changes to be made and the database to be maintained. The volume of new part numbers, most containing both "old" Macros and components as well as some "new" Macros and components, allows the qualification work on the new part number to "bridge" the new elements to the existing database. The need to merge data relating to changes such as design rules and process improvements is met by utilizing the Relmon as the vehicle to bridge the data.

Every Power ASIC part which is shipped is tied to the reliability database with four connections: The qualification testing was performed on the part number. This testing is designed to address any aspects of the part number which are outside the bounds of the existing reliability database, for example:

- New components or Macros.
- Components or Macros applied in a new way.
- New packaging or environmental conditions.
- Process improvements. The part number testing is performed on every part. This testing is designed to address three elements of reliability:
- Functional test coverage to assure that all customer specifications are guaranteed.
- Reliability test coverage to assure that all accessible portions of the chip are tested and appropriate voltage margins are applied.
- Parameter limits All parameter limits are examined to assure that limits reflect no more than expected variations.

The WAT (Wafer Acceptance Test) testing is performed on every wafer. This is a set of tests which must be passed for a wafer to be accepted for part number probing. This testing is designed to address three elements related to reliability:

Process control monitors These structures assure that the process is within acceptable bounds.

Representative devices These structures assure at the device level that the wafer has been appropriately processed.

Representative topology test elements These structures assure that aspects such as step coverage are under control. The Relmon (present on every wafer) is used in two ways to assure reliability:

Reliability monitoring Every week a sample of Relmons is subjected to 100 hours of stress testing to continuously monitor the process. Every quarter a sample is subjected to 1000 hours of stress.

Yield analysis In an ASIC product line there can be a great variety of part numbers in various stages of product life cycle. The Relmon is a constant reference that can be used to understand yield variations.

The reliability of the Power ASIC chip, operating at +90°C, was determined from the test data given in Figure 7. Since a large part of the testing was performed at accelerated chip temperatures of +125°C and +150°C it was necessary to transform this information to equivalent times at +90°C. This was accomplished by using the Arrhenius model of response[2]. The activation energy used in this model was 0.5425 electron-volts which is based in the Macro test data in Figure 6. From this information a Weibull model was used to calculate the expected failure rate at 60,000 operating hours at a chip temperature of +90°C. This failure rate was found to be 0.018% per thousand hours at a 50% confidence level. Also from the Weibull model it was found that beta was about 0.5 which means that these devices had a decreasing failure rate with time.

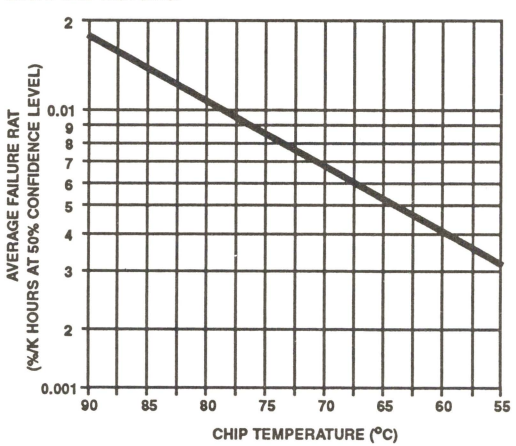


FIGURE 8. RELIABILITY OF POWER ASIC CHIP AT 60,000 OPERATING HOURS

The improvement in reliability of the power ASIC chip, when the operating chip temperature is lowered in the application, is shown in Figure 8. For example, this shows that the reliability is improved 2 to 1 when using a chip temperature of +75°C and 6 to 1 when using +55°C instead of +90°C.

Conclusion

This was a program to develop state-of-the-art Intelligent Power ASIC products. The concept of Concurrent Engineering proved to be very beneficial in the execution of this program. The following general observations and conclusions can be made:

1. A complex power integrated circuit was fabricated in record time on a semiconductor chip, which included over 23 types of Macros and assemblies plus a power switching section.
2. Concurrent activities and communication in Test Development Engineering, Advanced Design and Development Engineering and Advanced Reliability Engineering assured a timely and successful product development cycle.
3. Excellent teamwork that required the ultimate in communication, cooperation, commitment and leadership enabled shipment of production chips in the second year.
4. Over 11,000 test vehicles, which included TEGs or Components, Macros and ASIC circuits, were stressed under accelerated conditions as the product was developed.
5. Reliability was designed into the product early and evaluated concurrently which enabled us to exceed the expected reliability goal by a factor of about three to one.
6. The Relmon was developed to monitor reliability and update the data base.

Acknowledgment

The author wishes to acknowledge the analytical contributions and encouragement for this report from Peter Shafer, Ray Dyer, Jack Essom and Paulette Gaillard.

References

[1] E.A. Herr et al "Techniques for the Control of Integrated Circuit Quality and Reliability", Technical Report AFM-LTR-67-147, June 1967 Air Force Materials Laboratory, Wright Patterson AFB, Ohio 45433.

[2] E.A. Herr, A. Poe and A. Fox "Reliability Evaluation and Prediction for Discrete Semiconductors," IEEE Transactions on Reliability, August 1980, Volume R-29 Number 3, Catalogue No. ISSN-0018-9529, pp 208-216. 7

INTELLIGENT POWER ICs 13

PACKAGING INFORMATION

	PAGE
PART NUMBER - PACKAGE OUTLINE DESIGNATOR	13-2
DUAL-IN-LINE PLASTIC PACKAGES (PDIP)	13-5
SMALL OUTLINE PLASTIC PACKAGES (SOIC)	13-8
PLASTIC LEADED CHIP CARRIER PACKAGES (PLCC)	13-11
SINGLE-IN-LINE PLASTIC PACKAGES (SIP)	13-12
CERAMIC DUAL-IN-LINE METAL SEAL PACKAGES (SBDIP)	13-16
CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGES (CERDIP)	13-18
CERAMIC LEADLESS CHIP CARRIER PACKAGES (CLCC)	13-20
CERAMIC SOIC FLATPACK PACKAGES (SOIC FLATPACK)	13-21
METAL CAN PACKAGES (CAN)	13-22

Part Number - Package Outline Designator

PART NUMBER	PACKAGE DESCRIPTION	PACKAGE OUTLINE
CA723E, CE	14 Lead Dual-In-Line Plastic Package	E14.3
CA723T, CT	10 Lead TO-100 Metal Can Package	T10.C
CA1523E	14 Lead Dual-In-Line Plastic Package	E14.3
CA1524E	16 Lead Dual-In-Line Plastic Package	E16.3
CA1524F	16 Lead Ceramic Dual-In-Line Frit Seal Package	F16.3
CA2524E	16 Lead Dual-In-Line Plastic Package	E16.3
CA2524F	16 Lead Ceramic Dual-In-Line Frit Seal Package	F16.3
CA3020, A	12 Lead TO-101 Metal Can Package	T12.B
CA3059	14 Lead Dual-In-Line Plastic Package	E14.3
CA3079	14 Lead Dual-In-Line Plastic Package	E14.3
CA3085, A, B	8 Lead TO-99 Metal Can Package	T8.C
CA3085E, AE, BE	8 Lead Dual-In-Line Plastic Package	E8.3
CA3094T	8 Lead TO-99 Metal Can Package	T8.C
CA3094E	8 Lead Dual-In-Line Plastic Package	E8.3
CA3094M	8 Lead Small Outline Plastic Package	M8.15
CA3165E	8 Lead Dual-In-Line Plastic Package	E8.3
CA3165EI	14 Lead Dual-In-Line Plastic Package	E14.3
CA3228E	24 Lead Dual-In-Line Plastic Package	E24.6
CA3242E	16 Lead Dual-In-Line Plastic Package	E16.3
CA3262E, AE	16 Lead Dual-In-Line Plastic Package	E16.3
CA3262AQ	28 Lead Plastic Leaded Chip Carrier Package	N28.45
CA3272AQ, Q	28 Lead Plastic Leaded Chip Carrier Package	N28.45
CA3273	3 Lead Single-In-Line Plastic Package	Z3.1A
CA3274E	8 Lead Dual-In-Line Plastic Package	E8.3
CA3275E	14 Lead Dual-In-Line Plastic Package	E14.3
CA3277E	16 Lead Dual-In-Line Plastic Package	E16.3
CA3282AS1	15 Lead Plastic Single-In-Line Package (Staggered Vertical Lead Form)	Z15.05A
CA3282AS2	15 Lead Plastic Single-In-Line Package (Surface Mount "Gullwing" Lead Form)	Z15.05B
CA3292AQ	28 Lead Plastic Leaded Chip Carrier Package	N28.45
CA3524E	16 Lead Dual-In-Line Plastic Package	E16.3
CA3524F	16 Lead Ceramic Dual-In-Line Frit Seal Package	F16.3
CDP68HC68S1E	14 Lead Dual-In-Line Plastic Package	E14.3
CDP68HC68S1M	20 Lead Small Outline Plastic Package	M20.3
HIP0080AM	28 Lead Plastic Leaded Chip Carrier Package	N28.45
HIP0081AS1	15 Lead Plastic Single-In-Line Package (Staggered Vertical Lead Form)	Z15.05A
HIP0081AS2	15 Lead Plastic Single-In-Line Package (Surface Mount "Gullwing" Lead Form)	Z15.05B

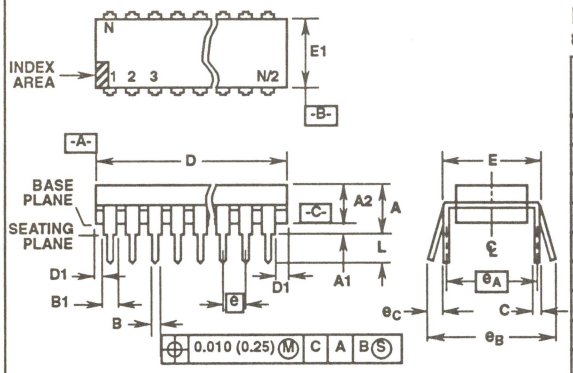
Part Number - Package Outline Designator (Continued)

PART NUMBER	PACKAGE DESCRIPTION	PACKAGE OUTLINE
HIP0082AS1	15 Lead Plastic Single-In-Line Package (Staggered Vertical Lead Form)	Z15.05A
HIP0082AS2	15 Lead Plastic Single-In-Line Package (Surface Mount "Gullwing" Lead Form)	Z15.05B
HIP1030AS	5 Lead Plastic Single-In-Line Package	Z5.067
HIP1031AS	5 Lead Plastic Single-In-Line Package	Z5.067
HIP1090AS	3 Lead Plastic Single-In-Line Package	Z3.1B
HIP2030IM	28 Lead Plastic Leaded Chip Carrier Package	N28.45
HIP2500IP	14 Lead Dual-In-Line Plastic Package	E14.3
HIP2500IPI	16 Lead Dual-In-Line Plastic Package	E16.3
HIP2500IB	16 Lead Small Outline Plastic Package	M16.3
HIP4010IB	20 Lead Small Outline Plastic Package	M20.3
HIP4011IS	15 Lead Plastic Single-In-Line Package (Surface Mount "Gullwing" Lead Form)	Z15.05B
HIP4080IP, AIP	20 Lead Dual-In-Line Plastic Package	E20.3
HIP4080IB, AIB	20 Lead Small Outline Plastic Package	M20.3
HIP4081IP, AIP	20 Lead Dual-In-Line Plastic Package	E20.3
HIP4081IB, AIB	20 Lead Small Outline Plastic Package	M20.3
HIP4082IP	16 Lead Dual-In-Line Plastic Package	E16.3
HIP4082IB	16 Lead Small Outline Plastic Package	M16.15
HIP5061DS	7 Lead Plastic Single-In-Line Package Staggered Surface Mount "Gullwing" Lead Form	Z7.05A
HIP5500IP	20 Lead Dual-In-Line Plastic Package	E20.3
HIP5500IB	20 Lead Small Outline Plastic Package	M20.3
HIP5600IS	3 Lead Plastic Single-In-Line Package	Z3.1B
HIP5600IB	8 Lead Small Outline Plastic Package	M8.15
HIP7010AP	14 Lead Dual-In-Line Plastic Package	E14.3
HIP7010AB	14 Lead Small Outline Plastic Package	M14.15
HIP7020AP	8 Lead Dual-In-Line Plastic Package	E8.3
HIP7020AB	8 Lead Small Outline Plastic Package	M8.15
HIP7030A0AM	68 Lead Plastic Leaded Chip Carrier Package	N68.95
HIP7030A2AP	28 Lead Dual-In-Line Plastic Package	E28.6
HIP7030A2AM	28 Lead Small Outline Plastic Package	M28.3
HIP7038A8IF	28 Lead Ceramic SOIC Flatpack Package	K28.E
HIP9010AB	20 Lead Small Outline Plastic Package	M20.3
HIP9020AP	14 Lead Dual-In-Line Plastic Package	E14.3
HIP9020AB	20 Lead Small Outline Plastic Package	M20.3
HV3-2405E-5, -9	8 Lead Dual-In-Line Plastic Package	E8.3
HV400IB	8 Lead Small Outline Plastic Package	M8.15
HV400IP	8 Lead Dual-In-Line Plastic Package	E8.3
HV400MJ/883	8 Lead Ceramic Dual-In-Line Metal Seal Package	D8.3
ICL7660CTV, MTV	8 Lead TO-99 Metal Can Package	T8.C

Part Number - Package Outline Designator (Continued)

PART NUMBER	PACKAGE DESCRIPTION	PACKAGE OUTLINE
ICL7660CBA	8 Lead Small Outline Plastic Package	M8.15
ICL7660CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7660SCBA, IBA	8 Lead Small Outline Plastic Package	M8.15
ICL7660SCPA, IPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7660SCTV, ITV, MTV	8 Lead TO-99 Metal Can Package	T8.C
ICL7662CTV, MTV, ITV	8 Lead TO-99 Metal Can Package	T8.C
ICL7662CPA, IPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7662CBD, CBD-O, IBD	14 Lead Small Outline Plastic Package	M14.15
ICL7663SCBA, IBA, ACBA, AIBA	8 Lead Small Outline Plastic Package	M8.15
ICL7663SCPA, IPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7663SCJA, IJA	8 Lead Ceramic Dual-In-Line Frit Seal Package	F8.3A
ICL7663SACPA, AIPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7663SACJA, AIJA	8 Lead Ceramic Dual-In-Line Frit Seal Package	F8.3A
ICL7665SCBA, IBA, ACBA, AIBA	8 Lead Small Outline Plastic Package	M8.15
ICL7665SCPA, IPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7665SCJA, IJA	8 Lead Ceramic Dual-In-Line Frit Seal Package	F8.3A
ICL7665SACPA, AIPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7665SACJA, AIJA	8 Lead Ceramic Dual-In-Line Frit Seal Package	F8.3A
ICL7667CBA	8 Lead Small Outline Plastic Package	M8.15
ICL7667CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7667CJA, MJA	8 Lead Ceramic Dual-In-Line Frit Seal Package	F8.3A
ICL7667CTV, MTV	8 Lead TO-99 Metal Can Package	T8.C
ICL7673CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL7673CBA	8 Lead Small Outline Plastic Package	M8.15
ICL7673ITV	8 Lead TO-99 Metal Can Package	T8.C
ICL8211CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL8211CBA	8 Lead Small Outline Plastic Package	M8.15
ICL8211CTY, MTY	8 Lead TO-99 Metal Can Package	T8.C
ICL8212CPA	8 Lead Dual-In-Line Plastic Package	E8.3
ICL8212CBA	8 Lead Small Outline Plastic Package	M8.15
ICL8212CTY, MTY	8 Lead TO-99 Metal Can Package	T8.C
SP600	22 Lead Dual-In-Line Plastic Package	E22.4
SP601	22 Lead Dual-In-Line Plastic Package	E22.4
SP710AS	3 Lead Plastic Single-In-Line Package	Z3.1B
SP720AP	16 Lead Dual-In-Line Plastic Package	E16.3
SP720AB	16 Lead Small Outline Plastic Package	M16.15
SP720MD	16 Lead Ceramic Dual-In-Line Metal Seal Package	D16.3
SP720MM	20 Pad Leadless Ceramic Chip Carrier Package	J20.A
SP721AP	8 Lead Dual-In-Line Plastic Package	E8.3
SP721AB	8 Lead Small Outline Plastic Package	M8.15

Dual-In-Line Plastic Packages (PDIP)



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

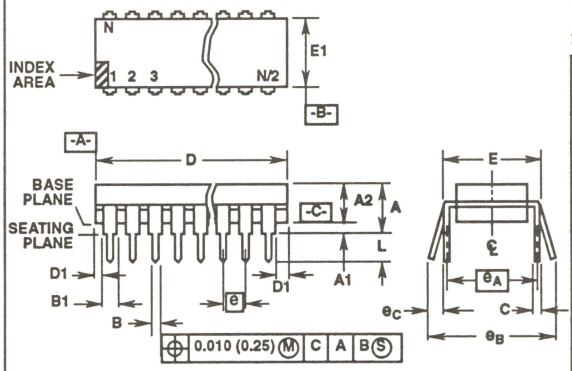
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP) (Continued)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

E22.4 (JEDEC MS-010-AA ISSUE C)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.065	1.15	1.65	8
C	0.009	0.015	0.229	0.381	-
D	1.065	1.120	27.06	28.44	5
D1	0.005	-	0.13	-	5
E	0.390	0.425	9.91	10.79	6
E1	0.330	0.390	8.39	9.90	5
e	0.100 BSC		2.54 BSC		-
e_A	0.400 BSC		10.16 BSC		6
e_B	-	0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		9

Rev. 0 12/93

E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

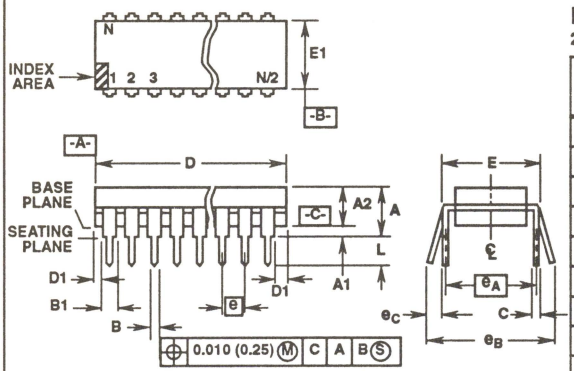
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP) (Continued)



E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

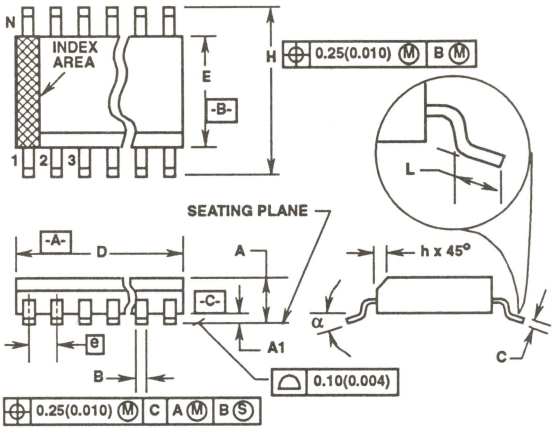
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

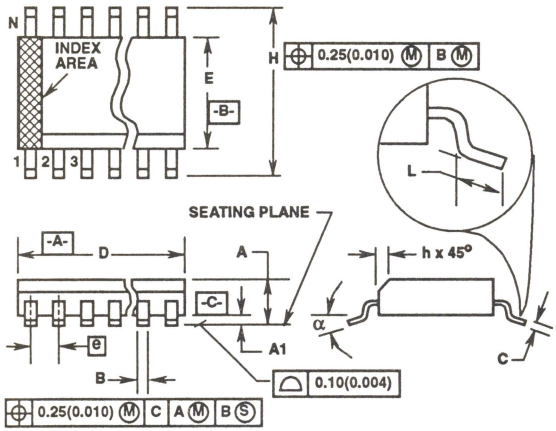
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC) (Continued)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

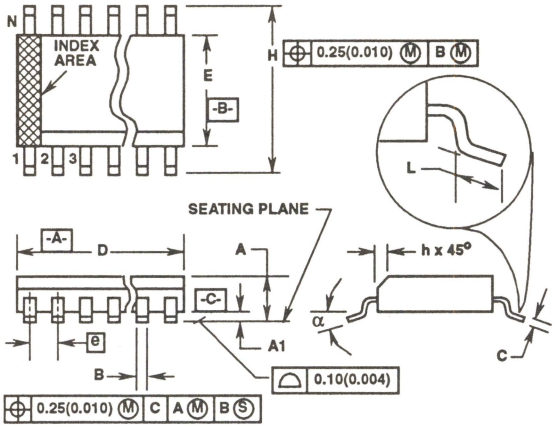
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC) (Continued)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

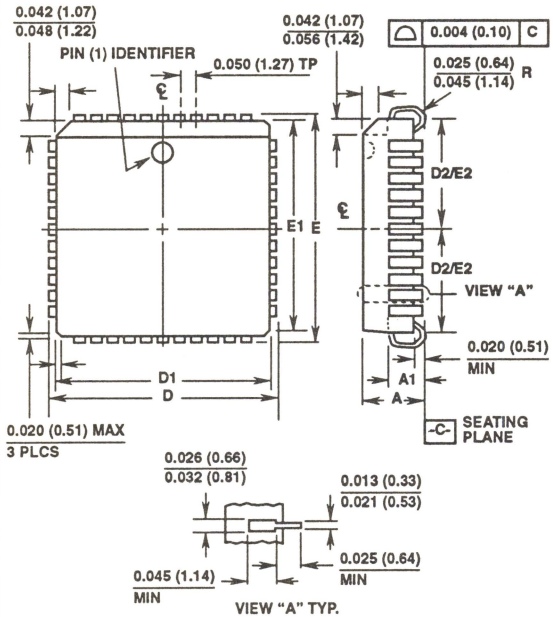
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier Packages (PLCC)



NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

N28.45 (JEDEC MS-018 ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

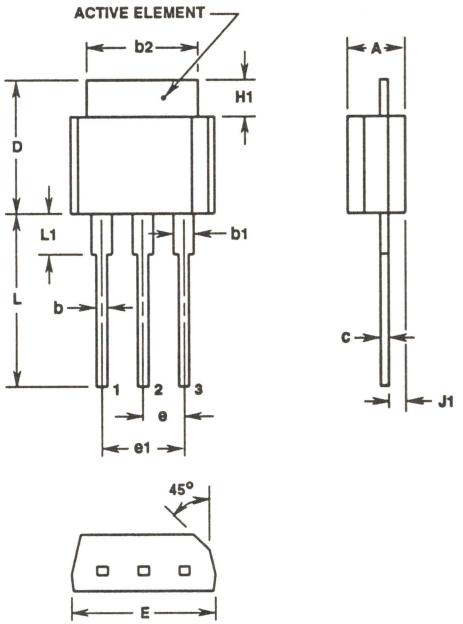
Rev. 0 12/93

N68.95 (JEDEC MS-018 ISSUE A)
68 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.985	0.995	25.02	25.27	-
D1	0.950	0.958	24.13	24.33	3
D2	0.441	0.469	11.21	11.91	4, 5
E	0.985	0.995	25.02	25.27	-
E1	0.950	0.958	24.13	24.33	3
E2	0.441	0.469	11.21	11.91	4, 5
N	68		68		6

Rev. 0 12/93

Single-In-Line Plastic Packages (SIP)



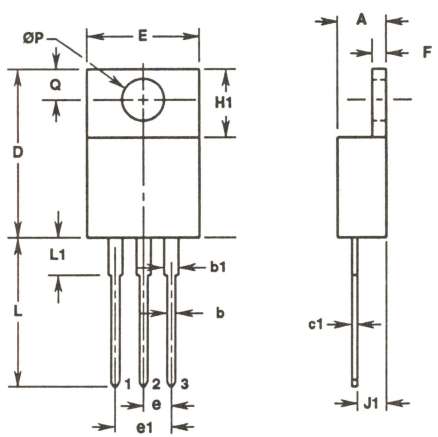
Z3.1A (JEDEC STYLE TO-202 MODIFIED)
3 LEAD SHORT TAB SINGLE-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.31	3.81	-
b	0.024	0.028	0.61	0.71	2, 3
b1	0.045	0.055	1.15	1.39	1, 2, 3
b_2	0.270	0.280	6.86	7.11	-
c	0.018	0.022	0.46	0.55	1, 2, 3
D	0.320	0.340	8.13	8.63	-
E	0.340	0.360	8.64	9.14	-
e	0.100 TYP		2.54 TYP		4
e1	0.200 BSC		5.08 BSC		4
H1	0.080	0.100	2.04	2.54	-
J1	0.035	0.045	0.89	1.14	5
L	0.410	0.440	10.42	11.17	-
L1	-	0.110	-	2.79	1

Rev. 0 2/94

NOTES:

1. Lead dimension and finish uncontrolled in zone L1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: INCH.



Z3.1B (JEDEC TO-220AB ISSUE J)
3 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

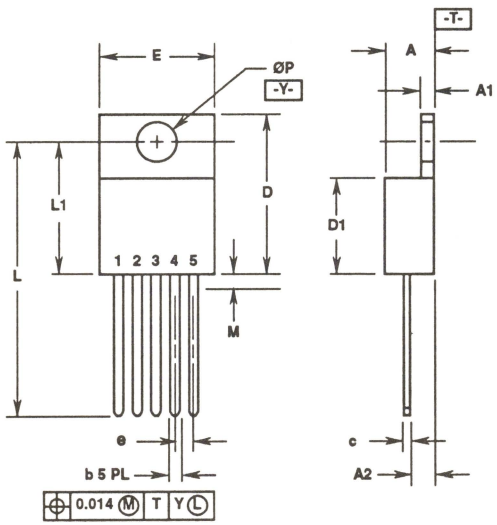
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.190	3.56	4.82	-
b	0.015	0.040	0.38	1.02	-
b1	0.045	0.070	1.14	1.77	1
c1	0.014	0.022	0.36	0.56	1
D	0.560	0.650	14.23	16.51	-
E	0.380	0.420	9.66	10.66	-
e	0.090	0.110	2.29	2.79	2
e1	0.190	0.210	4.83	5.33	2
F	0.020	0.055	0.51	1.39	-
H1	0.230	0.270	5.85	6.85	-
J1	0.080	0.115	2.04	2.92	3
L	0.500	0.580	12.70	14.73	-
L1	-	0.250	-	6.35	1
ØP	0.139	0.161	3.53	4.08	-
Q	0.100	0.135	2.54	3.43	-

Rev. 0 2/94

NOTES:

1. Lead dimension and finish uncontrolled in zone L1.
2. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
3. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
4. Controlling dimension: INCH.

Single-In-Line Plastic Packages (SIP) (Continued)



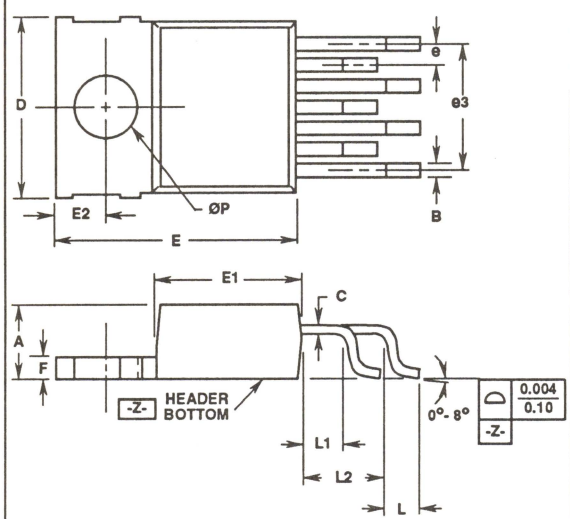
Z5.067 (JEDEC TS-001AA ISSUE A)
5 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.190	4.19	4.82	-
A1	0.035	0.055	0.89	1.39	-
A2	0.085	0.115	2.16	2.92	3
b	0.020	0.040	0.51	1.01	1
c	0.012	0.025	0.31	0.63	1
D	0.570	0.625	14.48	15.87	-
D1	0.330	0.370	8.39	9.39	-
e	0.067 BSC		1.70 BSC		2
E	0.390	0.415	9.91	10.54	-
L	0.945	1.045	24.00	26.54	-
L1	0.465	0.539	11.81	13.69	-
ØP	0.139	0.156	3.53	3.96	-
M	0.130	0.150	3.31	3.81	1

Rev. 0 2/94

NOTES:

1. Lead dimension and finish uncontrolled in zone M.
2. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
3. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
4. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
5. Controlling dimension: INCH.



Z7.05A
7 LEAD PLASTIC SINGLE-IN-LINE PACKAGE
STAGGERED SURFACE MOUNT "GULLWING" LEAD FORM

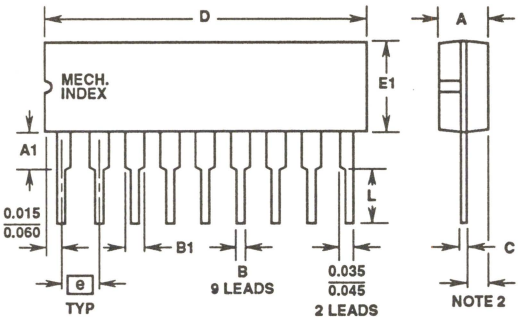
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.190	4.06	4.83
B	0.023	0.037	0.58	0.94
C	0.015	0.023	0.38	0.58
D	0.385	0.415	9.78	10.54
E	0.560	0.590	14.22	14.99
E1	0.326	0.335	8.28	8.50
E2	0.103	0.113	2.62	2.87
e	0.045	0.055	1.14	1.40
e3	0.295	0.305	7.49	7.75
F	0.045	0.055	1.14	1.40
L	0.065	0.080	1.66	2.03
L1	0.100	0.110	2.54	2.79
L2	0.200	0.210	5.08	5.33
N	7		7	
ØP	0.145	0.156	3.68	3.98

Rev. 0 2/94

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. N is the number of leads.
3. Controlling dimension: INCH.

Single-In-Line Plastic Packages (SIP) (Continued)



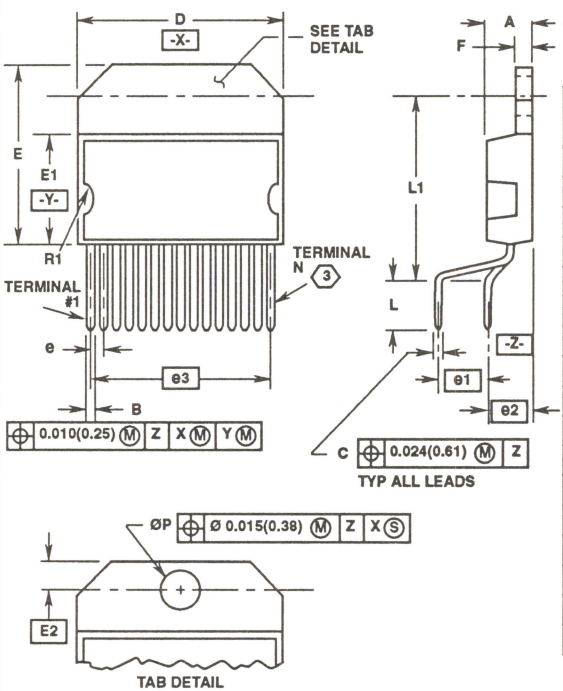
Z9.1
9 LEAD SINGLE-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.140	-	3.56	-
A1	0.090	0.120	2.29	3.05	-
B	0.014	0.020	0.36	0.51	-
B1	0.050	0.065	1.27	1.65	3
C	0.008	0.014	0.20	0.35	-
D	0.845	0.885	21.47	22.48	2
E1	0.240	0.260	6.10	6.61	2
e	0.100 BSC		2.54 BSC		-
L	0.125	0.150	3.18	3.81	-
N	9		9		4

Rev. 0 2/94

NOTES:

1. Lead within 0.010 inch radius of true position (TP) with maximum material condition.
2. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
3. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
4. N is the maximum number of terminal positions.
5. Controlling dimension: INCH.



Z15.05A (JEDEC MO-048 AB ISSUE A)
15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE
STAGGERED VERTICAL LEAD FORM

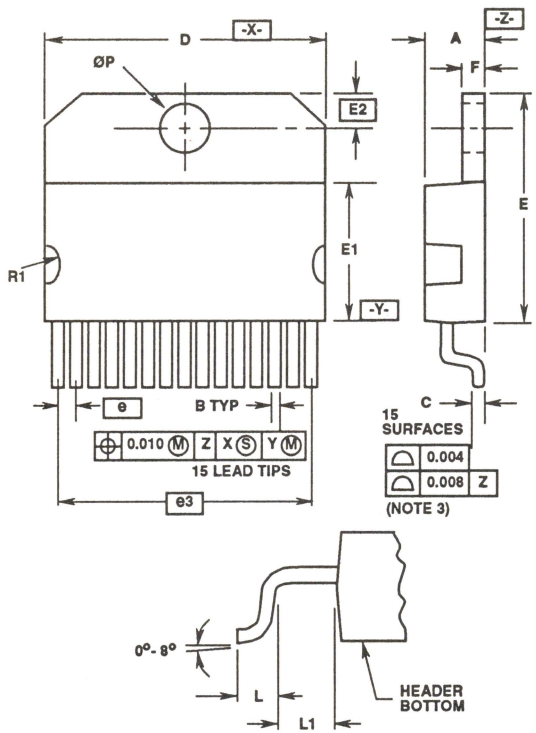
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.014	0.024	0.36	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e1	0.200 BSC		5.08 BSC	
e2	0.169 BSC		4.29 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.150	0.176	3.81	4.47
L_1	0.690	0.710	17.53	18.03
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

Rev. 0 2/94

NOTES:

1. Refer to series symbol list, JEDEC Publication No. 95.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. N is the number of terminals.
4. Controlling dimension: INCH.

Single-In-Line Plastic Packages (SIP) (Continued)



Z15.05B

15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE SURFACE MOUNT 'GULLWING' LEAD FORM

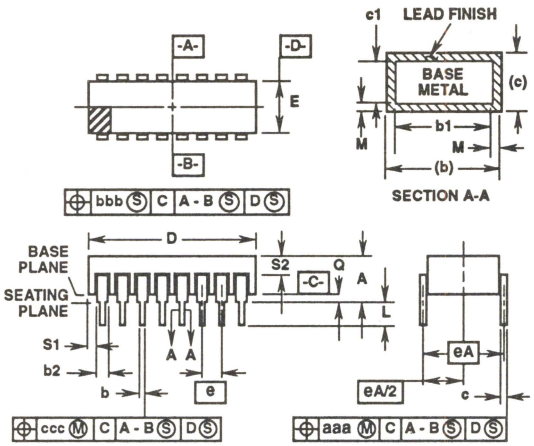
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.018	0.024	0.46	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.065	0.080	1.66	2.03
L1	0.098	0.108	2.49	2.74
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

Rev. 0 2/94

NOTES:

1. Dimensioning and Tolerancing per ANSI Y14.5M - 1982.
2. N is the number of terminals.
3. All lead surfaces are within 0.004 inch of each other. No lead can be more than 0.004 inch above or below the header plane, (-Z- Datum).
4. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

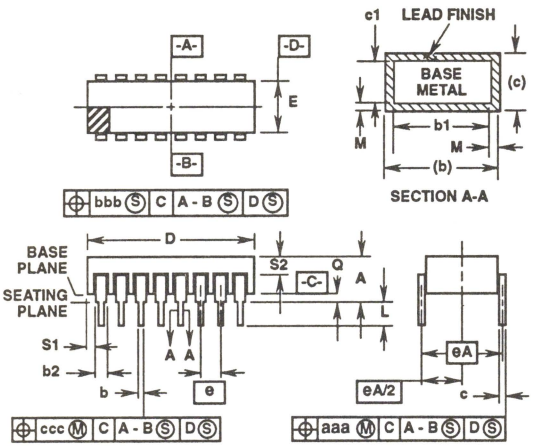
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP) (Continued)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

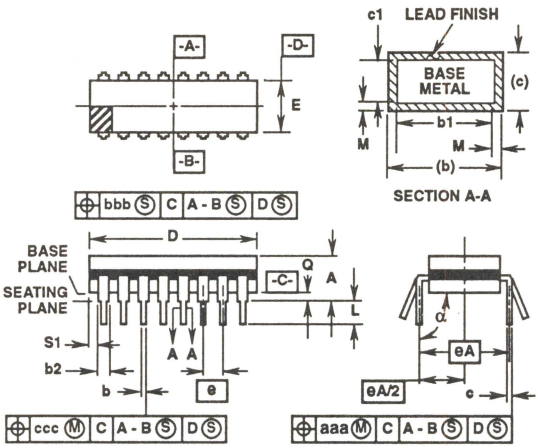
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

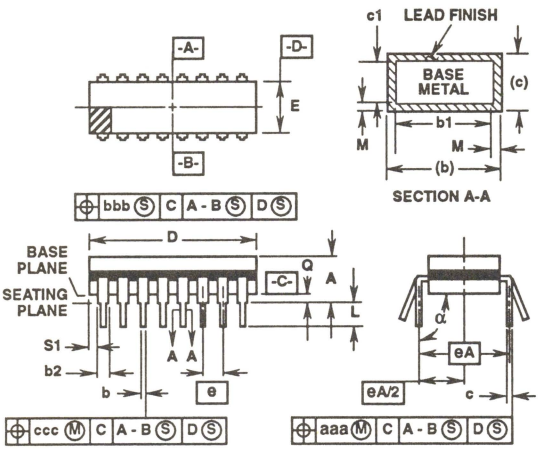
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CerDIP) (Continued)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

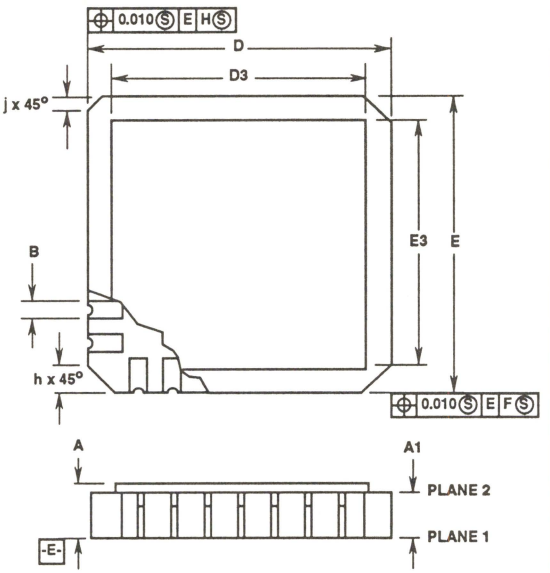
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

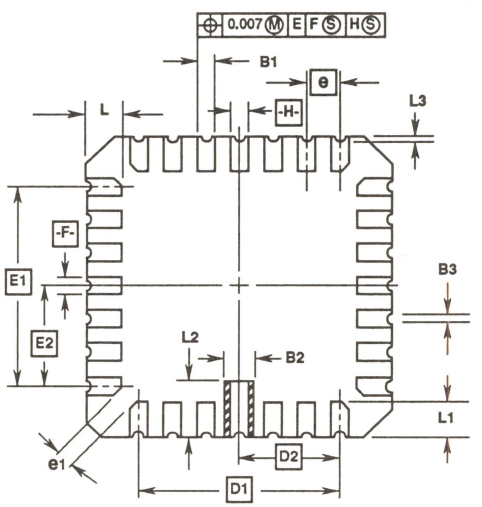
Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Leadless Chip Carrier Packages (CLCC)





J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD LEADLESS CERAMIC CHIP CARRIER

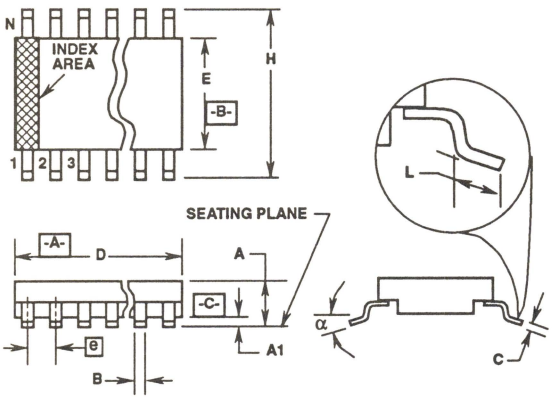
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 4/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

Ceramic SOIC Flatpack Packages (SOIC Flatpack)



K28.E

28 LEAD CERAMIC SOIC FLATPACK PACKAGE

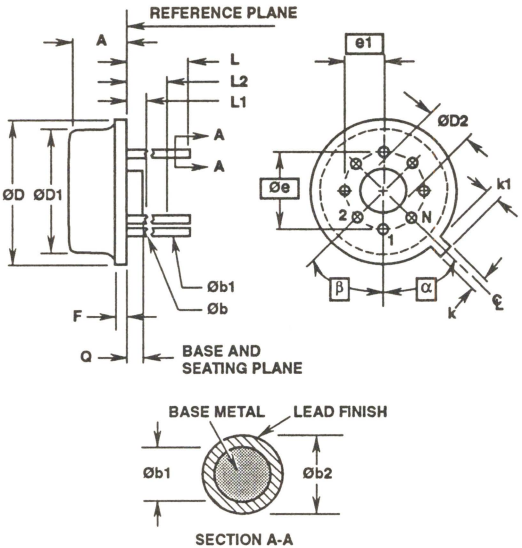
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.154	2.35	3.90	-
A1	0.004	0.018	0.10	0.45	-
B	0.013	0.020	0.33	0.51	5
C	0.006	0.013	0.15	0.32	-
D	0.697	0.720	17.70	18.30	-
E	0.289	0.301	7.35	7.65	-
e	0.05 BSC		1.27 BSC		-
H	0.393	0.420	10.00	10.65	-
L	0.015	0.050	0.40	1.27	2
N	28		28		3
α	0°	8°	0°	8°	-

Rev. 0 4/94

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "L" is the length of terminal for soldering to a substrate.
3. "N" is the number of terminal positions.
4. Terminal numbers are shown for reference only.
5. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
6. Controlling dimension: MILLIMETER.

Metal Can Packages (Can)



T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD TO-99 METAL CAN

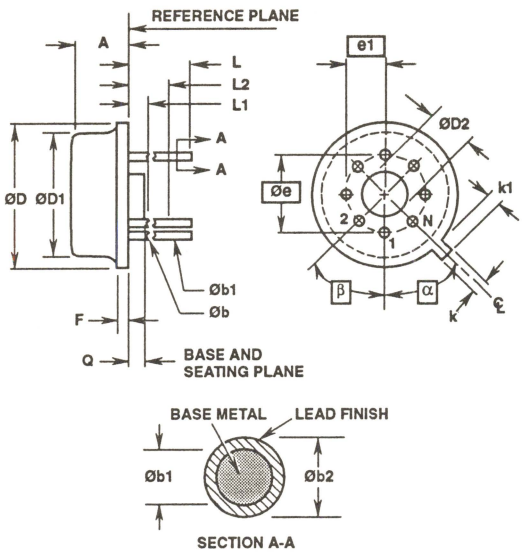
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

Rev. 0 4/94

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

Metal Can Packages (Can) (Continued)



NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

T10.C

10 LEAD TO-100 METAL CAN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	-	-	-	-	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	-	-	-	-	-
α	36° BSC		36° BSC		3
β	36° BSC		36° BSC		3
N	10		10		4

Rev. 0 4/94

T12.B

12 LEAD TO-101 METAL CAN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	-	-	-	-	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	-	-	-	-	-
α	30° BSC		30° BSC		3
β	30° BSC		30° BSC		3
N	12		12		4

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INTELLIGENT POWER ICs 14

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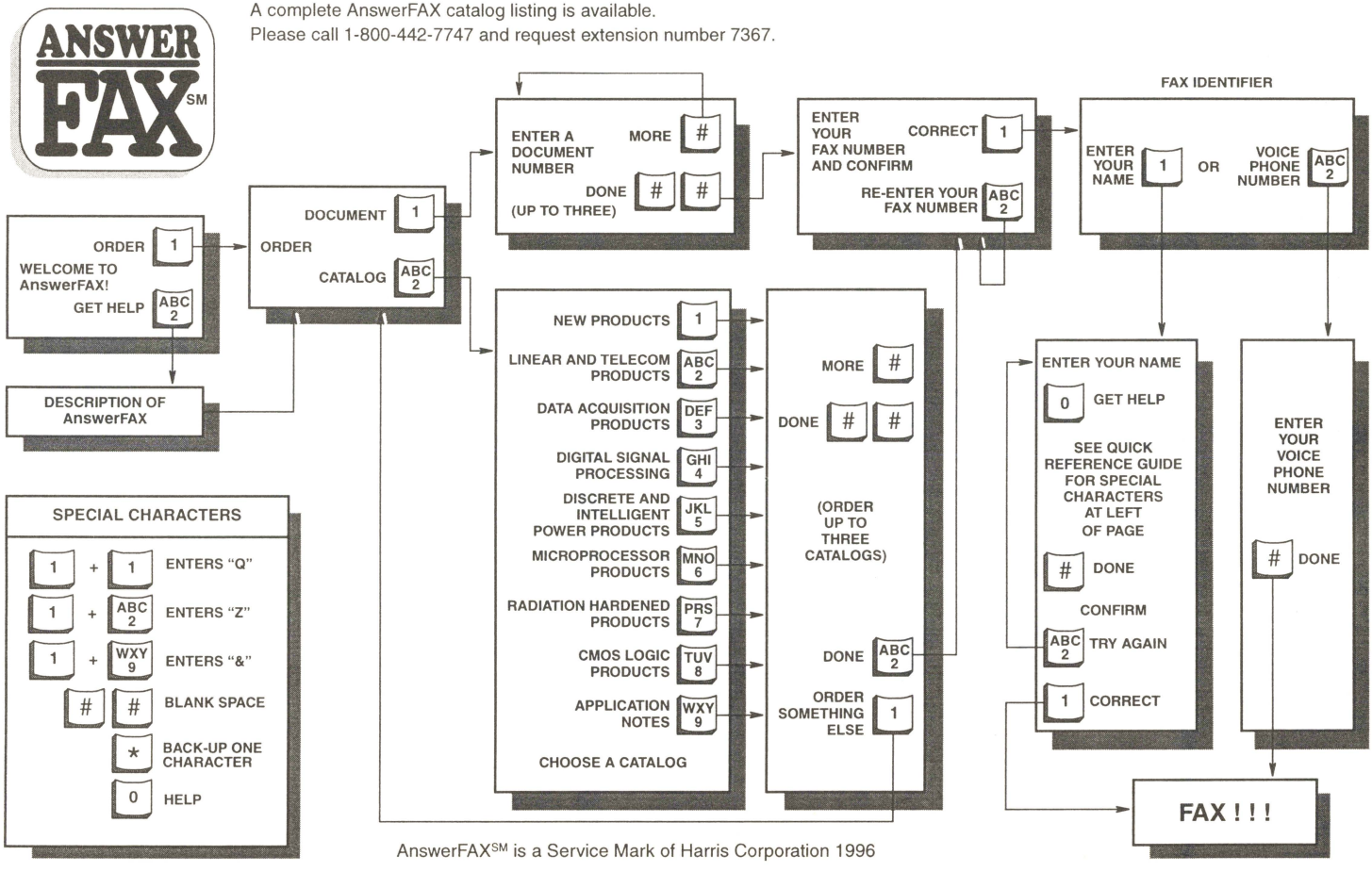
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	DB223B	**POWER MOSFETs** (1994: 1,328pp) This data book contains detailed technical information including standard power MOSFETs (the popular RF-series types, the IRF-series of industry replacement types, and JEDEC types), MegaFETs, logic-level power MOSFETs (L2FETs), ruggedized power MOSFETs, advanced discrete, high-reliability and radiation-hardened power MOSFETs.
	DB316	**POWER MOSFET DATA BOOK SUPPLEMENT** (1996: 380pp) This data book contains the data sheets of recently introduced products and also updates some of the data sheets in the Power MOSFET Data Book DB223B. These data sheets contain the detailed specification for these products.
	DB235B	**RADIATION HARDENED** (1993: 2,232pp) The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
	DB301B	**DATA ACQUISITION** (1994: 1,104pp) Product specifications on A/D converters (display, integrating, successive approximation, flash); D/A converters, switches, multiplexers, and other products.
	DB302B	**DIGITAL SIGNAL PROCESSING** (1994: 528pp) Product specifications on one-dimensional and two-dimensional filters, signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer).
	DB303.1	**MICROPROCESSOR PRODUCTS** (1997: 1,260pp) In the ever-changing IC marketplace, Harris Semiconductor has made a strong business commitment to continue servicing mature CMOS products and technologies. As always, we will supply mature, standard architecture microprocessor families for markets including cellular communications, PABX, networking systems, EDP peripherals, medical and avionics instrumentation.
	DB304.1	**INTELLIGENT POWER ICs** (1994: 946pp) This data book includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris quality and high reliability program.
	DB309.1	**MCT/IGBT/DIODES** (1995: 706pp) This MCT/IGBT/Diodes data book represents the full line of these products made by Harris Semiconductor Discrete Power Products for commercial applications.
	DB319	**HARRIS IGBT UFS SERIES SUPPLEMENT** (1997: 164pp) The UFS series IGBT (Insulated Gate Bipolar Transistor) Data Book Supplement represents a new generation of IGBT products from Harris Semiconductor Discrete Power Products for commercial applications. This data book supplement describes Harris Semiconductor's line of UFS (Ultra Fast Switching) IGBTs.
	DB314	**SIGNAL PROCESSING NEW RELEASES** (1995: 690pp) This data book represents the newest products made by Harris Semiconductor Data Acquisition Products, Linear Products, Telecom Products and Digital Signal Processing Products for commercial applications.
	DB315.1	**CROSS-REFERENCE GUIDE** (1996: 554pp) Listing of semiconductor products that are second-sourced by Harris Semiconductor.
	DB317	**COMMUNICATIONS DATA BOOK** (1997: 708pp) Technical information including data sheets and application notes for a variety of Harris Integrated Circuits targeted for the communications industry. These products include the PRISM 2.4GHz DSSS Wireless Transceiver Chip Set, the new HC5517 Ringing SLIC as well as Standard Linear, Data Acquisition, DSP and Power products.
	DB321	**APPLICATIONS FOR COMMUNICATION ICs** (1997: 392pp) Application Notes and Tech Briefs for Harris communication products that range from wireless PRISM™ 2.4GHz WLAN chip set to Telecom HC5517 ringing SLIC. Also Data Acquisition and Digital Signal Processing.
	DB318	**LPT/FCT CMOS LOGIC EXPANSION** (1997: 620pp) This data book fully describes Harris Semiconductor's LPT and FCT CMOS Logic ICs. It includes a complete set of data sheets for product specifications, application notes and techbriefs with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program.
	DB450.4	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1995: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
	DB500.3	**LINEAR ICs** (1996/97: 1446pp) Harris offers an extensive line of Linear components including: High Speed and General Purpose Op Amps, Comparators, Sample/Hold Amps, Video Crosspoint Switches, Special Analog Circuits and Transistor Arrays.
	Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This data book describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	PSG201.24	**PRODUCT SELECTION GUIDE** (1996: 834pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
	BR-057.3	**AnswerFAX CATALOG** (Fall 1996: 112pp) A Complete AnswerFAX Catalog listing.

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AnswerFAX Technical Support Application Note Listing

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
27007	BR007	Complete Listing of Harris Sales Offices, Representatives and Authorized Distributors World Wide (7 pages)
HARRIS SEMICONDUCTOR APPLICATION NOTES		
9001	AN001	Glossary of Data Conversion Terms (6 pages)
9002	AN002	Principles of Data Acquisition and Conversion (20 pages)
9004	AN004	The IH5009 Analog Switch Series (9 pages)
9007	AN007	Using the 8048/8049 Log/Antilog Amplifier (6 pages)
9009	AN009	Pick Sample-Holds by Accuracy and Speed and Keep Hold Capacitors in Mind (7 pages)
9012	AN012	Switching Signals with Semiconductors (4 pages)
9013	AN013	Everything You Always Wanted to Know About the ICL8038 (4 pages)
9016	AN016	Selecting A/D Converters (7 pages)
9017	AN017	The Integrating A/D Converter (5 pages)
9018	AN018	Do's and Don'ts of Applying A/D Converters (4 pages)
9020	AN020	A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing (23 pages)
9023	AN023	Low Cost Digital Panel Meter Designs (5 pages)
9027	AN027	Power Supply Design Using the ICL8211 and 8212 (8 pages)
9028	AN028	Build an Auto-Ranging DMM with the ICL7103A/8052A A/D Converter Pair (6 pages)
9030	AN030	ICL7104: A Binary Output A/D Converter for Microprocessors (16 pages)
9032	AN032	Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7107/7109 Family (8 pages)
9040	AN040	Using the ICL8013 Four Quadrant Analog Multiplier (6 pages)
9042	AN042	Interpretation of Data Converter Accuracy Specifications (11 pages)
9043	AN043	Video Analog-to-Digital Conversion (6 pages)
9046	AN046	Building a Battery Operated Auto Ranging DVM with the ICL7106 (5 pages)
9047	AN047	Games People Play with Intersil's A/D Converter's (27 pages)

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9048	AN048	Know Your Converter Codes (5 pages)
9049	AN049	Applying the 7109 A/D Converter (5 pages)
9051	AN051	Principles and Applications of the ICL7660 CMOS Voltage Converter (9 pages)
9052	AN052	Tips for Using Single Chip 3.5 Digit A/D Converters (9 pages)
9053	AN053	The ICL7650 A New Era in Glitch-Free Chopper Stabilized Amplifiers (19 pages)
9054	AN054	Display Driver Family Combines Convenience of Use with Microprocessor Interfaceability (18 pages)
9059	AN059	Digital Panel Meter Experiments for the Hobbyist (7 pages)
9108	AN108	82C52 Programmable UART (12 pages)
9109	AN109	82C59A Priority Interrupt Controller (14 pages)
9111	AN111	Harris 80C286 Performance Advantages Over the 80386 (12 pages)
9112	AN112	80C286/80386 Hardware Comparison (4 pages)
9113	AN113	Some Applications of Digital Signal Processing Techniques to Digital Video (5 pages)
9114	AN114	Real-Time Two-Dimensional Spatial Filtering with the Harris Digital Filter Family (43 pages)
9115	AN115	Digital Filter (DF) Family Overview (6 pages)
9116	AN116	Extended DF Configurations (10 pages)
9120	AN120	Interfacing the 80C286-16 With the 80287-10 (2 pages)
9121	AN121	Harris 80C286 Performance Advantages Over the 80386SX (14 pages)
9400	AN400	Using the HS-3282 ARINC Bus Interface Circuit (6 pages)
9509	AN509	A Simple Comparator Using the HA-2620 (1 page)
9514	AN514	The HA-2400 PRAM Four Channel Operational Amplifier (7 pages)
9515	AN515	Operational Amplifier Stability: Input Capacitance Considerations (2 pages)
9517	AN517	Applications of Monolithic Sample and Hold Amplifier (5 pages)
9519	AN519	Operational Amplifier Noise Prediction (4 pages)

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9521	AN521	Getting the Most Out of CMOS Devices for Analog Switching Jobs (7 pages)
9522	AN522	Digital to Analog Converter Terminology (3 pages)
9524	AN524	Digital to Analog Converter High Speed ADC Applications (3 pages)
9525	AN525	HA-5190/5195 Fast Settling Operational Amplifier (4 pages)
9526	AN526	Video Applications for the HA-5190/5195 (5 pages)
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9534	AN534	Additional Information on the HI-300 Series Switch (5 pages)
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9541	AN541	Using HA-2539 or HA-2540 Very High Slew Rate, Wideband Operational Amplifier (4 pages)
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9554	AN554	Low Noise Family HA-5101/02/04/11/12/14 (7 pages)
9556	AN556	Thermal Safe-Operating-Areas for High Current Op Amps (5 pages)
9557	AN557	Recommended Test Procedures for Analog Switches (6 pages)
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95290	AN5290	Integrated Circuit Operational Amplifiers (20 pages)
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96048	AN6048	Some Applications of A Programmable Power Switch/Amp (12 pages)
96077	AN6077	An IC Operational-Transconductance-Amplifier (OTA) With Power Capability (12 pages)
96157	AN6157	Applications of the CA3085 Series Monolithic IC Voltage Regulators (11 pages)
96182	AN6182	Features and Applications of Integrated Circuit Zero-Voltage Switches (CA3058, CA3059 and CA3079) (31 pages)
96315	AN6315	COS/MOS Interfacing Simplified (7 pages)
96386	AN6386	Understanding and Using the CA3130, CA3130A and CA3130B30A/30B BiMOS Operation Amplifiers (5 pages)
96459	AN6459	Why Use the CMOS Operational Amplifiers and How to Use it (4 pages)
96565	AN6565	Design of Clock Generators For Use With COSMAC Microprocessor CDP1802 (3 pages)
96669	AN6669	FET-Bipolar Monolithic Op Amps Mate Directly to Sensitive Sources (3 pages)
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97332	AN7332	The Application of Conductivity-Modulated Field-Effect Transistors (5 pages)
97374	AN7374	The CDP1871A Keyboard Encoder (9 pages)
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98603	AN8603	Improved IGBTs with Fast Switching Speed and High-Current Capability (4 pages)
98610	AN8610	Spicing-Up Spice II Software for Power MOSFET Modeling (8 pages)
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99325	AN9325	HIP4081, 80V High Frequency H-Bridge Driver (11 pages)
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99329	AN9329	Using the HI1176/HI1171 Evaluation Board (5 pages)
99330	AN9330	Using the HI1396 Evaluation Board (9 pages)
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99332	AN9332	Using the HI1276 Evaluation Board (10 pages)
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99336	AN9336	Mult-Meter Display Converter Eases DMM Design (6 pages)
99337	AN9337	Reduce CMOS-Multiplexer Troubles Through Proper Device Selection (6 pages)
99402	AN9402	Keeping the HI-0201 Switch Closed when Removing the V+ Supply (1 page)

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99405	AN9405	HIP4081A, 80V High Frequency H-Bridge Driver (11 pages)
660001	MM0001	HFA-0001 Spice Operational Amplifier Macro-Model (4 pages)
660002	MM0002	HFA-0002 Spice Operational Amplifier Macro-Model (4 pages)
660005	MM0005	HFA-0005 Spice Operational Amplifier Marco-Model (4 pages)
662500	MM2500	HA2500/02 Spice Operational Amplifier Macro-Model (5 pages)
662510	MM2510	HA-2510/12 Spice Operational Amplifier Macro-Model (4 pages)
662520	MM2520	HA-2520/22 Spice Operational Amplifier Macro-Model (4 pages)
662539	MM2539	HA-2539 Spice Operational Amplifier Macro-Model (4 pages)
662540	MM2540	HA-2540 Spice Operational Amplifier Macro-Model (4 pages)
662541	MM2541	HA-2541 Spice Operational Amplifier Macro-Model (5 pages)
662542	MM2542	HA-2542 Spice Operational Amplifier Macro-Model (5 pages)
662544	MM2544	HA-2544 Spice Operational Amplifier Macro-Model (5 pages)
662548	MM2548	HA-2548 Spice Operational Amplifier Macro-Model (5 pages)
662600	MM2600	HA-2600/02 Spice Operational Amplifier Macro-Model (5 pages)
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662850	MM2850	HA-2850 Spice Operational Amplifier Macro-Model (4 pages)
663046	MM3046	HFA3046/3096/3127/3128 Transistor Array Spice Models (4 pages)
665002	MM5002	HA-5002 Spice Buffer Amplifier Macro-Model (4 pages)
665004	MM5004	HA-5004 Spice Current Feedback Amplifier Macro-Model (4 pages)
665020	MM5020	HA-5020 Spice Current Feedback Operational Amplifier Macro-Model (4 pages)
665033	MM5033	HA-5033 Spice Buffer Amplifier Macro-Model (4 pages)
665101	MM5101	HA-5101 Spice Operational Amplifier Macro-Model (5 pages)
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665104	MM5104	HA-5104 Spice Operational Amplifier Macro-Model (5 pages)
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665114	MM5114	HA-5114 Spice Operational Amplifier Macro-Model (5 pages)
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665137	MM5137	HA-5137 Spice Operational Amplifier Macro-Model (4 pages)
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